CMOS 8-BIT MICROCONTROLLER

TMP90PR74ADF

1. OUTLINE AND CHARACTERISTICS

The TMP90PR74A is a system evaluation LSI having a built in One-Time PROM (56K byte) for TMP90CR74A.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP90CR74A by programming to the internal PROM.

PARTS NO.	PROM	RAM	PACKAGE	ADAPTER SOCKET NO.
TMP90PR74ADF	57344 × 8 bit	1024 × 8 bit	QFP100 (22 × 22 mm)	BM1190

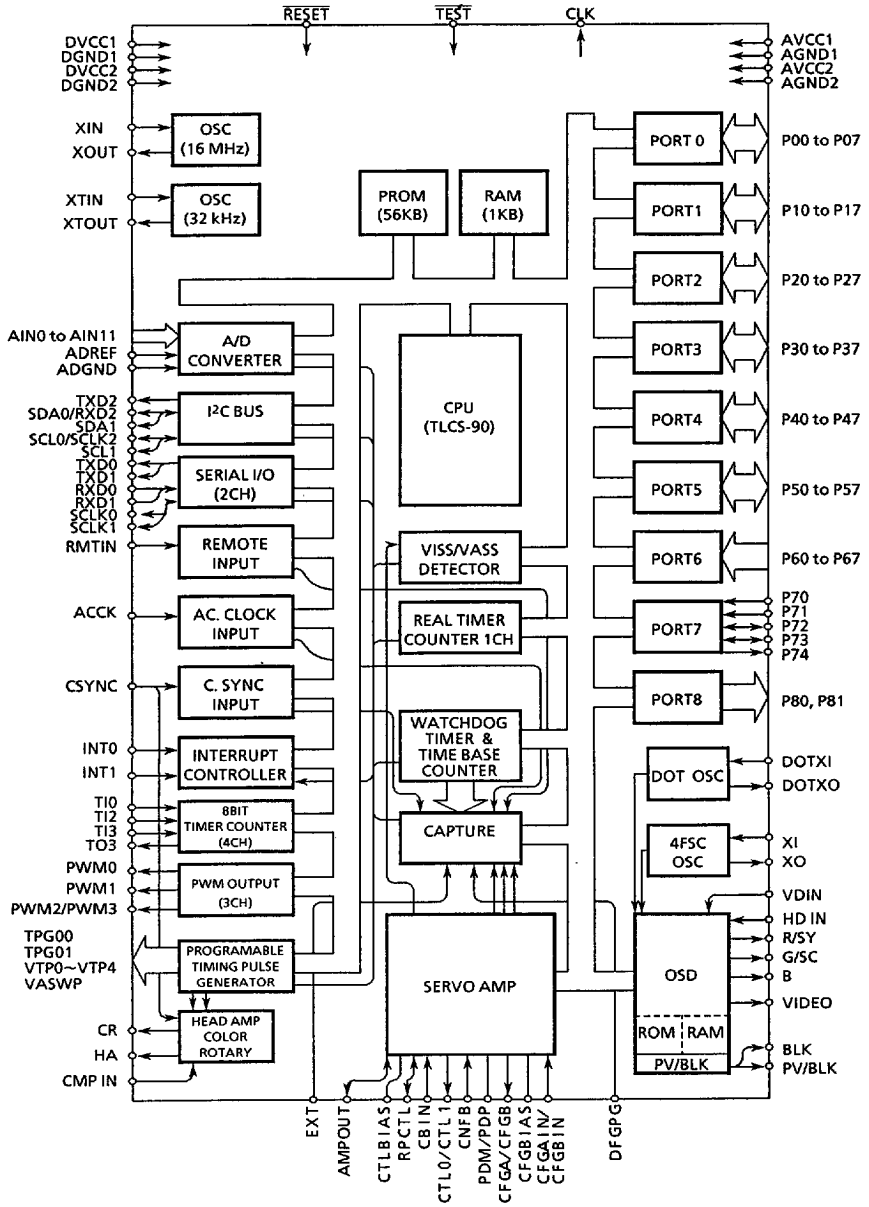


Fig 1.1 TMP90PR74ADF Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The pin assignment of TMP90PR74ADF is shown in Fig. 2.1 and its name and function are in Table 2.1.

2.1 Pin Assignment

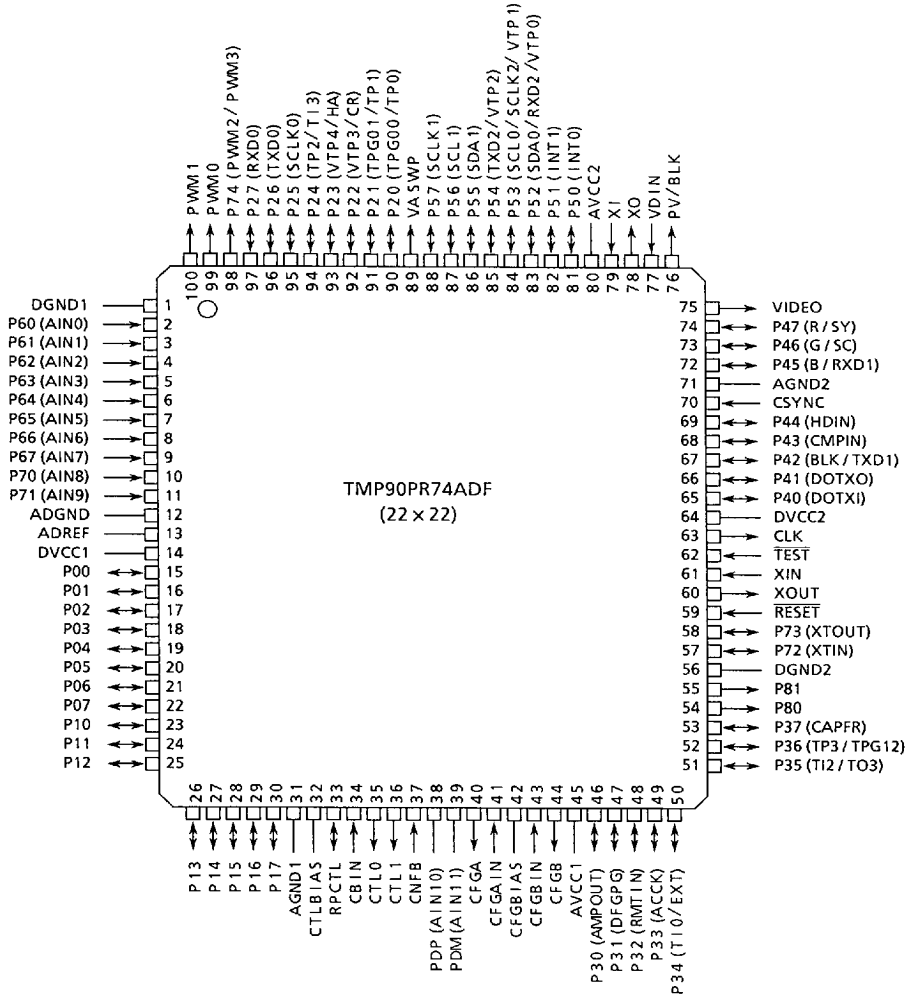


Fig. 2.1 Pin Assignment of TMP90PR74ADF

2.2 Pin name and pin functions

TMP90PR74A has two modes : MCU and PROM.

(1) MCU mode

In this mode, the 90PR74A is pin compatible with the 90CR74A.

Table 2.1 Pin name and pin functions (1/4)

Pin Name	No. of Pins	I/O Port structure	Function
P00 to P07	8	I/O 3-state	P00 to P07 : 8-bit I/O port. Input and output can be set in bit unit.
P10 to P17	8	I/O 3-state	P10 to P17 : 8-bit I/O port. Input and output can be set in bit unit.
P20 (TPG00 / TP0) P21 (TPG01 / TP1)	2	I/O 3-state Programmable Open Drain	P20, P21 : 2-bit I/O port. Input and output can be set in bit unit. TPG00/TPG01 : Timing Pulse Generator 0 (TPG0) TP0/TP1 : Timing Pulse (TP) output.
P22 (VTP3 / CR) P23 (VTP4 / HA)	2	I/O 3-state Programmable Open Drain	P22, P23 : 2-bit I/O port. Input and output can be set in bit unit. VTP3/VTP4 : Video Timing pulse (VTP) output. CR : Color Rotary output. HA : Head Amp switching signal output.
P24 (TP2 / TI3)	1	I/O 3-state Programmable Open Drain Schmitt input	P24 : 1-bit I/O port. Input and output can be set in bit unit. TP2 : Timing pulse (TP) output. TI3 : Event count input for Timer3 (TC3).
P25 (SCLK0)	1	I/O 3-state Schmitt input	P25 : 1-bit I/O port. Input and output can be set in bit unit. SCLK0 : Serial clock input/output for SIO0.
P26 (TXD0)	1	I/O 3-state	P26 : 1-bit I/O port. Input and output can be set in bit unit. TXD0 : Serial transmit data output for SIO0.
P27 (RXD0)	1	I/O 3-state Schmitt input	P27 : 1-bit I/O port. Input and output can be set in bit unit. RXD0 : Serial receive data input for SIO0.
P30 (AMPOUT)	1	I/O 3-state	P30 : 1-bit I/O port. Input and output can be set in bit unit. AMPOUT : Monitor output of Analog amp (CTL amp / CFG amp) for servo control.
P31 (DFGPG) P32 (RMTIN) P33 (ACCK)	3	I/O 3-state Schmitt input	P31, P32, P33 : 3-bit I/O port. Input and output can be set in bit unit. DFGPG : Input for Drum PG/FG conposite signal. RMTIN : Input for remote control signal. ACCK : Input for AC power frequency.
P34 (TI0 / EXT)	1	I/O 3-state Schmitt input	P34 : I/O port. Input and output can be set in bit unit. TI0 : Event Count input for Timer0 (TC0). EXT : External trigger input for Capture 0 (CAP0).
P35 (TI2 / TO3)	1	I/O 3-state Schmitt input	P35 : 1-bit I/O port. Input and output can be set in bit unit. TI2 : Event Count input for Timer2 (TC2). TO3 : Timer3 (TC3) output.

Table 2.1 Pin name and pin functions (2/4)

Pin Name	No. of Pins	I/O Port structure	Function
P36 (TP3 / TPG12)	1	I/O 3-state Schmitt input	P36 : 1-bit I/O port. Input and output can be set in bit unit. TP3 : Timing pulse (TP) output. TPG12 : Timing pulse generator (TPG1) output.
P37 (CAPFR)	1	I/O 3-state Programmable Open Drain	P37 : 1-bit I/O port. Input and output can be set in bit unit. CAPFR : Capstan motor control output.
P40 (DOTXI) P41 (DOTXO)	2	I/O 3-state	P40, P41 : 2-bit I/O port. Input and output can be set in bit unit. DOTXI / DOTXO : Oscillator terminal for OSD dot-clock.
P42 (BLK / TXD1)	1	I/O Open Drain	P42 : 1-bit I/O port. Input and output can be set in bit unit. BLK : Blanking output for OSD. TXD1 : Serial transmit data output for SIO1.
P43 (CMPIN) P44 (HDIN)	2	I/O 3-state Schmitt input	P43, P44 : 2-bit I/O port. Input and output can be set in bit unit. CMP IN : Comparator signal input for Head Amp switch. HD IN : Horizontal sync. signal input.
P45 (BLK / RXD1)	1	I/O Open Drain Schmitt input	P45 : 1-bit I/O port. Input and output can be set in bit unit. B : Blue output from OSD. RXD1 : Serial receive data input for SIO1.
P46 (G / SC) P47 (R / SY)	2	I/O 3-state	P46, P47 : 2-bit I/O port. Input and output can be set in bit unit. G, R : Green and Red output from OSD. SC, SY : Chroma, luminance Signal output from OSD.
P50 (INT0) P51 (INT1)	2	I/O 3-state Schmitt input	P50, P51 : 2-bit I/O port. Input and output can be set in bit unit. INT0, INT1 : External interrupt request.
P52 (SDA0/ RXD2/VTP0) P53 (SCL0/ SCLK2/VTP1)	2	I/O 3-state Programmable Open Drain Schmitt input	P52, P53 : 2-bit I/O port. Input and output can be set in bit unit. SDA0 : Serial data I/O for I²CBUS. SCL0 : Serial clock I/O for I²CBUS. RXD2 : Serial receive data input for SIO2. SCLK2 : Serial clock input/output for SIO2. VTP0, VTP1 : Video timing pulse (VTP) output.
P54 (TXD2/VTP2)	1	I/O 3-state Schmitt input	P54 : 1-bit I/O port. Input and output can be set. TXD2 : Serial transmit data output for SIO2. VTP2 : Video timing pulse (VTP) output.
P55 (SDA1) P56 (SCL1)	2	I/O 3-state Open Drain Schmitt input	P55, P56 : 2-bit I/O port. Input and output can be set in bit unit. SDA1 : Serial data input/output for I²CBUS. SCL1 : Serial clock input/output for I²CBUS.
P57 (SCLK1)	1	I/O Open Drain Schmitt input	P57 : 1-bit I/O port. Input and output can be set. SCLK1 : Serial clock input/output for SIO1.

Table 2.1 Pin name and pin functions (3/4)

Pin Name	No. of Pins	I/O Port structure	Function
P60 (AIN0) to P67 (AIN7) P70 (AIN8) to P71 (AIN9)	10	Input	P60 to P67 : 8-bit input port. P70, P71 : 2-bit input port. AIN0 to AIN9 : Analog input for A/D converter.
P72 (XTIN) P73 (XTOUT)	2	I/O 3-state	P72, P73 : 2-bit I/O port. Input and output can be set in bit unit. XTIN, XTOUT : Oscillator terminals for slow clock (32.768 kHz)
P74 (PWM2 / PWM3)	1	Output 3-state Programmable Open Drain	P74 : 1-bit output port. PWM2/PWM3 : 8-bit / 14-bit PWM (PWM2 / PWM3) output.
P80 P81	2	Output 3-state	P80, P81 : 2-bit output port.
PWM0 PWM1	2	Output 3-state Programmable Open Drain	PWM0 : 12-bit PWM (PWM0) output. PWM1 : 12-bit PWM (PWM1) output.
VASWP	1	Output 3-state	Video / Audio head switching control signal output.
CSYNC	1	Input Schmitt input	Composite sync. signal input.
CTLBIAS	1	–	Bias terminal for control (CTL) amplifier.
RPCTL	1	I/O	Input and output for Control (CTL) signal.
CBIN	1	Input	Bias input terminal for control (CTL) amplifier.
CTL0 CTL1	2	Output	CTL amplifier output for gain switching.
CNFB	1	Input	Negative feed-back terminal of CTL amplifier.
PDP (AIN10)	1		PDP : Terminal for Peak-Hold capacitor which keeps plus (positive) peak for control (CTL) Amplifier. AIN10 : Analog input for PDP level monitor.
PDM (AIN11)	1		PDM : Terminal for Peak-Hold capacitor which keeps plus (positive) peak for control (CTL) Amplifier. AIN11 : Analog input for PDM level monitor.

Table 2.1 Pin name and pin functions (4/4)

Pin Name	No. of Pins	I/O Port structure	Function
CFGA	1	Output	Capstan FG amplifier (CFGA amp.) output.
CFGA IN	1	Input	Capstan FG amplifier (CFGA amp.) input.
CFG BIAS	1	–	Capstan FG amplifier bias terminal.
CFGB IN	1	Input	Capstan FG amplifier (CFGB amp.) input.
CFGB	1	Output	Capstan FG amplifier (CFGB amp.) output.
VIDEO	1	Output	OSD video signal output.
PV / BLK	1	Output 4-state	Pseudo V-SYNC (PV) output / On Screen Display (OSD) Blanking (BLK) output.
VDIN	1	Input Schmitt input	Vertical sync signal input.
XI, XO	2	Input, Output	Oscillator terminals for 4fsc clock of OSD
CLK	1	Output	Clock output : 1/2 or 1/4 of system clock (16 MHz) is output. During RESET operation, output stays high. (Pulled up internally).
$\overline{\text{TEST}}$	1	Input	Test terminal : Should be connected to high.
XIN, XOUT	2	Input, Output	Oscillator terminals for main clock (16 MHz)
$\overline{\text{RESET}}$	1	Input Schmitt input	System reset input.
DVCC1 DVCC2	2	–	Digital Power supply.
DGND1 DGND2	2	–	Digital Ground.
AVCC1 AVCC2	1	–	Analog Power supply.
AGND1 AGND2	1	–	Analog Ground.
ADREF	1	–	A/D converter reference voltage.
ADGND	1	–	A/D converter Ground.

(2) PROM mode pin functions pin disposal

Table 2.2 (2) PROM mode name and function, pin disposal

Pin function name	No. of pins	I/O	Function	Pin name (MCU mode)
A7 to A0	8	Input	Address Input	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P35
D7 to D0	8	I/O	Data Input / Output	P07 to P00
$\overline{OE}$	1	Input	Output Enable Signal Input	P80
$\overline{CE}$	1	Input	Chip Enable Signal Input	P34
$\overline{PGM}$	1	Input	Program control Input	P81
VPP	1	power supply	12.5 V / 5 V (Program power supply)	$\overline{TEST}$
VCC	2	power supply	5 V	DVCC1, DVCC2
GND	2	power supply	0 V	DGND1, DGND2

Pin name	No. of pins	I/O	Pin Setting
P37 to P36	2	I/O	Be fixed to "L" level
P33	1	I/O	Be fixed to "L" level
P32 to P31	2	I/O	Be fixed to "H" level
P30	1	I/O	Be fixed to "L" level
P47 to P40	8	I/O	Be fixed to "L" level
P57 to P50	8	I/O	Be fixed to "L" level
P67 to P60	8	Input	Be fixed to "L" level
P74	1	Output	Open
P73 to P72	2	I/O	Be fixed to "L" level
P71 to P70	2	Input	Be fixed to "L" level
PWM0, PWM1	2	Output	Open
ADREF	1		Be fixed to "L" level
ADGND	1		Be fixed to "L" level
$\overline{RESET}$	1	Input	Be fixed to "L" level
CLK	1	Input	Be fixed to "L" level
X1	1	Input	Resonator connection pin
X2	1	Output	
(Other)	24		Open

3. OPERATION

The TMP90PR74A is the OTP version of the TMP90CR74A that is replaced an internal ROM from Mask ROM to EPROM.

Refer to the TMP90PR74A except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in relation to the TMP90CR74A.

The TMP90PR74A has an MCU mode and a PROM mode.

3.1 MCU Mode

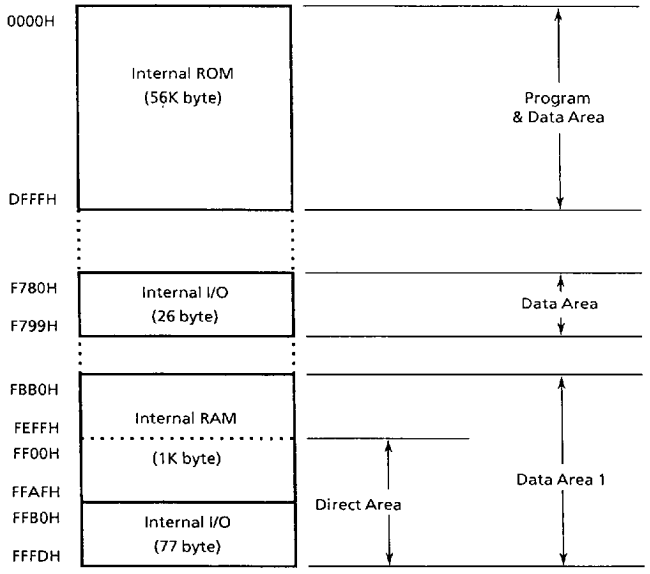
(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

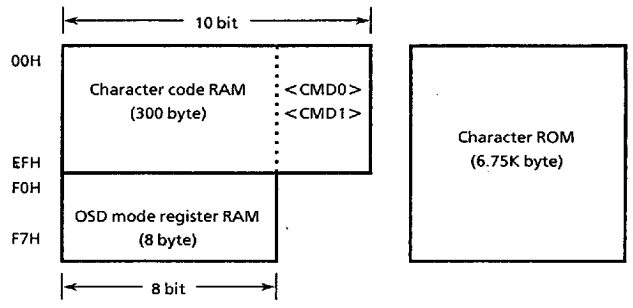
In the MCU mode, the operation is same as that of TMP90CR74A.

(2) Memory Map

Figure 3.1.1 show the memory map of TMP90PR74A.



(a) Memory map for CPU



(b) Memory map for OSD control RAM and character ROM

Figure 3.1.1 TMP90PR74A Memory Map

3.2 PROM Mode

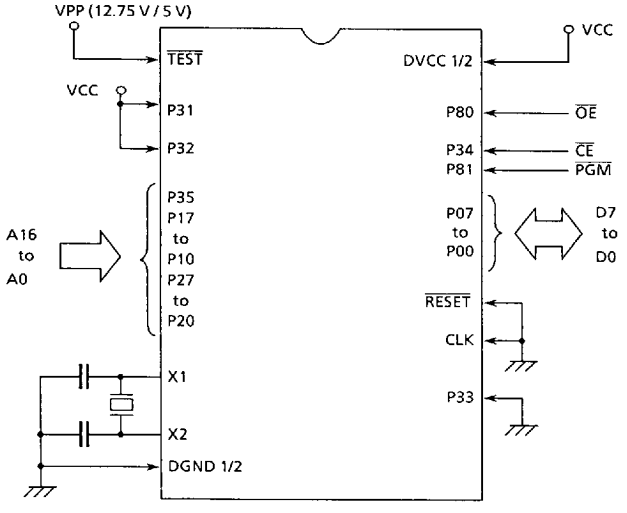
(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level, and P32, P33 pins to the "H" level.

The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket. The device selection (ROM Type) should be "TC571000D" with following conditions.

Size : 1M bit (128K × 8 bit), VPP : 12.75V ± 0.25V, TPW : 0.1 ms
VCC: 6.25V ± 0.25V
Address area: 0000H to DFFFH
Electric · Signature function: not exist

Figure 3.2.1 shows the setting of pins in PROM mode.



- For other pins, refer to the section on pin function (Table 2.2 (2))
- Use the 10 M to 16 MHz resonator in case of programming and verification by a general EPROM programmer.

Figure 3.2.1 PROM Mode Pin Setting

(2) Programming Flow Chart

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1 ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1 ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

Figure 3.2.2 shows the programming flowchart.

(3) How to program using a general-purpose PROM programmer

i) Adapters

BM1190

ii) Adapter setting

Switch (SW1) is set to side N.

iii) PROM programmer specifying

PROM type is specified to TC571000AD.

Writing voltage : 12.75 V (High-speed program mode)

iv) Data transfer (Copy) (Note1)

TMP90PR74A has a program PROM (address 0000 to DFFFH) and a OSD display character generator PROM (address 10000 to 13FFFH).

They are allocated in different address areas. They must be separately transferred to the PROM programmer.

0000 to DFFFH : Program EPROM

10000 to 13FFFH : Character generator EPROM

v) Writing address is specified

Program EPROM

Start address : 0000H

End address : DFFFH

Character-generator EPROM (Note2)

Start address : 10000H

End address : 13FFFH

vi) Writing

Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note1) TMP90PR74A does not support the electric signature mode. If the signature is used in PROM program, a device is damaged. The signature must not be used.

Note2) Data of the character generator consists of 6 bits. Unnecessary upper 2 bits must be written by "1".

(4) Setting of the security bit

TMP90PR74A has the security bit (1 bit) in the PROM cell. If the security bit is programmed to "0", the content of the PROM is disable to read in PROM mode.

Note1) The PROM data for the character generator can be always read even if the security bit is set.

How to program the security bit

First, set a switch (SW1) of the adapter socket to the S side. Additionally, set the start and end addresses to "0000H" by writing FEH in the address 0000H of the PROM programmer. Program according to the operating procedures of the PROM programmer. Thus, the built-in PROM is set to be the security bit.

Start address	:	0000H
End address	:	0000H
Data of Address 0000H	:	FEH

(5) Flowchart

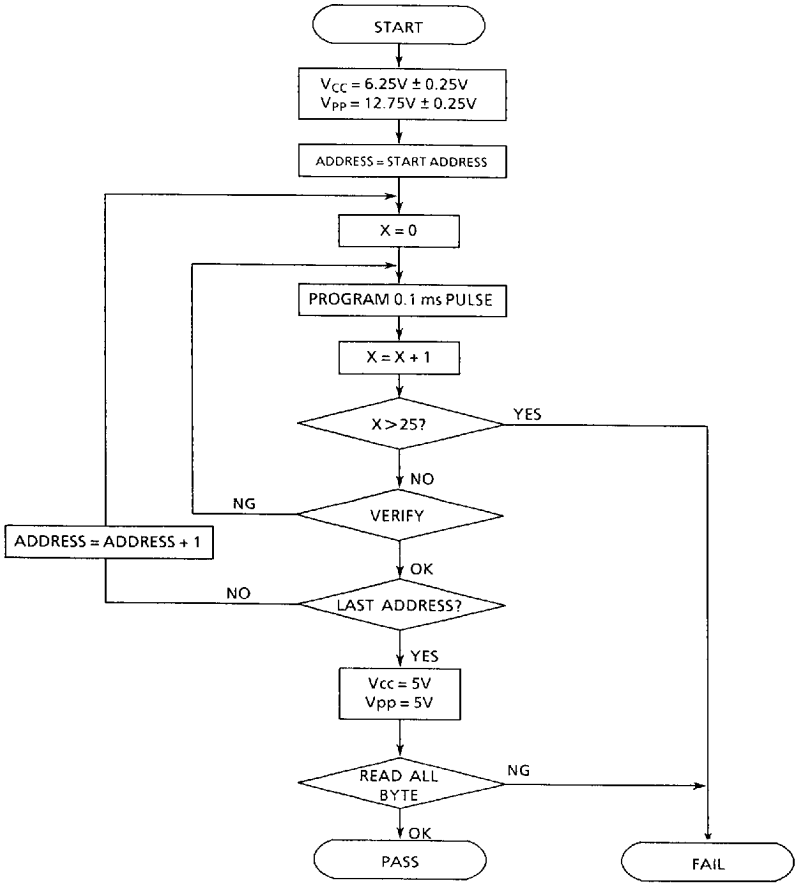


Figure 3.2.2 Flowchart

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS (or note)	RATING	UNIT
Supply voltage	V_{CC}	DVCC1, DVCC2, AVCC1, AVCC2	− 0.5 to + 6.5	V
Programming voltage	V_{PP}	TEST	− 0.5 to + 14	V
Input voltage	V_{IN}		− 0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT1}		− 0.5 to V_{CC} + 0.5	V
Output Current (Per 1 pin)	I_{OUT1}	Analog output pin (Source current)	− 10	mA
	I_{OUT2}	Digital output pin (Source current)	− 3.2	mA
	I_{OUT3}	Analog output pin (Sink current)	10	mA
	I_{OUT4}	Digital output pin (Sink current)	3.2	mA
Output Current (Total)	ΣI_M	$\Sigma I_M = \Sigma I_{OUT1} + \Sigma I_{OUT2}$	− 50	mA
	ΣI_P	$\Sigma I_P = \Sigma I_{OUT3} + \Sigma I_{OUT4}$	100	mA
Power Dissipation (Ta = 70°C)	P_D		700	mW
Soldering Temperature (time)	T_{SOLDER}		260 (10 s)	°C
Storage Temperature	T_{STG}		− 65 to + 150	°C
Operating Temperature	Topr		− 20 to + 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, Topr = − 20 to + 70 °C)

PARAMETER		CONDITION	SYMBOL	Min.	Max.	UNIT
Supply voltage		fc = 16 MHz	V_{CCf}	4.75	5.25	V
		fs = 32 kHz	V_{CCS}	3.00		V
Input High Voltage	Normal input	Vcc ≧ 4.75 V	V_{IH1}	V_{CC} × 0.70	V_{CC}	V
	Hysteresis input	Vcc ≧ 4.75 V	V_{IH2}	V_{CC} × 0.75		V
	Allof degital input	Vcc < 4.75 V	V_{IH3}	V_{CC} × 0.90		V
Input Low Voltage	Normal input	Vcc ≧ 4.75 V	V_{IL1}	0	V_{CC} × 0.30	V
	Hysteresis input	Vcc ≧ 4.75 V	V_{IL2}		V_{CC} × 0.25	V
	Allof degital input	Vcc < 4.75 V	V_{IL3}		V_{CC} × 0.10	V
Clock Frequency	XIN / XOUT		fc	−	16.0	MHz
	XTIN / XTOUT		fs	30.0	34.0	kHz

DC Characteristics (Topr = − 20 to + 70 °C)

PARAMETER		CONDITION	SYMBOL	Min.	Typ.	Max.	UNIT
Digital Current consumption	NORMAL	V_{CC} = 5.5 V fc = 16 MHz, fs = 32.8 kHz	I_{CCO1}	−	60	80	mA
	IDLE		I_{CCL1}	−	25	35	mA
	SLOW	V_{CC} = 3V, 0 ≦ V_{IN} ≦ V_{CC}	I_{CCO2}	−	150	300	μA
	SLEEP		I_{CCL2}	−	80	150	μA
	STOP	V_{CC} = 5.25 V	I_{CCS}	−	−	50	μA
Analog Current consumption	NORMAL	$AV_{CC}1 = AV_{CC}2$ = 5.0 V	I_{CCA}	−	25	40	mA
High-level output voltage		V_{CC} = 4.5V, I_{OH} = − 0.7 mA	V_{IH1}	V_{CC} − 0.4	−	−	V
High-level output voltage		V_{CC} = 4.5V, I_{OH} = − 200 μA	V_{OH2}	2.4	−	−	V
Low-level output voltage		V_{CC} = 4.5V, I_{OL} = 1.6 mA	V_{OL1}	−	−	0.4	V
Low-level output voltage (I²C Bus port)		V_{CC} = 4.5V, I_{OL} = 3.0 mA	V_{OL2}	−	−	0.4	V
Hysteresis voltage			V_{HS}	−	0.70	−	V
INPUT Leakage Current		0 V ≦ Vin ≦ V_{CC}	I_{LI}	−	0.05	± 10	μA
OUTPUT Leakage Current		0.2 V ≦ VOUT ≦ V_{CC} − 0.2 V	I_{LO}	−	0.05	± 10	μA
RESET pin Pull-up resistor		V_{CC} = 5.5V, Vin = 0.2 V	I_{RST}	30	−	120	μA

A/D Conversion characteristic (Topr = − 20 to + 70 °C, V_{CC} = 4.75 to 5.25 V)

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{REF}	V_{CC} − 1.5	V_{CC}	V_{CC}	V
	V_{AGND}	V_{SS}	V_{SS}	V_{SS}	V
Analog Input voltage	V_{AIN}	V_{AGND}		V_{REF}	V
Supply Current for ADREF	I_{REF}	−	0.6	1.0	mA
Total error (Ta = 25 °C, V_{CC} = V_{REF} = 5.0 V)		−	−	± 3	LSB

Characteristics of CTL AMP (Topr = − 20 to + 70 °C, V_{CC} = 5.0 V)

BLOCK	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
CTL BIAS AMP	No load output voltage	V_{CB}	2.4	2.5	2.6	V	No load
	Output voltage (with high load)	V_{CBH}	−	−	+ 70	mV	I si = 5 mA, Difference from V_{CB}
	Output voltage (with low load)	V_{CBL}	− 70	−	−	mV	I so = − 5 mA, Difference from V_{CB}
REC CTL AMP	HIGH output voltage	V_{ROH}	3.2	−	−	V	I so = − 5 mA
	LOW output voltage	V_{ROL}	−	−	1.8	V	I si = 5 mA
	D/A CONVERTER Differential error	V_{RDA}	−	−	$\pm\frac{1}{2}$	LSB	
	SW REC internal resistance	R_{REC}	55	85	130	Ω	ON by SW REC
PB CTL AMP	Input offset voltage	V_{COF}	− 15	−	+ 15	mV	RPCTL terminal
	Input bias current	I_{CIB1}	− 750	−	+ 750	nA	RPCTL terminal
		I_{CIB2}	− 750	−	+ 750	nA	CNFB terminal
	HIGH output voltage	V_{COH}	3.6	−	−	V	I so = − 2 mA
	LOW output voltage	V_{COL}	−	−	1.2	V	I si = 2 mA
	Voltage gain	G_{C1}	−	60	−	dB	f : 1 kHz, Vin : 1 mV, 60 dB
		G_{C2}	−	51	−	dB	f : 10 kHz, Vin : 1 mV, 60 dB
	Feed back resistance	R_{SHORT}	5	10	20	kΩ	Fig 3.20.1 (a) r3, SW internal resistance
		R_{AMP2}	20	40	60	kΩ	Fig 3.20.1 (a) r4, SW internal resistance
	Resistance of Analog SW	R_{PB}	−	−	500	Ω	ON by SWPLY
		R_{BIAS}	−	−	500	Ω	ON by SWBAS
		R_{AMP0}	−	−	500	Ω	ON by <CAMP0>
		R_{AMP1}	−	−	500	Ω	ON by <CAMP1>
CTL PLUS SCHUMITTE	PDP Charge current	I_{CP}	4	−	−	mA	V_{COH} = 3.5 V, V_{PDP} = 2.0 V
	PDP Leakage current	I_{LP}	−	−	− 350	nA	V_{COL} = 1.5 V, V_{PDP} = 2.5 V R_{PDP} : OFF
	PDP Maximum output voltage	V_{OP}	4.3	4.7	−	V	Charge current : 0.1 mA
	PHSPDUP Resistance	R_{PDP}	5	10	20	kΩ	Fig 3.20.1 (a) r5, r6, SW internal resistance
	1/2 level of Peak-hold Schmitt	V_{CSPA}	−	50	−	%	
	Manual Schmitt level	V_{CSP1}	−	100	−	mV	100 mV mode (to V_{CB})
		V_{CSP2}	−	200	−	mV	200 mV mode (to V_{CB})
		V_{CSP3}	−	300	−	mV	300 mV mode (to V_{CB})
		V_{CSP4}	−	500	−	mV	500 mV mode (to V_{CB})
	Noise Limit (plus)	V_{CSPL}	−	100	−	mV	to V_{CB}
CTL MINUS SCHUMITTE	PDM Charge current	I_{CM}	− 4	−	−	mA	V camp = 1.5V, V pdp = 2.5V
	PDM Leakage current	I_{LM}	−	−	− 10	nA	V camp = 3.5V, V pdp = 2.5V R_{PDM} : OFF
	PDM Minimum output voltage	V_{OM}	−	0.3	0.7	V	Charge current : − 0.1 mA
	PHSPDUP Resistance	R_{PDM}	5	10	20	kΩ	
	1/2 level of Peak-hold Schmitt	V_{CSMA}	−	50	−	%	
	Manual Schmitt level	V_{CSM1}	−	− 100	−	mV	− 100 mV mode (to V_{CB})
		V_{CSM2}	−	− 200	−	mV	− 200 mV mode (to V_{CB})
		V_{CSM3}	−	− 300	−	mV	− 300 mV mode (to V_{CB})
		V_{CSM4}	−	− 500	−	mV	− 500 mV mode (to V_{CB})
	Noise Limit (minus)	V_{CSML}	−	− 100	−	mV	(to V_{CB})

Characteristics of CFG AMP (Topr = − 20 to + 70 °C、 V_{CC} = 5.0 V)

BLOCK	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
FG BIAS AMP	No load output voltage	V_{FB}	2.4	2.5	2.6	V	No load
	Output voltage (with high load)	V_{FBH}	−	−	+ 150	mV	I si = 5 mA, Difference from V_{FB}
	Output voltage (with low load)	V_{FBL}	− 150	−	−	mV	I so = − 5 mA, Difference from V_{FB}
FG A AMP	Input offset voltage	V_{FAOF}	− 15	−	+ 15	mV	
	Input bias voltage	V_{FAI}	− 750	−	+ 750	nA	
	HIGH output voltage	V_{FAOH}	4.3	4.7	−	V	I so = − 0.2 mA
	LOW output voltage	V_{FAOL}	−	0.3	0.7	V	I si = 0.2 mA
	Voltage gain	G_{FA1}	−	40	−	dB	f : 1 kHz, Vin : 10mV, 40dB
		G_{FA2}	−	37	−	dB	f : 10 kHz, Vin : 10mV, 40dB
FG B AMP	Input offset voltage	V_{FBOF}	− 15	−	+ 15	mV	
	Input bias voltage	I_{FB1}	− 750	−	+ 750	nA	
	HIGH output voltage	V_{FBOH}	4.3	4.7	−	V	I so = − 0.2 mA
	LOW output voltage	V_{FBOL}	−	0.3	0.7	V	I si = 0.2 mA
	Voltage gain	G_{FB1}	−	40	−	dB	f : 1 kHz, Vin : 10mV, 40dB
		G_{FB2}	−	37	−	dB	f : 10 kHz, Vin : 1mV, 40dB
FG A SCHUMITTE	P Schmitt Voltage 1	V_{FASP1}	−	80	−	mV	80 mV mode (to V_{FB})
	P Schmitt Voltage 2	V_{FASP2}	−	120	−	mV	120 mV mode (to V_{FB})
	M Schmitt Voltage 1	V_{FASM1}	−	− 80	−	mV	− 80 mV mode (to V_{FB})
	M Schmitt Voltage 2	V_{FASM2}	−	− 120	−	mV	− 120 mV mode (to V_{FB})
FG B SCHUMITTE	P Schmitt Voltage 1	V_{FBSP1}	−	80	−	mV	80 mV mode (to V_{FB})
	P Schmitt Voltage 2	V_{FBSP2}	−	120	−	mV	120 mV mode (to V_{FB})
	M Schmitt Voltage 1	V_{FBSM1}	−	− 80	−	mV	− 80 mV mode (to V_{FB})
	M Schmitt Voltage 2	V_{FBSM2}	−	− 120	−	mV	− 120 mV mode (to V_{FB})

Characteristics of OSD AMP (Topr = – 20 to + 70 °C, V_{CC} = 5.0 V)

OUTPUT PIN	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
SC	Bias voltage	V_B	–	2.5	–	V	
	Burst amplitude	V_b	–	0.29	–	V_{P-P}	
	Chroma amplitude 1 / Burst amplitude	V_1 / V_b	–	2.0	–	–	
SY	Sync. tip level	V_S	–	1.60	–	V	
	Sync. to Pedestal	$\triangle V_{SP}$	–	0.60	–	V	$\triangle V_{SP} = V_P - V_S$
	Sync. to Luminance voltage 0	$\triangle V_{S0}$	–	0.66	–	V	$\triangle V_{S0} = V_0 - V_S$
	Sync. to Luminance voltage 1	$\triangle V_{S1}$	–	0.80	–	V	$\triangle V_{S1} = V_1 - V_S$
	Sync. to Luminance voltage 2	$\triangle V_{S2}$	–	1.08	–	V	$\triangle V_{S2} = V_2 - V_S$
	Sync. to Luminance voltage 3	$\triangle V_{S3}$	–	1.50	–	V	$\triangle V_{S3} = V_3 - V_S$
	Sync. to 100% White Level	$\triangle V_{SW}$	–	2.00	–	V	$\triangle V_{SW} = V_W - V_S$
VIDEO	Color Burst amplitude	V_{Cb}	–	0.29	–	V_{P-P}	
	Chroma amplitude 1 / Burst amplitude	V_{C1} / V_{Cb}	–	2.0	–	–	
	Sync. tip level	VI_S	–	1.00	–	V	
	Sync. to Pedestal	$\triangle VI_{SP}$	–	0.30	–	V	$\triangle VI_{SP} = VI_P - VI_S$
	Sync. to Luminance voltage 0	$\triangle VI_{S0}$	–	0.33	–	V	$\triangle VI_{S0} = VI_0 - VI_S$
	Sync. to Luminance voltage 1	$\triangle VI_{S1}$	–	0.40	–	V	$\triangle VI_{S1} = VI_1 - VI_S$
	Sync. to Luminance voltage 2	$\triangle VI_{S2}$	–	0.54	–	V	$\triangle VI_{S2} = VI_2 - VI_S$
	Sync. to Luminance voltage 3	$\triangle VI_{S3}$	–	0.75	–	V	$\triangle VI_{S3} = VI_3 - VI_S$
	Sync. to 100% White Level	$\triangle VI_{SW}$	–	1.00	–	V	$\triangle VI_{SW} = VI_W - VI_S$

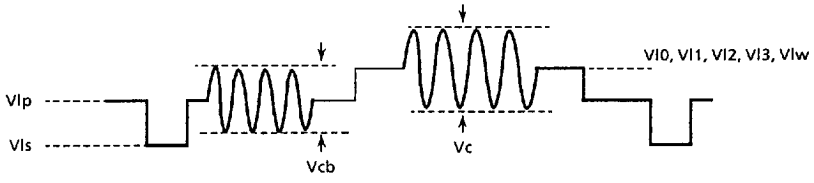


Fig 4.1 OSD VIDEO Output Waveform

Characteristics of PV/BLK (Topr = – 20 to + 70 °C、 V_{CC} = 5.00 V)

MODE	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
MIXOFF = 0	HIGH output voltage	V_H	4.70	–	5.00	V	I = + 100 μA
	MIDDLE-HIGH output voltage	VM2	3.00	3.30	3.60	V	I = ± 10 μA
	MIDDLE-LOW output voltage a	VM1a	1.30	1.60	2.00	V	I = ± 100 μA
	MIDDLE-LOW output voltage b	VM1b	1.30	1.60	2.00	V	I = ± 10 μA
	LOW output voltage	V_L	0.00	–	0.30	V	I = – 100 μA
MIXOFF = 1	HIGH output voltage	V_H	4.70	–	–	V	I = + 100 μA
	LOW output voltage	V_L	–	–	0.30	V	I = – 100 μA

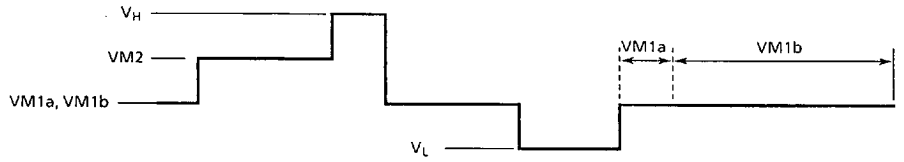


Fig 4.2 PV / BLK Output Waveform

DC Characteristic, AC Characteristic (PROM mode) (V_{SS} = 0V)

(1) Read Operation (PROM mode)
DC Characteristic, AC Characteristic

TA = −20 to 70°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	0.7 × V_{CC}	V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	−0.3	0.3 × V_{CC}	V
t_{ACC}	Address to Output Delay	C_L = 50pF	–	2.25TCYC + α	ns

TCYC = 250ns (16 MHz Clock)
α = 100ns

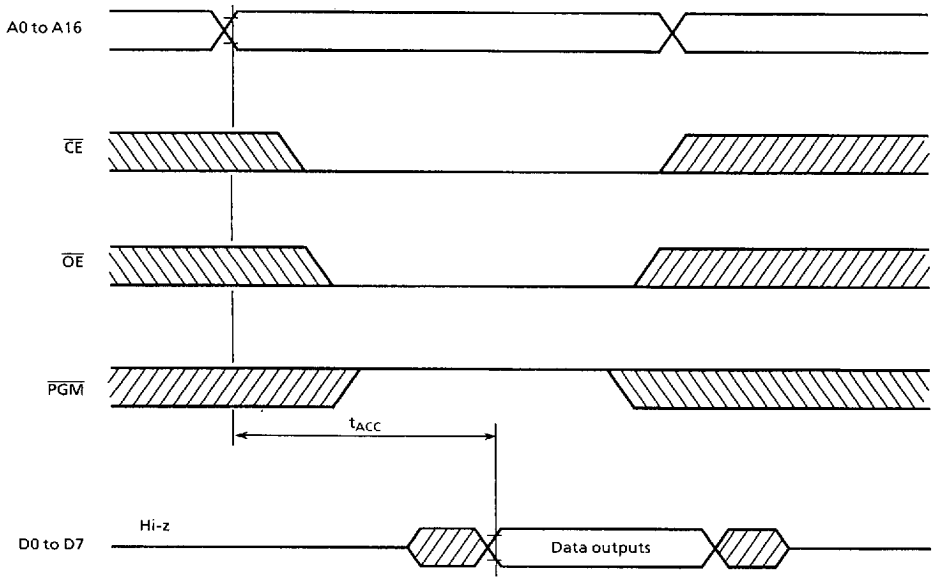
(2) Programming Operation (PROM mode)
DC Characteristic, AC Characteristic

TA = 25 ± 5°C Vcc = 6.25V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programing Algorithm	–	12.50	12.75	13.00	V
V_{IH}	Input High Voltage (D0 to D7)	–	0.2V_{CC} + 1.1		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 to D7)	–	−0.3		0.2V_{CC}-0.1	V
V_{IH1}	Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	−0.3		0.3V_{CC}	V
t_{PW}	$\overline{CE}$ Program Pulse Width	V_{PP} = 12.75V	0.095	0.1	0.105	ms

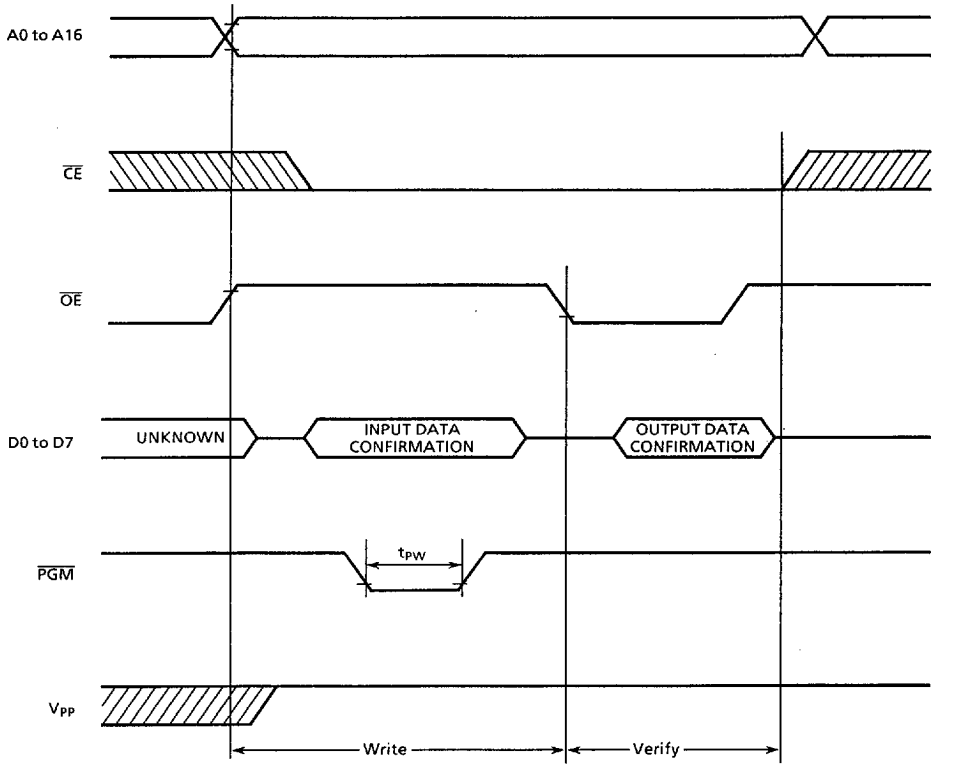
4.1 DC/AC Characteristic

Read Operation Timing Chart (PROM mode)



4.2 Program Operation Timing Chart (PROM mode)

High Speed Program Formula



Note 1) Force VPP (12.75V) power supply and V_{CC} power supply at the same time, or V_{PP} (12.75V) power supply later than V_{CC} power supply. And interrupt VPP (12.75V) power supply and V_{CC} power supply at the same time, or V_{PP} (12.75V) power supply before V_{CC} power supply.

2) Please attend to drawing and rising in the programming (mode) in 12.75V to the V_{PP} as there is some possibility that you give "DAMAGE" to the devices.

3) Don't force more than 14V (voltage) including over shoot to the V_{PP} pin in the programming as maximum rating of V_{PP} pin is 14V (voltage).