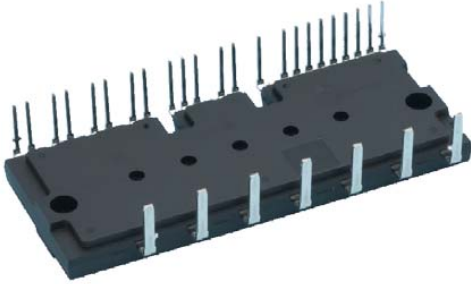


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## OUTLINE



## MAIN FEATURES AND RATINGS

- 3 phase DC/AC inverter
- 1200V / 5A
- Built-in LPT-CSTBT (5th generation IGBT)
- Insulated transfer molding package
- N-side IGBT open emitter

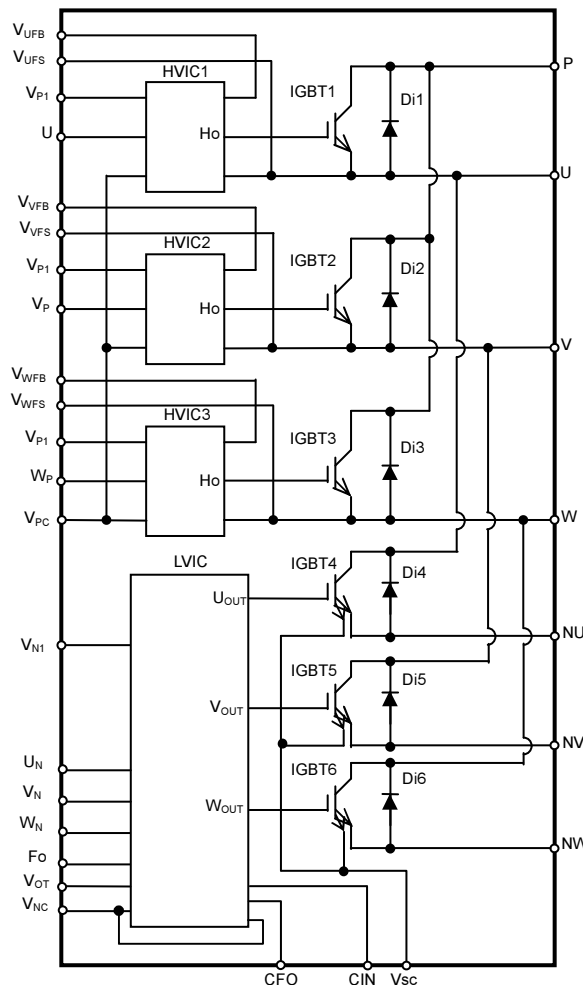
## APPLICATION

- AC 400V class motor control

## INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC)
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E80276

## INTERNAL CIRCUIT



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**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC}$	Supply voltage	Applied between P-NU,NV,NW	900	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	1000	V
$V_{CES}$	Collector-emitter voltage		1200	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$	5	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$ , up to 1ms	10	A
$P_C$	Collector dissipation	$T_C = 25^\circ\text{C}$ , per 1 chip	44.6	W
$T_j$	Junction temperature		-20~+150	$^\circ\text{C}$

**CONTROL (PROTECTION) PART**

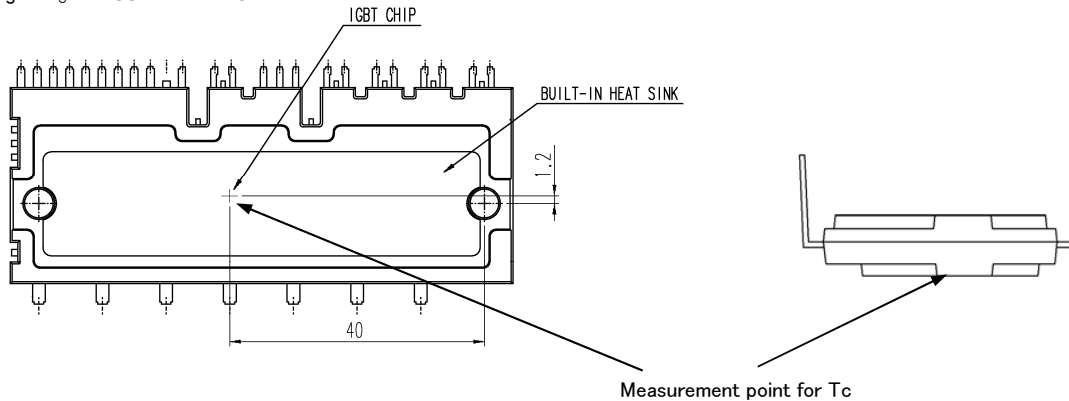
Symbol	Parameter	Condition	Ratings	Unit
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{PC}$ , $V_{N1}-V_{NC}$	20	V
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	20	V
$V_{IN}$	Input voltage	Applied between $U_P$ , $V_P$ , $W_P-V_{PC}$ , $U_N$ , $V_N$ , $W_N-V_{NC}$	-0.5~ $V_D+0.5$	V
$V_{FO}$	Fault output supply voltage	Applied between $F_O-V_{NC}$	-0.5~ $V_D+0.5$	V
$I_{FO}$	Fault output current	Sink current at $F_O$ terminal	1	mA
$V_{SC}$	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$ , Inverter Part $T_j = 125^\circ\text{C}$ , non-repetitive, up to 2 $\mu\text{s}$	800	V
$T_C$	Module case operation temperature	(Note 1)	-20~+100	$^\circ\text{C}$
$T_{stg}$	Storage temperature		-40~+125	$^\circ\text{C}$
$V_{iso}$	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	$V_{rms}$

Note 1:  $T_C$  measurement point is described in Fig. 1.

Fig. 1:  $T_C$  MEASUREMENT POINT



**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 2)	Inverter IGBT part (per 1/6 module)	-	-	2.24	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	2.74	K/W

Note 2: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100 $\mu\text{m}$ ~+200 $\mu\text{m}$  on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink  $R_{th(c-f)}$  is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  is about 0.2K/W (per 1/6 module, grease thickness: 20 $\mu\text{m}$ , thermal conductivity: 1.0W/m $\cdot$ k).

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**ELECTRICAL CHARACTERISTICS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15\text{V}, V_{IN}= 5\text{V}, I_C= 5\text{A}$	$T_j= 25^\circ\text{C}$	-	1.90	2.60	V
			$T_j= 125^\circ\text{C}$	-	2.00	2.70	
$V_{EC}$	FWDi forward voltage	$V_{IN}= 0\text{V}, -I_C= 5\text{A}$	-	2.20	2.80	V	
$t_{on}$	Switching times	$V_{CC}= 600\text{V}, V_D= V_{DB}= 15\text{V}$ $I_C= 5\text{A}, T_j= 125^\circ\text{C}, V_{IN}= 0\leftrightarrow 5\text{V}$ Inductive Load (upper-lower arm)		0.50	1.20	1.90	$\mu\text{s}$
$t_{C(on)}$				-	0.60	0.90	$\mu\text{s}$
$t_{off}$				-	2.40	3.50	$\mu\text{s}$
$t_{C(off)}$				-	0.60	0.90	$\mu\text{s}$
$t_{rr}$				-	0.50	-	$\mu\text{s}$
$I_{CES}$	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	$T_j= 25^\circ\text{C}$	-	-	1	mA
			$T_j= 125^\circ\text{C}$	-	-	10	

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$I_D$	Circuit current	Total of $V_{P1}-V_{PC}, V_{N1}-V_{NC}$	$V_D=15\text{V}, V_{IN}=0\text{V}$	-	-	5.60	mA
			$V_D=15\text{V}, V_{IN}=5\text{V}$	-	-	5.60	
$I_{DB}$		Each part of $V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}$	$V_D=V_{DB}=15\text{V}, V_{IN}=0\text{V}$	-	-	1.10	mA
			$V_D=V_{DB}=15\text{V}, V_{IN}=5\text{V}$	-	-	1.10	
$I_{SC}$	Short circuit trip level	$-20^\circ\text{C}\leq T_j\leq 125^\circ\text{C}, R_s= 261\Omega (\pm 1\%),$ Not connecting outer shunt resistors to NU, NV, NW terminals (Note 3)	8.5	-	-	A	
$UV_{DBt}$	P-side Control supply under-voltage protection(UV)	$T_j\leq 125^\circ\text{C}$	Trip level	10.0	-	12.0	V
$UV_{DBr}$			Reset level	10.5	-	12.5	V
$UV_{Dt}$	N-side Control supply under-voltage protection(UV)	$T_j\leq 125^\circ\text{C}$	Trip level	10.3	-	12.5	V
$UV_{Dr}$			Reset level	10.8	-	13.0	V
$V_{FOH}$	Fault output voltage	$V_{SC} = 0\text{V}, F_O$ terminal pulled up to 5V by 10k $\Omega$	4.9	-	-	V	
$V_{FOL}$		$V_{SC} = 1\text{V}, I_{FO} = 1\text{mA}$	-	-	0.95	V	
$t_{FO}$	Fault output pulse width	$C_{FO}=22\text{nF}$ (Note 4)	1.6	2.4	-	ms	
$I_{IN}$	Input current	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA	
$V_{th(on)}$	ON threshold voltage	Applied between $U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}$		-	-	3.5	V
$V_{th(off)}$	OFF threshold voltage			0.8	-	-	
$V_{OT}$	Temperature output	LVIC temperature = 85 $^\circ\text{C}$ (Note 5)	3.57	3.63	3.69	V	

Note 3: Short circuit protection detects sense current divided from main current at N-side IGBT and works for N-side IGBT only. In the case that outer shunt resistor is inserted into main current path, protection current level  $I_{SC}$  changes. For details, please refer the application note for this DIPIPM.

4: Fault signal is output when short circuit or N-side control supply under-voltage protection works. The fault output pulse-width  $t_{FO}$  depends on the capacitance of  $C_{FO}$ . ( $C_{FO}(\text{typ.}) = t_{FO} \times (9.1 \times 10^{-6})$  [F])

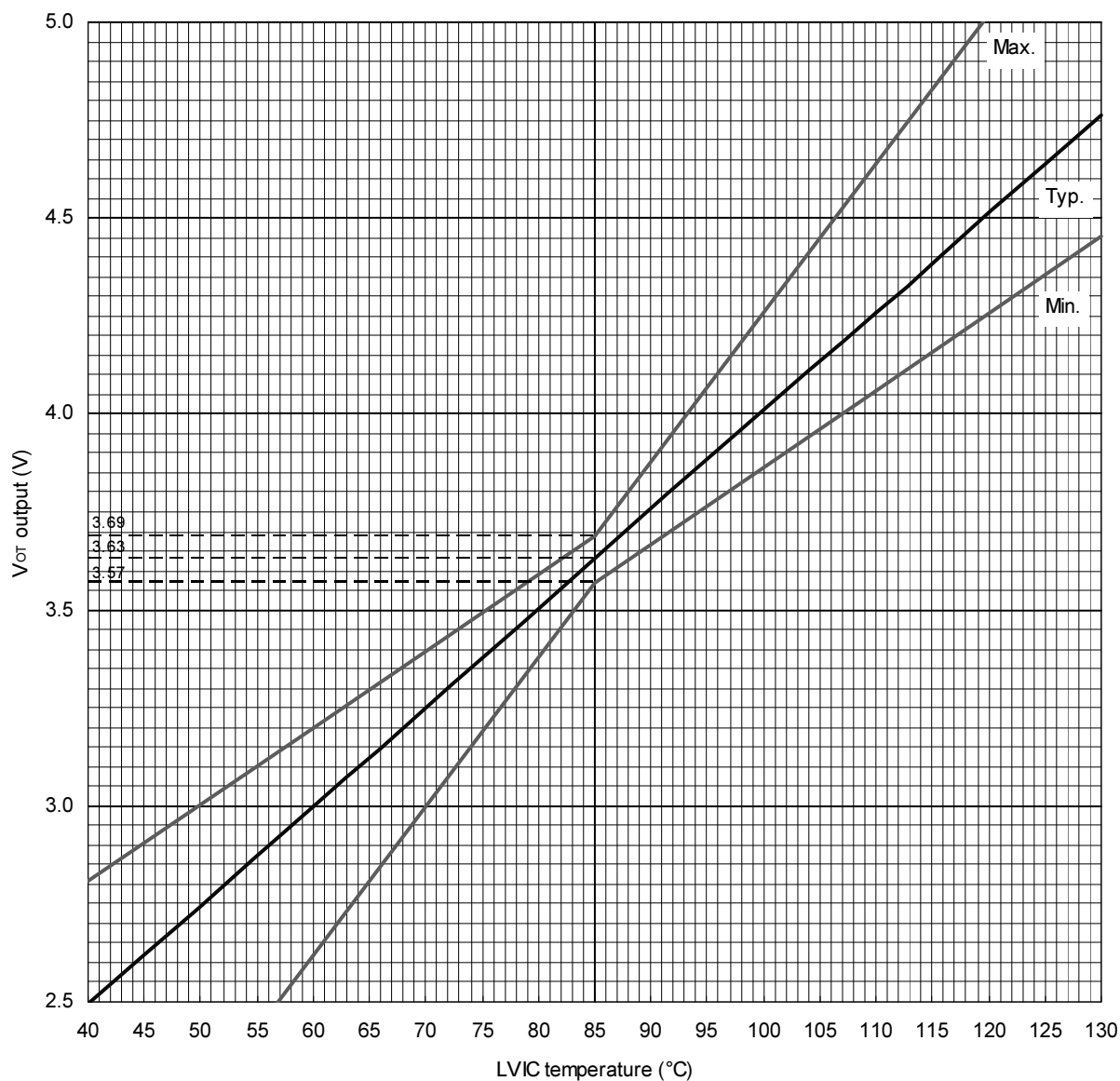
5: DIPIPM doesn't shut down IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM immediately. This output might exceed 5V when temperature rises excessively, so it is recommended to insert a clamp Di between controller supply (e.g. 5V) and  $V_{OT}$  output for overvoltage protection. Temperature of LVIC vs.  $V_{OT}$  output characteristics is described in Fig.2

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Fig. 2 Temperature of LVIC vs.  $V_{OT}$  Output Characteristics



Please refer the application note about the usage of  $V_{OT}$  too.

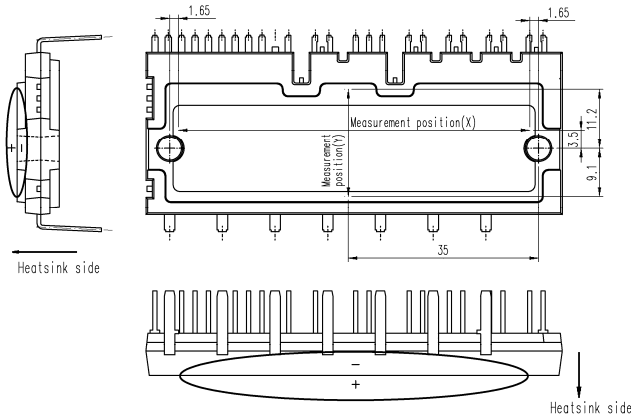
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## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18N·m	0.98	1.18	1.47	N·m
Terminal pulling strength	Load 19.6N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Load 9.8N, 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	46	-	g
Heat-sink flatness		(Note 6)	-50	-	100	μm

Note 6: Measurement point of heat-sink flatness



## RECOMMENDED OPERATION CONDITIONS

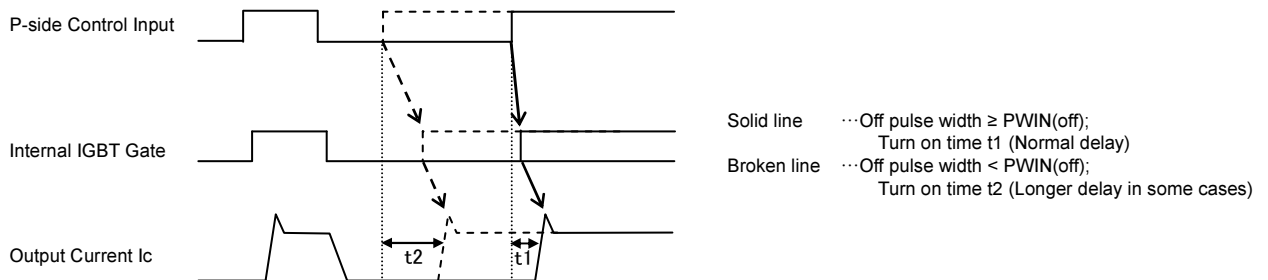
Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	350	600	800	V	
$V_D$	Control supply voltage	Applied between $V_{P1}$ - $V_{PC}$ , $V_{N1}$ - $V_{NC}$	13.5	15.0	16.5	V	
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}$ - $V_{UFS}$ , $V_{VFB}$ - $V_{VFS}$ , $V_{WFB}$ - $V_{WFS}$	13.0	15.0	18.5	V	
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	+1	V/μs	
$t_{dead}$	Arm shoot-through blocking time	For each input signal	3.0	-	-	μs	
$f_{PWM}$	PWM input frequency	$T_C \leq 100^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$	-	-	20	kHz	
$I_O$	Allowable r.m.s. current	$V_{CC} = 600\text{V}$ , $V_D = 15\text{V}$ , P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$ (Note 7)				A rms	
		$f_{PWM} = 5\text{kHz}$	-	-	2.7		
		$f_{PWM} = 15\text{kHz}$	-	-	1.9		
PWIN(on)	Minimum input pulse width	(Note 8)	2.0	-	-	μs	
PWIN(off)		$350 \leq V_{CC} \leq 800\text{V}$ , $13.5 \leq V_D \leq 16.5\text{V}$ , $13.0 \leq V_{DB} \leq 18.5\text{V}$ , $-20^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$ , N line wiring inductance less than 10nH (Note 9)	$I_C \leq 5\text{A}$	2.5	-		-
		$5 < I_C \leq 8.5\text{A}$	2.9	-	-		
$V_{NC}$	$V_{NC}$ variation	Between $V_{NC}$ -NU, NV, NW (including surge)	-5.0	-	+5.0	V	
$T_J$	Junction temperature		-20	-	+125	°C	

Note 7: The allowable r.m.s. current value depends on the actual application conditions.

Note 8: DIPIPM might not make response to the input on signal with pulse width less than PWIN (on).

Note 9: IPM might make no response or delayed response (P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Please refer Fig. 3 about delayed response.

Fig. 3 About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



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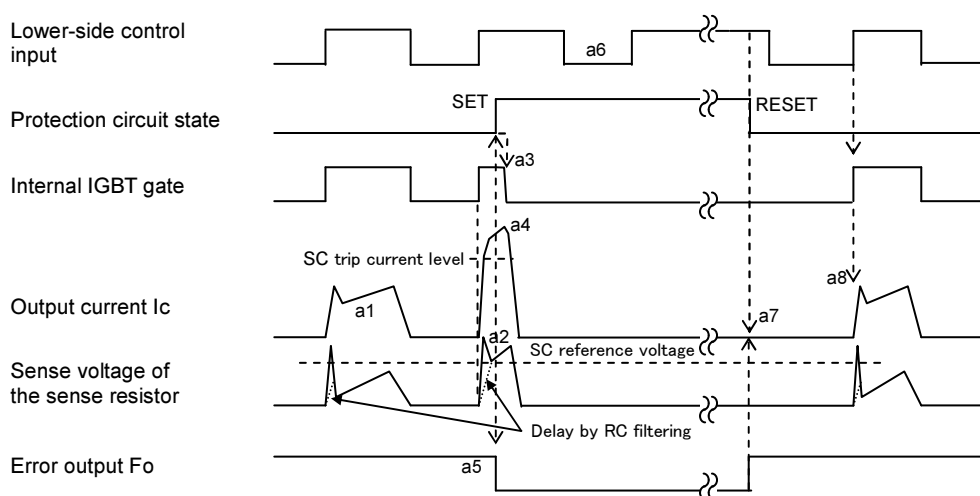
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Fig. 4 Timing Charts of DIIPM Protective Functions

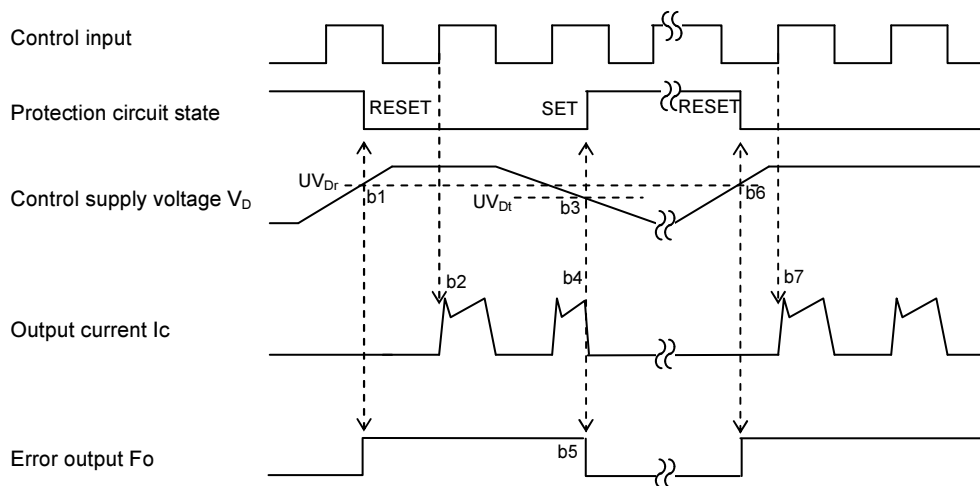
[A] Short-Circuit Protection (N-side only with the external sense resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)  
(It is recommended to set RC time constant 1.5~2.0 $\mu$ s so that IGBT shut down within 2.0 $\mu$ s when SC occurs.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. F<sub>O</sub> outputs with a fixed pulse width determined by the external capacitor C<sub>FO</sub>.
- a6. Input = "L": IGBT OFF
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.



[B] Under-Voltage Protection (N-side, UV<sub>D</sub>)

- b1. Control supply voltage V<sub>D</sub> exceeds under voltage reset level (UV<sub>Dr</sub>), but IGBT turns ON by next ON signal (L→H).  
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3. V<sub>D</sub> level drops to under voltage trip level. (UV<sub>Dt</sub>).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. Fo outputs for the period determined by the capacitance C<sub>FO</sub>, but output is extended during V<sub>D</sub> keeps below UV<sub>Dr</sub>.
- b6. V<sub>D</sub> level reaches UV<sub>Dr</sub>.
- b7. Normal operation: IGBT ON and outputs current by next ON signal (L→H).



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### [C] Under-Voltage Protection (P-side, $UV_{DB}$ )

- c1. Control supply voltage  $V_{DB}$  rises. After the voltage reaches under voltage reset level  $UV_{DBr}$ , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3.  $V_{DB}$  level drops to under voltage trip level ( $UV_{DBt}$ ).
- c4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no  $F_o$  signal output.
- c5.  $V_{DB}$  level reaches  $UV_{DBr}$ .
- c6. Normal operation: IGBT ON and outputs current by next ON signal (L→H).

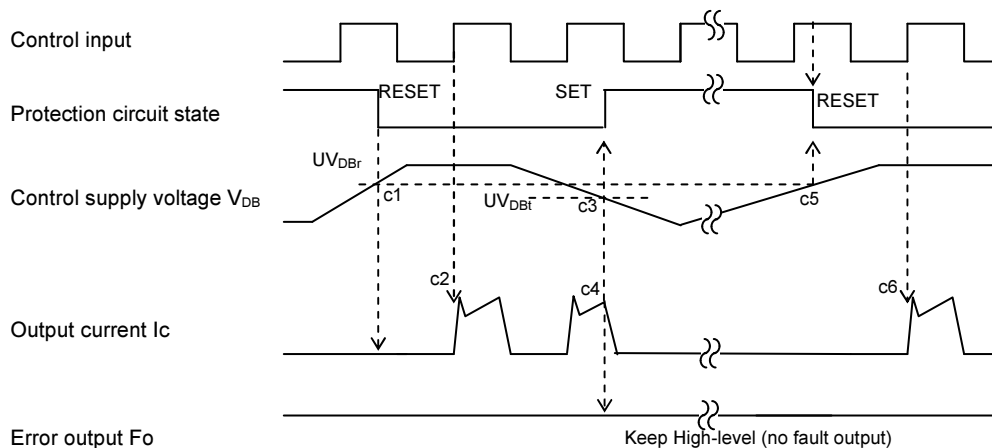
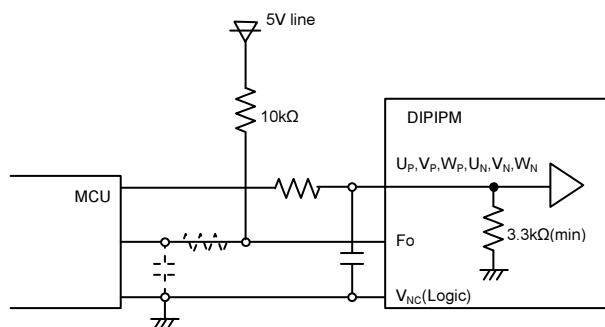


Fig. 5 MCU I/O Interface Circuit

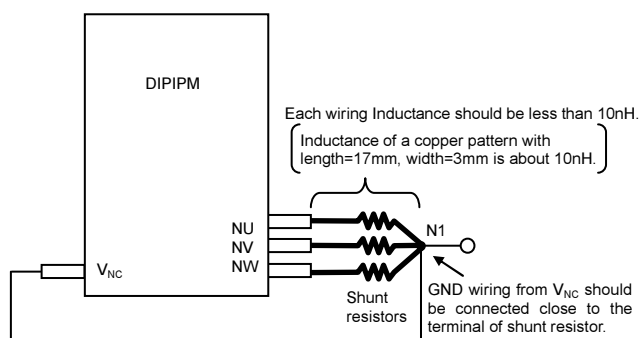


Note)

Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. But because noisier in the application for 1200V, it is strongly recommended to insert RC filter. (Time constant: over 100ns. e.g. 100Ω, 1000pF) The DIPIPM input signal interface integrates a min. 3.3kΩ pull-down resistor. Therefore, when using RC filter, be careful to satisfy turn-on threshold voltage requirement.

$F_o$  output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits  $F_o$  sink current  $I_{F_o}$  under 1mA. In the case of pulling up to 5V supply, over 5.1kΩ is needed. (10kΩ is recommended.)

Fig. 6 Wiring Pattern around the Shunt Resistor in the Case of Inserting into Main Current Path

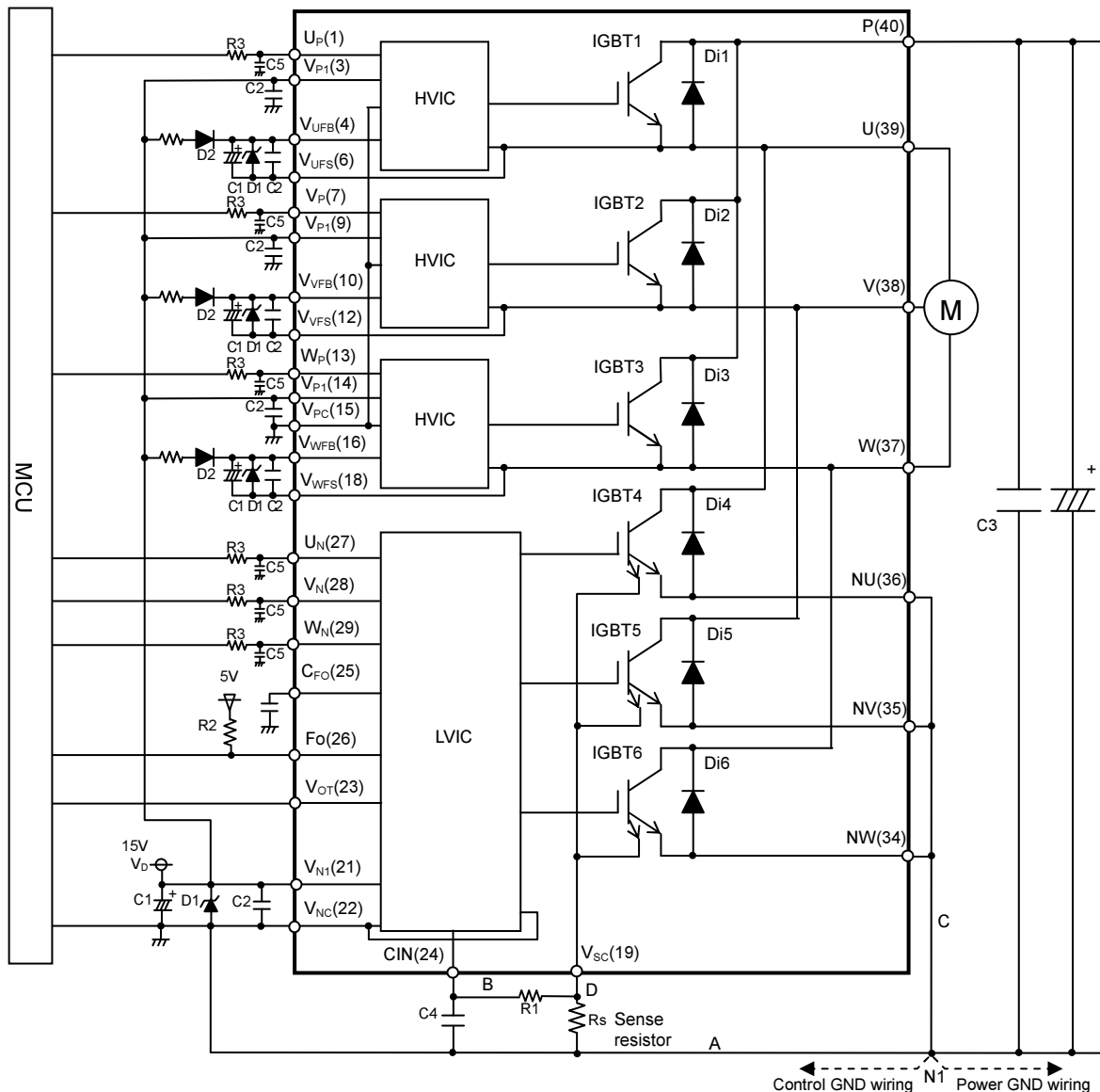


Low inductance shunt resistor like surface mounted (SMD) type is recommended. Protection current level  $I_{sc}$  changes by inserting shunt resistor.

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Fig. 7 Example of Application Circuit



**Note**

- 1: If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.
- 2: It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 3: To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally inserting a 0.1 $\mu$ ~0.22 $\mu$ F snubber capacitor C3 between the P-N1 terminals is recommended.
- 4: R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2 $\mu$ s. (1.5 $\mu$ s~2 $\mu$ s is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may lead to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)
- 5: To prevent erroneous operation, the wiring of A, B, C should be as short as possible.
- 6: For sense resistor, the variation within 1% (including temperature characteristics), low inductance type is recommended. And the over 1/8W is recommended, but it is necessary to evaluate in your real system finally.
- 7: To prevent erroneous SC protection, the wiring from Vsc terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.
- 8: All capacitors should be mounted as close to the terminals of the DIPIM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.22 $\mu$ ~2.0 $\mu$ F, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- 9: Input drive is High-active type. There is a min. 3.3k $\Omega$  pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. And it is strongly recommended to insert RC filter (e.g. R3=100 $\Omega$  and C5=1000pF) and confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
- 10: Fof output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V, 15V) by a resistor that makes IFof up to 1mA. (IFof is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10k $\Omega$  (5k $\Omega$  or more) is recommended.)
- 11: Error signal output width (tFo) can be set by the capacitor connected to Cfo terminal. Cfo(typ.) = tFo x (9.1 x 10<sup>-6</sup>) (F)
- 12: High voltage (VRRM = 1200V or more) and fast recovery diode (trr < less than 100ns or less) should be used for D2 in the bootstrap circuit.
- 13: If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt  $\leq$  +/-1V/ $\mu$ s, Vripple  $\leq$  2Vp-p.
- 14: For DIPIM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIM.



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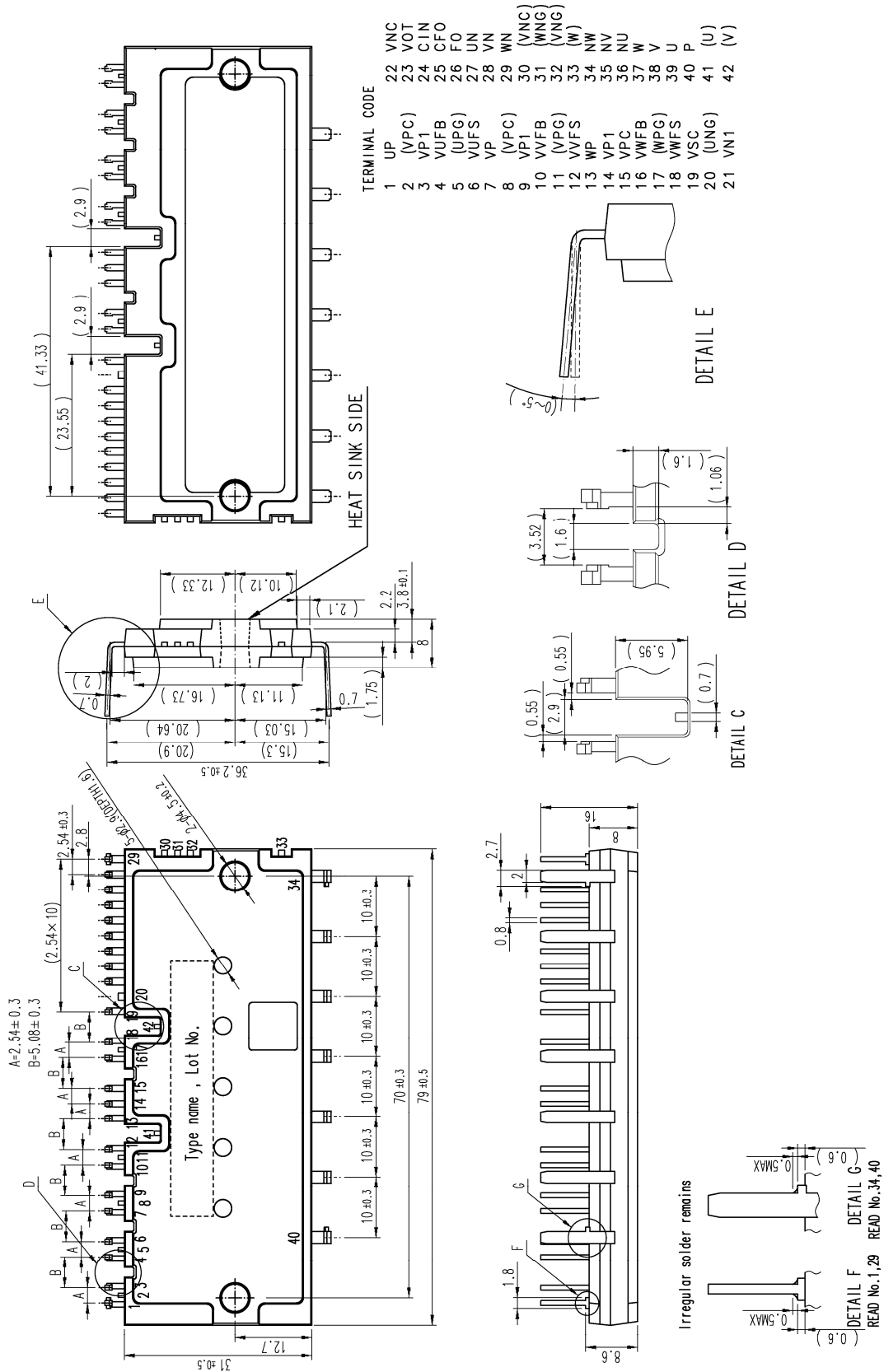
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Fig. 8 Package Outlines

Dimensions in mm



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Revision Record

Rev.	Date	Page	Revised contents
1	3/15/2011	-	New
2	1/31/2012	-	Change document format
		7	Add Fig.6.
		8	Revise notes.

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