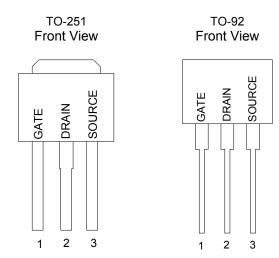


GENERAL DESCRIPTION

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

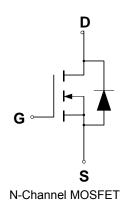
PIN CONFIGURATION



FEATURES

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and V_{DS}(on) Specified at Elevated Temperature

SYMBOL



ABSOLUTE MAXIMUM RATINGS

Rating		Value	Unit
Drain to Current – TO-251(Continuous)		1.0	
TO-92 (Continuous)		0.5	А
 Pulsed 	I _{DM}	2.0	
Gate-to-Source Voltage — Continue		±30	V
 Non-repetitive 	V _{GSM}	±40	V
Total Power Dissipation			
TO-251		30	W
TO-92		3	
Operating and Storage Temperature Range		-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy $-$ T _J = 25 $^\circ\!\mathbb{C}$		20	mJ
(V _{DD} = 100V, V _{GS} = 10V, I _{AS} = 2A, L = 10mH, R _G = 25Ω)			
Thermal Resistance – Junction to Case		1.0	°C/W
 Junction to Ambient 	θ _{JA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C



ORDERING INFORMATION

Part Number	Package
CMT01N60GN251	TO-251
CMT01N60XN251*	TO-251
CMT01N60GN92	TO-92
CMT01N60XN92*	TO-92

*Note: G : Suffix for Pb Free Product

X : Suffix for Halogen Free Product

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 25 $^\circ\!\mathrm{C}$.

				CMT01N60)	
Cha	racteristic	Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		V _{(BR)DSS}	600			V
$(V_{GS} = 0 V, I_D = 250 \mu A)$						
Drain-Source Leakage Current						
(V _{DS} = 600 V, V _{GS} = 0 V) (V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125℃)		I _{DSS}			1	uA
					3	
Gate-Source Leakage Current-Forward					100	0
$(V_{gsf} = 30 \text{ V}, V_{DS} = 0 \text{ V})$		I _{GSSF}			100	nA
Gate-Source Leakage Current-Reverse					100	nA
(V _{gsr} =- 30 V, V _{DS} = 0 V)		I _{GSSR}			100	ΠA
Gate Threshold Voltage		N _e	2.0		4.0	V
$(V_{DS} = V_{GS}, I_D = 250 \ \mu A)$		$V_{GS(th)}$	2.0		4.0	
Static Drain-Source On-Resistan	ce (V _{GS} = 10 V, I _D = 0.5A) *					
TO-251		R _{DS(on)}			11	Ω
TO-92						
Forward Transconductance (V_{DS} \geq 50 V, I _D = 0.5A) *		g fs		320		mhos
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$	C _{iss}		210		pF
Output Capacitance	$(v_{DS} = 25 \text{ v}, v_{GS} = 0 \text{ v}, f = 1.0 \text{ MHz})$	C _{oss}		28		pF
Reverse Transfer Capacitance	1 - 1.0 (MI 12)	Crss		4.2		pF
Turn-On Delay Time	(V _{DD} = 300 V, I _D = 1.0 A,	t _{d(on)}		8		ns
Rise Time	$V_{DD} = 300 \text{ V}, \text{ ID} = 1.0 \text{ A},$ $V_{GS} = 10 \text{ V},$	tr		21		ns
Turn-Off Delay Time	$R_{\rm G} = 18\Omega$) *	t _{d(off)}		18		ns
Fall Time	$R_{\rm G} = 18\Omega$	t _f		24		ns
Total Gate Charge	(V _{DS} = 400 V, I _D = 1.0 A,	Qg		8.5		nC
Gate-Source Charge	$V_{GS} = 400 \text{ V}, \text{ ID} = 1.0 \text{ A},$ $V_{GS} = 10 \text{ V})^*$	Q _{gs}		1.8		nC
Gate-Drain Charge	VGS = 10 V)	Q _{gd}		4		nC
Internal Drain Inductance	ternal Drain Inductance			4.5		nH
(Measured from the drain lead	0.25" from package to center of die)					
Internal Drain Inductance		Ls		7.5		nH
•	d 0.25" from package to source bond					
pad)						
SOURCE-DRAIN DIODE CHAR	ACTERISTICS				· · -	
Forward On-Voltage(1)	(I _S = 1.0 A, V _{GS} = 0 V,	V _{SD}		**	1.5	V
Forward Turn-On Time	$d_{IS}/d_t = 100A/\mu s$)	t _{on}				ns
Reverse Recovery Time	• • •	trr		350		ns

* Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%

** Negligible, Dominated by circuit inductance



TYPICAL ELECTRICAL CHARACTERISTICS

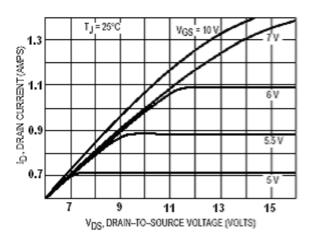


Figure 1. On-Region Characteristics

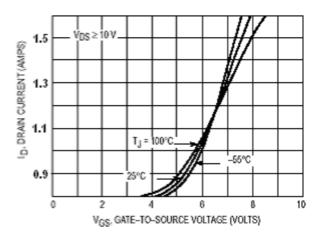
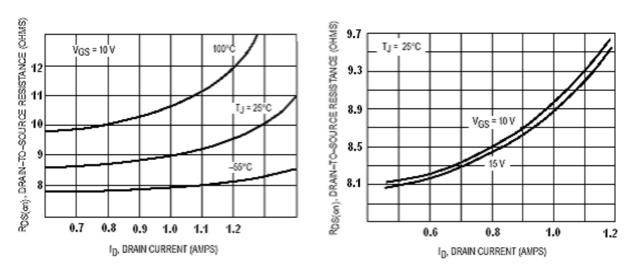


Figure 2. Transfer Characteristics





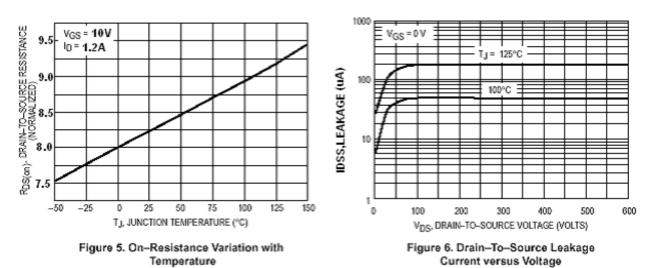
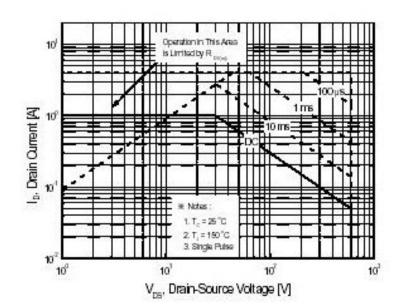


Figure 3. On–Resistance versus Drain Current and Temperature

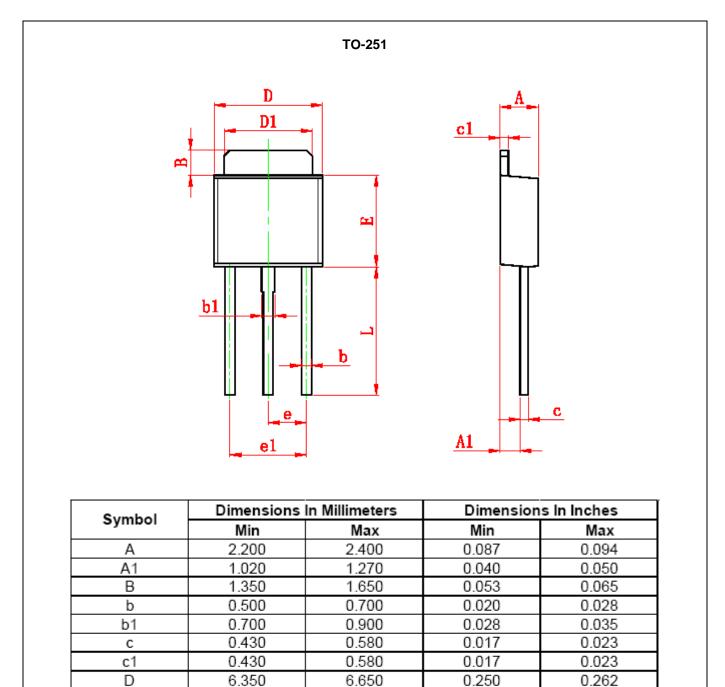
Figure 4. On–Resistance versus Drain Current and Gate Voltage



Maximum Safe Operating Area



PACKAGE DIMENSION



D1

Е

е

e1

L

5.400

5.700

4.700

7.900

2.300 TYP

0.205

0.213

0.177

0.295

0.091 TYP

5.200

5.400

4.500

7.500

0.213

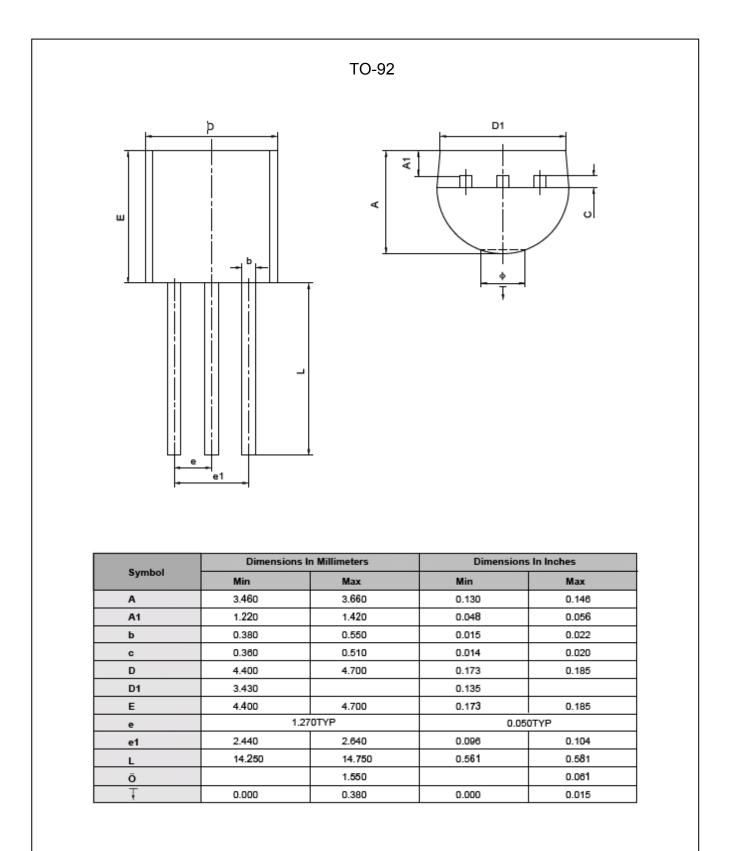
0.224

0.185

0.311



CMT01N60 Power Field Effect Transistor





IMPORTANT NOTICE

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HsinChu Headquarter	Sales & Marketing
5F-1, No. 11, Park Avenue II, Science-Based Industrial Park,	21F., No. 96, Sec. 1, Sintai 5th Rd., Sijhih City, Taipei County 22102,
HsinChu City, Taiwan	Taiwan R.O.C
TEL: +886-3-567 9979	TEL: +886-2-2696 3558
FAX: +886-3-567 9909	FAX: +886-2-2696 3559