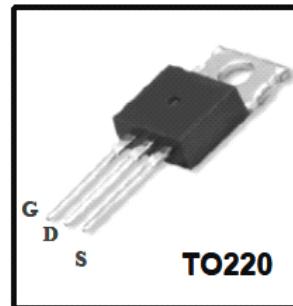
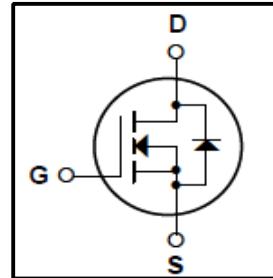


Silicon N-Channel MOSFET
Features

- 8A,500V,RDS(on)(Max 0.8Ω)@VGS=10V
- Ultra-low Gate Charge(Typical 59nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150°C)


General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for high efficiency switch model power supplies, power factor correction and half bridge and full bridge resonant topology line a Electronic lamp ballast.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	500	V
I_D	Continuous Drain Current(@ $T_c=25^\circ C$)	8	A
	Continuous Drain Current(@ $T_c=100^\circ C$)	5.1	A
I_{DM}	Drain Current Pulsed	(Note1)	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Total Power Dissipation(@ $T_c=25^\circ C$)	134	W
	Derating Factor above 25°C	1.0	W/C
T_J, T_{stg}	Junction and Storage Temperature	-55~150	°C
T_L	Channel Temperature	300	°C

*Drain current limited by junction temperature

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	0.93	°C/W
R_{QCS}	Thermal Resistance, Case-to-Sink	-	0.5	-	°C/W
R_{QJA}	Thermal Resistance, Junction-to-Ambient	-	-	62	°C/W

Electrical Characteristics (T_c = 25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G = ±10 μA, V _{DS} = 0 V	±30	-	-	V	
Drain cut-off current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V	-	-	10	μA	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 250 μA, V _{GS} = 0 V	500	-	-	V	
Break Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C	-	0.5	-	V/°C	
Gate threshold voltage	V _{GS(th)}	V _{DS} = 10 V, I _D = 250 μA	2	-	4	V	
Drain-source ON resistance	R _{DSD(ON)}	V _{GS} = 10 V, I _D = 4.0 A	-	-	0.80	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 40 V, I _D = 4.0 A	-	7.3	-	S	
Input capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	1400	1800	pF	
Reverse transfer capacitance	C _{rss}		-	34	44		
Output capacitance	C _{oss}		-	145	190		
Switching time	Rise time	tr	V _{DD} = 250 V, I _D = 8 A R _G = 9.1 Ω R _D = 31 Ω (Note 4,5)	-	22	55	ns
	Turn-on time	t _{on}		-	65	140	
	Fall time	t _f		-	125	260	
	Turn-off time	t _{off}		-	75	160	
Total gate charge (gate-source plus gate-drain)	Q _g	V _{DD} = 400 V, V _{GS} = 10 V, I _D = 8 A (Note 4,5)	-	59	70	nC	
Gate-source charge	Q _{gs}		-	7	9		
Gate-drain ("miller") Charge	Q _{gd}		-	28	32		

Source-Drain Ratings and Characteristics (T_a = 25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	8	A
Pulse drain reverse current	I _{DRP}	-	-	-	32	A
Forward voltage (diode)	V _{DSF}	I _{DR} = 8 A, V _{GS} = 0 V	-	-	1.4	V
Reverse recovery time	t _{rr}	I _{DR} = 8 A, V _{GS} = 0 V, dI _{DR} / dt = 100 A / μs	-	390	-	ns
Reverse recovery charge	Q _{rr}		-	4.2	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=9mH,I_{AS}=8A,V_{DD}=50V,R_G=25Ω,Starting T_J=25°C

3.I_{SD}≤8A,di/dt≤300A/us, V_{DD}<BV_{DSS},STARTING T_J=25°C

4.Pulse Test: Pulse Width≤300us,Duty Cycles≤2%

5.Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

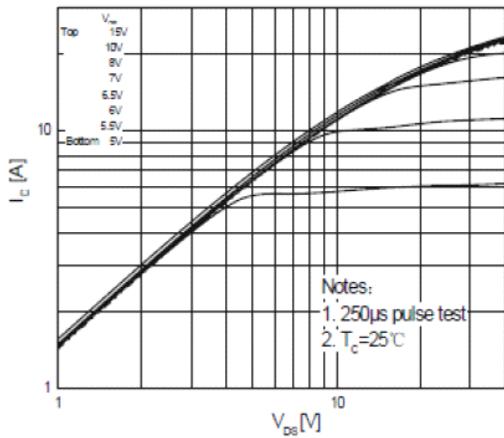


Fig. 1 On-State Characteristics

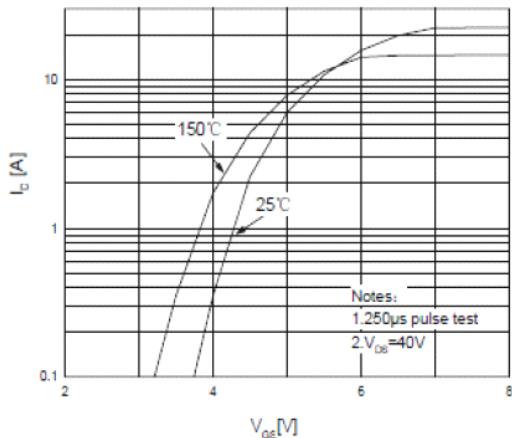


Fig.2 Transfer Characteristics

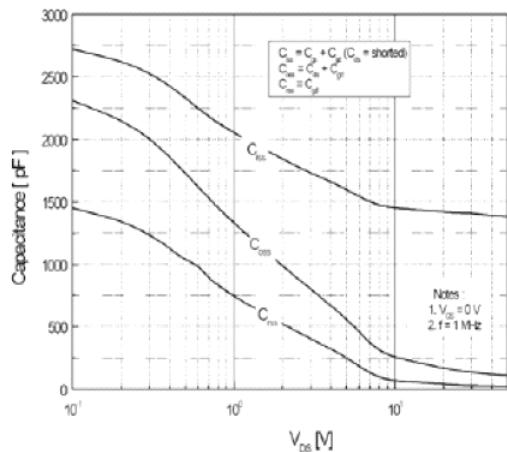


Fig.3 Capacitance Variation vs Drain Voltage

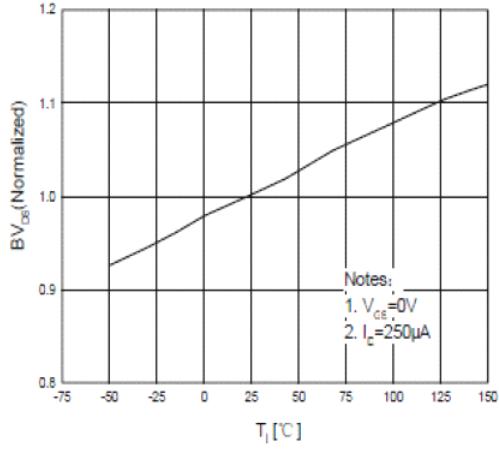


Fig.4 Maximum Avalanche Energy vs On-State Current

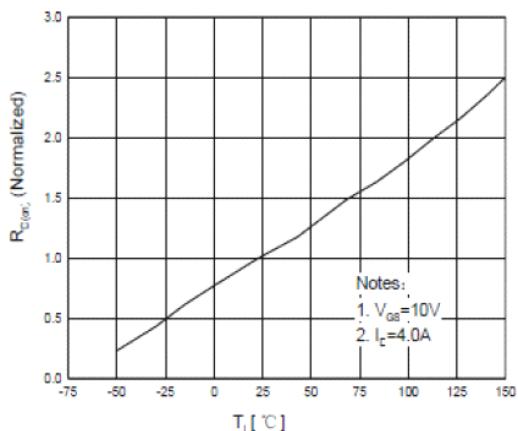


Fig.5 On-Resistance Variation vs Junction Temperature

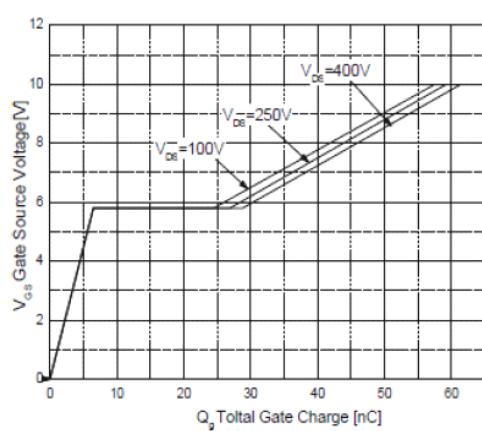


Fig.6 Gate Charge Characteristics

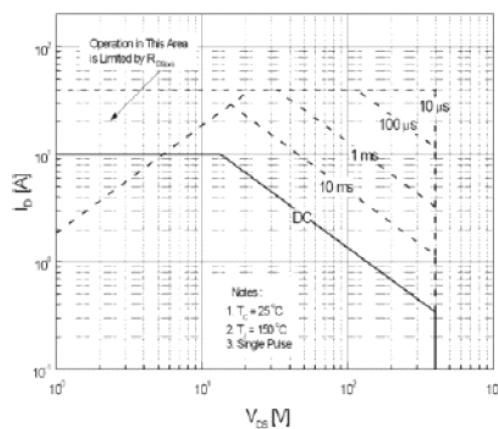


Fig.7 Maximum Safe Operation Area

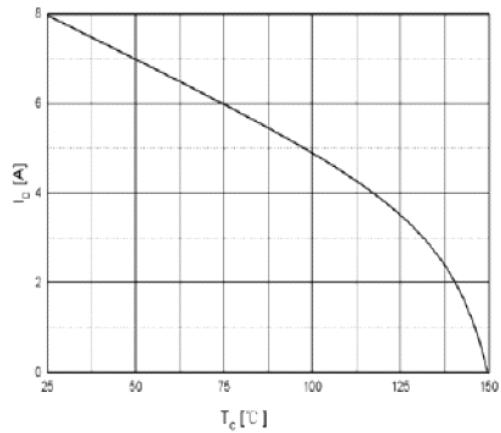


Fig.8 Maximum Drain Current vs Case Temperature

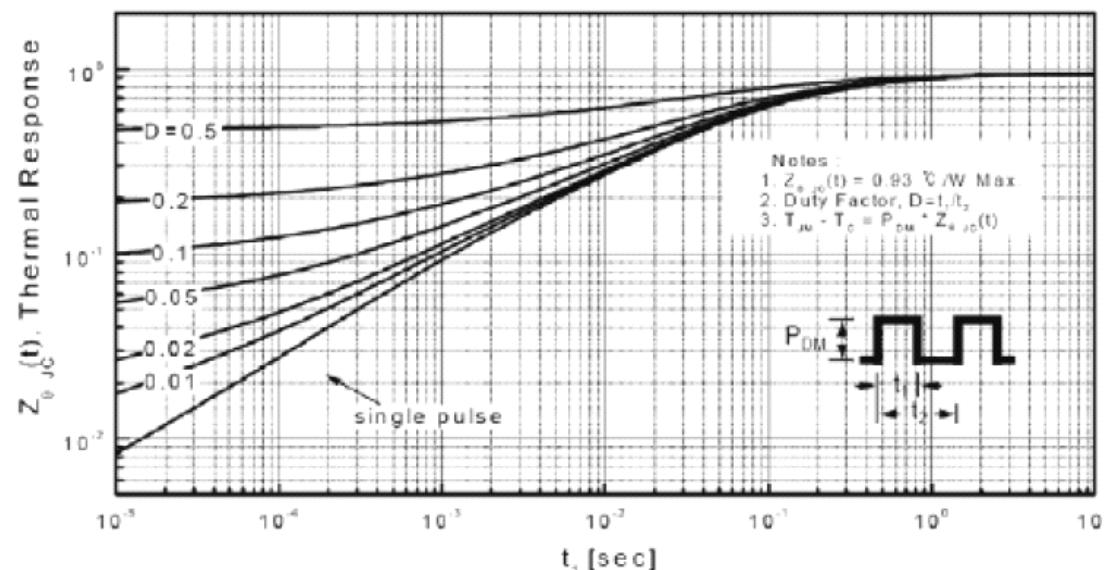


Fig.9 Transient Thermal Response Curve

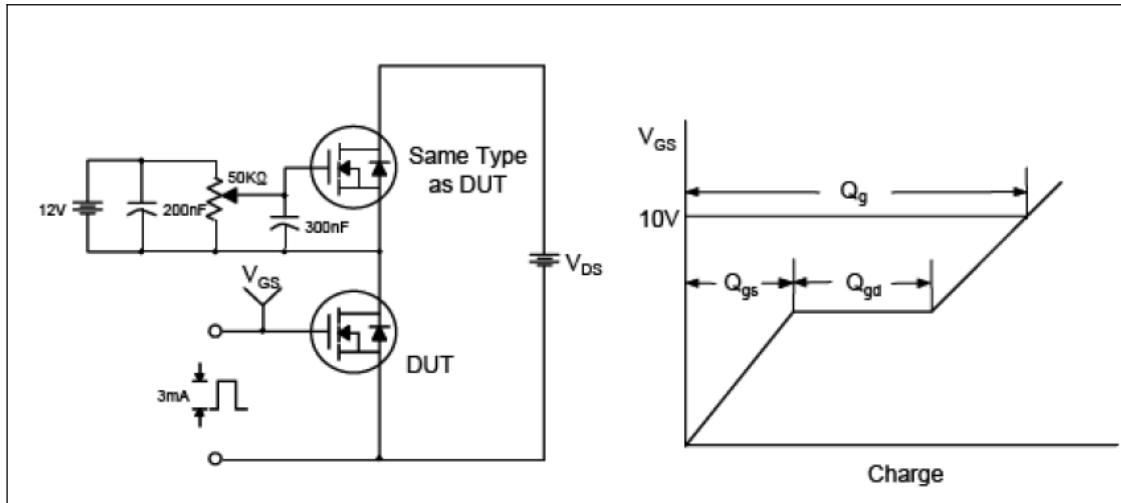


Fig.10 Gate Test Circuit & Waveform

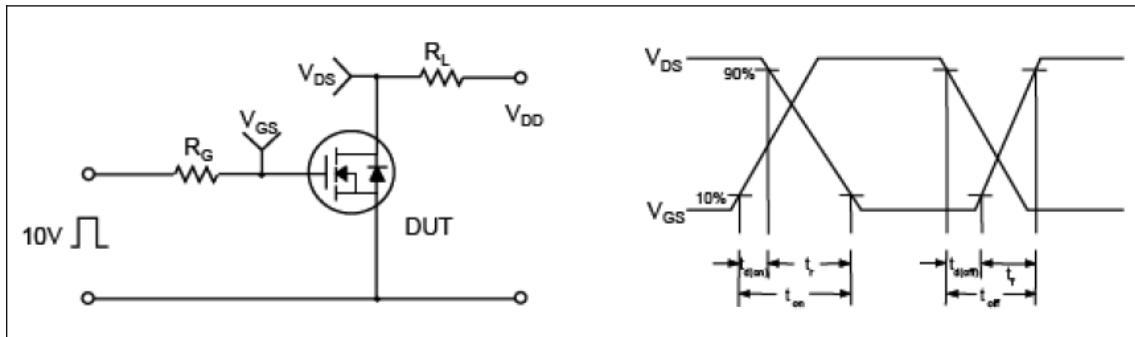


Fig.11 Resistive Switching Test Circuit & Waveform

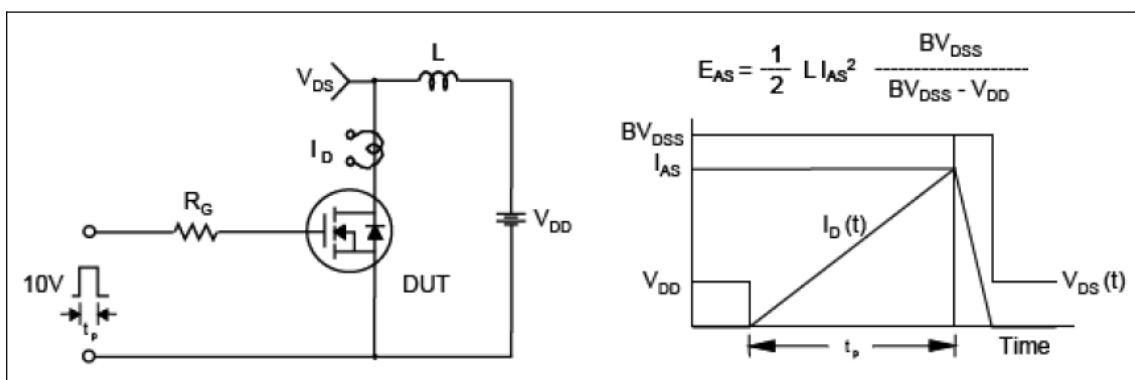


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

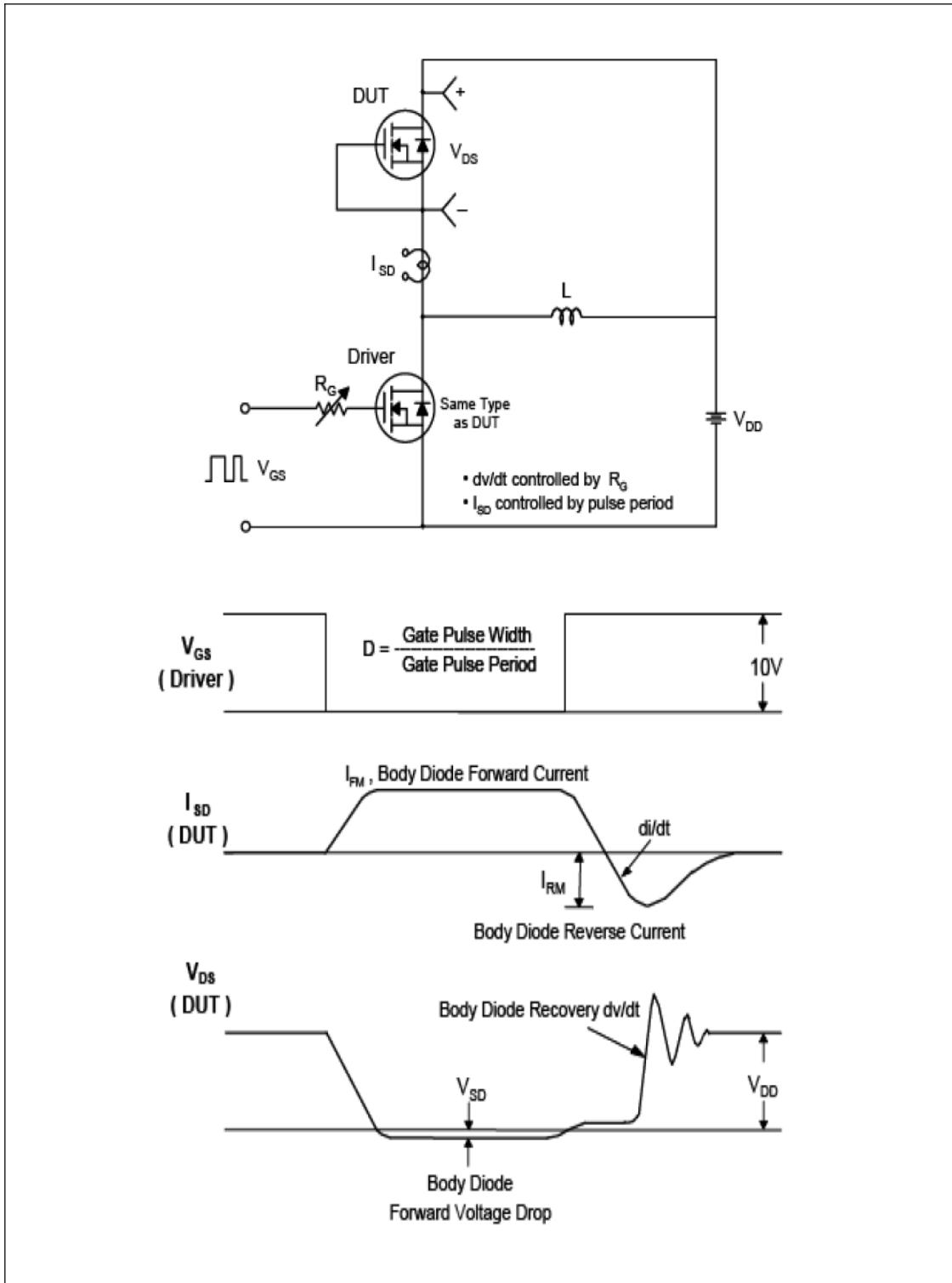


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-220C Package Dimension

