Ordering number : ENA0259

SANYO Semiconductors
DATA SHEET

LA79500E

Monolithic Linear IC
For TV
6-input, 3-output Switch

Overview

This LA79500E is a 6-input, 3-output switch for TV.

Functions

- Composite 6 inputs with 3 outputs
- Component 2 inputs with 2 outputs
- Audio 8 inputs with 3 outputs (L/R)
- Serial control with I^2C bus
- General purpose I/O
- Acceptance from Y/C comb filter output
- S1, S2 protocol interface
- Y/C MIX circuit
- All video and audio output Gains are selectable by a single bit as 0 or 6dB.
- Sync-tip clamps include a simple signal detector readable over I^2C bus.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		13	V
Allowable current electric power	Pd max	* Mounted on a board.	1600	mW
Operating temperature	Topr		-25 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a board : 114.3×76.1×1.6mm^3, glass epoxy resin.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommending supply voltage	V_{CC}		12	V
Operating supply voltage	V_{CC} op		11.4 to 12.7	V

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Electrical Characteristics/Operating Conditions at Ta = 25°C, V_{CC} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current consumption	I_{CC}	No signal, No load	67	90	113	mA
[Video system]						
Frequency response characteristics	frv	100kHz/7MHz	-1.0	0	1.0	dB
Maximum input level	Ddv	f = 100kHz, output THD = 1% input	1.4	1.6		Vp-p
Voltage gain 1	GVv1	6dB select	5.9	6.4	6.9	dB
Voltage gain 2	GVv2	0dB select	0.0	0.4	0.9	dB
Cross talk	Vctv	f = 3.58MHz		-60	-55	dB
[Audio system]						
Voltage gain 1	GVa1	6dB select	5.9	6.4	6.9	dB
Voltage gain 2	GVa2	0dB select	0.0	0.4	0.9	dB
Frequency response characteristics	Fra	100Hz/20kHz	-1.0	0	1.0	dB
Total harmonic distortion	THD	f = 1kHz, 2.2Vp-p input		0.03	0.05	%
Maximum input level	Dda	f = 1kHz, output THD = 0.3% input	2.3	2.5		Vrms
Cross talk	Vcta	f = 1kHz, 1Vp-p input		-90	-80	dB
Supply Ripple rejection ratio	SRrr	f = 100Hz, 0.3Vp-p applied to V_{CC}		-55	-40	dB
S/N ratio	S/Na	f = 1kHz, 1Vrms input		-100	-90	dB
[Logic system]						
High level input voltage	ViH		3.5		5.0	V
Low level input voltage	ViL		0		1.5	V
Low level output voltage	VoL	SDA 3mA current supplied	0		0.4	V
High level input current	IiH	V_{IH} = 4.5V	0		10	μA
Low level input current	IiL	V_{IL} = 0.4V	0		10	μA
Maximum clock frequency	fscl		0		100	kHz
Minimum waiting time for data change	tBUF		4.7			μs
Minimum waiting time for data transfer start	tHD:STA		4.0			μs
Low level clock Pulse width	tLOW		4.7			μs
High level clock pulse width	tHIGH		4.0			μs
Minimum waiting time for start preparation	tSU:STA		4.7			μs
Minimum data hold time	tHD:DAT		0			μs
Minimum data preparation time	tSU:DAT		250			ns
Rise time	tR				1	μs
Fall time	tF				300	ns
Minimum waiting time for stop preparation	tSU:STO		4.7			μs
GPIO1/2/3/4/5/6 (Pin5/13/27/33/55/63)						
High level input voltage	GPIH		3.5			V
Low level input voltage	GPIL				1.5	V
High level output voltage	GPOH	50μA current loaded	4.0			V
Low level output voltage	GPOL	1mA current supplied			1.0	V
DC_OUT (Pin67)						
High level output voltage	DCOH	DC_OUT (BUS Write) 11 R_L =100kΩ	4.0	4.5		V
Middle level output voltage	DCOM	DC_OUT (BUS Write) 10 R_L =100kΩ	1.4	1.9	2.4	V
Low level output voltage	DCOL	DC_OUT (BUS Write) 01/00 R_L =100kΩ			0.5	V
DC_IN (Pin66)						
High level input voltage	DCIH	DC_IN (BUS read) 10	3.0			V
Middle level input voltage	DCIM	DC_IN (BUS read) 01	1.5	1.9	2.3	V
Low level input voltage	DCIL	DC_IN (BUS read) 00			1.0	V

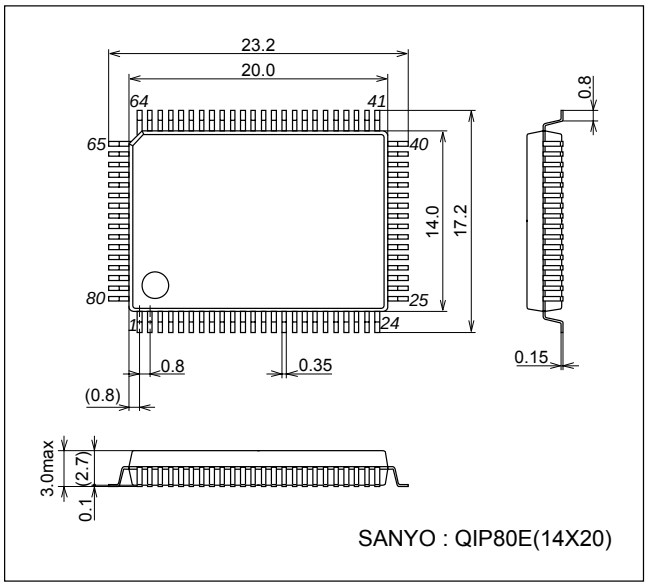
Terminal Voltage/ Input Impedance

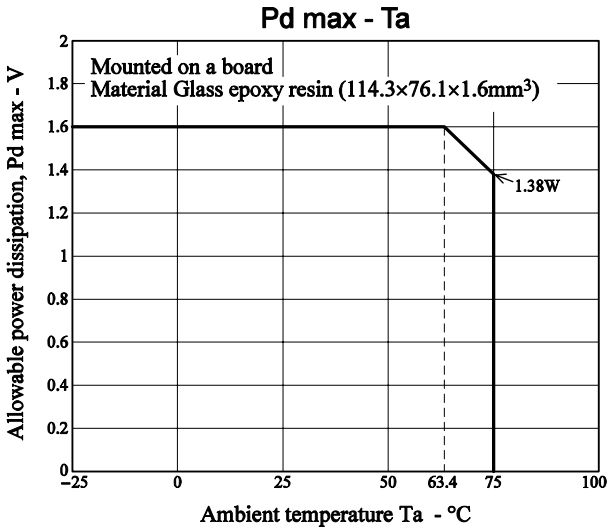
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Video signal inputs terminal voltage (Pin6/14/34/71/75/78)	CVYIV		2.0	2.5	3.0	V
Video signal outputs terminal voltage (Pin46/56/64)	CVYOV		2.0	2.5	3.0	V
Y signal inputs terminal voltage (Pin8/16/21/28/36/80/65)	YIV		2.0	2.5	3.0	V
Y/V signal outputs terminal voltage (Pin54/62)	YOV		2.0	2.5	3.0	V
C signal inputs terminal voltage (Pin2/10/18/38/68)	CIV		2.3	2.8	3.3	V
C signal outputs terminal voltage (Pin52/60)	COV		2.3	2.8	3.3	V
C signal inputs terminal impedance (Pin2/10/18/38/68)	CIz		8.0	10.0	12.0	kΩ
Pb/Pr signal inputs terminal voltage (Pin23/25/30/32)	PbrIV		2.0	2.5	3.0	V
Pb/Pr signal outputs terminal voltage (Pin49/50/57/58)	PbrOV		1.9	2.4	2.9	V
Audio signal inputs terminal voltage (Pin1/7/9/15/17/22/24/29/31 /35/37/70/72/74/76/79)	AIV		5.3	5.8	6.3	V
Audio signal outputs terminal voltage (Pin45/47/51/53/59/61)	AOV		4.7	5.2	5.7	V
Audio signal inputs terminal impedance (Pin1/7/9/15/17/22/24/29/31 /35/37/70/72/74/76/79)	AIz		40.0	50.0	60.0	kΩ

Package Dimensions

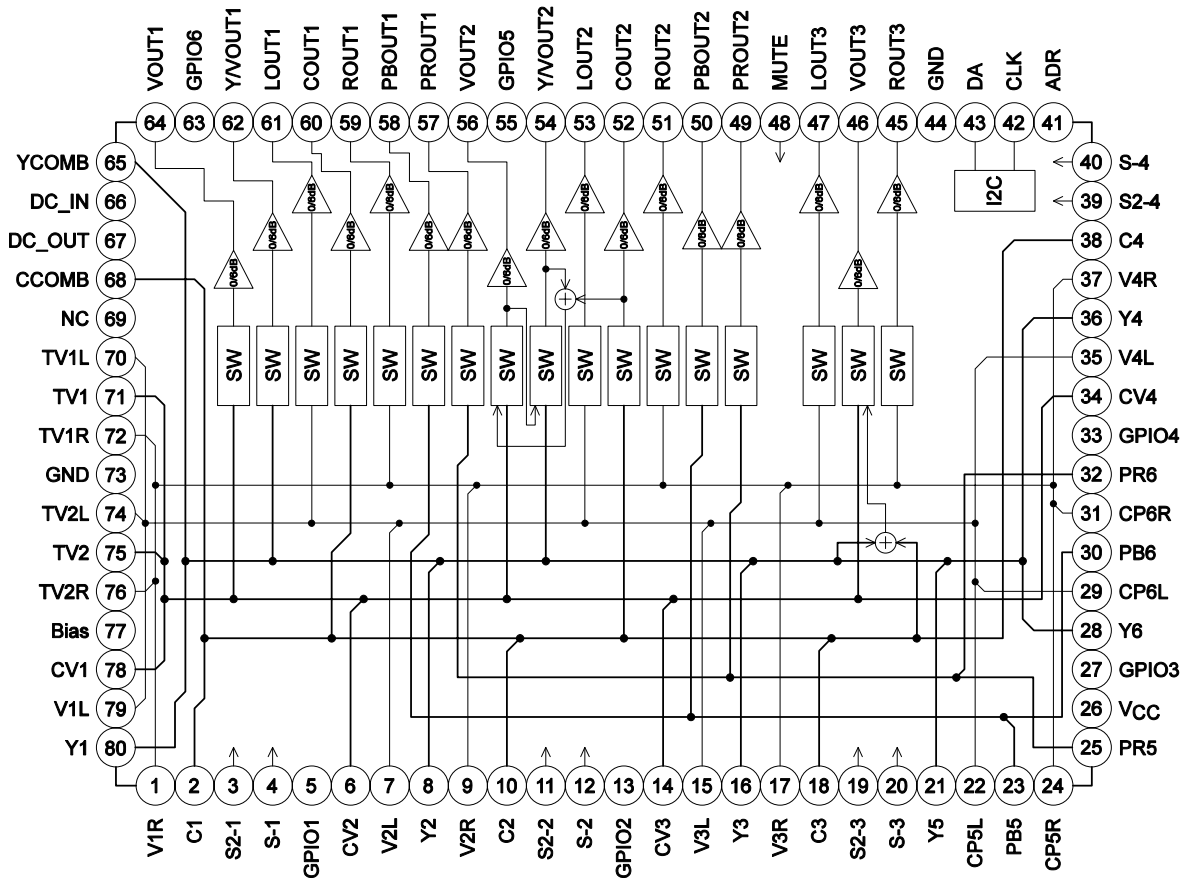
unit : mm

3174A

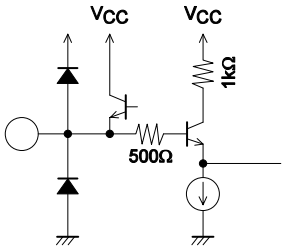
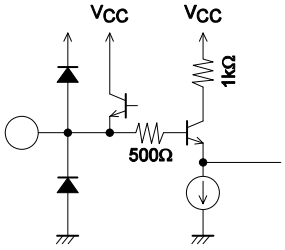
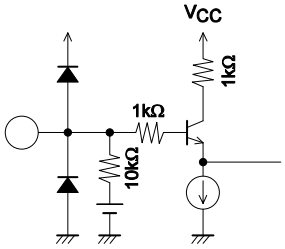
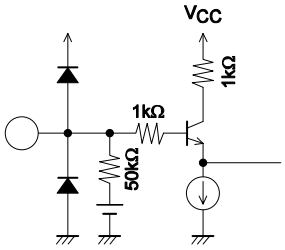
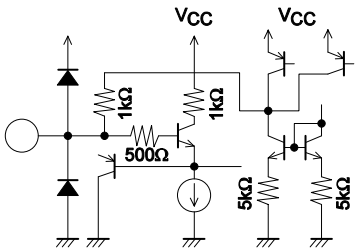
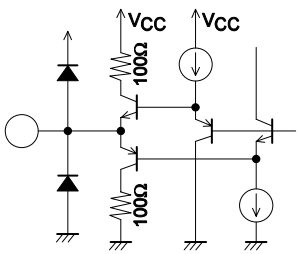




Block Diagram



Pin Description

Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent circuit
71 75 78 6 14 34	TV1 TV2 CV1 CV2 CV3 CV4	2.5	Video signal inputs. Input composite video signals.	
80 8 16 36 21 28	Y1 Y2 Y3 Y4 Y5 Y6	2.5	Y/C separation signal inputs. Input luminance signals.	
2 10 18 38	C1 C2 C3 C4	2.8	Y/C separation signal inputs. Input chrominance signals.	
70, 72 74, 76 79, 1 7, 9 15, 17 35, 37 22, 24 29, 31	TV1L, TV1R TV2L, TV2R V1L, V1R V2L, V2R V3L, V3R V4L, V4R CP5L, CP5R CP6L, CP6R	5.8	Audio signal inputs.	
25 23 32 30	PR5 PB5 PR6 PB6	2.5	Component PB/PR inputs.	
64 56 46	VOUT1 VOUT2 VOUT3	2.5	Video signal outputs. Output composite video signals.	

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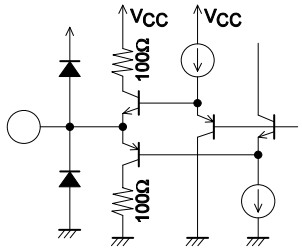
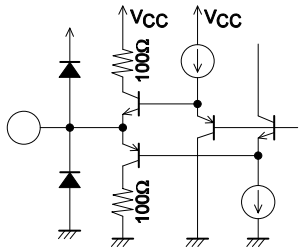
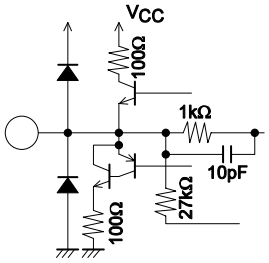
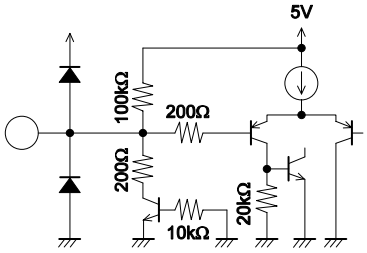
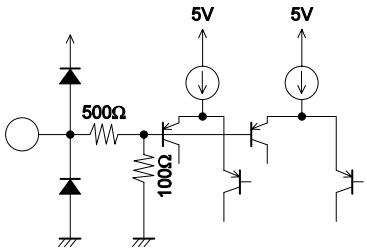
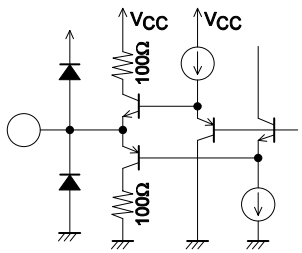
Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent circuit
62 54	Y/VOUT1 Y/VOUT2	2.5	Video signal outputs. Either composite video signal output or luminance signal output can be selected by I^2C bus control.	
60 52	COUT1 COUT2	2.8	Video signal outputs. Output chorominance signals.	
61 53 47 59 51 45	LOUT1 LOUT2 LOUT3 ROUT1 ROUT2 ROUT3	5.2	Audio signal outputs.	
4 12 20 40	S-1 S-2 S-3 S-4		Composite video/S selector. The detection results are written to the status register. S signal at 3.5V or less. Composite video signal at 3.5V or more. This pin is pulled up to 5V by a 100kΩ resistor, so the composite video signalis selected when open.	
3 11 19 39	S2-1 S2-2 S2-3 S2-4		Detects the S2-compatible DC superimposed onto the C signal. 4:3 video signal at 1.3V or less. 4:3 letter-box signal at 1.3V or moreto2.5V or less. 16:9 picture squeezed signal at 2.5V or more. This pin is pulled down to GND by a 100kΩ resistor, so the 4:3 video signal is selected when open.	
57 58 49 50	PROUT1 PBOUT1 PROUT2 PBOUT2	2.4	Component PB/PR outputs.	

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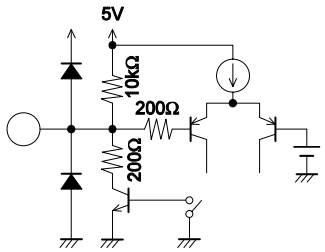
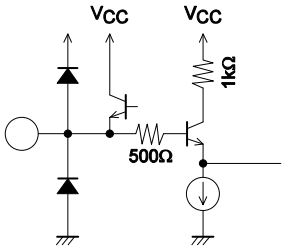
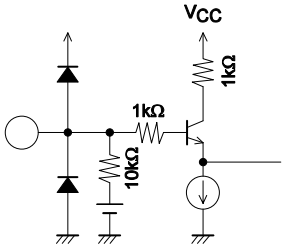
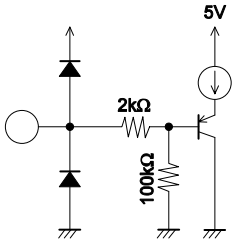
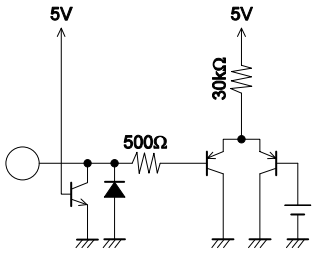
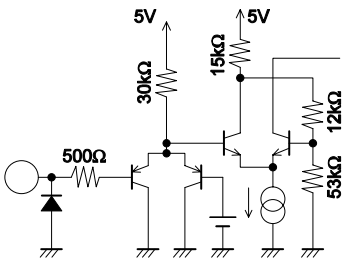
Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent circuit
5 13 27 33 55 63	GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6		General purpose I/O.	
65	YCOMB	2.5	The YCOMB pin inputs the signal obtained by Y/C separating the VOUT1 pin output.	
68	CCOMB	2.8	The CCOMB pin inputs the signal obtained by Y/C separating the VOUT1 pin output.	
41	ADR		Selects the slave address for the I^2C bus. 90H at 1.5V or less. 92H at 2.5V or more. 90H when open.	
43	DATA		I^2C bus signal input V_{IL}max = 1.5V V_{IH}min = 3.0V V_{OL}max = 0.4V	
42	CLK		I^2C bus signal input V_{IL}max = 1.5V V_{IH}min = 3.0V	

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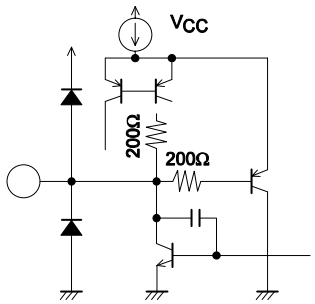
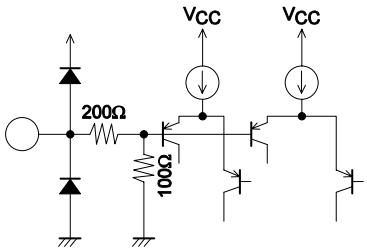
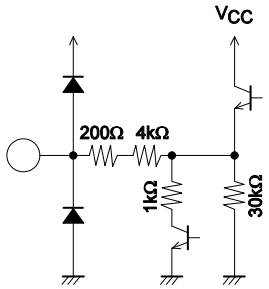
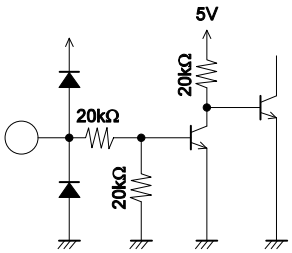
Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent circuit
77	BIAS	10.2	Internal reference bias. Connect to GND via a capacitor.	
66	DC_IN		Detection Pin of DC input 1.3V or less : 00 1.3V or more to 2.5V or less : 01 2.5V or more : 10 This pin is pulled down to GND by a 100kΩ resistor.	
67	DC_OUT		Outputs the S2-compatible DC. Control is perfomed by the I^2C bus. S2 protocol output impedance of 10±3Kohm is realized by attaching external resisitance of 4.7kohm. DC_OUT (bus) Output DC 00 0V 01 0V 10 1.9V 11 4.5V	
48	MUTE		ALL signal output mute. Mute OFF at 1.5V or less Mute ON at 2.0V or more. Mute OFF when open.	
26	V_{CC}	12.0	V_{CC}	
44 73	GND	0.0	GND	
69	NC		Not connected	

Serial Control Specification

Slave address

MSB							LSB
1	0	0	1	0	0	ADR	R/W

ADR : This bit sets the slave address set by the address pin.

0 : address pin “LOW”

1 : address pin “HIGH”

R/W : Read/write mode

0 : Control data write

1 : Staus register read

Data format (Write mode)

S	Slave address (8bit)	A	Sub address (8bit)	A	Data address (8bit) 00 to 05 Group	A	P

Start condition　　Acknowledge　　Stop condition

Sub address and Data byte

Write mode

* : indicates undefined

Sub address	Data byte (Underline is initial setting.)							
	MSB D8	D7	D6	D5	D4	D3	D2	LSB D1
00 (0000 0000)	VOUT1 Gain 0 : 0dB 1 : 6dB	VOUT1 000 : TV1　100 : CV3 001 : TV2　101 : CV4 010 : CV1　110 : MUTE 011 : CV2　111 : MUTE			L/ROUT1 000 : TV1　100 : V3 001 : TV2　101 : V4 010 : V1　110 : MUTE 011 : V2　111 : Pr/Pb			L/ROUT1 Gain 0 : 0dB 1 : 6dB
01 (0000 0001)	VOUT2 Gain 0 : 0dB 1 : 6dB	VOUT2 000 : TV1　100 : CV3 001 : TV2　101 : CV4 010 : CV1　110 : MUTE 011 : CV2　111 : Y+C			L/ROUT2 000 : TV1　100 : V3 001 : TV2　101 : V4 010 : V1　110 : MUTE 011 : V2　111 : Pr/Pb			L/ROUT2 Gain 0 : 0dB 1 : 6dB
02 (0000 0010)	VOUT3 Gain 0 : 0dB 1 : 6dB	VOUT3 000 : TV1　100 : CV3 001 : TV2　101 : CV4 010 : CV1　110 : MUTE 011 : CV2　111 : Y+C			L/ROUT3 000 : TV1　100 : V3 001 : TV2　101 : V4 010 : V1　110 : MUTE 011 : V2　111 : Pr/Pb			L/ROUT3 Gain 0 : 0dB 1 : 6dB
03 (0000 0011)	*	VOUT3 Y+C 00 : Y1/C1 01 : Y2/C2 10 : Y3/C3 11 : Y4/C4	*		L/ROUT1 0 : Pr5/Pb5 1 : Pr6/Pb6	L/ROUT2 0 : Pr5/Pb5 1 : Pr6/Pb6	L/ROUT3 0 : Pr5/Pb5 1 : Pr6/Pb6	*
04 (0000 0100)	Y/COUT1 Gain 0 : 0dB 1 : 6dB	Y/C/Pr/PbOUT1 000 : Y1/C1　100 : Y/CCOMB 001 : Y2/C2　101 : Y5/Pr5/Pb5 010 : Y3/C3　110 : Y6/Pr6/Pb6 011 : Y4/C4　111 : MUTE			GPO1 0 : Low 1 : High	GPO2 0 : Low 1 : High	GPO3 0 : Low 1 : High	GPO4 0 : Low 1 : High
05 (0000 0101)	Y/COUT2 Gain 0 : 0dB 1 : 6dB	Y/C/Pr/PbOUT2 & VOUT2 Y+C 000 : Y1/C1　100 : VOUT2 001 : Y2/C2　101 : Y5/Pr5/Pb5 010 : Y3/C3　110 : Y6/Pr6/Pb6 011 : Y4/C4　111 : MUTE			GPO5 0 : Low 1 : High	GPO6 0 : Low 1 : High	DC_OUT 00/01 : 0V (Low) 10 : 1.9V (Mid) 11 : 4.5V (High)	

VOUT1/2/3 gain : VOUT1/2/3 output gain selector
- 0 : 0dB output
- 1 : 6dB output

Y/COUT1/2 : Y/VOUT1/2 and COUT1/2, Pr/PbOUT1/2 output gain selector
- 0 : 0dB output
- 1 : 6dB output

L/ROUT1/2/3 gain : LOUT1/2/3 and ROUT1/2/3 output gain selector
- 0 : 0dB output
- 1 : 6dB output

VOUT1/2/3 : These bits select the input signals output to each video output
- 0 : Selects the TV1 input
- 1 : Selects the TV2 input
- 2 : Selects the CV1 input
- 3 : Selects the CV2 input
- 4 : Selects the CV3 input
- 5 : Selects the CV4 input
- 6 : MUTE
- 7 : MUTE (VOUT1), Y+C (VOUT2 / 3) (VOUT2:Set *2)

L/ROUT1/2/3(1) : These bits select the input signals output to each Audio L/R output
- 0 : Selects the TV1L/R input
- 1 : Selects the TV2L/R input
- 2 : Selects the V1L/R input
- 3 : Selects the V2L/R input
- 4 : Selects the V3L/R input
- 5 : Selects the V4L/R input
- 6 : MUTE
- 7 : Selects the Pr/Pb (Cr/Cb) mode *1

*1 L/ROUT1/2/3(2) : This bit selects the input signals output to CP5L/R, CP6L/R output
- 0 : Selects the CP5L/R input
- 1 : Selects the CP6L/R input

VOUT3 Y+C : These bits select the Y+C input signals output to VOUT3 (Y+C mode)
- 0 : Selects the Y1/C1 input
- 1 : Selects the Y2/C2 input
- 2 : Selects the Y3/C3 input
- 3 : Selects the Y4/C4 input

*2 Y/C/Pr/PbOUT1/2 & VOUT2 Y+C : These bits select the input signals output to each Video output
- 0 : Selects the Y1/C1 input
- 1 : Selects the Y2/C2 input
- 2 : Selects the Y3/C3 input
- 3 : Selects the Y4/C4 input
- 4 : Selects the Y/CCOMB input, VOUT2 output
- 5 : Selects the Y5/Pr5/Pb5 input
- 6 : Selects the Y6/Pr6/Pb6 input
- 7 : Mute

GPO1/2/3/4/5/6 : This bit set the output from GPIO1/2/3/4/5/6
- 0 : LOW(1.0V or less)
- 1 : HIGH(4.0V or more)

DC_OUT : These bits set the DC voltage output from Pin67 (DC_OUT)
- 0 : 0V
- 1 : 0V
- 2 : 1.9V
- 3 : 4.5V

Data format (Read mode)

S	Slave address (8bit)	A	DATA1 (8bit)	A	DATA2 (8bit)	A	DATA3 (8bit)	A	DATA4 (8bit)	A	DATA5 (8bit)	A	P

↑ Start condition ↑ Acknowledge ↑ Stop condition

Read mode

* : indicates undefined

	Data byte							
	MSB D8	D7	D6	D5	D4	D3	D2	LSB D1
DATA1	TV1 0 : No sig. 1 : Signal	TV2 0 : No sig. 1 : Signal	CV1 0 : No sig. 1 : Signal	CV2 0 : No sig. 1 : Signal	CV3 0 : No sig. 1 : Signal	CV4 0 : No sig. 1 : Signal	*	*
DATA2	YCOMB 0 : No sig. 1 : Signal	Y1 0 : No sig. 1 : Signal	Y2 0 : No sig. 1 : Signal	Y3 0 : No sig. 1 : Signal	Y4 0 : No sig. 1 : Signal	Y5 0 : No sig. 1 : Signal	Y6 0 : No sig. 1 : Signal	*
DATA3	GPI1 0 : Low 1 : High	GPI2 0 : Low 1 : High	GPI3 0 : Low 1 : High	GPI4 0 : Low 1 : High	GPI5 0 : Low 1 : High	GPI6 0 : Low 1 : High	DC_IN 00 : 1.3V or less 01 : 1.3V or more to 2.5V or less 10 : 2.5V or more	
DATA4	$\overline{\text{S-1 SEL}}$ 1 : Low 0 : High	$\overline{\text{S-2 SEL}}$ 1 : Low 0 : High	$\overline{\text{S-3 SEL}}$ 1 : Low 0 : High	$\overline{\text{S-4 SEL}}$ 1 : Low 0 : High	*	*	*	*
DATA5	S2-1 00 : 4:3 video sig. 01 : 4:3 Letter-box 10 : 16:9 11 : No sig.		S2-2 00 : 4:3 video sig. 01 : 4:3 Letter-box 10 : 16:9 11 : No sig.		S2-3 00 : 4:3 video sig. 01 : 4:3 Letter-box 10 : 16:9 11 : No sig.		S2-4 00 : 4:3 video sig. 01 : 4:3 Letter-box 10 : 16:9 11 : No sig.	

S-1 SEL to S-4 SEL

1 : S-1 to S-4 pins are grounded.

0 : S-1 to S-4 pins are not grounded.

S2-1 to S2-4

S2-1 to S2-4 are actually determined by comparing the S2-1 to S2-4 pin DC voltages with two threshold. However, when the S-1 to S-4 pins are OPEN(HIGH) the outputs are fixed to “11”.

S2-1 to S2-4 : DATA bit

1.3V or less : 00

1.3V or more to 2.5V or less : 01

2.5V or more : 10

S-1 to S-4 OPEN (HIGH) : 11

1) Data transfer manual : [1] is High level. [0] is Low level.

I^2C-BUS control system is adopted in SW LSI and SW LSI is controlled by SCL (Serial Clock) and SDA (Serial Data). At first, please set up the START condition*1 by these two terminals (SCL and SDA). And next, please input the 8bits data which should be synchronized with SCL into SDA terminal Still more, please give priority to high rank bit at data transfer order (MSB→LSB). The 9th bit is called as ACK (Acknowledge), SW LSI sends [0] to the SDA terminal during SCL [1] period. So, please open the port of micro-processor during this period. And next, please transfer sub-address data (called as Group) and control data. As thus the Data transfer Stop condition*2 is finished.

*1 : SDA rise up during SCI is [1] *2 : SDA fall down during SCL is [1]

2) Transfer data format

The transfer data is composed by START condition , Slave address data, sub-address data, control data and STOP condition.
There are 6 control groups.
After setting up the START condition, please transfer the Slave Address. sub-address data and next control data (Please see the Fig.1)
Slave Address is composed by 7bits, and this bit 8th bit should be set as [0] at write mode and [1] at read mode. This 8th bit called as R/W bit, and this bit shows the data transmission direction. [0] means send mode (accept mode with SW LSI) and [1] means accept mode (send mode with SW LSI) fundamentally.
The both of sub-address data and control data are composed by 8bits, and the one control action is defined with combination of these two data. And if you want to control 2 or more groups at the same mode, you can realize it by sending some control data together.
The data makes meaning with all bits, so you cannot stop the sending until all data transfer is over. If you want to stop transfer action, please transfer the STOP condition.

You can select how to send as follws.(write mode)

Pattern A Start condition + Slave Address + Sub Address 00 + Data 00 + Data 01 + Data 02 + Data 03 + Data 04 + Data 05 + Stop condition
Pattern B Start condition + Slave Address + Sub Address 01 + Data 01 + Data 02 + Data 03 + Data 04 + Data 05 + Stop condition
Pattern C Start condition + Slave Address + Sub Address 02 + Data 02 + Data 03 + Data 04 + Data 05 + Stop condition
Pattern D Start condition + Slave Address + Sub Address 03 + Data 03 + Data 04 + Data 05 + Stop condition
Pattern E Start condition + Slave Address + Sub Address 04 + Data 04 + Data 05 + Stop condition
Pattern F Start condition + Slave Address + Sub Address (01 or 02 or 03 or 04 or 05) + Data (01 or 02 or 03 or 04 or 05) + Stop condition (send only 1Data)

START condition	Slave Address	R/W	ACK	Sub-Address	ACK	Control data	ACK	···	STOP condition

Fig.1 Data Structure

3) Initialize

SW LSI is initialized as the following mode for circuit protection. Please see “SERIAL CONTROL TABLE”.

Characteristics of the SDA and SCL 1/0 stages for SW LSI

Parameter	Symbol	Ratings		Unit
		Min	Max	
LOW level input voltage	VIL	0	1.5	V
HIGH level input voltage	VIH	3.5	5.0	V
LOW level output current	IOL		3.0	mA
SCL clock frequency	fSCL		100	kHz
Set-up time for a repeated START condition	tSU:STA	4.7		μs
Hold time START condition. After this period, the first clock pulse is generated.	tHD:STA	4.0		μs
LOW period of the SCL clock	tLOW	4.7		μs
Rise time of both SDA and SDL signals	tR	0	1.0	μs
HIGH period of the SCL clock	tHIGH	4.0		μs
Fall time of both SDA and SDL signals	tF	0	1.0	μs
Data hold time	tHD:DAT	0		μs
Data set-up time	tSU:DAT	250		ns
Set-up time for STOP condition	tSU:STO	4.0		μs
BUS fred time between a STOP and START condition	tBUF	4.7		μs

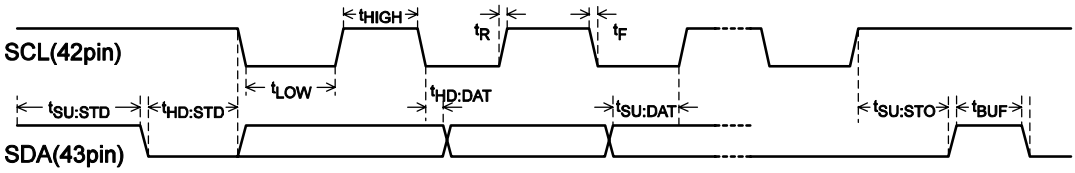
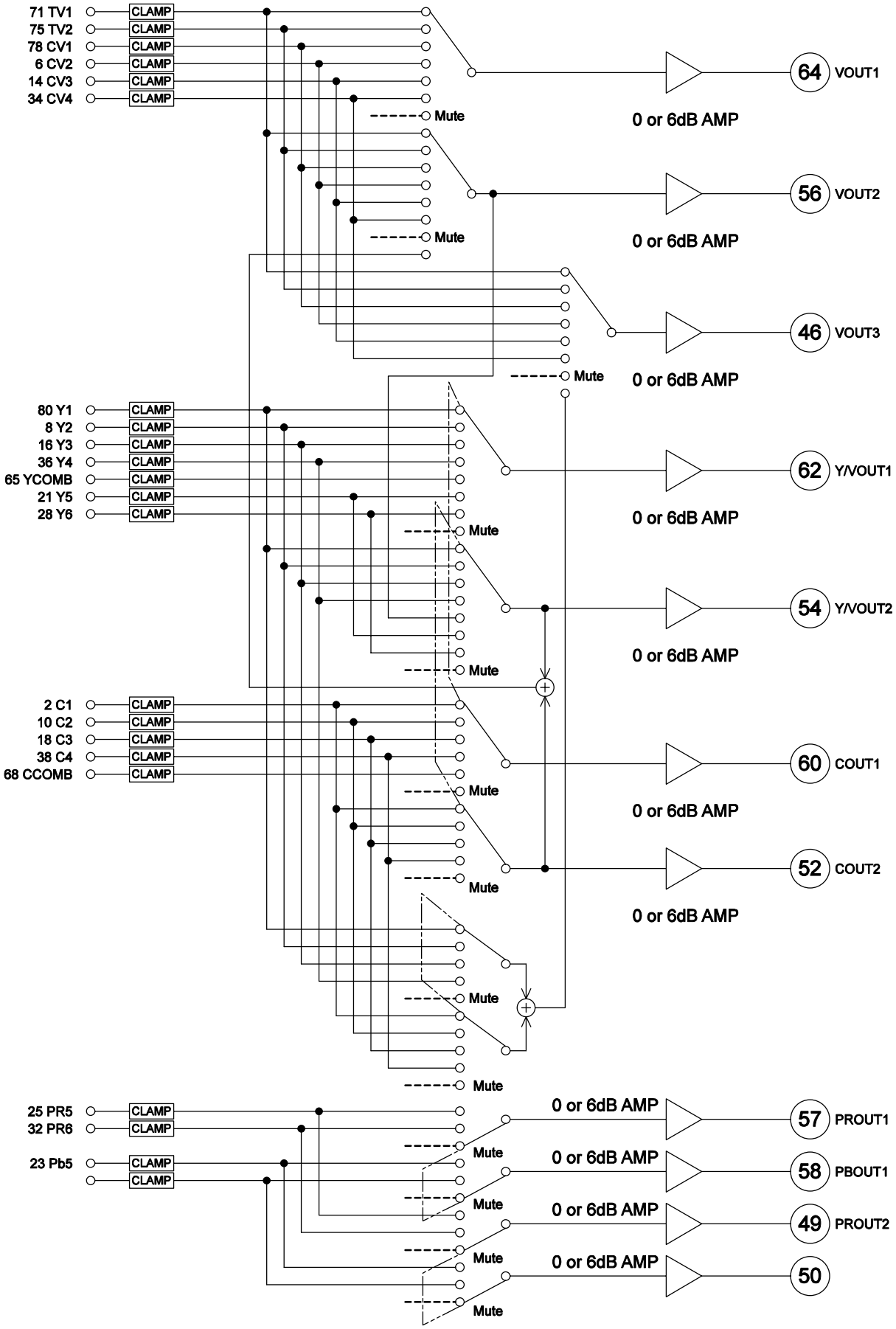
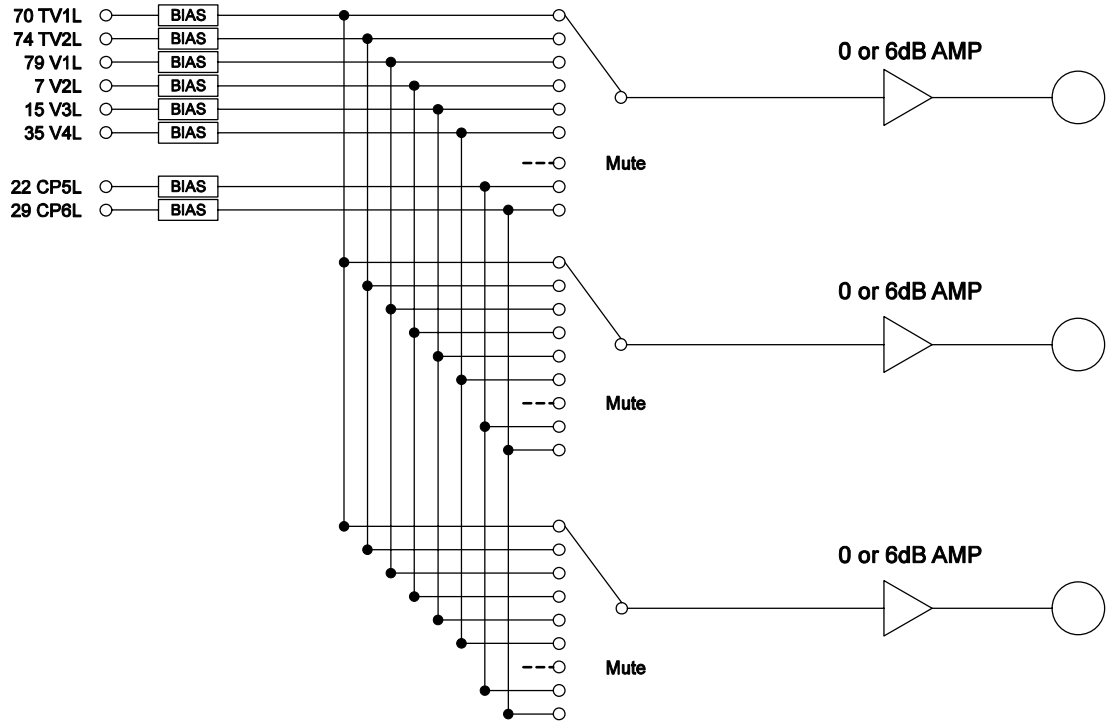


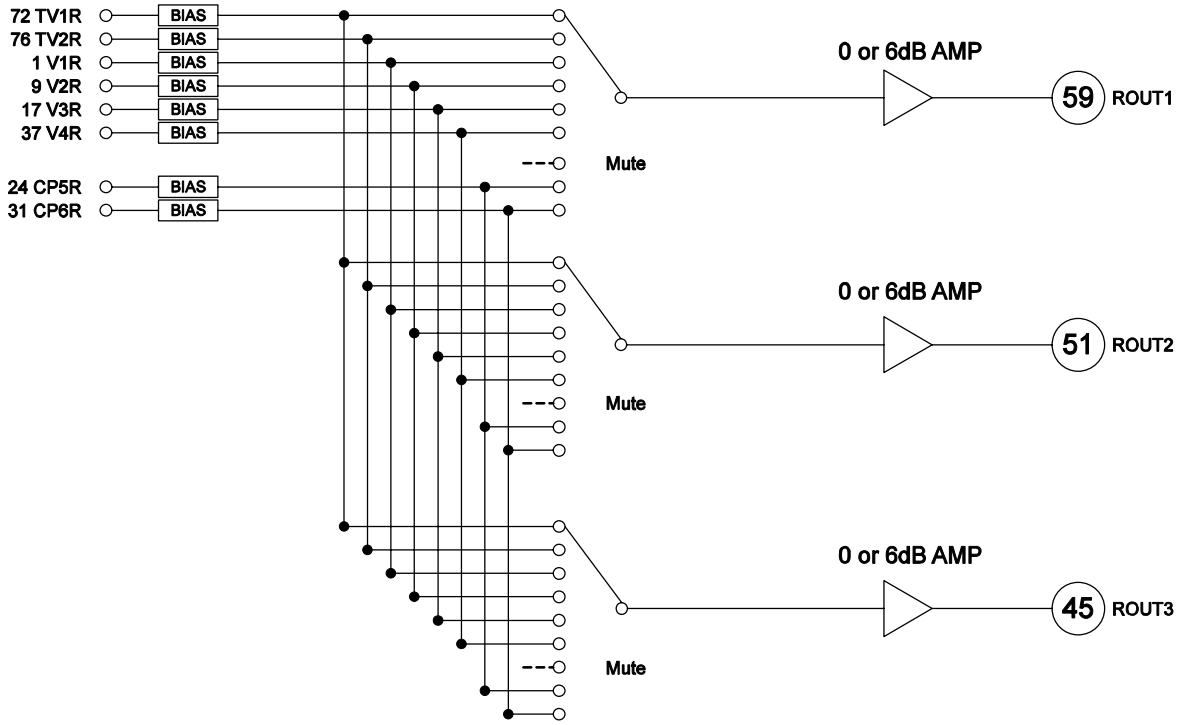
Fig.2 Definition of timing

Video Block


71 TV1
75 TV2
78 CV1
6 CV2
14 CV3
34 CV4
CLAMP
Mute
0 or 6dB AMP
64 VOUT1
56 VOUT2
46 VOUT3
80 Y1
8 Y2
16 Y3
36 Y4
65 YCOMB
21 Y5
28 Y6
62 Y/VOUT1
54 Y/VOUT2
2 C1
10 C2
18 C3
38 C4
68 CCOMB
60 COUT1
52 COUT2
25 PR5
32 PR6
23 Pb5
57 PROUT1
58 PBOUT1
49 PROUT2
50

Audio Block


70 TV1L
74 TV2L
79 V1L
7 V2L
15 V3L
35 V4L
22 CP5L
29 CP6L
BIAS
Mute
0 or 6dB AMP


72 TV1R
76 TV2R
1 V1R
9 V2R
17 V3R
37 V4R
24 CP5R
31 CP6R
BIAS
Mute
0 or 6dB AMP
59 ROUT1
51 ROUT2
45 ROUT3

Test Circuit