EN39SL160AH/L
16 Megabit (1024K x 16-bit) Flash Memory With 4Kbytes Uniform Sector, CMOS 1.8 Volt-only

FEATURES

- Single power supply operation
  - Full voltage range:1.65-1.95 volt for read and write operations.
  - Ideal for battery-powered applications.
- High performance
  - Access times as fast as 70 ns
- Low power consumption (typical values at 5 MHz)
  - 5 mA typical active read current
  - 15 mA typical program/erase current
  - 0.2 μA typical standby current
- Uniform Sector Architecture:
  - 512 sectors of 2-Kword
  - 32 blocks of 32-Kword
  - Any sector or block can be erased individually
- WP#/ACC Input pin:
  - Write protect (WP#) function allows protection the first or last blocks, regardless of block protect status
  - Acceleration (ACC) function acceleration program timing.
- Block Group protection:
  - Hardware locking of blocks to prevent program or erase operations within individual blocks
  - Additionally, temporary Block Unprotect allows code changes in previously locked blocks.
- High performance program/erase speed
  - Word program time: 8μs typical
  - Sector erase time: 90ms typical
  - Block erase time: 180ms typical
  - Chip erase time: 4s typical
- JEDEC Standard Embedded Erase and Program Algorithms
- JEDEC standard DATA# polling and toggle bits feature
- Single Sector, Block and Chip Erase
- Chip Unprotect Mode
- Erase Suspend / Resume modes:
  Read or program another Sector/Block during Erase Suspend Mode
- Low Vcc write inhibit ≤ 1.2V
- Minimum 100K endurance cycle
- Package Options
  - 48-ball 6mm x 8mm TFBGA
  - 48-ball 4mm x 6mm WFBGA
- Industrial temperature Range

GENERAL DESCRIPTION

The EN39SL160AH/L is a 16-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 1,048,576 words. Any word can be programmed typically in 8μs.The EN39SL160AH/L features 1.8V voltage read and write operation, with access time as fast as 70ns to eliminate the need for WAIT statements in high-performance microprocessor systems.

The EN39SL160AH/L has separate Output Enable (OE#), Chip Enable (CE#), and Write Enable (WE#) controls, which eliminate bus contention issues. This device is designed to allow either single Sector/Block or full chip erase operation, where each block can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

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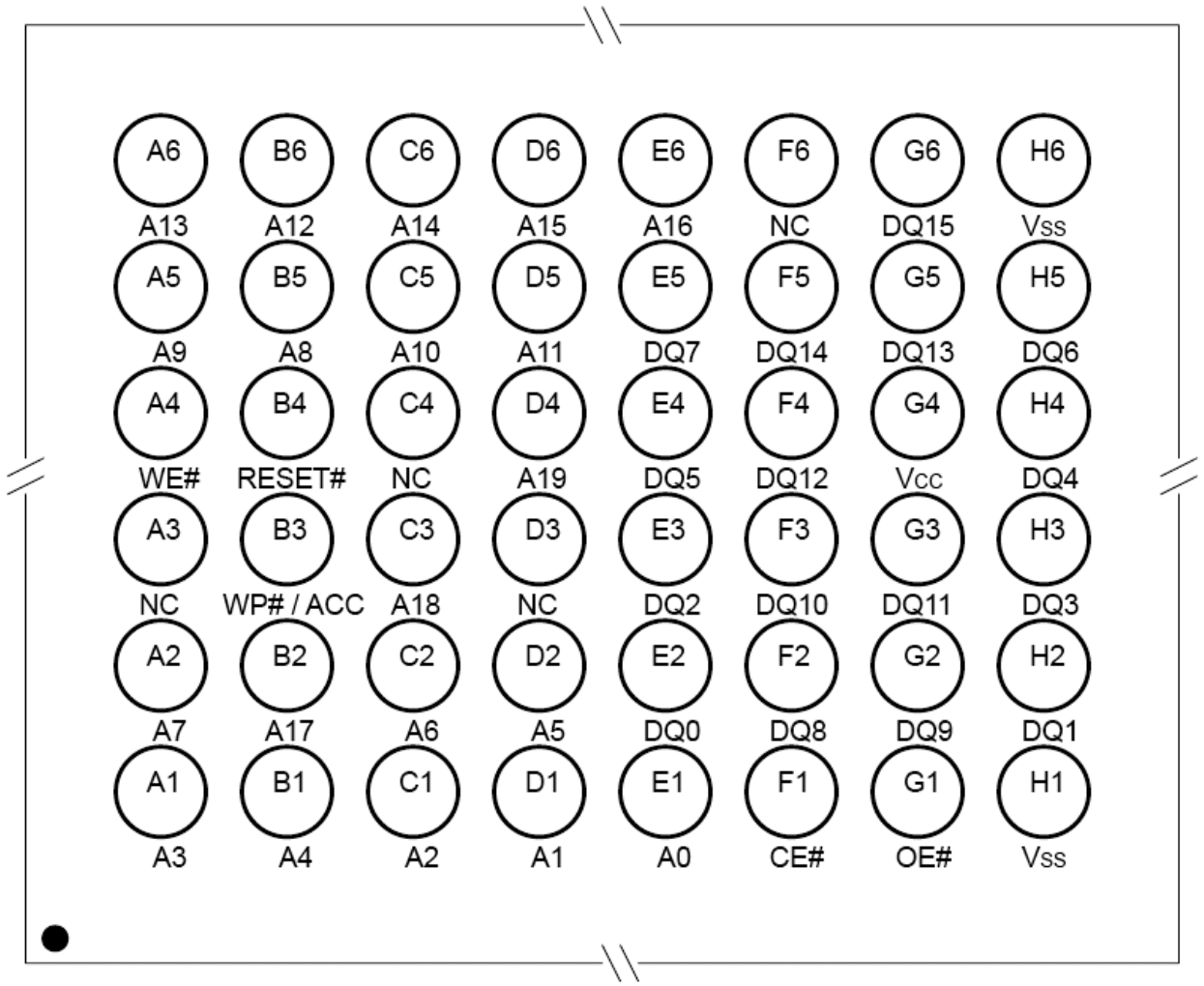
CONNECTION DIAGRAMS

TFBGA
Top View, Balls Facing Down



WFBGA
Top View, Balls Facing Down

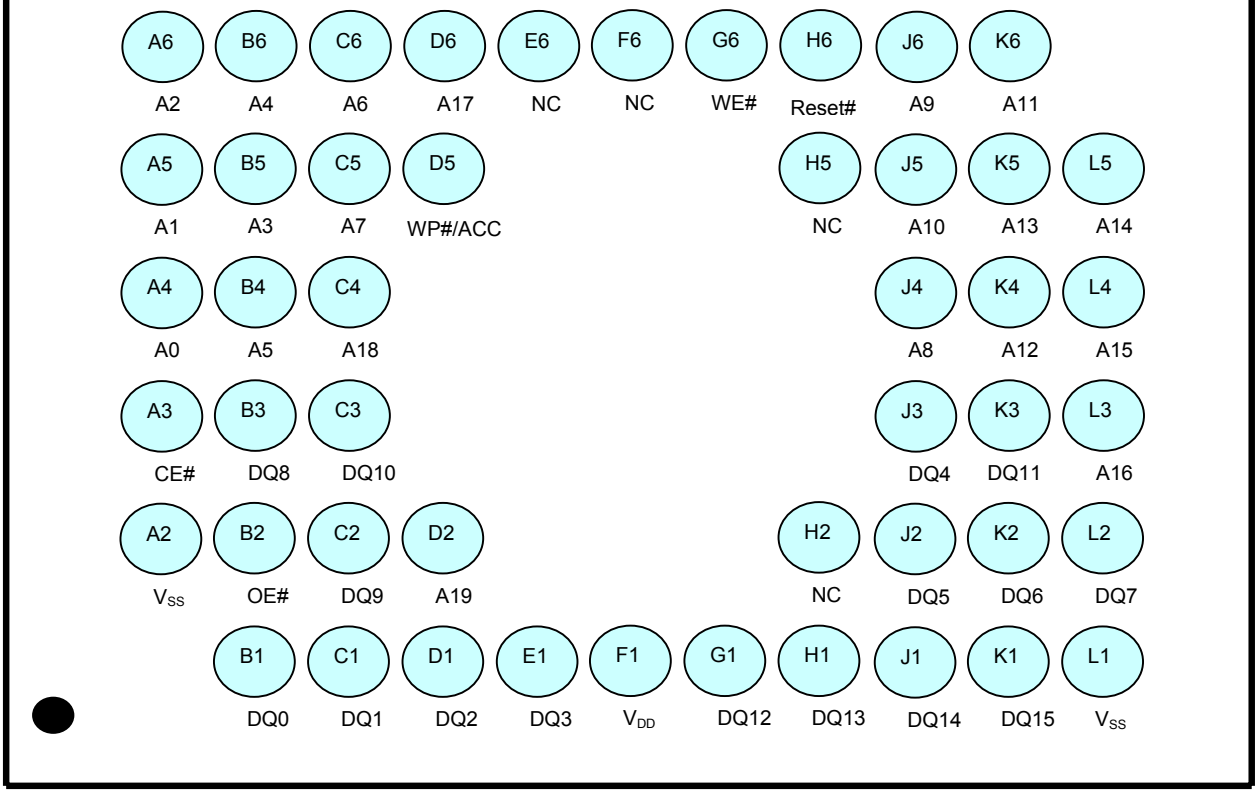


Table 1. PIN DESCRIPTION

Pin Name	Function
A0-A19	Addresses
DQ0-DQ15	16 Data Inputs/Outputs
CE#	Chip Enable
OE#	Output Enable
RESET#	Hardware Reset Pin
WE#	Write Enable
WP#/ACC	Hardware write protect/acceleration pin
Vcc	Supply Voltage (1.65-1.95V)
Vss	Ground
NC	Not Connected to anything

Figure 1. LOGIC DIAGRAM

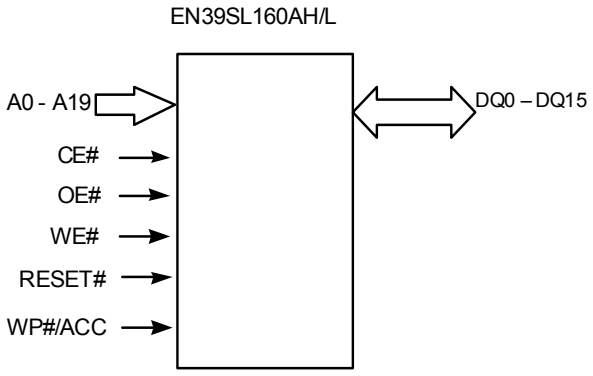


Table 2. Uniform Sector / Block Architecture (Block 24 ~ 31)

Block	Sector	Address Range (X16)	Sector Size (Kwords)	A19	A18	A17	A16	A15	A14	A13	A12	A11
31	511	0FF800h-0FFFFFh	2	1	1	1	1	1	1	1	1	1
	510	0FF000h-0FF7FFh	2	1	1	1	1	1	1	1	1	0
	509	0FE800h-0FEFFFh	2	1	1	1	1	1	1	1	0	1
	508	0FE000h-0FE7FFh	2	1	1	1	1	1	1	1	0	0
	507	0FD800h-0FDFFFh	2	1	1	1	1	1	1	0	1	1
	506	0FD000h-0FD7FFh	2	1	1	1	1	1	1	0	1	0
	505	0FC800h-0FCFFFh	2	1	1	1	1	1	1	0	0	1
	504	0FC000h-0FC7FFh	2	1	1	1	1	1	1	0	0	0
	503	0FB800h-0FBFFFh	2	1	1	1	1	1	0	1	1	1
	502	0FB000h-0FB7FFh	2	1	1	1	1	1	0	1	1	0
	501	0FA800h-0FAFFFh	2	1	1	1	1	1	0	1	0	1
	500	0FA000h-0FA7FFh	2	1	1	1	1	1	0	1	0	0
	499	0F9800h-0F9FFFh	2	1	1	1	1	1	0	0	1	1
	498	0F9000h-0F97FFh	2	1	1	1	1	1	0	0	1	0
	497	0F8800h-0F8FFFh	2	1	1	1	1	1	0	0	0	1
	496	0F8000h-0F87FFh	2	1	1	1	1	1	0	0	0	0
30	495	0F7800h-0F7FFFh	2	1	1	1	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	480	0F0000h-0F07FFh	2	1	1	1	1	0	0	0	0	0
29	479	0EF800h-0EFFFFh	2	1	1	1	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	464	0E8000h-0E87FFh	2	1	1	1	0	1	0	0	0	0
28	463	0E7800h-0E7FFFh	2	1	1	1	0	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	448	0E0000h-0E07FFh	2	1	1	1	0	0	0	0	0	0
27	447	0DF800h-0DFFFFh	2	1	1	0	1	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	432	0D8000h-0D87FFh	2	1	1	0	1	1	0	0	0	0
26	431	0D7800h-0D7FFFh	2	1	1	0	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	416	0D0000h-0D07FFh	2	1	1	0	1	0	0	0	0	0
25	415	0CF800h-0CFFFFh	2	1	1	0	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	400	0C8000h-0C87FFh	2	1	1	0	0	1	0	0	0	0
24	399	0C7800h-0C7FFFh	2	1	1	0	0	0	1	1	1	1
	398	0C7000h-0C77FFh	2	1	1	0	0	0	1	1	1	0
	397	0C6800h-0C6FFFh	2	1	1	0	0	0	1	1	0	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	386	0C1000h-0C17FFh	2	1	1	0	0	0	0	0	1	0
	385	0C0800h-0C0FFFh	2	1	1	0	0	0	0	0	0	1
	384	0C0000h-0C07FFh	2	1	1	0	0	0	0	0	0	0

Table 2. Uniform Sector / Block Architecture (Block 16 ~ 23)

Block	Sector	Address Range (X16)	Sector Size (Kwords)	A19	A18	A17	A16	A15	A14	A13	A12	A11
23	383	0BF800h-0BFFFFh	2	1	0	1	1	1	1	1	1	1
	382	0BF000h-0BF7FFh	2	1	0	1	1	1	1	1	1	0
	381	0BE800h-0BEFFFh	2	1	0	1	1	1	1	1	0	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	370	0B9000h-0B97FFh	2	1	0	1	1	1	0	0	1	0
	369	0B8800h-0B8FFFh	2	1	0	1	1	1	0	0	0	1
	368	0B8000h-0B87FFh	2	1	0	1	1	1	0	0	0	0
22	367	0B7800h-0B7FFFh	2	1	0	1	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	352	0B0000h-0B07FFh	2	1	0	1	1	0	0	0	0	0
21	351	0AF800h-0AFFFFh	2	1	0	1	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	336	0A8000h-0A87FFh	2	1	0	1	0	1	0	0	0	0
20	335	0A7800h-0A7FFFh	2	1	0	1	0	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	320	0A0000h-0A07FFh	2	1	0	1	0	0	0	0	0	0
19	319	09F800h-09FFFFh	2	1	0	0	1	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	304	098000h-0987FFh	2	1	0	0	1	1	0	0	0	0
18	303	097800h-097FFFh	2	1	0	0	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	288	090000h-0907FFh	2	1	0	0	1	0	0	0	0	0
17	287	08F800h-08FFFFh	2	1	0	0	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	272	088000h-0887FFh	2	1	0	0	0	1	0	0	0	0
16	271	087800h-087FFFh	2	1	0	0	0	0	1	1	1	1
	270	087000h-0877FFh	2	1	0	0	0	0	1	1	1	0
	269	086800h-086FFFh	2	1	0	0	0	0	1	1	0	1
	268	086000h-0867FFh	2	1	0	0	0	0	1	1	0	0
	267	085800h-085FFFh	2	1	0	0	0	0	1	0	1	1
	266	085000h-0857FFh	2	1	0	0	0	0	1	0	1	0
	265	084800h-084FFFh	2	1	0	0	0	0	1	0	0	1
	264	084000h-0847FFh	2	1	0	0	0	0	1	0	0	0
	263	083800h-083FFFh	2	1	0	0	0	0	0	1	1	1
	262	083000h-0837FFh	2	1	0	0	0	0	0	1	1	0
	261	082800h-082FFFh	2	1	0	0	0	0	0	1	0	1
	260	082000h-0827FFh	2	1	0	0	0	0	0	1	0	0
	259	081800h-081FFFh	2	1	0	0	0	0	0	0	1	1
	258	081000h-0817FFh	2	1	0	0	0	0	0	0	1	0
	257	080800h-080FFFh	2	1	0	0	0	0	0	0	0	1
	256	080000h-0807FFh	2	1	0	0	0	0	0	0	0	0

Table 2. Uniform Sector / Block Architecture (Block 8 ~ 15)

Block	Sector	Address Range (X16)	Sector Size (Kwords)	A19	A18	A17	A16	A15	A14	A13	A12	A11
15	255	07F800h-07FFFFh	2	0	1	1	1	1	1	1	1	1
	254	07F000h-07F7FFh	2	0	1	1	1	1	1	1	1	0
	253	07E800h-07EFFFh	2	0	1	1	1	1	1	1	0	1
	252	07E000h-07E7FFh	2	0	1	1	1	1	1	1	0	0
	251	07D800h-07DFFFh	2	0	1	1	1	1	1	0	1	1
	250	07D000h-07D7FFh	2	0	1	1	1	1	1	0	1	0
	249	07C800h-07CFFFh	2	0	1	1	1	1	1	0	0	1
	248	07C000h-07C7FFh	2	0	1	1	1	1	1	0	0	0
	247	07B800h-07BFFFh	2	0	1	1	1	1	0	1	1	1
	246	07B000h-07B7FFh	2	0	1	1	1	1	0	1	1	0
	245	07A800h-07AFFFh	2	0	1	1	1	1	0	1	0	1
	244	07A000h-07A7FFh	2	0	1	1	1	1	0	1	0	0
	243	079800h-079FFFh	2	0	1	1	1	1	0	0	1	1
	242	079000h-0797FFh	2	0	1	1	1	1	0	0	1	0
	241	078800h-078FFFh	2	0	1	1	1	1	0	0	0	1
	240	078000h-0787FFh	2	0	1	1	1	1	0	0	0	0
14	239	077800h-077FFFh	2	0	1	1	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	224	070000h-0707FFh	2	0	1	1	1	0	0	0	0	0
13	223	06F800h-06FFFFh	2	0	1	1	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	208	068000h-0687FFh	2	0	1	1	0	1	0	0	0	0
12	207	067800h-067FFFh	2	0	1	1	0	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	192	060000h-0607FFh	2	0	1	1	0	0	0	0	0	0
11	191	05F800h-05FFFFh	2	0	1	0	1	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	176	058000h-0587FFh	2	0	1	0	1	1	0	0	0	0
10	175	057800h-057FFFh	2	0	1	0	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	160	050000h-0507FFh	2	0	1	0	1	0	0	0	0	0
9	159	04F800h-04FFFFh	2	0	1	0	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	144	048000h-0487FFh	2	0	1	0	0	1	0	0	0	0
8	143	047800h-047FFFh	2	0	1	0	0	0	1	1	1	1
	142	047000h-0477FFh	2	0	1	0	0	0	1	1	1	0
	141	046800h-046FFFh	2	0	1	0	0	0	1	1	0	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	130	041000h-0417FFh	2	0	1	0	0	0	0	0	1	0
	129	040800h-040FFFh	2	0	1	0	0	0	0	0	0	1
	128	040000h-0407FFh	2	0	1	0	0	0	0	0	0	0

Table 2. Uniform Sector / Block Architecture (Block 0 ~ 7)

Block	Sector	Address Range (X16)	Sector Size (Kwords)	A19	A18	A17	A16	A15	A14	A13	A12	A11
7	127	03F800h-03FFFFh	2	0	0	1	1	1	1	1	1	1
	126	03F000h-03F7FFh	2	0	0	1	1	1	1	1	1	0
	125	03E800h-03EFFFh	2	0	0	1	1	1	1	1	0	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	114	039000h-0397FFh	2	0	0	1	1	1	0	0	1	0
	113	038800h-038FFFh	2	0	0	1	1	1	0	0	0	1
	112	038000h-0387FFh	2	0	0	1	1	1	0	0	0	0
6	111	037800h-037FFFh	2	0	0	1	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	96	030000h-0307FFh	2	0	0	1	1	0	0	0	0	0
5	95	02F800h-02FFFFh	2	0	0	1	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	80	028000h-0287FFh	2	0	0	1	0	1	0	0	0	0
4	79	027800h-027FFFh	2	0	0	1	0	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	64	020000h-0207FFh	2	0	0	1	0	0	0	0	0	0
3	63	01F800h-01FFFFh	2	0	0	0	1	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	48	018000h-0187FFh	2	0	0	0	1	1	0	0	0	0
2	47	017800h-017FFFh	2	0	0	0	1	0	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	32	010000h-0107FFh	2	0	0	0	1	0	0	0	0	0
1	31	00F800h-00FFFFh	2	0	0	0	0	1	1	1	1	1
	⋮	⋮	2	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	16	008000h-0087FFh	2	0	0	0	0	1	0	0	0	0
0	15	007800h-007FFFh	2	0	0	0	0	0	1	1	1	1
	14	007000h-0077FFh	2	0	0	0	0	0	1	1	1	0
	13	006800h-006FFFh	2	0	0	0	0	0	1	1	0	1
	12	006000h-0067FFh	2	0	0	0	0	0	1	1	0	0
	11	005800h-005FFFh	2	0	0	0	0	0	1	0	1	1
	10	005000h-0057FFh	2	0	0	0	0	0	1	0	1	0
	9	004800h-004FFFh	2	0	0	0	0	0	1	0	0	1
	8	004000h-0047FFh	2	0	0	0	0	0	1	0	0	0
	7	003800h-003FFFh	2	0	0	0	0	0	0	1	1	1
	6	003000h-0037FFh	2	0	0	0	0	0	0	1	1	0
	5	002800h-002FFFh	2	0	0	0	0	0	0	1	0	1
	4	002000h-0027FFh	2	0	0	0	0	0	0	1	0	0
	3	001800h-001FFFh	2	0	0	0	0	0	0	0	1	1
	2	001000h-0017FFh	2	0	0	0	0	0	0	0	1	0
	1	000800h-000FFFh	2	0	0	0	0	0	0	0	0	1
	0	000000h-0007FFh	2	0	0	0	0	0	0	0	0	0

PRODUCT SELECTOR GUIDE

Product Number		EN39SL160AH/L	
Speed Option	Full Voltage Range: Vcc=1.65 – 1.95 V	**-70**	**-90**
Max Access Time, ns (t_{acc})		70	90
Max CE# Access, ns (t_{ce})		70	90
Max OE# Access, ns (t_{oe})		30	35

BLOCK DIAGRAM

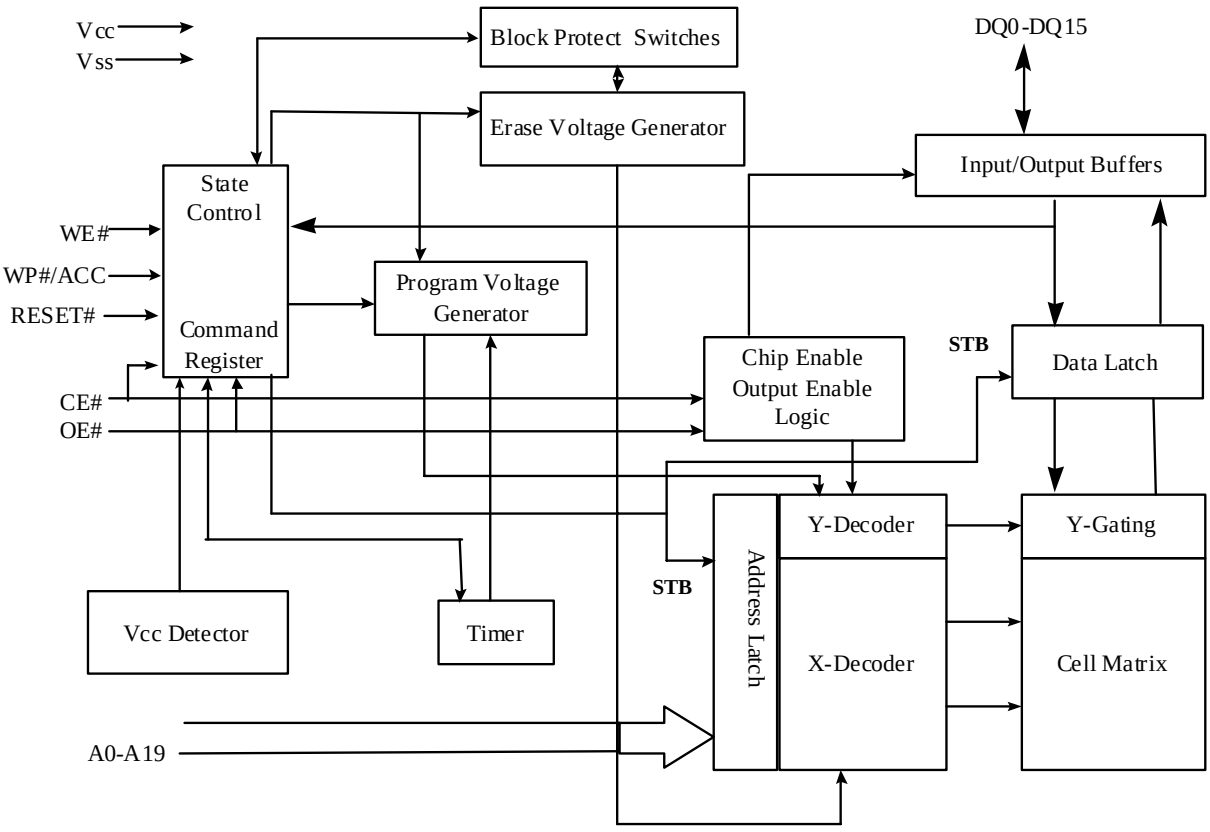


Table 3. OPERATING MODES

16M FLASH USER MODE TABLE

Operation	CE#	OE#	WE#	Reset#	WP#/ ACC	A0-A19 (Note 1)	DQ0-DQ15
Read	L	L	H	H	L / H	A_{IN}	D_{OUT}
Write	L	H	L	H	(Note 1)	A_{IN}	D_{IN}
CMOS Standby	$V_{cc} \pm 0.2V$	X	X	$V_{cc} \pm 0.2V$	X	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Hardware Reset	X	X	X	L	X	X	High-Z
Temporary Block Unprotect	X	X	X	V_{ID}	(Note 1)	A_{IN}	D_{IN}
Block Group Protect (Note 2)	L	H	L	V_{ID}	X	Block Address, A6 =L, A1 = H, A0 = L	D_{IN}
Chip Unprotect (Note 2)	L	H	L	V_{ID}	(Note 1)	Block Address, A6 =L, A1 = H, A0 = L	D_{IN}

L=logic low= V_{IL}, H=Logic High= V_{IH}, $V_{ID} = V_{HH} = 10.0 \pm 1.0V$, X=Don't Care (either L or H, but not floating!),
D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In,

Notes:
1. If WP#/ACC = V_{IL}, the first or last blocks are protected. If WP#/ACC = V_{IH} the first or last block protection depends on whether they were last protected or unprotected. If WP#/ACC = V_{HH}, all blocks will be unprotected.
2. Please refer to "Block Group Protection and Chip Unprotection ", Flowchart 7a and Flowchart 7b.

Table 4. DEVICE IDENTIFICTION (Autoselect Codes)

16M FLASH MANUFACTURER/DEVICE ID TABLE

Description	CE#	OE#	WE#	A19 to A12	A11 to A10	A9[2]	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Eon	L	L	H	X	X	V_{ID}	H[1] L	X	L	X	L	L	X	1Ch
														7Fh
Device ID (top boot block)	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	27h	4Ah
Device ID (bottom boot block)	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	27h	4Bh
Block Protection Verification	L	L	H	SA	X	V_{ID}	X	X	L	X	H	L	X	01h (Protected)
													X	00h (Unprotected)

Note:
1. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh. A further Manufacturing ID must be read with A8=H.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

USER MODE DEFINITIONS

Standby Mode

The EN39SL160AH/L has a CMOS-compatible standby mode, which reduces the current to < 0.2μA (typical). It is placed in CMOS-compatible standby when the CE# pin is at $V_{CC} \pm 0.2$. RESET# pin must also be at CMOS input levels. If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.2V$, the device will be in the standby modes, but the standby current will be greater. The outputs are in a high-impedance state independent of the OE# input.

Read Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors/blocks, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" additional details.

Output Disable Mode

When the OE# pin is at a logic high level (V_{IH}), the output from the EN39SL160AH/L is disabled. The output pins are placed in a high impedance state.

Auto Select Identification Mode

The autoselect mode provides manufacturer and device identification, and block protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (9.0 V to 11.0 V) on address pin A9. Address pins A8, A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying block protection, the block address must appear on the appropriate highest order address bits. Refer to the corresponding block Address Tables. The Command Definitions table shows the remaining address bits that are don't-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Write Mode

Write operations, including programming data and erasing sectors/blocks of memory, require the host system to write a command or command sequence to the device. Write cycles are initiated by placing the word address on the device's address inputs while the data to be written is input on DQ[15:0] in Word Mode. The host system must drive the CE# and WE# pins Low and the OE# pin High for a valid write operation to take place. All addresses are latched on the falling edge of WE# and CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. The system is not required to provide further controls or timings. The device automatically provides internally generated program / erase

pulses and verifies the programmed /erased cells' margin. The host system can detect completion of a program or erase operation by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits.

The 'Command Definitions' section of this document provides details on the specific device commands implemented in the EN39SL160AH/L.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at Vss±0.3 V, the device draws CMOS standby current (Icc2). If RESET# is held at V_{IL} but not within Vss±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firm- ware from the Flash memory.

Block Group Protection and Chip Unprotection

The hardware block group protection feature disables both program and erase operations in any block. The hardware chip unprotection feature re-enables both program and erase operations in previously protected blocks. A block group implies three or four adjacent blocks that would be protected at the same time. Please see the following tables which show the organization of block groups.

There are two methods to enable this hardware protection circuitry. The first one requires only that the RESET# pin be at V_{ID} and then standard microprocessor timings can be used to enable or disable this feature. See Flowchart 7a and 7b for the algorithm and Figure 12 for the timings. When doing Chip Unprotect, all the other blocks should be protected first.

The second method is meant for programming equipment. This method requires V_{ID} be applied to both OE# and A9 pin and non-standard microprocessor timings are used. This method is described in a separate document called EN39SL160AH/L Supplement, which can be obtained by contacting a representative of Eon Silicon Solution, Inc.

Table 5. Block Group Organization for (Un)Protection (Block Group 5~9)

Block Group	Block	Sector	Address range (X16)
9	31	511	0FF800h-0FFFFFh
		⋮	⋮
		496	0F8000h-0F87FFh
8	30	495	0F7800h-0F7FFFh
		⋮	⋮
		480	0F0000h-0F07FFh
	29	479	0EF800h-0EFFFFh
		⋮	⋮
		464	0E8000h-0E87FFh
	28	463	0E7800h-0E7FFFh
		⋮	⋮
		448	0E0000h-0E07FFh
7	27	447	0DF800h-0DFFFFh
		⋮	⋮
		432	0D8000h-0D87FFh
	26	431	0D7800h-0D7FFFh
		⋮	⋮
		416	0D0000h-0D07FFh
	25	415	0CF800h-0CFFFFh
		⋮	⋮
		400	0C8000h-0C87FFh
	24	399	0C7800h-0C7FFFh
		⋮	⋮
		384	0C0000h-0C07FFh
6	23	383	0BF800h-0BFFFFh
		⋮	⋮
		368	0B8000h-0B87FFh
	22	367	0B7800h-0B7FFFh
		⋮	⋮
		352	0B0000h-0B07FFh
	21	351	0AF800h-0AFFFFh
		⋮	⋮
		336	0A8000h-0A87FFh
	20	335	0A7800h-0A7FFFh
		⋮	⋮
		320	0A0000h-0A07FFh
5	19	319	09F800h-09FFFFh
		⋮	⋮
		304	098000h-0987FFh
	18	303	097800h-097FFFh
		⋮	⋮
		288	090000h-0907FFh
	17	287	08F800h-08FFFFh
		⋮	⋮
		272	088000h-0887FFh
	16	271	087800h-087FFFh
		⋮	⋮
		256	080000h-0807FFh

Table 5. Block Group Organization for (Un)Protection (Block Group 0~4)

Block Group	Block	Sector	Address range (X16)
4	15	255	07F800h-07FFFFh
		⋮	⋮
		240	078000h-0787FFh
	14	239	077800h-077FFFh
		⋮	⋮
		224	070000h-0707FFh
	13	223	06F800h-06FFFFh
		⋮	⋮
		208	068000h-0687FFh
	12	207	067800h-067FFFh
		⋮	⋮
		192	060000h-0607FFh
3	11	191	05F800h-05FFFFh
		⋮	⋮
		176	058000h-0587FFh
	10	175	057800h-057FFFh
		⋮	⋮
		160	050000h-0507FFh
	9	159	04F800h-04FFFFh
		⋮	⋮
		144	048000h-0487FFh
	8	143	047800h-047FFFh
		⋮	⋮
		128	040000h-0407FFh
2	7	127	03F800h-03FFFFh
		⋮	⋮
		112	038000h-0387FFh
	6	111	037800h-037FFFh
		⋮	⋮
		96	030000h-0307FFh
	5	95	02F800h-02FFFFh
		⋮	⋮
		80	028000h-0287FFh
	4	79	027800h-027FFFh
		⋮	⋮
		64	020000h-0207FFh
1	3	63	01F800h-01FFFFh
		⋮	⋮
		48	018000h-0187FFh
	2	47	017800h-017FFFh
		⋮	⋮
		32	010000h-0107FFh
	1	31	00F800h-00FFFFh
		⋮	⋮
		16	008000h-0087FFh
0	0	15	007800h-007FFFh
		⋮	⋮
		0	000000h-0007FFh

Write Protect / Accelerated Program (WP# / ACC)

The WP#/ACC pin provides two functions. The Write Protect (WP#) function provides a hardware method of protecting the first or last 64K-byte Block. The ACC function allows faster manufacturing throughput at the factory, using an external high voltage.

When WP#/ACC is Low, the device protects the first or last 64K-byte Block; no matter the blocks are protected or unprotected using the method described in "Block/Block Group Protection & Chip Unprotection", Program and Erase operations in these blocks are ignored.

When WP#/ACC is High, the device reverts to the previous protection status of the first or last 64K-byte Block. Program and Erase operations can now modify the data in the first or last 64K-byte Block unless the block is protected using Block Protection.

When WP#/ACC is raised to V_{HH} the memory automatically enters the Accelerated Program mode, this mode permit the system to skip the normal command unlock sequences and program byte/word locations directly to reduces the time required for program operation. When WP#/ACC returns to V_{IH} or V_{IL} normal operation resumes. The transitions from V_{IH} or V_{IL} to V_{HH} and from V_{HH} to V_{IH} or V_{IL} must be slower than t_{VHH}, see Figure 14

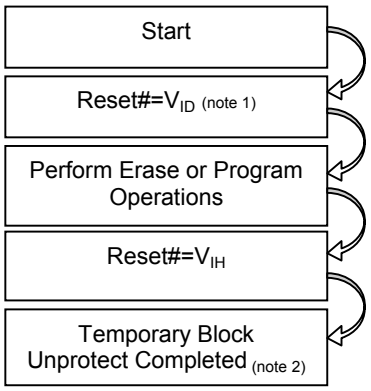
Note that the WP#/ACC pin must not be left floating or unconnected. In addition, WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming. It could cause the device to be damaged.

Never raise this pin to V_{HH} from any mode except Read mode. Otherwise the memory may be left in an indeterminate state.

A 0.1μF capacitor should be connected between the WP#/ACC pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Accelerated Program mode.

Temporary Block Unprotect

This feature allows temporary unprotection of previously protected block groups to change data while in-system. The Block Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected blocks can be programmed or erased by simply selecting the Block addresses. Once is removed from the RESET# pin, all the previously protected blocks are protected again. See accompanying figure and timing diagrams for more details.



Notes:
1. All protected blocks unprotected.
2. Previously protected blocks protected again.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{acc} + 30ns. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output is latched and always available to the system. Icc_5 in the DC Characteristics table represents the automatic sleep mode current specification.

COMMON FLASH INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data.

The system can read CFI information at the addresses given in Tables 6-8. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode and the system can read CFI data at the addresses given in Tables 6–8. The system must write the reset command to return the device to the autoselect mode.

Table 6. CFI Query Identification String (1)

Adresses (Word Mode)	Adresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

1. Refer to CFI publication 100 for more details.

Table 7. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0016h	Vcc Min (write /erase) DQ7-DQ4: volts, DQ3 –DQ0: 100 millivolts
1Ch	38h	0020h	Vcc Max (write /erase) DQ7-DQ4: volts, DQ3 –DQ0: 100 millivolts
1Dh	3Ah	0000h	Vpp Min. voltage (00h = no Vpp pin present)
1Eh	3Ch	0000h	Vpp Max. voltage (00h = no Vpp pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word program 2^N µs
20h	40h	0000h	Typical timeout for Min, size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual sector/block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual sector/block erase 2^N times typical
26h	4Ch	0000h	Max timeout for full chip erase 2^N times typical (00h = not supported)

Table 8. Device Geometry Definition

Addresses (Word mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0015h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description; 0002h = x8/x16 asynchronous interface.
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Sector/Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00FFh 0001h 0010h 0000h	Erase Sector Region 1 Information (y+1 = Number of sectors; z x 256B = sector size) y = 511 + 1 = 512 sectors (01FFh = 511) z = 16 x 256 Bytes = 4 KByte/sector (0010h = 16)
31h 32h 33h 34h	62h 64h 66h 68h	001Fh 0000h 0000h 0001h	Erase Block Region 2 Information (y+1 = Number of blocks; z x 256B = block size) y = 31 + 1 = 32 blocks (001Fh = 31) z = 256 x 256 Bytes = 64 KByte/block (0100h = 256)

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

Low V_{CC} Write Inhibit

When Vcc is less than V_{LKO}, the device does not accept any write cycles. This protects data during Vcc power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than V_{LKO}.

Write Pulse “Glitch” protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one. If CE#, WE#, and OE# are all logical zero (not recommended usage), it will be considered a read.

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with CE# = V_{IL}, WE# = V_{IL} and OE# = V_{IH}, the device will not accept commands on the rising edge of WE#.

COMMAND DEFINITIONS

The operations of EN39SL160AH/L are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Block Protection, Program, Sector/Block Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 9). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

Table 9. EN39SL160AH/L Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	xxx	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
										100	1C				
		Byte		AAA		555		AAA		000	7F				
										200	1C				
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	X01	274A				
		Byte		AAA		555		AAA		X02	4A				
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	X01	274B				
		Byte		AAA		555		AAA		X02	4B				
	Block Protect Verify	Word	4	555	AA	2AA	55	555	90	(BA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(BA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Block Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	50
		Byte		AAA		555		AAA		AAA		555			
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend			1	xxx	B0										
Erase Resume			1	xxx	30										
CFI Query		Word	1	55	98										
		Byte		AA											

Address and Data values indicated in hex
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care
PD = Program Data: data to be programmed at location PA
BA = Block Address: address of the Block to be erased or verified. Address bits A19-A15 uniquely select any Block
SA = Sector Address: address of the Sector to be erased or verified. Address bits A19-A11 uniquely select any Sector

Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following an Erase Suspend command, Erase Suspend mode is entered. The system can read array data using the standard read timings, with the only difference in that if it reads at an address within erase suspended sectors/blocks, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See next section for details on Reset.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a block is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires V_{ID} on address bit A9 and is intended for PROM programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 4 any number of times, without needing another command sequence.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Programming Command

Programming the EN39SL160AH/L is performed by using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of CE# or WE#, whichever is last; data is latched on the rising edge of CE# or WE#, whichever is first.

Programming status may be checked by sampling data on DQ7 (DATA# polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a 0 to a 1. Only an erase operation can change a data from 0 to 1. When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Flowchart 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and to the Chip, Sector/Block Erase Operation Timings for timing waveforms.

Sector/Block Erase Command Sequence

Sector/Block erase is a six bus cycle operation. The sector/block erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector/block to be erased, and the sector/block erase command. The Command Definitions table shows the address and data requirements for the sector/block erase command sequence.

Once the sector/block erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector/Block Erase Operations Timing diagram for timing waveforms.

Erase Suspend / Resume Command

The Erase Suspend command allows the system to interrupt a sector/block erase operation and then read data from, or program data to, any sector/block not selected for erasure. This command is valid only during the sector/block erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector/block erase operation, the device requires a maximum of 20 μs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector/block not selected for erasure. (The device “erase suspends” all sector/blocks selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors/blocks produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector/block is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.
After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors/blocks. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Erase Suspend Mode.

The system must write the Erase Resume command (address bits are don't-care) to exit the erase suspend mode and continue the sector/block erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

WRITE OPERATION STATUS

DQ7: DATA# Polling

The EN39SL160AH/L provides DATA# polling on DQ7 to indicate the status of the embedded operations. The DATA# Polling feature is active during the embedded Programming, Sector/Block Erase, Chip Erase, and Erase Suspend. (See Table 6)

When the embedded Programming is in progress, an attempt to read the device will produce the complement of the data last written to DQ7. Upon the completion of the embedded Programming, an attempt to read the device will produce the true data written to DQ7. For the embedded Programming, DATA# polling is valid after the rising edge of the fourth WE# or CE# pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a "0" at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the "1" at the DQ7 output during the read cycles. For Chip Erase, the DATA# polling is valid after the rising edge of the sixth WE# or CE# pulse in the six-cycle sequence. DATA# polling is valid after the last rising edge of the WE# or CE# pulse for chip erase or sector/block erase.

DATA# Polling must be performed at any address within a sector/block that is being programmed or erased and not a protected sector/block. Otherwise, DATA# polling may give an inaccurate result if the address used is in a protected block.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable (OE#) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for DATA# Polling (DQ7) is shown on Flowchart 5. The DATA# Polling (DQ7) timing diagram is shown in Figure 8.

DQ6: Toggle Bit I

The EN39SL160AH/L provides a "Toggle Bit" on DQ6 to indicate to the host system the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by active OE# or CE#) will result in DQ6 toggling between "zero" and "one". Once the embedded Program or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During embedded Programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four-cycle sequence. During Erase operation, the Toggle Bit is valid after the rising edge of the sixth WE# pulse for sector/block erase or chip erase.

In embedded Programming, if the block being written to is protected, DQ6 will toggles for about 2 μs, then stop toggling without the data in the block having changed. In Sector/Block Erase or Chip Erase, if all selected blocks are protected, DQ6 will toggle for about 100 μs. The chip will then return to the read mode without changing data in all protected blocks.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a "1" on DQ5.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1." Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector/Block Erase Timer

After writing a sector/block erase command sequence, the output on DQ3 can be used to determine whether or not an erase operation has begun. (The sector/block erase timer does not apply to the chip erase command.) When sector/block erase starts, DQ3 switches from "0" to "1." This device does not support multiple sector/block erase command sequences so it is not very meaningful since it immediately shows as a "1" after the first 30h command. Future devices may support this feature.

DQ2: Erase Toggle Bit II

The "Toggle Bit" on DQ2, when used with DQ6, indicates whether a particular sector/block is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector/block is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors/blocks that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector/block is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors/blocks are selected for erasure. Thus, both status bits are required for sector/block and mode information. Refer to the following table to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section "DQ2: Toggle Bit" explains the algorithm. See also the "DQ6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to

perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Flowchart 6).

Write Operation Status

Operation		DQ7 (note2)	DQ6	DQ5 (note1)	DQ3	DQ2 (note2)
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector/Block	1	No Toggle	0	N/A	Toggle
	Reading within Non-Erase Suspended Sector/Block	Data	Data	Data	Data	Data
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5:Exceeded Timing Limits" for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

Table 10. Status Register Bits

DQ	Name	Logic Level	Definition
7	DATA# POLLING	'1'	Erase Complete or erase Sector/Block in Erase suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erase Sector/Block during Erase Suspend
		DQ7#	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	TIME OUT BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	ERASE TIME OUT BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Sector/Block Erase or Erase suspend on currently addressed Sector/Block. (When DQ5=1, Erase Error due to currently addressed Sector/Block. Program during Erase Suspend on-going at current address
		DQ2	Erase Suspend read on non Erase Suspend Sector/Block

Notes:

DQ7 DATA# Polling: indicates the P/E C status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6 Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

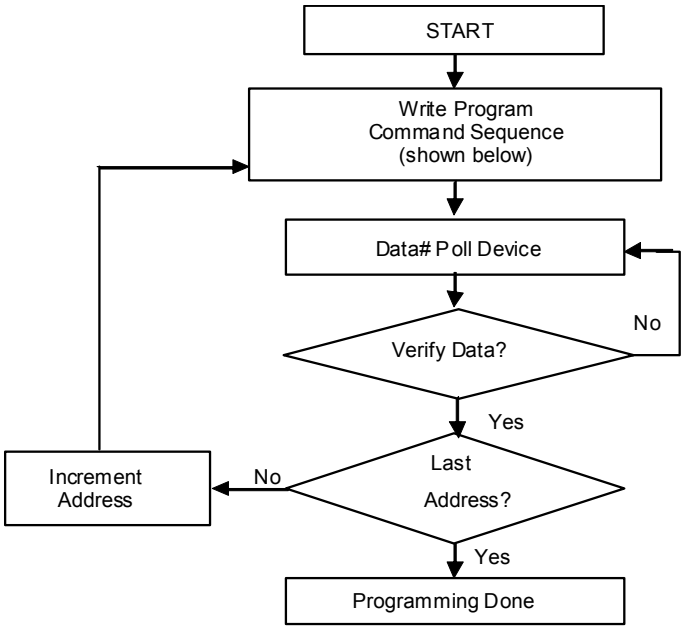
DQ5 Time Out Bit: set to "1" if failure in programming or erase

DQ3 Sector/Block Erase Command Timeout Bit :Operation has started. Only possible command is Erase suspend (ES).

DQ2 Toggle Bit: indicates the Erase status and allows identification of the erased Sector/Block

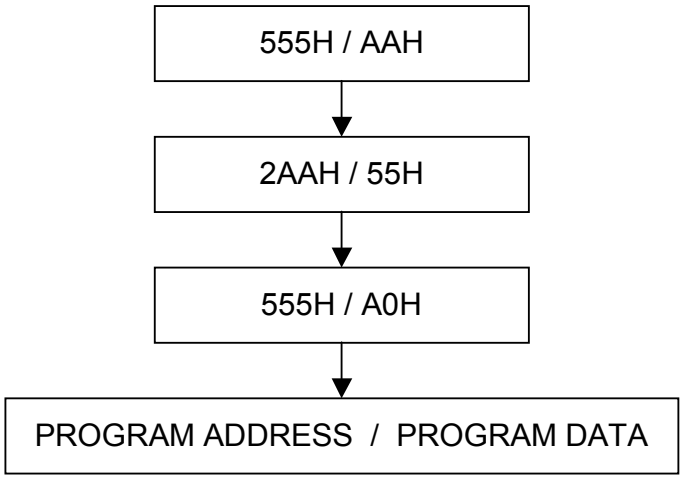
EMBEDDED ALGORITHMS

Flowchart 1. Embedded Program

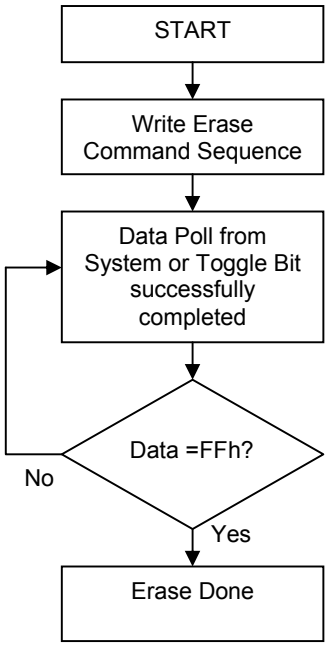


Flowchart 2. Embedded Program Command Sequence

See the Command Definitions section for more information on WORD mode.

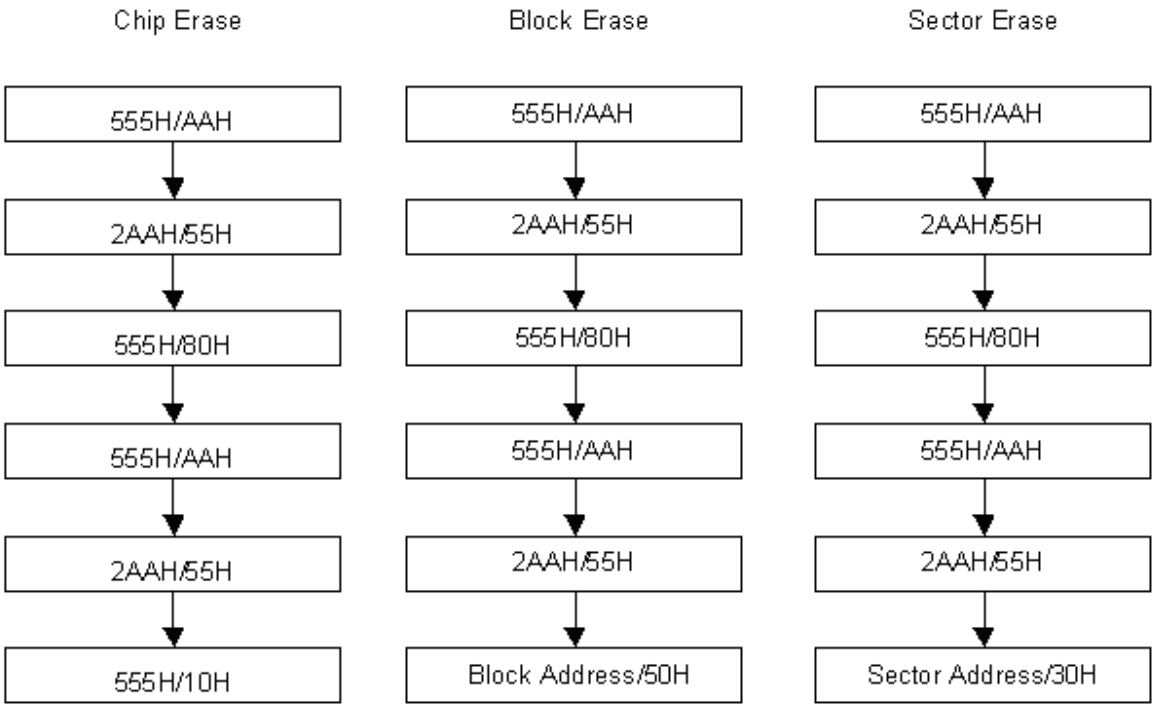


Flowchart 3. Embedded Erase

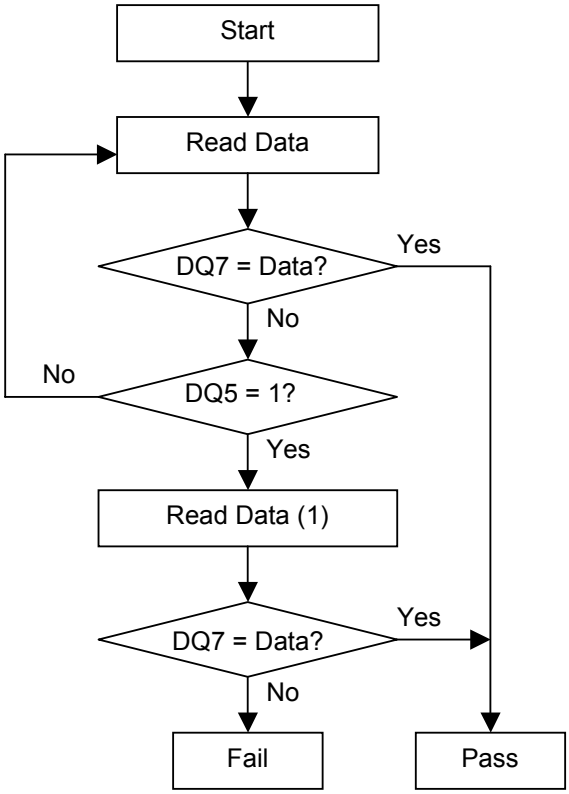


Flowchart 4. Embedded Erase Command Sequence

See the Command Definitions section for more information on WORD mode.

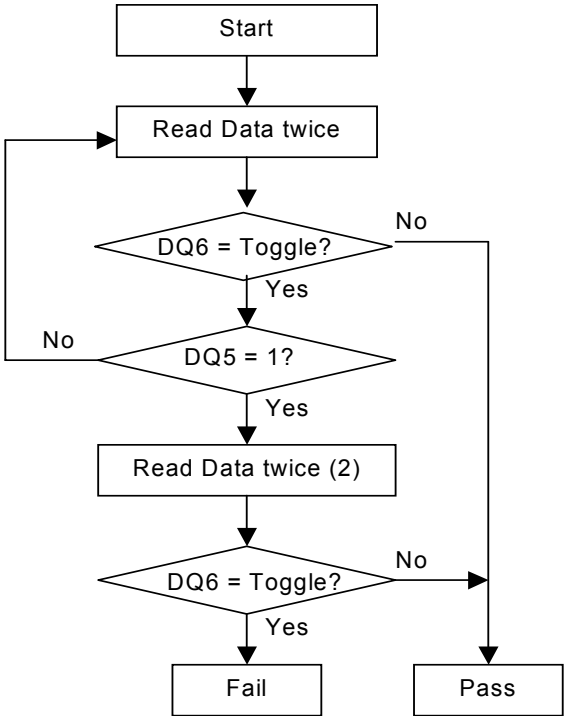


Flowchart 5. DATA# Polling Algorithm



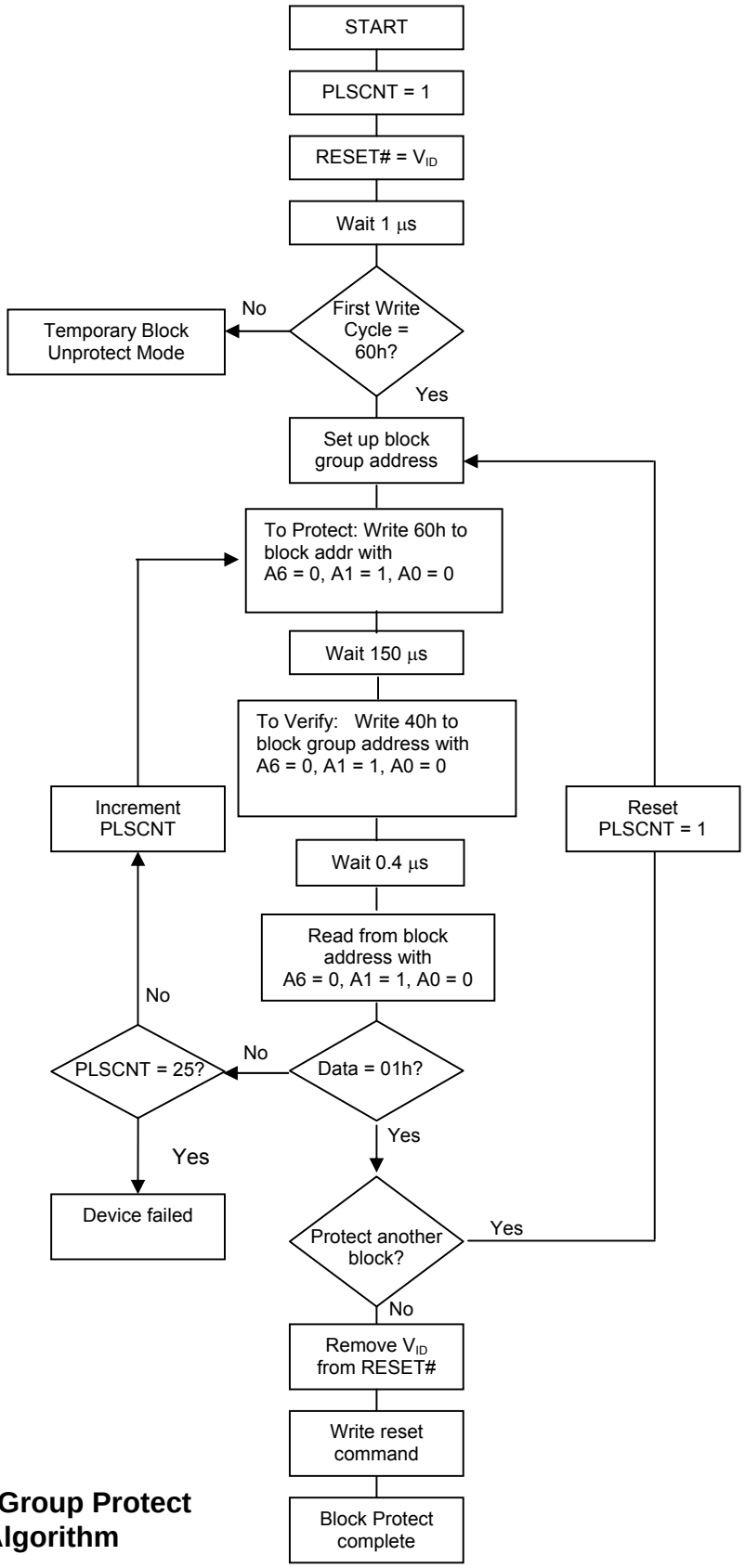
Notes:
(1) This second read is necessary in case the first read was done at the exact instant when the status data was in transition.

Flowchart 6. Toggle Bit Algorithm



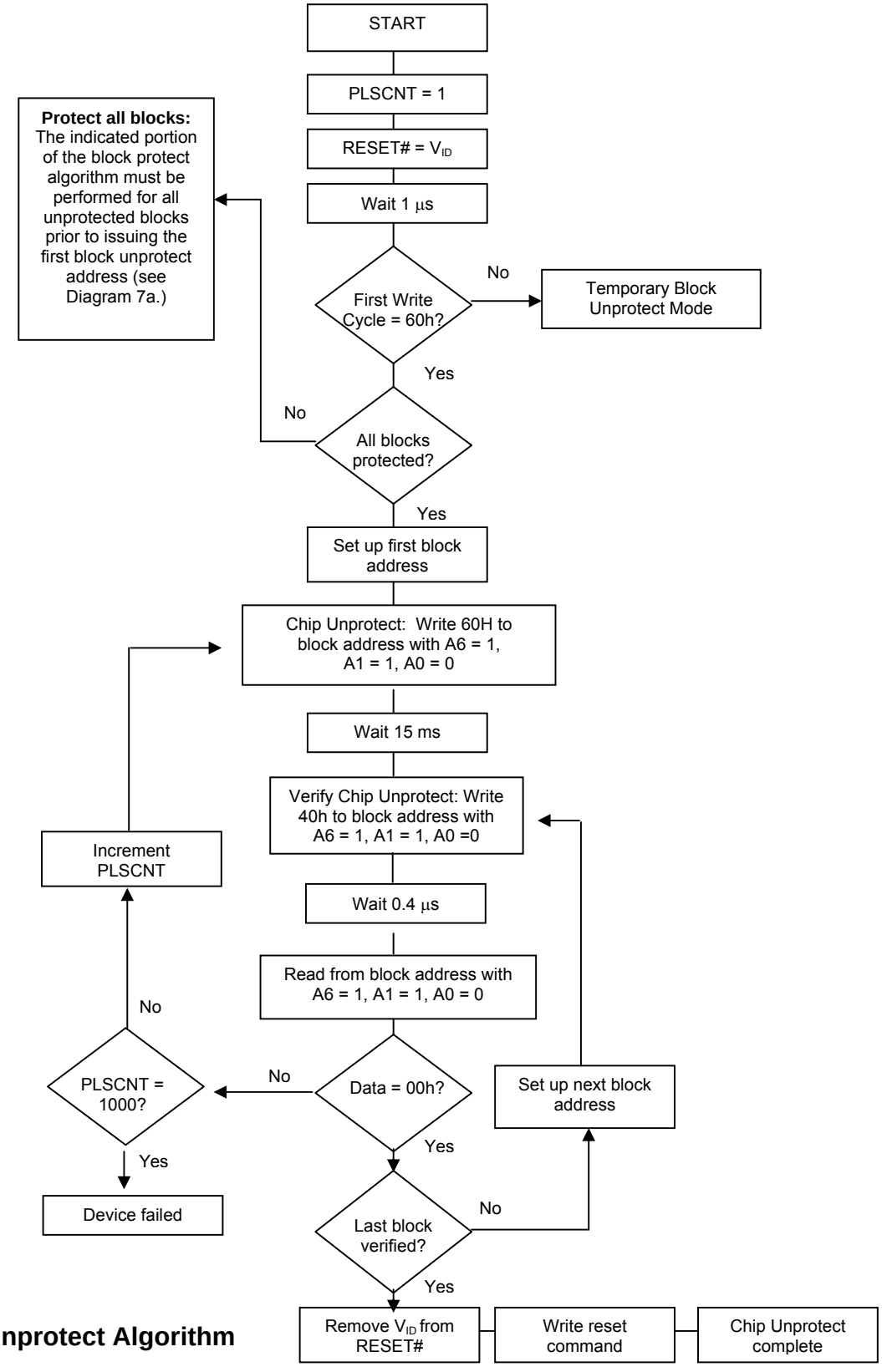
Notes:
(2) This second set of reads is necessary in case the first set of reads was done at the exact instant when the status data was in transition.

Flowchart 7a. In-System Block Group Protect Flowchart



Block Group Protect Algorithm

Flowchart 7b. In-System Chip Unprotect Flowchart



Chip Unprotect Algorithm

Table 11. DC Characteristics

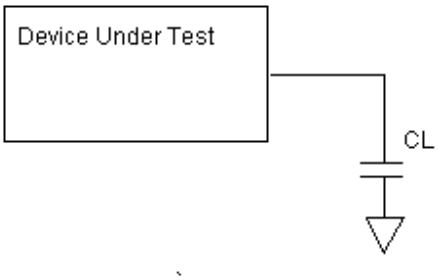
(T_a = - 40°C to 85°C or - 45°C to 125°C; V_{CC} = 1.65-1.95V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ Vcc			±3	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤ Vcc			±3	µA
I_{CC1}	Active Read Current (Byte mode)	CE# = V_{IL}, OE# = V_{IH}, F=5MHz		5	10	mA
	Active Read Current (Word mode)			5	10	mA
I_{CC2}	Supply Current (Standby)	CE# = RESET# = Vcc (Note 1)		0.2	5.0	µA
	Supply Current (Standby) For Automotive (-45°C to +125°C)	CE# = RESET# = Vcc (Note 1)		0.2	15	µA
I_{CC3}	VCC , Reset Current	CE# = RESET# = Vss ± 0.2 V (Note 1)		0.2	5.0	µA
	VCC , Reset Current For Automotive (-45°C to +125°C)	CE# = RESET# = Vss ± 0.2 V (Note 1)		0.2	15	µA
I_{CC4}	Supply Current (Program or Erase)	Program or Erase in progress		15	25	mA
I_{CC5}	Automatic Sleep Mode	V_{IH} = Vcc ± 0.2 V V_{IL} = Vss ± 0.2 V		0.2	5.0	µA
	Automatic Sleep Mode For Automotive (-45°C to +125°C)	V_{IH} = Vcc ± 0.2 V V_{IL} = Vss ± 0.2 V		0.2	15	µA
V_{IL}	Input Low Voltage		-0.5		0.3 x VCC	V
V_{IH}	Input High Voltage		0.7 x Vcc		Vcc + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA,	Vcc - 0.1			V
V_{ID}	A9 Voltage (Electronic Signature)		9.0	10.0	11.0	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}			50	µA
V_{LKO}	Supply voltage (Erase and Program lock-out)		1.2		1.5	V

Notes

1. RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.
2. Maximum I_{CC} specifications are tested with Vcc = Vcc max.

Test Conditions



Test Specifications

Test Conditions	-70	-90	Unit
Output Load Capacitance, C_L	30		pF
Input Rise and Fall times	5		ns
Input Pulse Levels	0.0-2.0		V
Input timing measurement reference levels	1/2 Vcc		V
Output timing measurement reference levels	1/2 Vcc		V

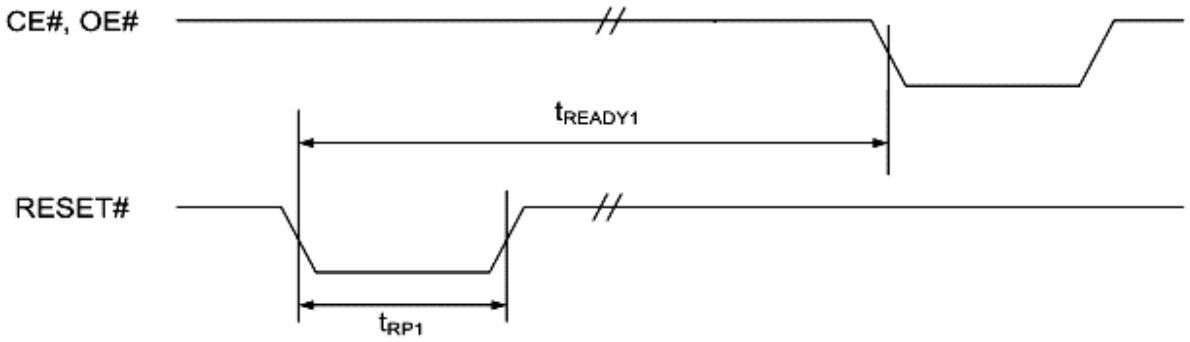
AC CHARACTERISTICS

Hardware Reset (Reset#)

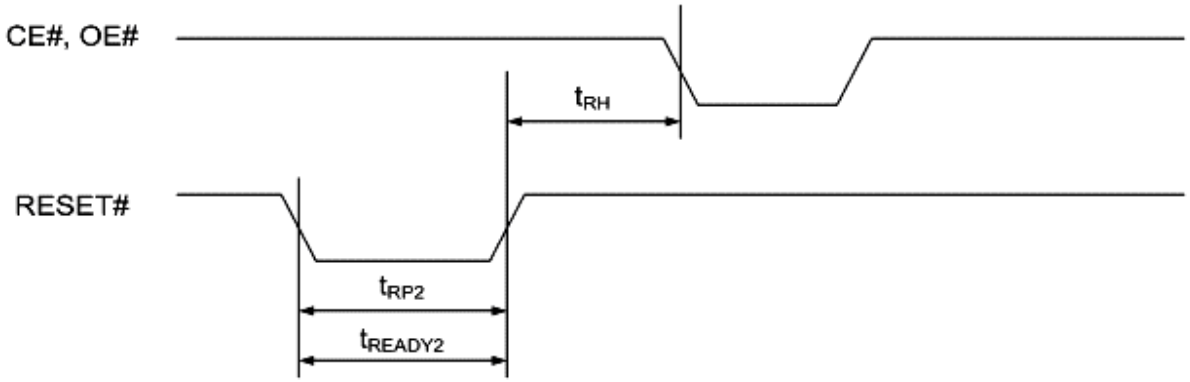
(T_a = - 40°C to 85°C or - 45°C to 125°C; V_{CC} = 1.65-1.95V)

Parameter Std	Description	Test Setup	Speed		Unit
			-70	-90	
t_{RP1}	RESET# Pulse Width (During Embedded Algorithms)	Min	10		us
t_{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	Min	500		ns
t_{RH}	Reset# High Time Before Read	Min	50		ns
t_{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	Max	20		us
t_{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	Max	500		ns

Figure 2. AC Waveforms for RESET#
Reset# Timings



Reset Timing during Embedded Algorithms



Reset Timing NOT during Embedded Algorithms

AC CHARACTERISTICS

Table 12. AC CHARACTERISTICS

(T_a = - 40°C to 85°C or - 45°C to 125°C; V_{CC} = 1.65-1.95 V)

Read-only Operations Characteristics

Parameter Symbols		Description		Test Setup		Speed Options		Unit
JEDEC	Standard					-70	-90	
t_{AVAV}	t_{RC}	Read Cycle Time			Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay		OE# = V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z			Max	20		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z			Max	20		ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, whichever occurs first			Min	0		ns
	t_{OEH}	Output Enable Hold Time	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes:

1. High Z is Not 100% tested.
2. For – 70, 90 Vcc =1.65 – 1.95V Output Load : 30pF
   Input Rise and Fall Times: 5ns Input Rise Levels: 0.0 V to Vcc
   Timing Measurement Reference Level, Input and Output: 1/2 Vcc

Figure 3. AC Waveforms for READ Operations

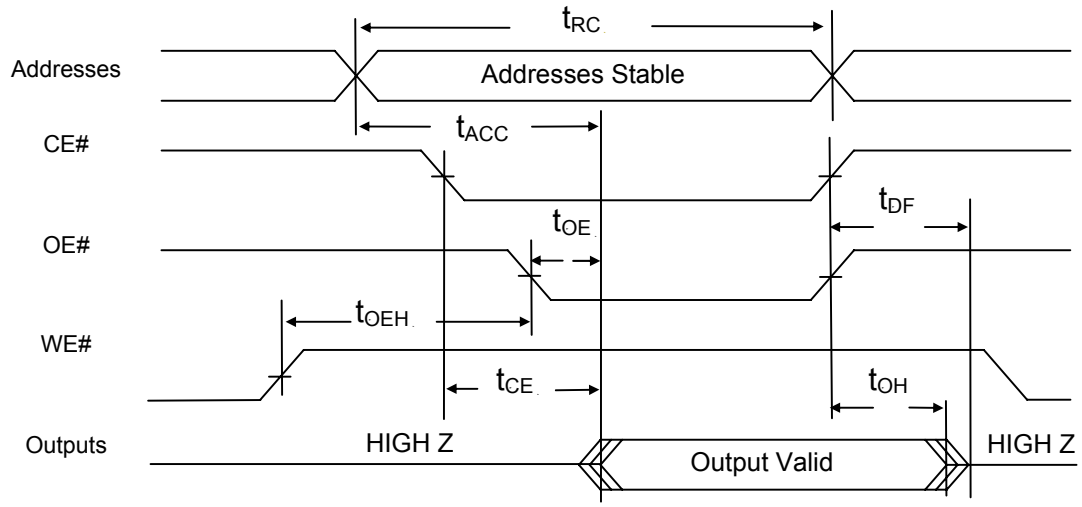


Table 13. AC CHARACTERISTICS

(T_a = - 40°C to 85°C or - 45°C to 125°C; V_{CC} = 1.65-1.95V)

Write (Erase/Program) Operations

Parameter Symbols		Description			Speed Options		
JEDEC	Standard				-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	40	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	45	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	25	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)		Typ	8		µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 2)	Sector	Typ	0.09		s
			Block	Typ	0.18		s
			Chip	Typ	4		s
	t_{VCS}	Vcc Setup Time (Note 1)		Min	50		µs

Notes:
1. Not 100% tested.
2. See Erase and Programming Performance for more information.

Table 14. AC CHARACTERISTICS

(T_a = - 40°C to 85°C or - 45°C to 125°C; V_{CC} = 1.65-1.95V)

Write (Erase/Program) Operations

Alternate CE# Controlled Writes

Parameter Symbols		Description			Speed Options		
JEDEC	Standard				-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45		ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	40	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write (OE# High to CE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	45	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)		Typ	8		µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 2)	Sector	Typ	0.09		s
			Block	Typ	0.18		s
			Chip	Typ.	4		s

Notes:
1. Not 100% tested.
2. See Erase and Programming Performance for more information.

Table 15. ERASE AND PROGRAMMING PERFORMANCE

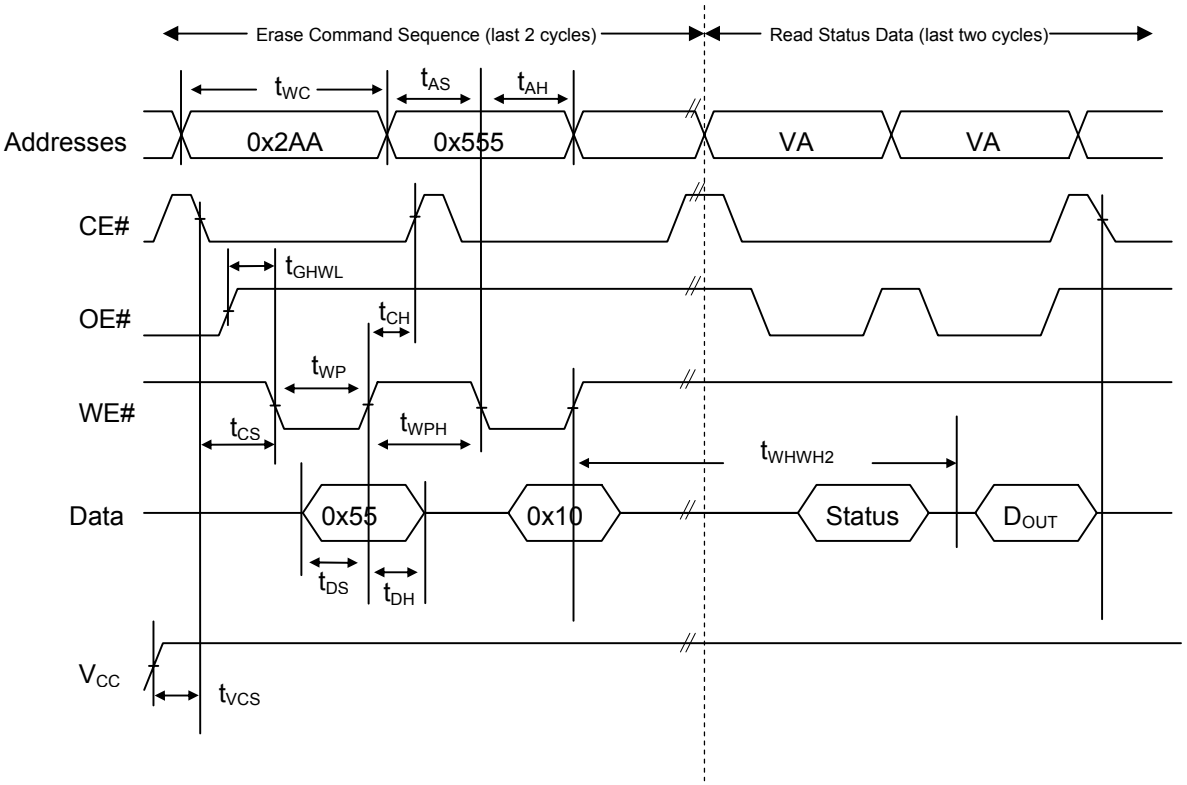
Parameter	Limits			Comments
	Typ	Max	Unit	
Sector Erase Time	0.09	0.4	sec	Excludes 00H programming prior to erasure
Block Erase Time	0.18	2	sec	
Chip Erase Time	4	35	sec	
Word Programming Time	8	200	µs	Excludes system level overhead
Chip Programming Time	8	11	sec	
Erase/Program Endurance	100K		cycles	Minimum 100K cycles

Table 16. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years

AC CHARACTERISTICS

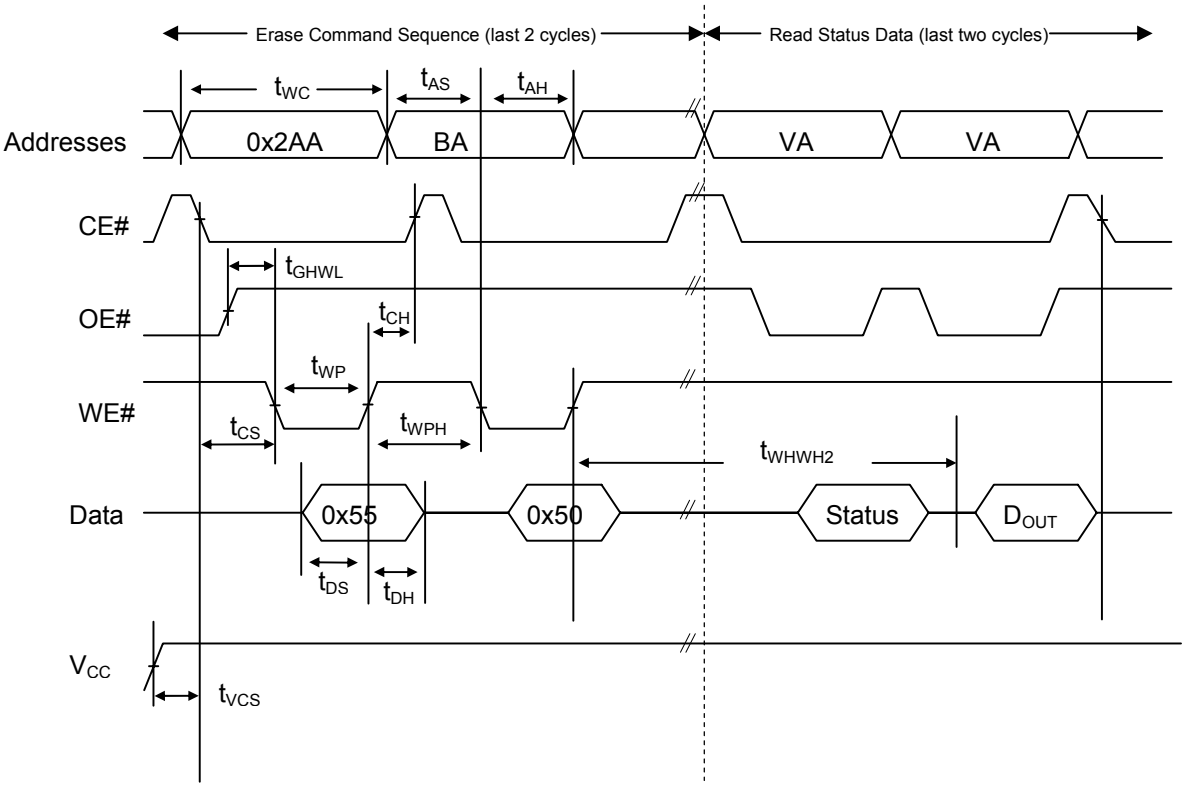
Figure 4. AC Waveforms for Chip Erase Operations Timings



Notes:
1. VA=Valid Address for reading status, D_{out} = true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

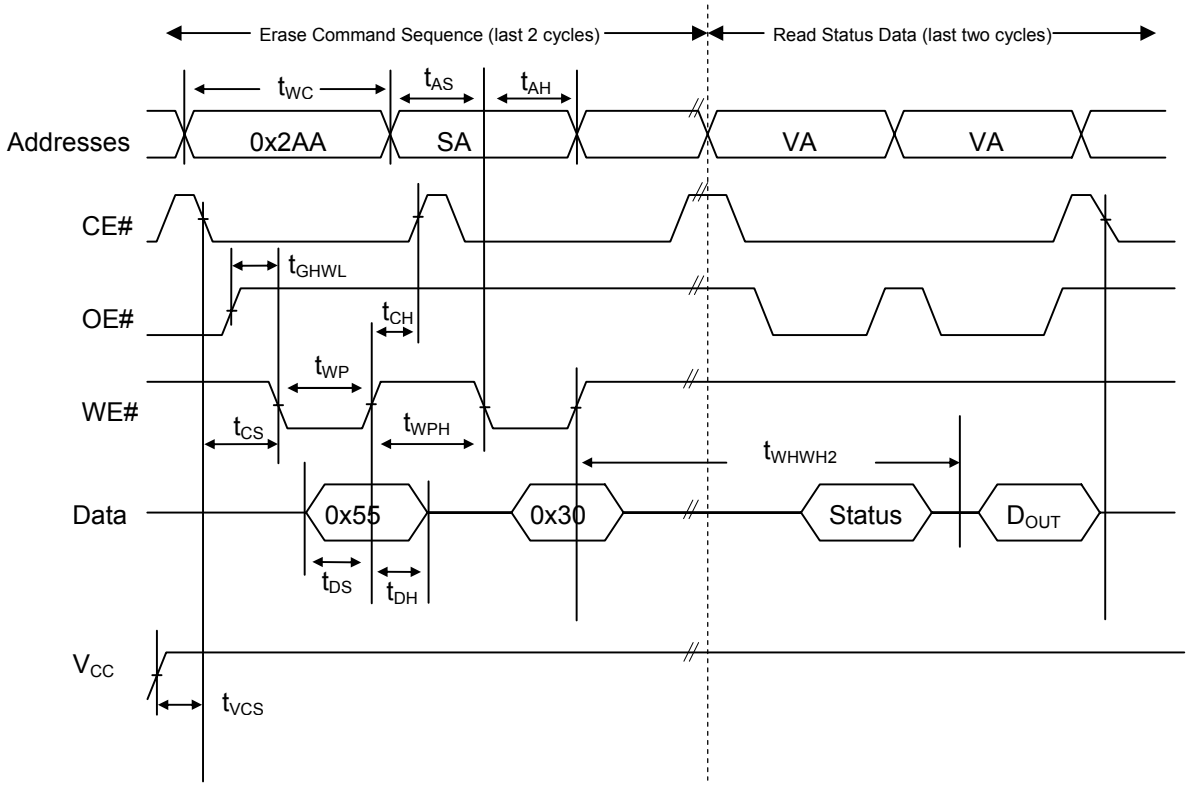
AC CHARACTERISTICS

Figure 5. AC Waveforms for Block Erase Operations Timings



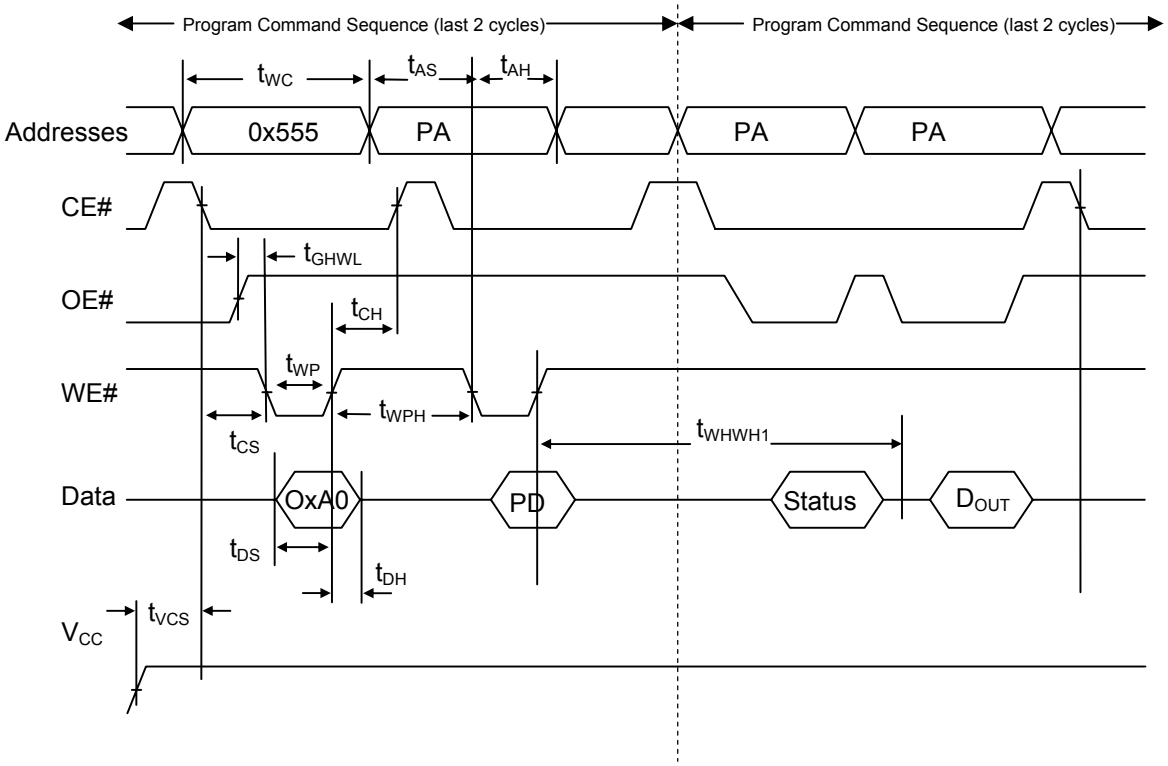
Notes:
1. BA=Block Address (for block erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

Figure 6. AC Waveforms for Sector Erase Operations Timings



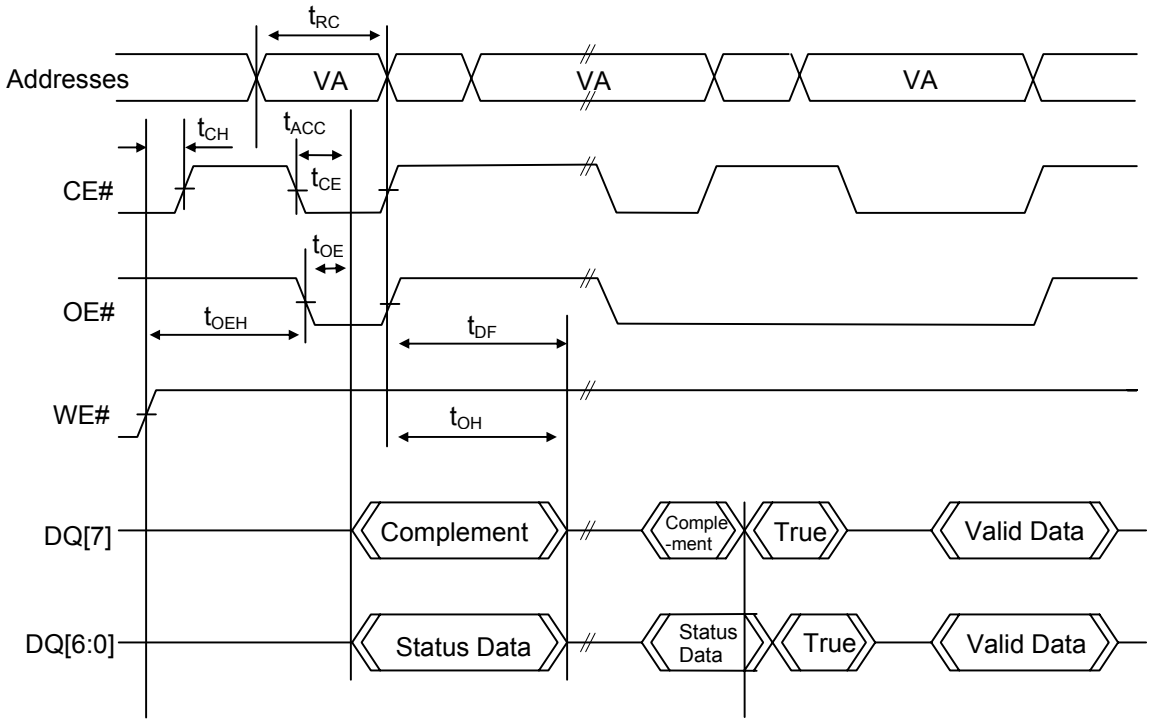
Notes:
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out} =true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

Figure 7. Program Operation Timings



Notes:
1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 8. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:
1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 9. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

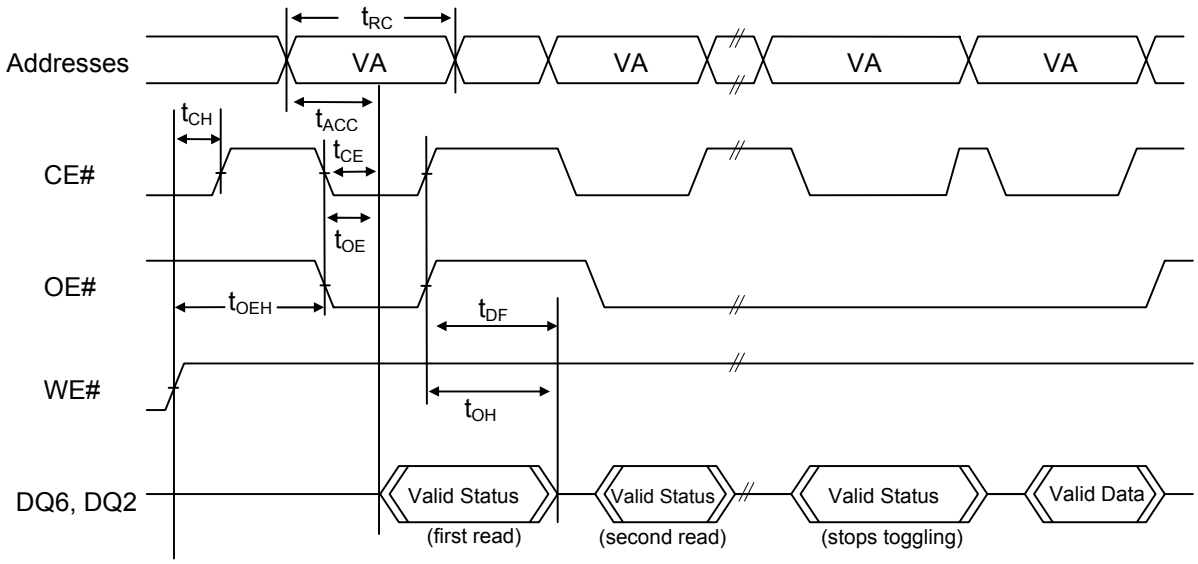
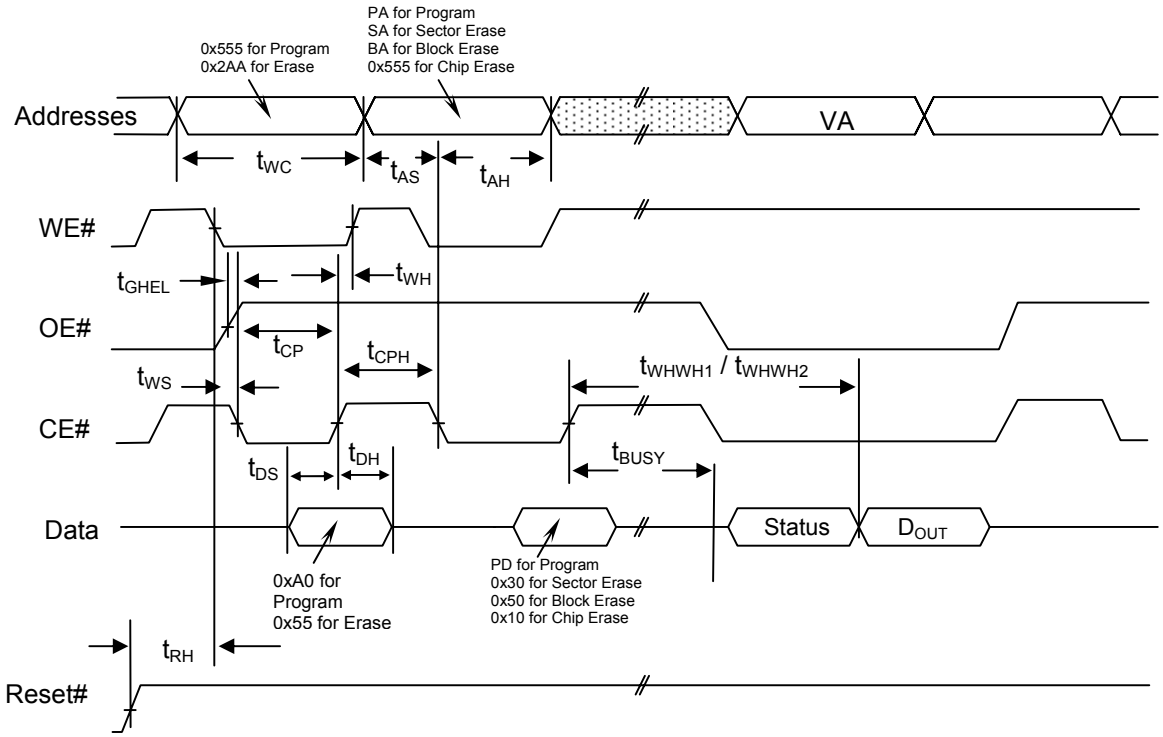


Figure 10. Alternate CE# Controlled Write Operation Timings



Notes:

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
D_{out} = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last status read cycle
Reset# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 11. DQ2 vs. DQ6

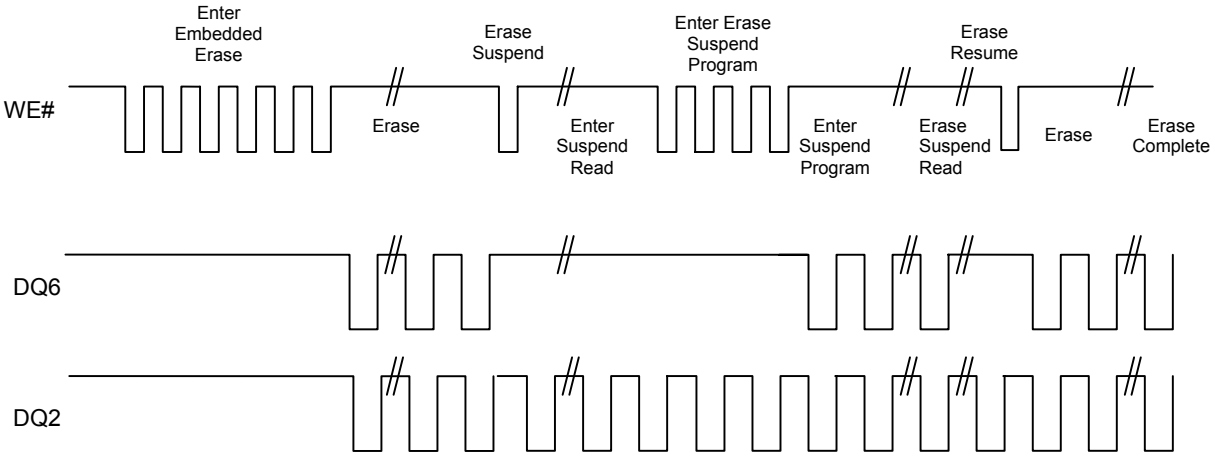
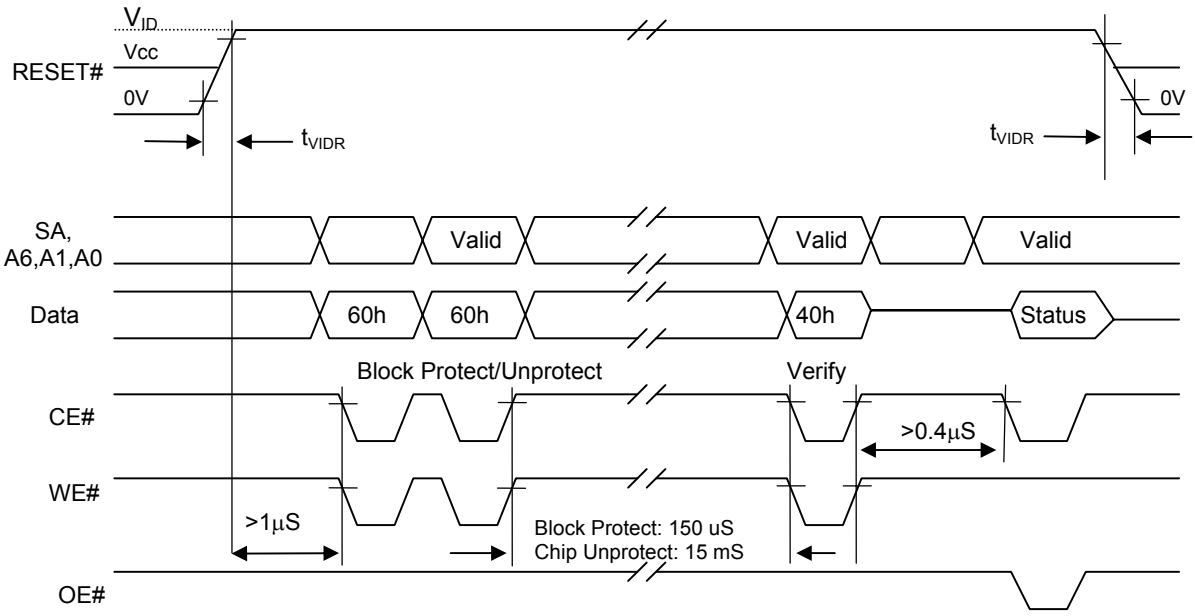


Figure 12. Block Group Protect and Chip Unprotect Timing Diagram



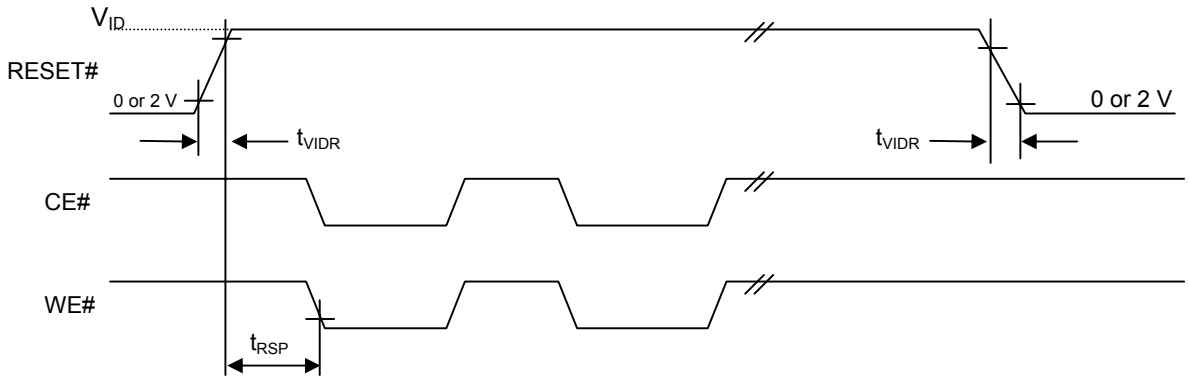
Notes:
Use standard microprocessor timings for this device for read and write cycles.
For Block Group Protect, use A6=0, A1=1, A0=0. For Chip Unprotect, use A6=1, A1=1, A0=0.

Temporary Block Unprotect

Parameter Std	Description		Speed Option		Unit
			-70	-90	
t_{VIDR}	V_{ID} Rise and Fall Time	Min	500		ns
t_{RSP}	RESET# Setup Time for Temporary Block Unprotect(Note)	Min	4		μs

Notes: t_{RSP} is Not 100% tested.

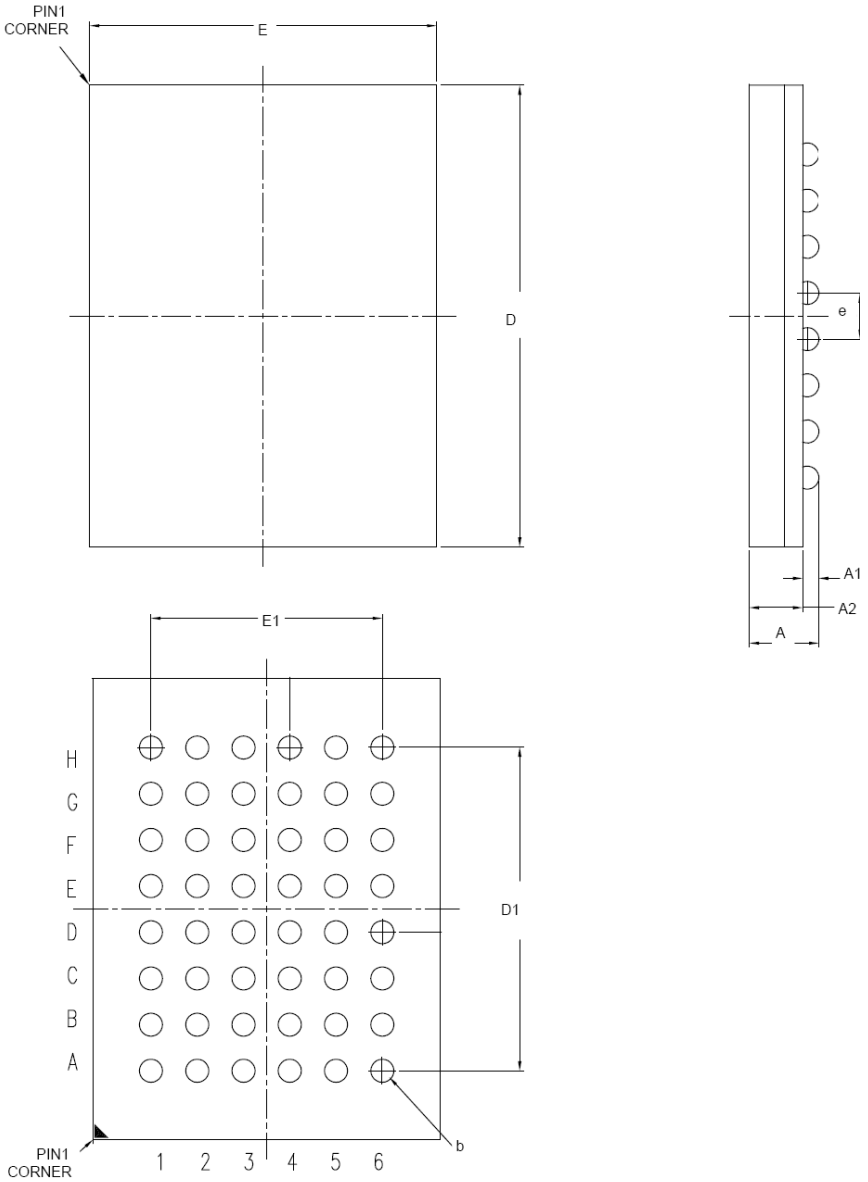
Figure 13. Temporary Block Unprotect Timing Diagram



Write Protect / Accelerated Program

Figure 14. Accelerated Program Timing Diagram

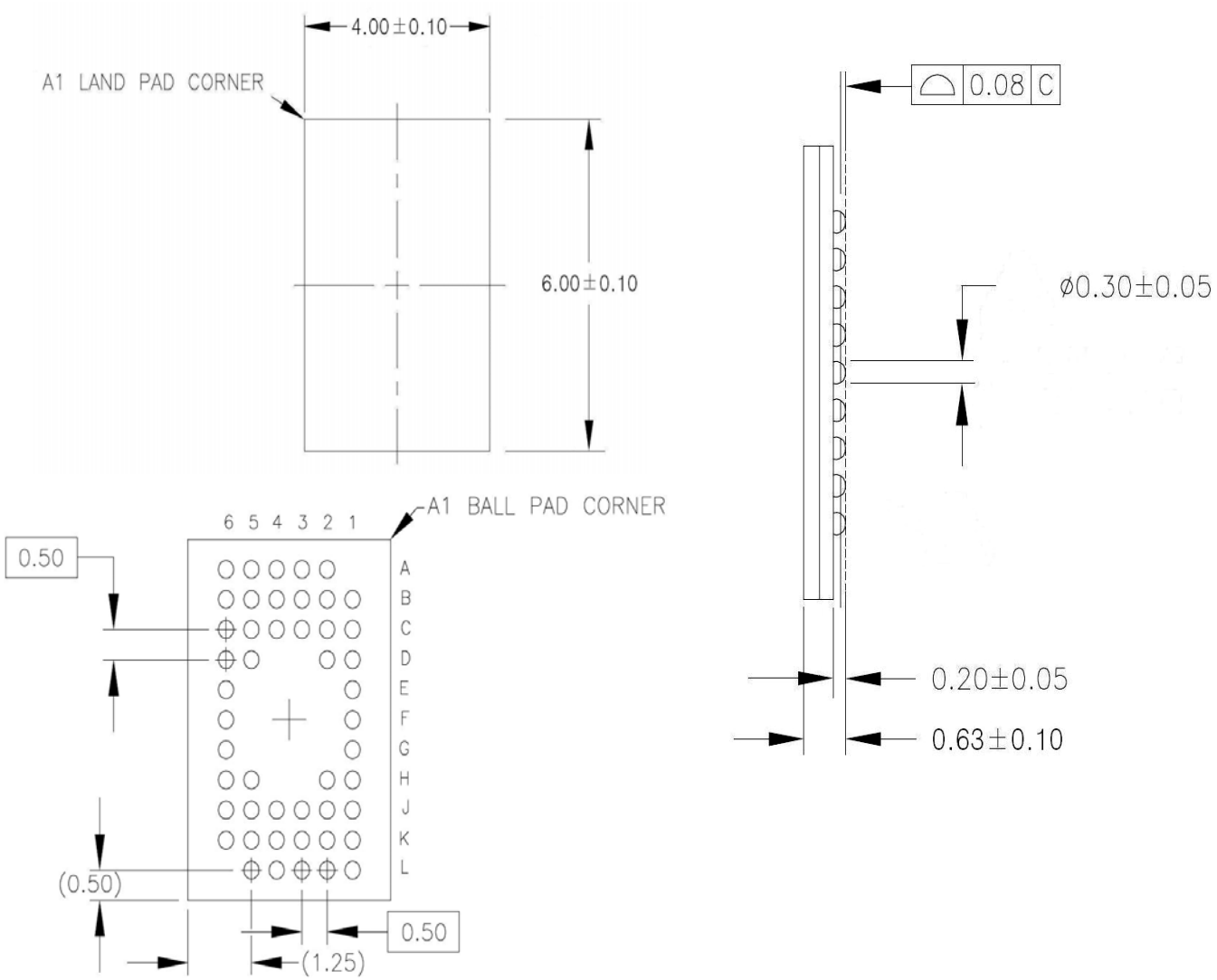
Figure 15. 48L TFBGA 6mm x 8mm package outline



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.30
A1	0.23	0.29	- - -
A2	0.84	0.91	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	- - -	5.60	- - -
E1	- - -	4.00	- - -
e	- - -	0.80	- - -
b	0.35	0.40	0.45

Note : 1. Coplanarity: 0.1 mm

Figure 16. 48L WFBGA 4mm x 6mm package outline



Note : Controlling dimensions are in millimeters (mm).

ABSOLUTE MAXIMUM RATINGS

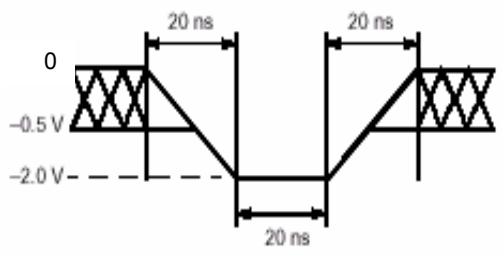
Parameter		Value	Unit
Storage Temperature		-65 to +150	℃
Plastic Packages		-65 to +125	℃
Ambient Temperature With Power Applied		-55 to +125	℃
Output Short Circuit Current[1]		200	mA
Voltage with Respect to Ground	A9, OE#, Reset# [2]	-0.5 to +11.0	V
	All other pins [3]	-0.5 to Vcc+0.5	V
	Vcc	-0.5 to + Vcc+0.5	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# pins is –0.5V. During voltage transitions, A9, OE#, RESET# pins may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 9.0V which may overshoot to 11V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

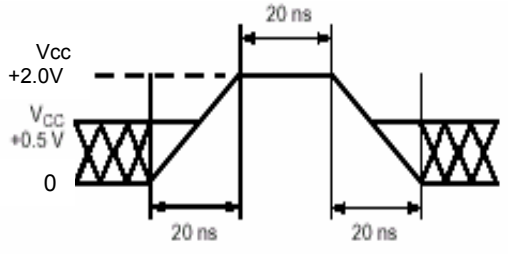
RECOMMENDED OPERATING RANGES[1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices Automotive Devices	-40 to 85 -45 to 125	℃
Operating Supply Voltage Vcc	Full Voltage Range: 1.65 to 1.95	V

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

Eon products’ New Top Marking

cFeon

cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX
Lot Number: XXXXX
Date Code: XXXXX

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

ORDERING INFORMATION

EN39SL160A H - 70 B I P

PACKAGING CONTENT
P = RoHS compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A = Automotive (-45°C to +125°C)

PACKAGE
B = 48-Ball Thin Fine Pitch Ball Grid Array (TFBGA)
0.8mm pitch, 6mm x 8mm package
N = 48-Ball Very-Very-Thin-Profile Fine Pitch
Ball Grid Array (WFBGA)
0.5mm pitch, 4mm x 6mm package

SPEED
70 = 70ns
90 = 90ns

SECTOR for WRITE PROTECT (WP#/ACC=L)
H = Highest address block protected
L = Lowest address block protected

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
39SL = 1.8V Serial 4KByte Uniform-Sector FLASH
160 = 16 Megabit (1024K x 16)
A = version identifier

The valid combinations of EN39SL160A.

Base Part Number	Sector for Write Protect (WP#/ACC=L)	Speed	Package	Temperature	Packaging Content
EN39SL160A	H	70	B, N	I	P
	L	70	B, N	I	P
EN39SL160A	H	90	B, N	A	P
	L	90	B, N	A	P

Revisions List

Revision No	Description	Date
A	Initial Release	2010/10/15
B	1. Add Speed option of 90ns. 2. Add Temperature option of Automotive (-45°C to +125°C). 3. Update ORDERING INFORMATION on page 49.	2011/02/23
C	Correct the typo for the connection diagrams of WFBGA on page 3.	2011/09/15