64Mx32 Flash Multi-Chip Package
3.0V Page Mode Flash Memory

FEATURES

- Single power supply operation
  - 3 volt read, erase, and program operations
- I/O Control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- Flexible sector architecture
  - Five hundred twelve 64 Kword (128 Kbyte) sectors
  - Two hundred fifty-six 64 Kword (128 Kbyte) sectors
  - One hundred twenty-eight 64 Kword (128 Kbyte) sectors
- Compatibility with JEDEC standard
  - Provides software compatibility for single-power supply flash, and superior inadvertent write protection
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Software features
  - Program Suspend and Resume: read other sectors before programming operation is completed
  - Erase Suspend and Resume: read/program other sectors before an erase operation is completed
  - Data# polling and toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- Hardware features
  - Advanced Sector Protection
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

PERFORMANCE CHARACTERISTICS

- High Performance
  - 100, 120 ns
  - 8-word/16-byte page read buffer
  - 25 ns page read times
  - 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
- Package option
  - 107 BGA, 14mm x 17mm
  - 1.0mm pitch

GENERAL DESCRIPTION

The W764MB2V-XSBX device is a 3.0V single power flash memory. The device utilizes four organized as 33,554,432 words or 67, 108,864 bytes. The device has 64 -bit wide data bus that can also function as an 32-bit wide data bus by using the BYTE# input. The device can be programmed either in the host system or in standard EPROM programmers.

Each device requires a single 3.0 volt power supply for both read and write functions. In addition to a V_{CC} input, an high-voltage accelerated program (WP / ACC) input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The devices are entirely command set compatible with the JEDEC single power-supply Flash standard. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) status bits or monitor the Ready / Busy# (RY / BY#) output to determine whether the operation is complete. To facilitate programming, an Unlock Bypass mode reduces command sequence over head by requiring only two write cycles to program data instead of four.

The I/O (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on all input levels (address, chip control, and DQ input levels) to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in a 1.8 V or 3 V system environment as required.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. Persistent Sector Protection provides in-system, comand-enabled protection of any combination of sectors using a single power supply at V_{CC}. Password Sector Protection prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password.

The erase Suspend / Erase Resume feature allows the host system to pause and erase operation in a given sector to read or program any other sector and then complete the erase operation. The Program Suspend / Program Resume feature enables the host system to pause the program operation in a given sector to read any other sector and then complete the program operation.

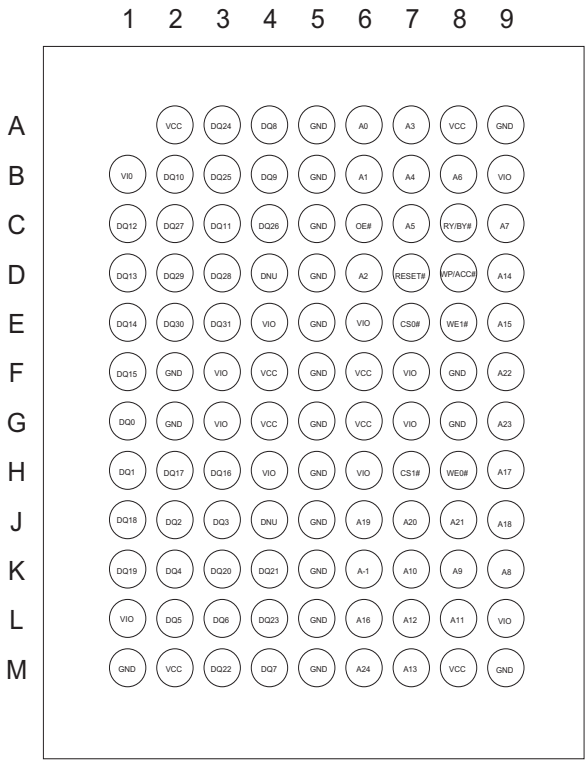
The hardware RESET# pin terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the standby mode when it detects specific voltage levels on CS# and RESET#, or when addresses have been stable for a specified period of time.

The Secured Silicon Sector provides a 128-work/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

The Write Protect (WP# / ACC) feature protects the first or last sector by asserting a logic low on the WP# pin.

FIG 1: PIN CONFIGURATION (TOP VIEW)

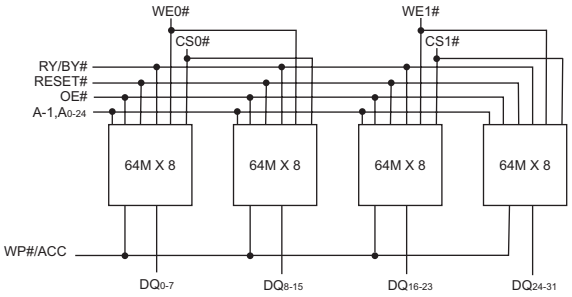


PIN DESCRIPTION

DQ_{0-63}	Data Inputs/Outputs
$A_{0-24, A-1*}$	Address Inputs
$WE\#_{0-1}$	Write Enables
$CS\#_{0-1}$	Chip Selects
OE#	Output Enable
RESET#	Hardware Reset
WP#/ACC	Hardware Write Protection/Acceleration
RY/BY#	Ready/Busy Output
V_{CC}	Power Supply
V_{IO}	I/O Power Supply
GND	Ground
DNU	Do Not Use

* A-1 is the least significant address.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Storage Temperature Range	-55 to +125	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:

1. Minimum DC voltage on input or input or I/Os is -0.5V. During voltage transitions, inputs or I/Os may overshoot V_{SS} to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/Os us VCC + 0.5V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0V for periods up to 20ns
2. Minimum DC input voltage on pins A9, OE#, and ACC is 0.5V. During voltage transitions, A9, OE#, and ACC may overshoot V_{SS} to -2.0V for periods of up to 20ns. Maximum DC input voltage on pin A9, OE#, and ACC is +12.5V which may overshoot to +14.0V for periods up to 20ns
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
4. Stresses above those listed under Absolute Maxium Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of the data sheet is not implied. Exposure of the device to absolute maxium rating conditons for extended peroids may affect device reliability

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE

T_A = +25°C, F = 1.0MHz

Parameter	Symbol	Max	Unit
WE1-4# capacitance	C_{WE}	TBD	pF
CS1-4# capacitance	C_{CS}	TBD	pF
Data I/O capacitance	$C_{I/O}$	TBD	pF
Address input capacitance	C_{AD}	TBD	pF
RESET# capacitance	C_{RS}	TBD	pF
RY/BY# capacitance	C_{RB}	TBD	pF
OE# capacitance	C_{OE}	TBD	pF

This parameter is guaranteed by design but not tested.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS – CMOS COMPATIBLE

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Load Current (1)	I_{LI}	V_{IN} = V_{SS} to V_{CC}, #V_{CC} = $V_{CC(MAX)}$			WP/ACC: ±2.0	µA
					Others: ±1.0	
A9 Input Load Current	I_{LIT}	V_{CC} = to $V_{CC(MAX)}$; A9 = 12.5V			35	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, # V_{CC} = $V_{CC(MAX)}$			±1.0	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CE# = V_{IL}#, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$; # f = 1 MHz, Byte Mode		24	80	mA
		CE# = V_{IL}#, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$; # f = 5MHz, Word Mode		120	200	mA
V_{CC} Intra-Page Read Current (1)	I_{CC2}	CE# = V_{IL}#, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$; f = 10MHz		1	10	mA
V_{CC} Active Erase/Program Current (2,3)	I_{CC3}	CE# = V_{IL}#, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$		200	320	mA
V_{CC} Standby Current	I_{CC4}	V_{CC} = $V_{CC(MAX)}$; V_{IO} = V_{CC}; OE# = V_{IH}; # V_{IL} = V_{SS} + 0.3V/-0.1V; # CE#, RESET# = V_{SS} ± 0.3V		4	20	µA
V_{CC} Reset Current	I_{CC5}	V_{CC} = $V_{CC(MAX)}$; V_{IO} = V_{SS} + 0.3V/-0.1V; RESET# = V_{SS} ± 0.3V		4	20	µA
Automatic Sleep Mode (4)	I_{CC6}	V_{CC} = $V_{CC(MAX)}$; V_{IO} = V_{CC}; V_{IH} = V_{CC} ± 0.3V; #V_{IL} = V_{SS} + 0.3V/-0.1V; WP#/A_{CC} = V_{IH}		4	20	µA
A_{CC} Accelerated Program Current	I_{ACC}	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = $V_{CC(MAX)}$, #WP#/A_{CC} = V_{IH}	WP#/A_{CC} pin	40	80	mA
			V_{CC} pin	200	320	
Input Low Voltage (5)	V_{IL}		-0.1		0.3 x V_{IO}	V
Input High Voltage (5)	V_{IH}		0.7 x V_{IO}		V_{IO} + 0.3	V
Voltage for ACC Erase/Program Acceleration	V_{HH}	V_{CC} = 2.7 - 3.6V	11.5		12.5	V
Voltage for Autoselect and Temporary Sector Unprotect	V_{ID}	V_{CC} = 2.7 - 3.6V	11.5		12.5	V
Output Low Voltage (5)	V_{OL}	I_{OL} = -100 µA			0.15 x V_{IO}	V
Output High Voltage (5)	V_{OH}	I_{OH} = -100 µA	0.85 x V_{IO}			V
Low V_{CC} Lock-Out Voltage	V_{LKO}		2.3		2.5	V

NOTES:
1. The I_{CC} current is typically less than 2 mA/MHz, with OE# at V_{IH}
2. I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.
3. Not 100% tested.
4. Automatic sleep mode enables the lower power mode when addresses remain stable for t_{ACC} + 30ns.
5. V_{IO} = 1.65-1.95V or 2.7-3.6V.
6. V_{CC} = 3 V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at 3V.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-100 Min	-100 Max	-120 Min	-120 Max	Unit
Write Cycle Time (3)	t_{AVAV}	t_{WC}	100		120		ns
Chip Select Setup Time (3)	t_{ELWL}	t_{CS}	0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	35		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		ns
Write Enable Pulse Width High (3)	t_{WHWL}	t_{WPH}	30		30		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			500		500	µs
Sector Erase (2)	t_{WHWH2}			3.5		5	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		ns
VCC Setup Time	t_{VCS}		50		50		µs
Address Setup Time to OE# low during toggle bit polling		t_{ASO}	15		15		ns
Write Recovery Time from RY/BY# (3)		t_{RB}	0		0		ns
Program/Erase Valid to RY/BY#		t_{BUSY}	90		90		ns

NOTES:
1. Typical value for t_{WHWH1} is 60 µs.
2. Typical value for t_{WHWH2} is 0.5 sec.
3. Guaranteed by design, but not tested.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter		Symbol		-100 Min	-100 Max	-120 Min	-120 Max	Unit
Read Cycle Time (1)		t_{AVAV}	t_{RC}	100		120		ns
Address Access Time		t_{AVQV}	t_{ACC}		100		120	ns
Chip Select Access Time		t_{ELQV}	t_{CE}		100		120	ns
Page Access Time			t_{PACC}		25		30	ns
Output Enable to Output Valid		t_{GLQV}	t_{OE}		25		35	ns
Chip Select High to Output High Z		t_{EHQZ}	t_{DF}		20		20	ns
Output Enable High to Output High Z		t_{GHQZ}	t_{DF}		20		20	ns
Output Hold from Addresses, CS# or OE# Change, Whichever occurs first		t_{AXQX}	t_{OH}	0		0		ns
Output Enable Hold Time (1)	Read		t_{OEH}	0		0		ns
	Toggle and Data# Polling			10		10		ns

1. Guaranteed by design, not tested.

FIGURE 2: AC WAVEFORMS FOR READ OPERATIONS

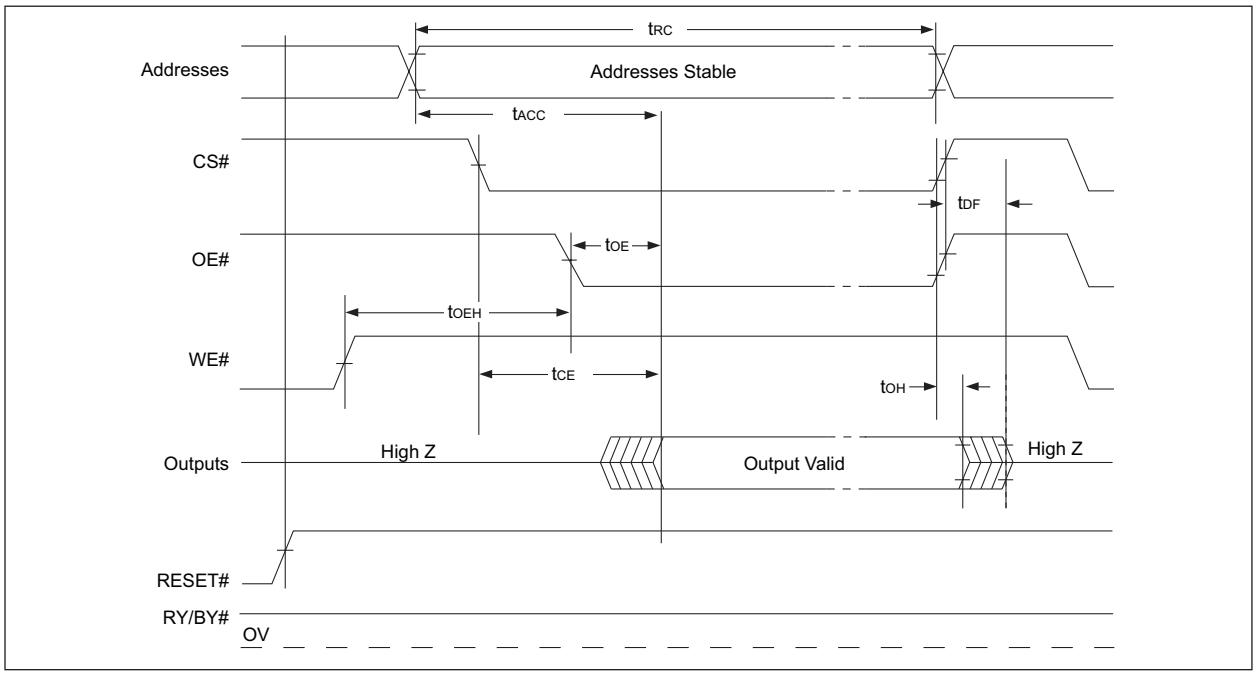
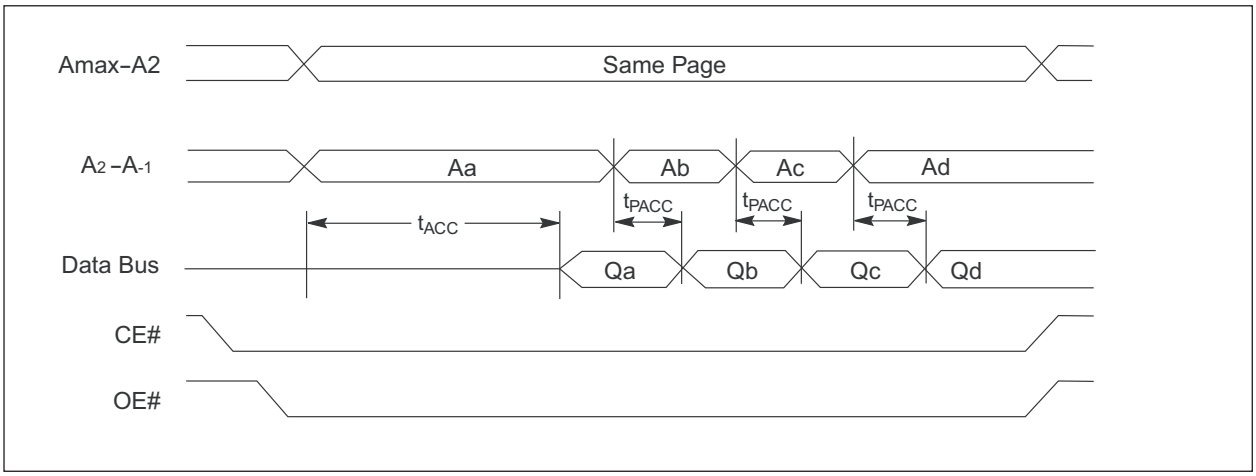


FIGURE 3: PAGE READ TIMING



AC CHARACTERISTICS – HARDWARE RESET (RESET#)

Parameter	Symbol	Min	Max	Unit
RESET# Pin Low (During Embedded Algorithms) to Read Mode (1)	t_{ready}		20	µs
RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (1)	t_{ready}		500	ns
RESET# Pulse Width	t_{RP}	500		ns
RESET# High Time Before Read (1)	t_{RH}	50		ns
RESET# Low to Standby Mode (1)	t_{RPD}	20		µs
RY/BY# Recovery Time	t_{RB}	0		ns

NOTE: 1. Not tested.

FIGURE 4: RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

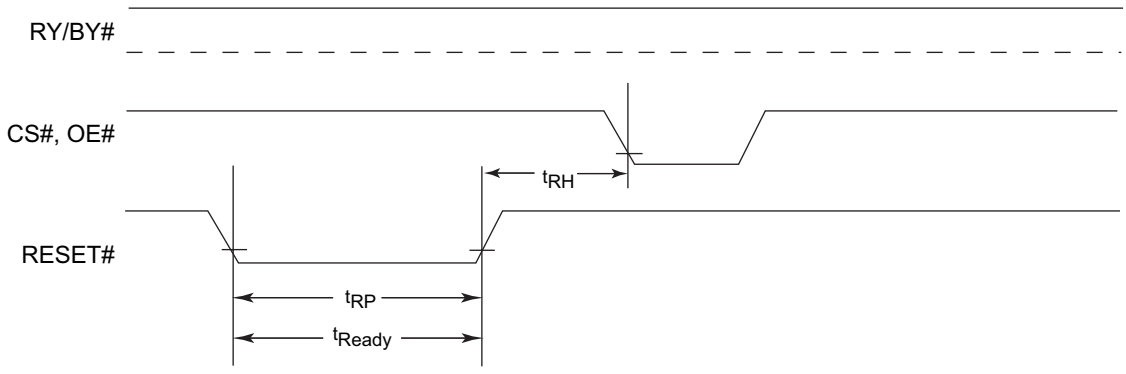


FIGURE 5: RESET TIMINGS DURING EMBEDDED ALGORITHMS

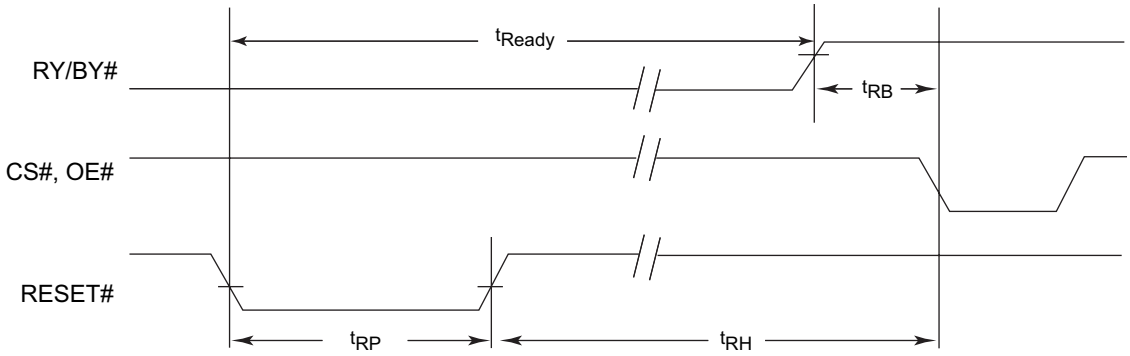
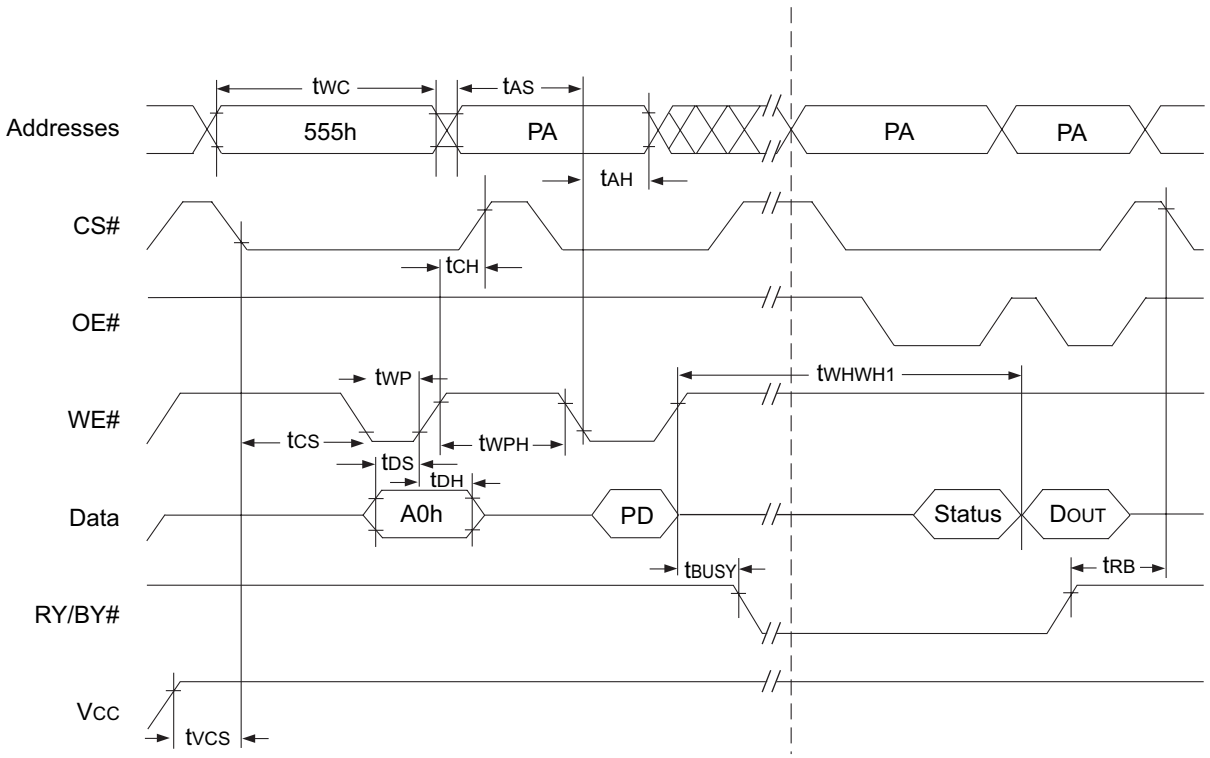


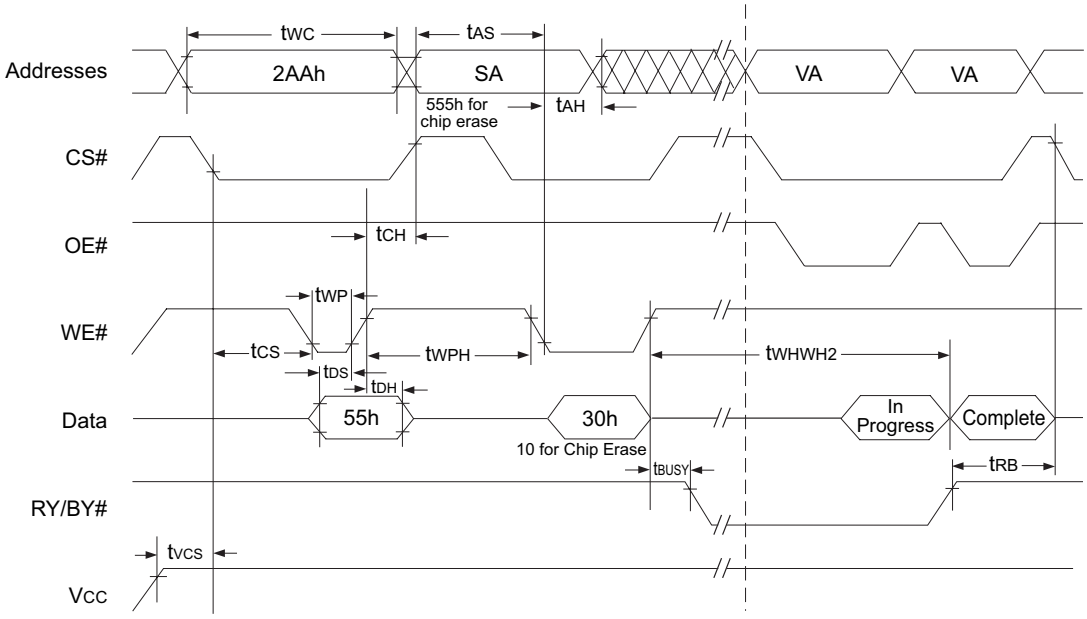
FIGURE 6: PROGRAM OPERATIONS



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. DOUT is the output of the data written to the device.
4. Figure indicates last two bus cycles of four bus cycle sequence.

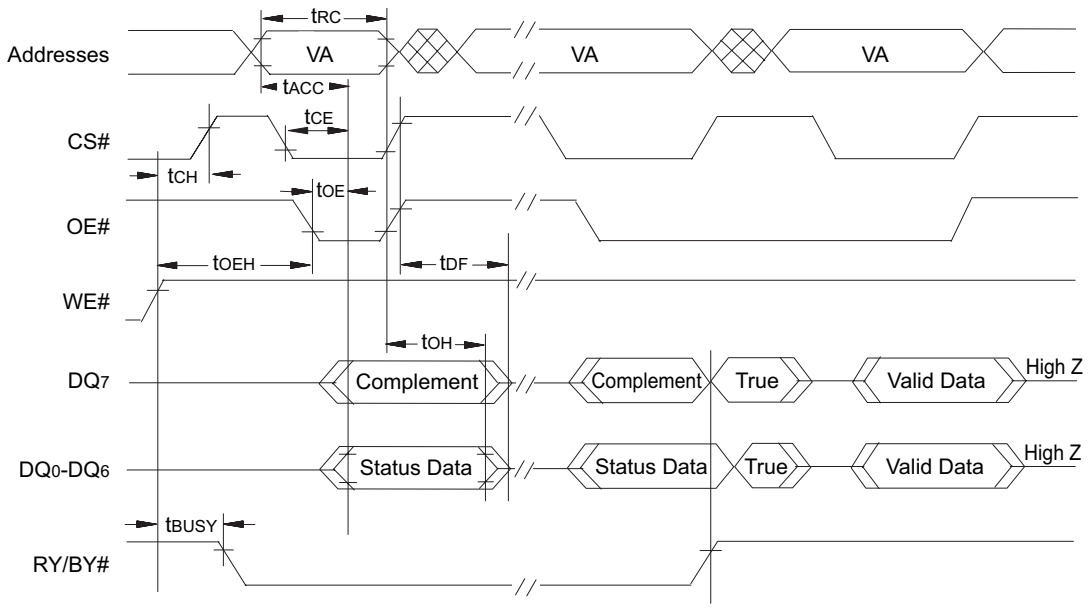
FIGURE 7: ACCELERATED PROGRAM TIMING DIAGRAM

FIGURE 8: CHIP/SECTOR ERASE OPERATION TIMINGS



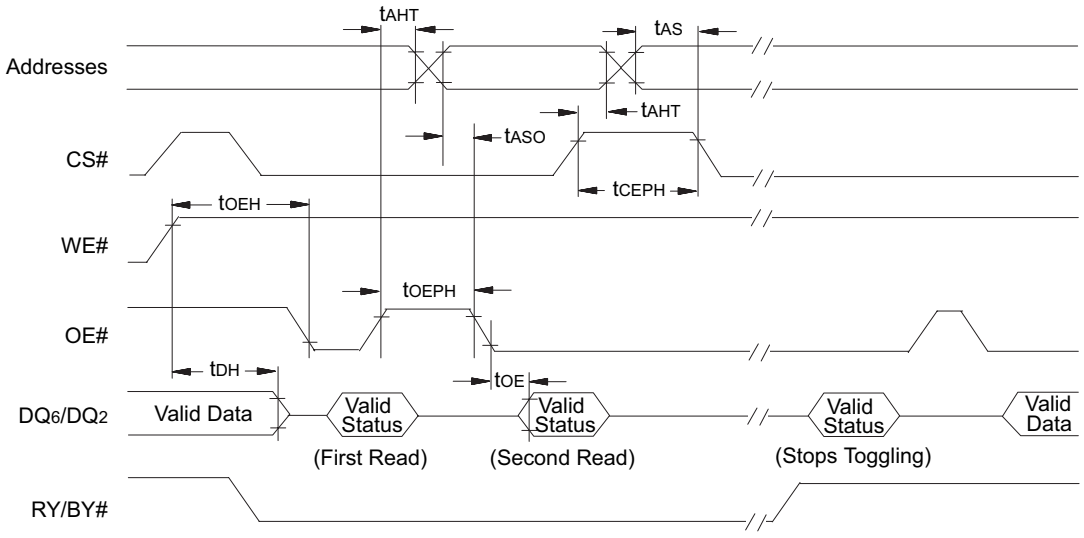
NOTES: 1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data

FIGURE 9: DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



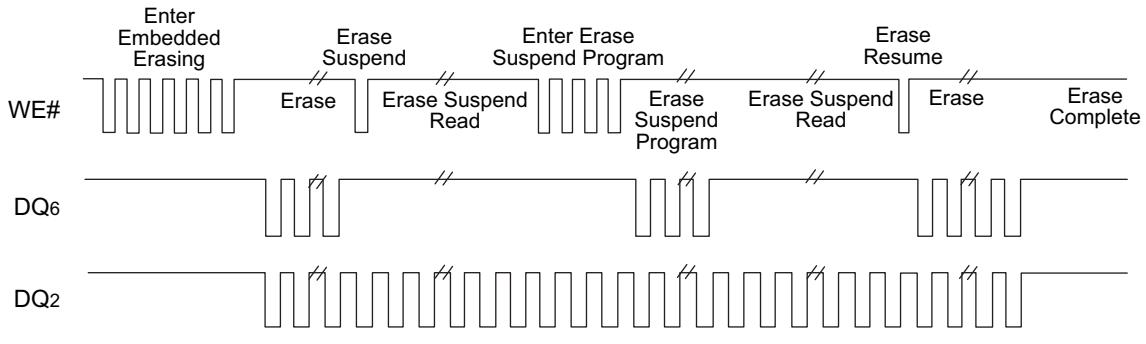
NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

FIGURE 10: TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



NOTE: VA = Valid address, not required for DQ_6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

FIGURE 11: DQ2 Vs. DQ6



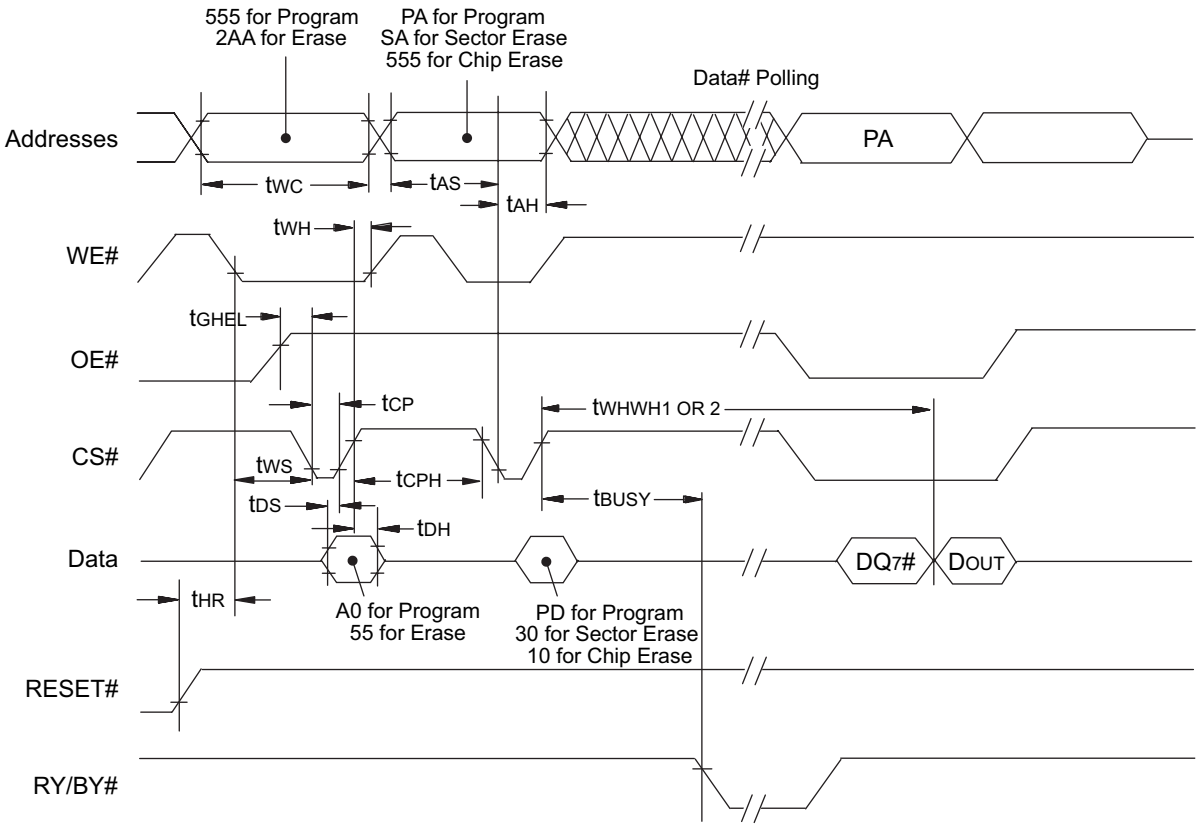
NOTE: DQ_2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CS# to toggle DQ_2 and DQ_6.

AC CHARACTERISTICS – ALTERNATE CS# CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter				Speed Options		
JEDEC	Std	Description		100	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (1)	Min	100	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	0	ns
t_{WLEL}	T_{WS}	WE# Setup Time	Min	0	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	0	ns
t_{ELEH}	t_{CP}	CS# Pulse Width	Min	35	35	ns
t_{EHEL}	t_{CPH}	CS# Pulse Width High	Min	30	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	60	6	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation	Typ	54	54	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.5	05	sec

NOTE: 1. Not tested.

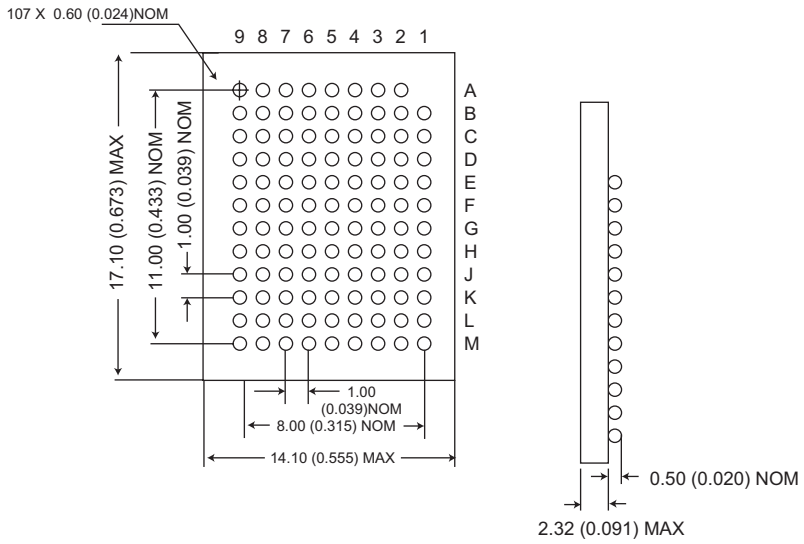
FIGURE 12: ALTERNATE CS# CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS



NOTES:
1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. DQ7 is the complement of the data written to the device. D_{OUT} is the data written to the device.

PACKAGE: 107 PBGA (PLASTIC BALL GRID ARRAY)

BOTTOM VIEW



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W 7 64M32 V XXX SB X

White Eletronic Designs Corp.

Flash:

Organization, 64M x 32:

3.3V Power Supply:

Access Time (ns):
- 100 = 100ns
- 120 = 120ns
- ES = Non-qualified product [1]

Package Type:
- SB = 107 PBGA, 14mm x 17mm

Devise Grade:

M = Military	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

Blank = No temperature range specified for non-qualified product

NOTE 1: W764M32V-ESSB is only available product until completion of qualification.

Document Title

64Mx32 Flash 3.3V

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	November 2005	Advanced
Rev 1	Changes (All Pages) 1.1 Add AC + DC characteristics and timing diagrams 1.2 Update package dimensions 1.3 Add preliminary pinout	February 2006	Advanced
Rev 2	Changes (Pg. 1, 3, 16) 2.1 Correct typographical error in pinout on page 3, ball 'B4' is DQ9	March 2006	Advanced