NEC

MOS INTEGRATED CIRCUIT
μPD78P054Y

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78P054Y is a product in which the on-chip mask ROM of the μPD78054Y is replaced by one-time PROM which can be written to once only, or by EPROM which can be programmed, erased, and reprogrammed.

As program write by user is possible, the μPD78P054Y is best suited for evaluation, short-run and multiple-device production, and early rise upon system development.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μPD78054Y Series User's Manual (Preliminary): In preparation

FEATURES

- Pin compatible with mask ROM products (except the V_{PP} pin)
- Internal PROM : 32K bytes*
- Internal high-speed RAM : 1024 bytes*
- Buffer RAM : 32 bytes
- Operable in the same range of supply voltage as mask ROM products (2.0 to 6.0 V) ★

* Internal PROM and internal high-speed RAM capacities can be changed by memory size switching register.

Differs from Mask ROM Products in Following Points

- The same memory mapping as mask ROM products is enabled by setting the memory size switching register.
- Pins P60 to P63 do not incorporate a pull-up resistor.

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM
μPD78P054YGC-3B9	80-pin plastic QFP (□14 mm)	One-Time PROM
μPD78P054YGK-BE9	80-pin plastic TQFP (□12 mm)	One-Time PROM
μPD78P054YKK-T	80-pin ceramic WQFN (LCC with window)(□14 mm)	EPROM

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

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The mark ★ shows major revised points.

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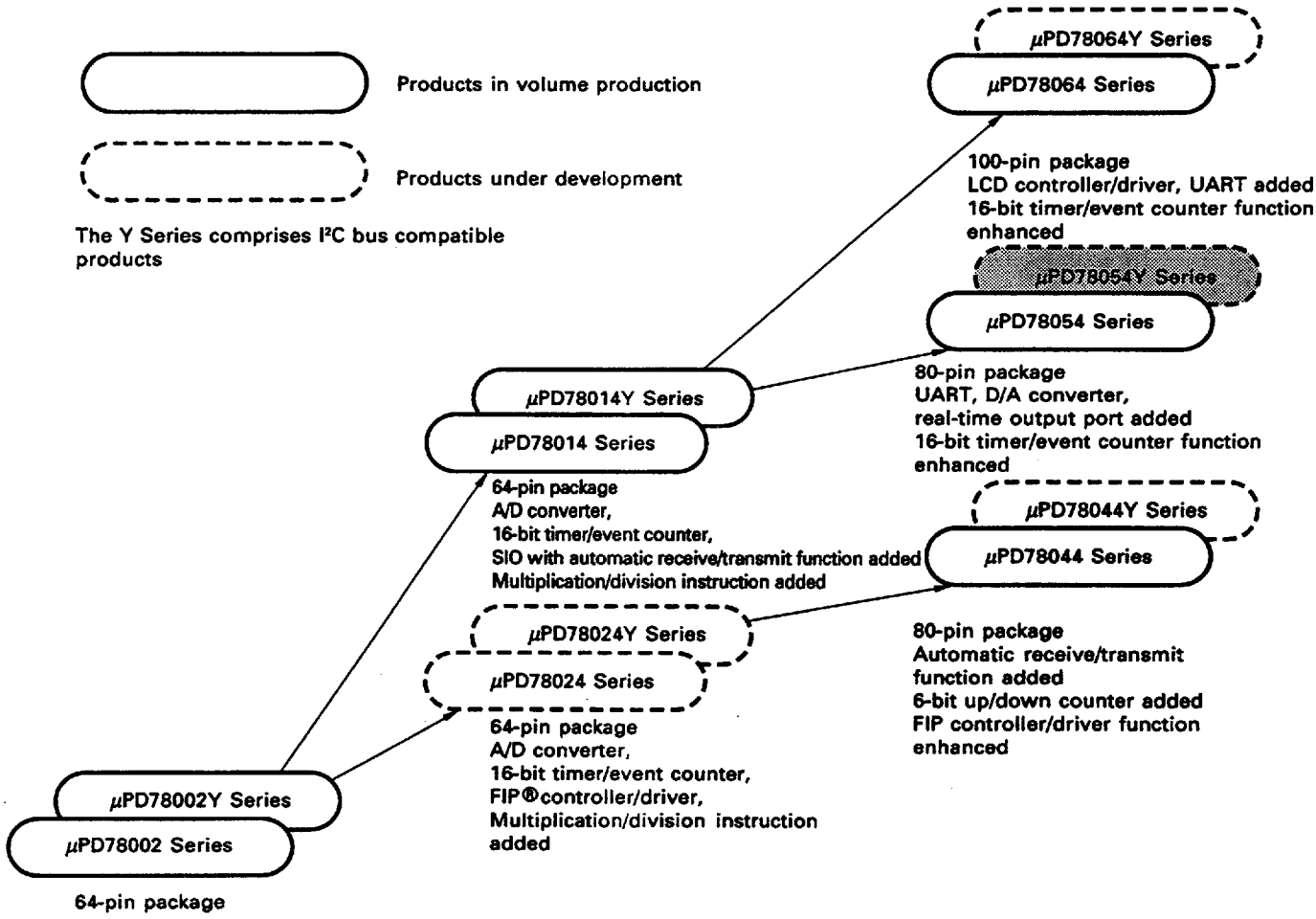
QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/O SERIES DEVELOPMENT



FUNCTION DESCRIPTION

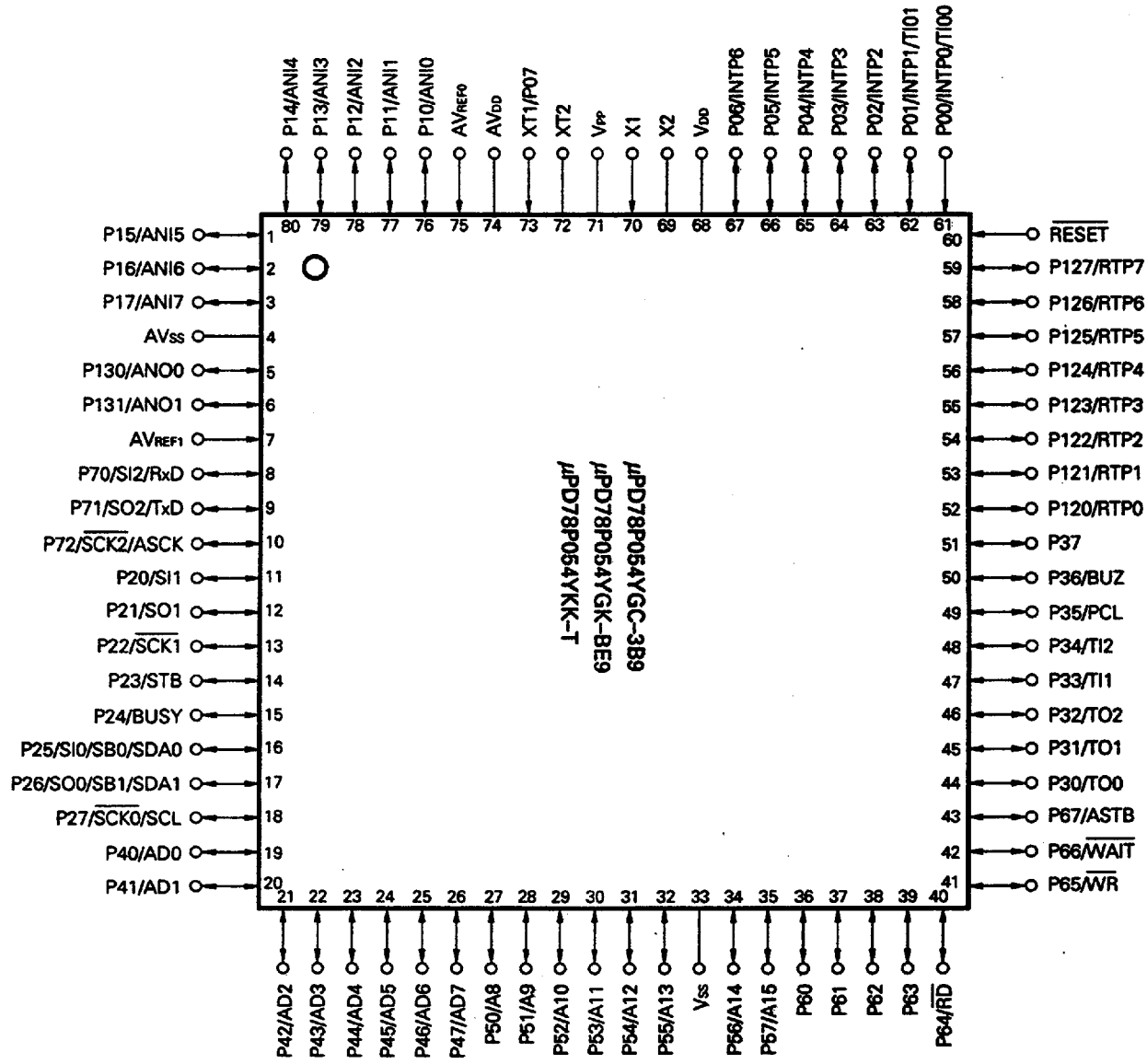
Item		Function
Internal memory		• PROM : 32K bytes* • RAM Internal high-speed RAM : 1024 bytes* Buffer RAM : 32 bytes
Memory space		64K bytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycles		Instruction execution time variable function is built in.
	When main system clock is selected	0.4μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (when operating at 5.0 MHz)
	When subsystem clock is selected	122 μs (when operating at 32.768 kHz)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports		Total : 69 • CMOS input : 2 • CMOS input/output : 63 • N-ch open-drain input/output : 4
A/D converter		• 8-bit resolution × 8 ch
D/A converter		• 8-bit resolution × 2 ch
Serial interface		• 3-wire/2-wire/I²C bus mode selectable : 1 ch • 3-wire mode (with on-chip max. 32-byte auto transmitting/receiving function) : 1 ch • 3-wire/UART mode selectable : 1 ch
Timer		• 16-bit timer/event counter : 1 ch • 8-bit timer/event counter : 2 ch • Watch timer : 1 ch • Watchdog timer : 1 ch
Timer output		3 pins (14-bit PWM output enable: 1 pin)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (when operating at main system clock 5.0 MHz) 32.768 kHz (when operating at subsystem clock 32.768 kHz)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz (when operating at main system clock 5.0 MHz)
Vectored interrupt	Maskable interrupt	Internal : 13, External : 7
	Non-maskable interrupt	Internal : 1
	Software interrupt	Internal : 1
Test input		Internal : 1, External : 1
Operating voltage range		V_{DD} = 2.0 to 6.0 V
Package		• 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (□12 mm) • 80-pin ceramic WQFN (LCC with window) (□14 mm)

* Internal PROM/internal high-speed RAM capacity can be changed by the memory size switching register.

PIN CONFIGURATION (Top View)

(1) Normal operating mode

80-pin plastic QFP (□14 mm)
80-pin plastic TQFP (□12 mm)
80-pin ceramic WQFN (LCC with window)(□14 mm)

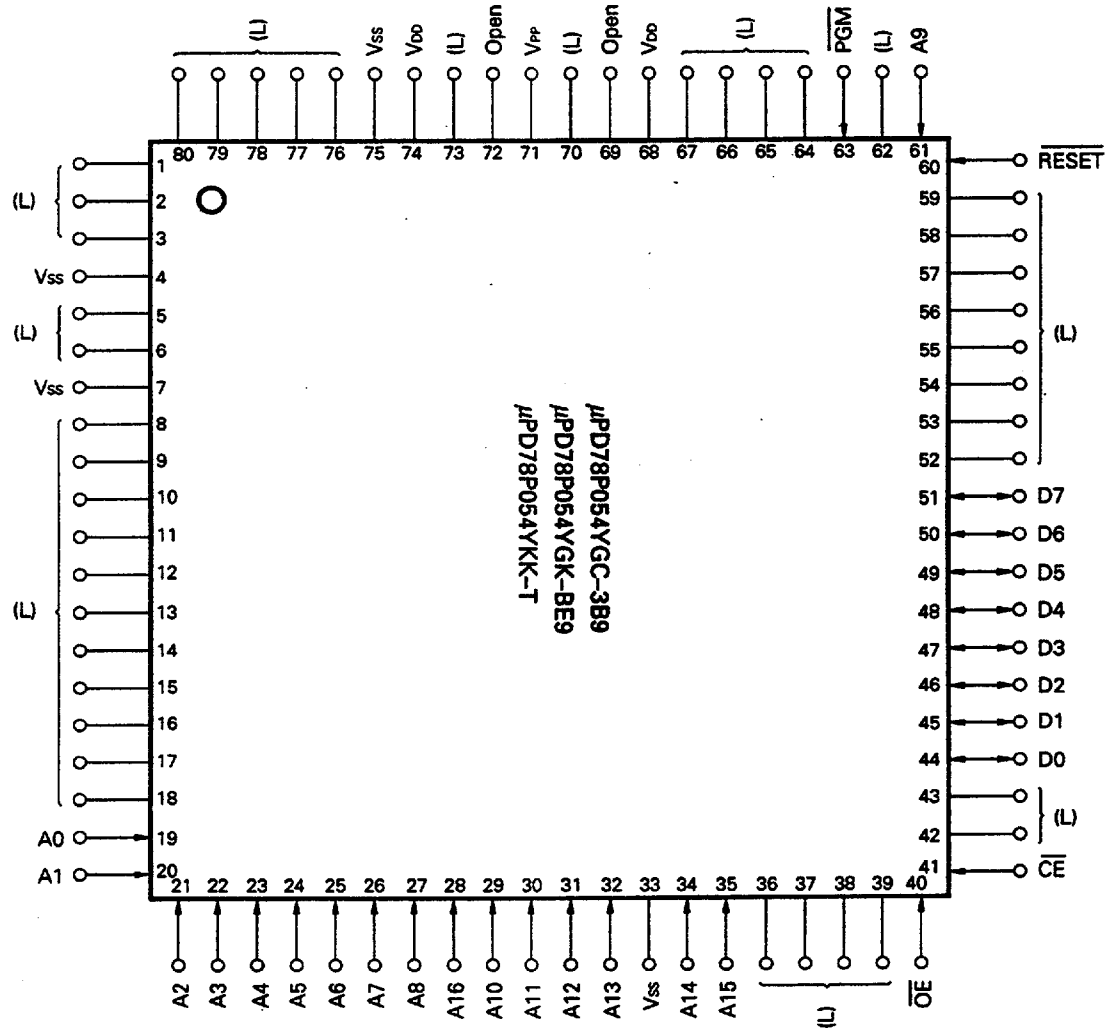


Note
1. **Connect V_{PP} pin to V_{SS}.**
2. **Connect AV_{DD} pin to V_{DD}.**
3. **Connect AV_{SS} pin to V_{SS}.**

P00 to P07	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
P70 to P72	:	Port 7
P120 to P127	:	Port 12
P130, P131	:	Port 13
RTP0 to RTP7	:	Real-Time Output Port
INTP0 to INTP6	:	Interrupt From Peripherals
TI00, TI01	:	Timer Input
TI1,TI2	:	Timer Input
TO0 to TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0 to SI2	:	Serial Input
SO0 to SO2	:	Serial Output
$\overline{SCK0}$ to $\overline{SCK2}$	:	Serial Clock
SCL	:	Serial Clock
SDA0, SDA1	:	Serial Data
RxD	:	Receive Data
TxD	:	Transmit Data
ASCK	:	Asynchronous Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
AD0 to AD7	:	Address/ Data Bus
A8 to A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
$AV_{REF0,1}$	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground

(2) PROM programming mode

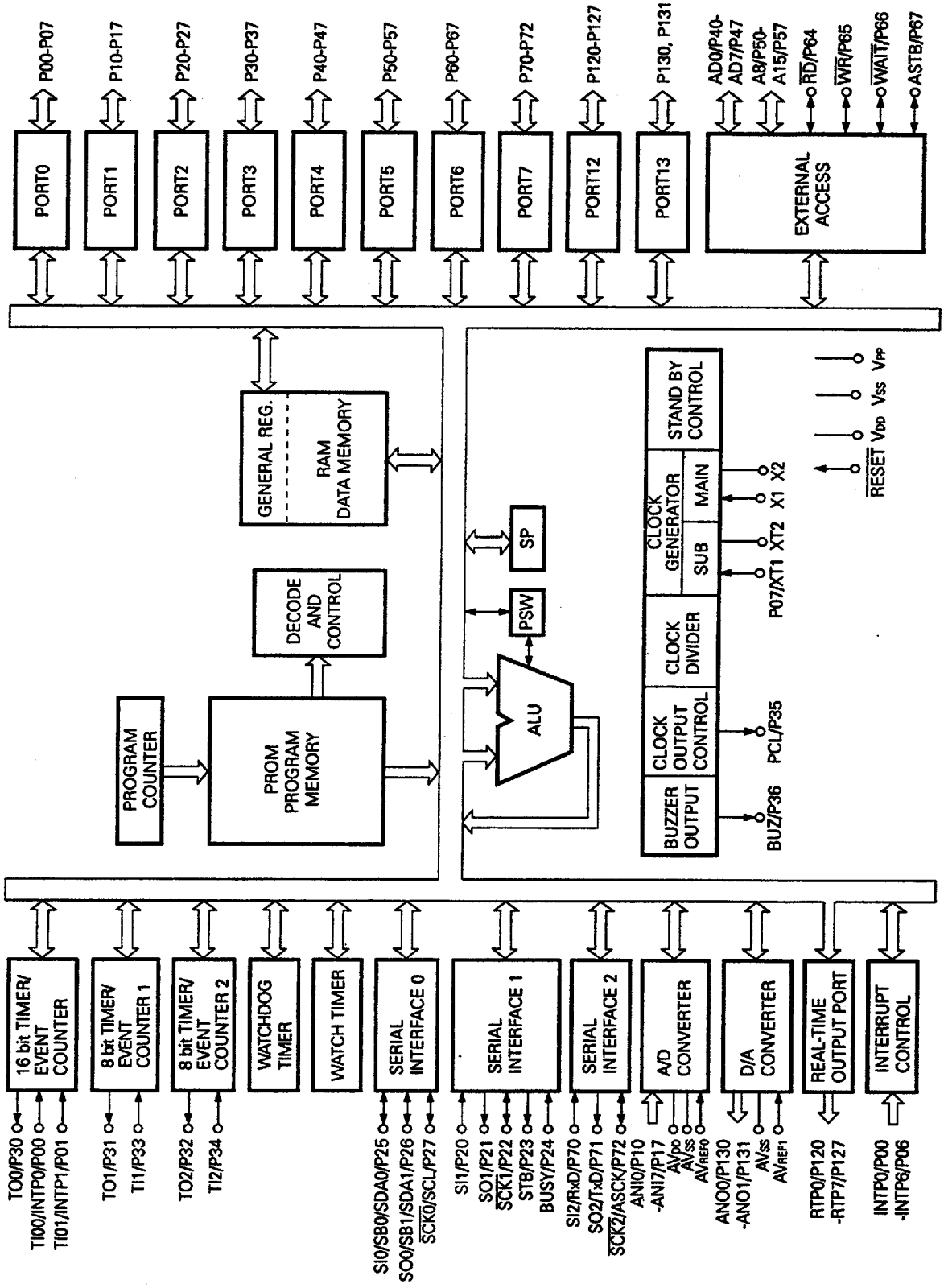
80-pin plastic QFP (□14 mm), 80-pin plastic TQFP (□12 mm)
80-pin ceramic WQFN (LCC with window)(□14 mm)



Note 1. (L) : Individually connect to Vss via a pull-down resistor.
2. Vss : Connect to GND.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open : No connection

A0 to A16	: Address Bus	$\overline{\text{RESET}}$	: Reset
D0 to D7	: Data Bus	V_{DD}	: Power Supply
$\overline{\text{CE}}$	: Chip Enable	V_{PP}	: Programming Power Supply
$\overline{\text{OE}}$	: Output Enable	Vss	: Ground
$\overline{\text{PGM}}$	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78P054Y AND MASK ROM PRODUCTS

The μPD78P054Y is a single-chip microcomputer with an on-chip one-time writable PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions except for PROM specification, and mask option of P60 to P63 pins, to the same as those of mask ROM products by setting the memory size switching register.

Differences between the μPD78P054Y and mask ROM products are shown in Table 1-1.

Table 1-1 Differences between μPD78P054Y and Mask ROM Products

Item	μPD78P054Y	Mask ROM Products
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask option of P60 to P63 pins	Pull-up resistor is not incorporated	Pull-up resistor can be incorporated by mask option

Note For the μPD78P054Y, the internal PROM/internal high-speed RAM capacities can be set by the memory size switching register.
The internal PROM becomes to 32K bytes and the internal high-speed RAM becomes 1K bytes by the $\overline{\text{RESET}}$ input.

2. PIN FUNCTION TABLE

2.1 PINS IN NORMAL OPERATING MODE

(1) Port pins (1/2)

Pin Name	Input/Output	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 8-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07*1	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software. *2		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{SCK0}$/SCL
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

* 1. When P07/XT1 pins are used as the input ports, set the processor clock control register bit 6 (FRC) to 1 (Be sure not to use the feedback resistor of the subsystem clock oscillation circuit.)
2. When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, a pull-up resistor becomes automatically unused.

(1) Port pins (2/2)

Pin Name	Input/Output	Function		After Reset	Dual-Function Pin
P40 to P47	Input/output	Port 4 8-bit input/output port Input/output is specifiable as 8-bit unit. When used as the input port, it is possible to connect a pull-up resistor by software. Test flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	Input/output	Port 5 8-bit input/output port It is possible to directly drive LED. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port Input/output is specifiable bit-wise.	N-ch open-drain input/output port. It is possible to directly drive LED.	Input	—
P61					
P62					
P63					
P64			When used as the input port, it is possible to connect a pull-up resistor by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P127	Input/output	Port 12 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	ANO0, ANO1

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	After Reset	Dual-Function Pin
INTP0	Input	External interruption inputs, with specifiable valid edges (rising edge, falling edge, and both rising and falling edges) .	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial data input of the serial interface	Input	P25/SB0/SDA0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial data output of the serial interface	Input	P26/SB1/SDA1
SO1				P21
SO2				P71/TxD
SB0	Input/output	Serial data input/output of the serial interface	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input/output	Serial clock input/output of the serial interface	Input	P27/SCL
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
STB	Output	Automatic transmitting/receiving strobe output of the serial interface	Input	P23
BUSY	Input	Automatic transmitting/receiving busy input of the serial interface	Input	P24
RxD	Input	Serial data input for asynchronous serial interface	Input	P70/SI2
TxD	Output	Serial data output for asynchronous serial interface	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Dual-Function Pin
TO0	Output	16-bit timer output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port which outputs data in synchronization with trigger.	Input	P120 to P127
AD0 to AD7	Input/output	Low-order address/data bus when expanding memory to the outside.	Input	P40 to P47
A8 to A15	Output	High-order address bus when expanding memory to the outside.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for the external memory read operation	Input	P64
$\overline{WR}$		Strobe signal output for the external memory write operation	Input	P65
$\overline{WAIT}$	Input	Wait insertion when accessing external memory	Input	P66
ASTB	Output	Strobe output to externally latches address information which is output to ports 4 and 5 for accessing external memory.	Input	P67
ANI0 to ANI7	Input	Analog input of A/D converter	Input	P10 to P17
ANO0, ANO1	Output	Analog output of D/A converter	Input	P130, P131
AV_{REF0}	Input	Reference voltage input of A/D converter	—	—
AV_{REF1}	Input	Reference voltage input of D/A converter	—	—
AV_{DD}	—	Analog power supply of A/D converter, connected to V_{DD}	—	—
AVss	—	Ground potential of A/D converter, connected to Vss	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{PP}	—	High-voltage applied during program write/ verification. Normally, connected to Vss in normal operating mode	—	—
Vss	—	Ground potential	—	—

2.2 PINS IN PROM PROGRAMMING MODE

Pin Name	Input/Output	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/ verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$	Input	Read strobe input to PROM
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programing mode.
V_{DD}	——	Positive power supply
Vss	——	Ground potential

2.3 PIN INPUT/OUTPUT CIRCUITS AND RECOMMEDED CONNECTION OF UNUSED PINS

Types of input/output circuits of the pins and recommeded connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Fig. 2-1.

Table 2-1 Type of Input/Output Circuit of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
P00/INTP0/TI00	2	Input	Connect to Vss.
P01/INTP1/TI01	8-A	Input/output	Input : Connect to Vss. Output : Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to Vss.
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connect to VDD or Vss. Output : Leave open.
P20/SI1	8-A	Input/output	Input : Connect to VDD or Vss. Output : Leave open.
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A	Input/output	Input : Connect to VDD or Vss. Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Input : Connect to Vss. Output : Leave open. ★

Table 2-1 Type of Input/Output Circuit of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
P50/A8 to P57/A15	5-A	Input/output	Input : Connect to V_{DD} or Vss. Output : Leave open.
P60 to P63	13		
P64/$\overline{RD}$	5-A		
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/SI2/RxD	8-A	Input/output	Input : Connect to V_{DD} or Vss. Output : Leave open.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A	Input/output	Input : Connect to V_{DD} or Vss. Output : Leave open.
P130/ANO0, P131/ANO1	12-A	Input/output	Input : Connect to V_{DD} or Vss. Output : Leave open.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open
AV_{REF0}	—		Connect to Vss
★ AV_{REF1}			Connect to V_{DD}
AV_{DD}			
AV_{SS}			Connect to Vss
V_{PP}			

Fig. 2-1 List of Pin Input/Output Circuits (1/2)

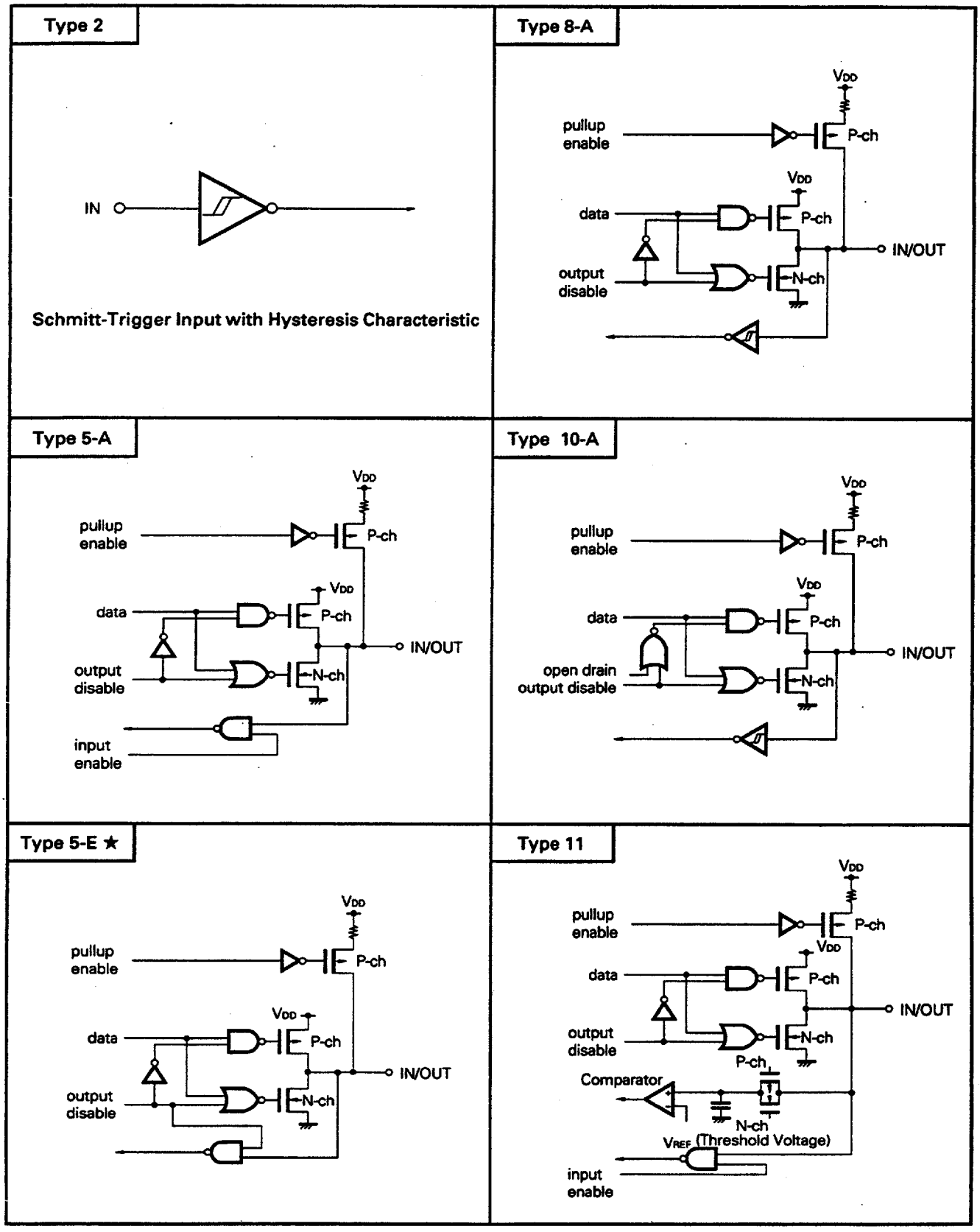
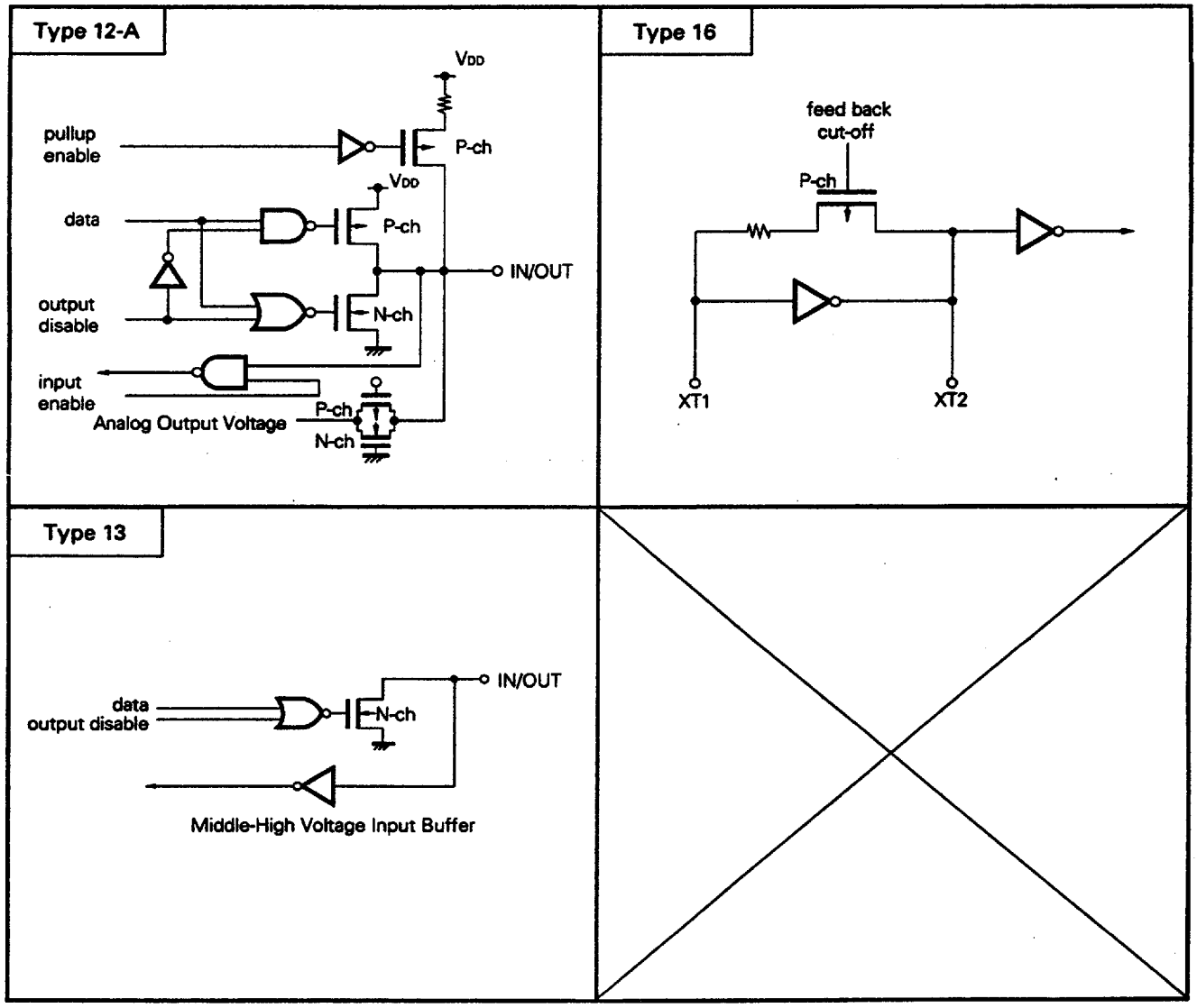


Fig. 2-1 List of Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM product having different internal memories (ROM, RAM).

The IMS is set up by the 8-bit memory manipulation instruction.

C8H will result by the $\overline{\text{RESET}}$ input.

Fig. 3-1 Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16K bytes
0	1	1	0	24K bytes
1	0	0	0	32K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which makes the memory mapping the same as that of the various mask ROM products.

Table 3-1 Memory Size Switching Register Setting Examples

Target Mask ROM Product	IMS Setting Value
μPD78052Y	44H
μPD78053Y	C6H
μPD78054Y	C8H

4. PROM PROGRAMMING

The μPD78P054Y has an on-chip 32K-byte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For connecting unused pins, refer to **"Pin Configuration (2) PROM programming mode."**

4.1 OPERATING MODES

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1 Operating Modes of PROM Programming

Operating Mode \ Pin	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

Remarks ×: L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P054Ys are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly, after the write.

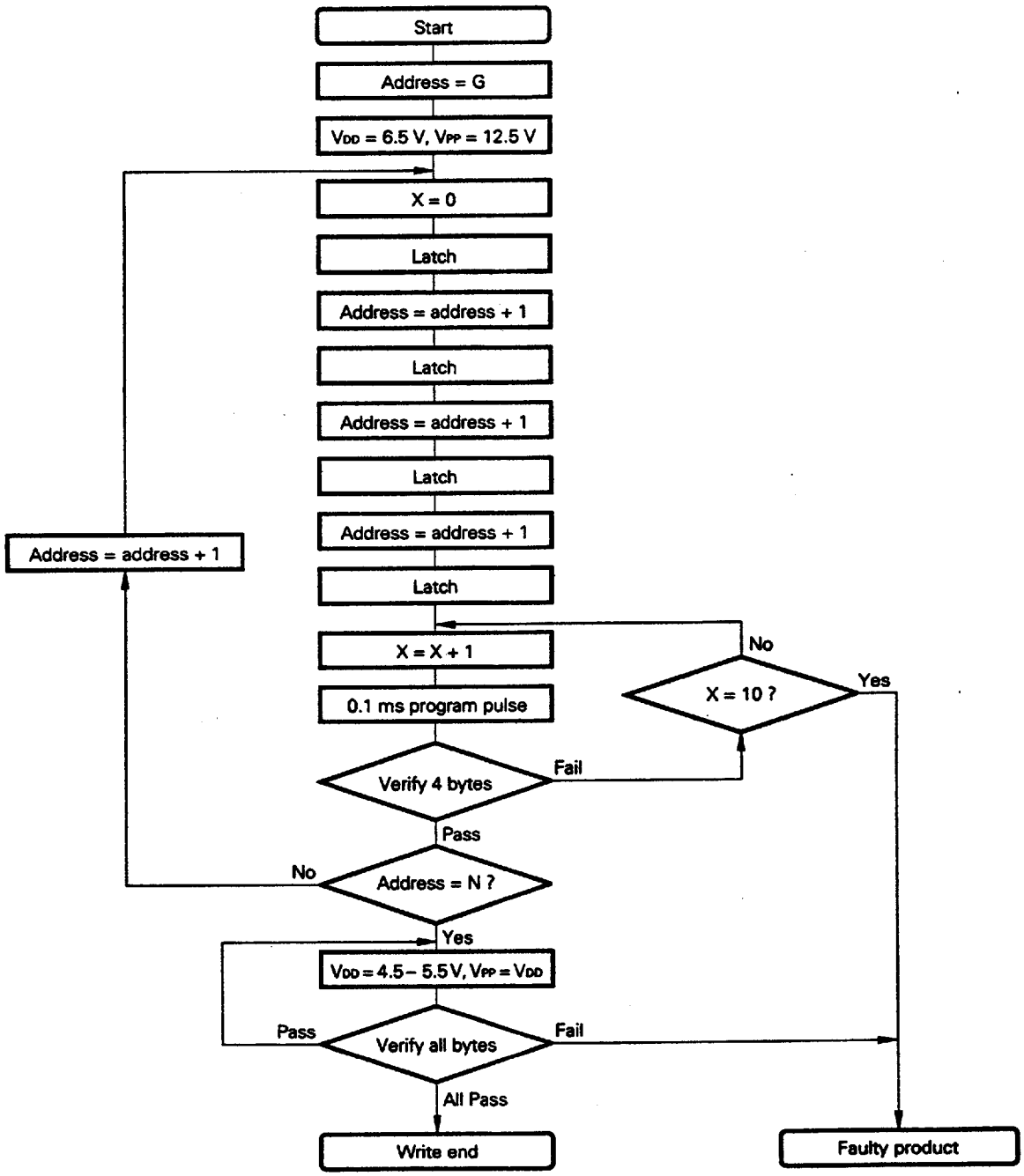
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P054Ys are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

4.2 PROM WRITE PROCEDURE

Fig. 4-1 Page Program Mode Flowchart



Remarks 1. G = Start address
2. N = Program last address

Fig. 4-2 Page Program Mode Timing

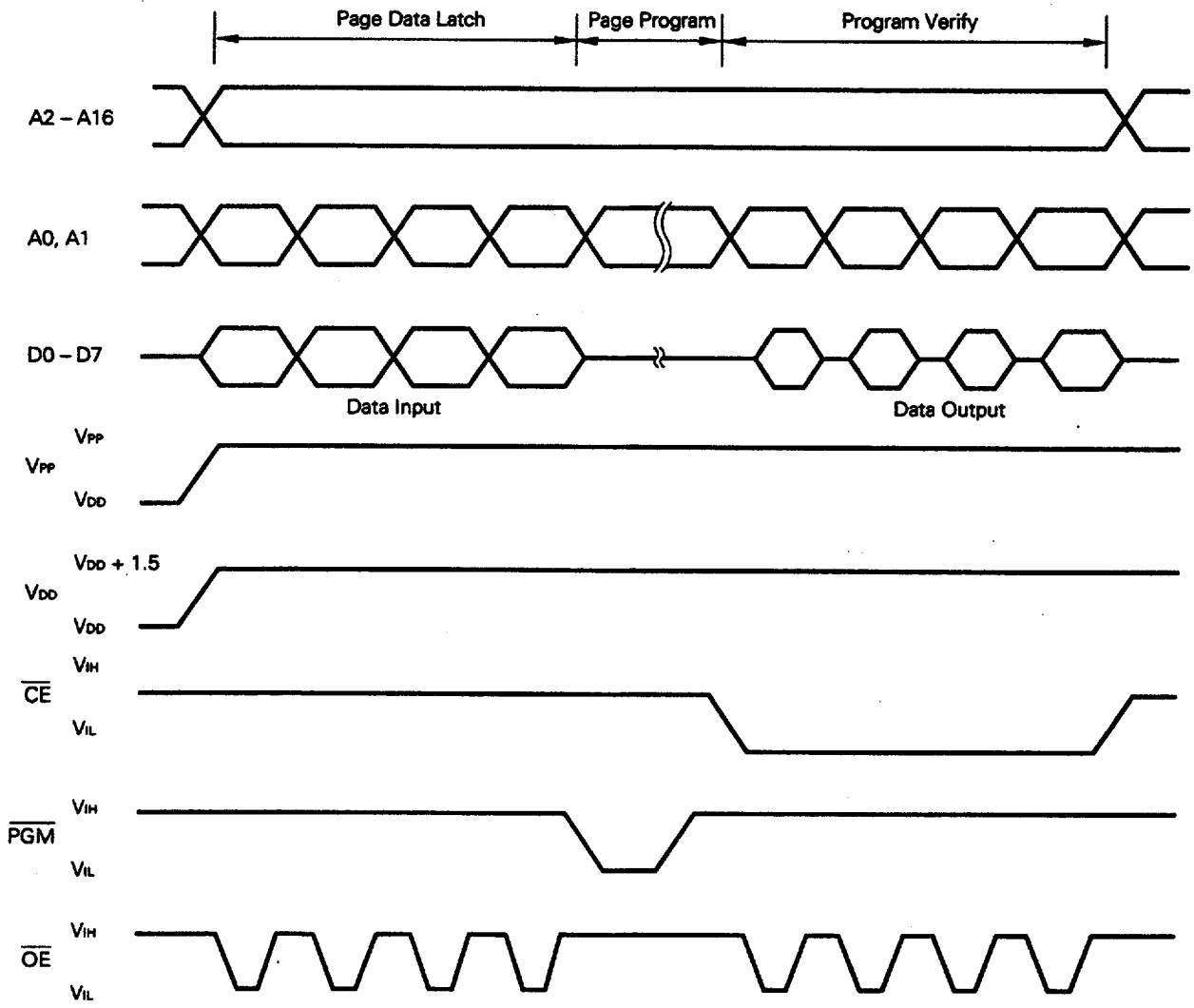
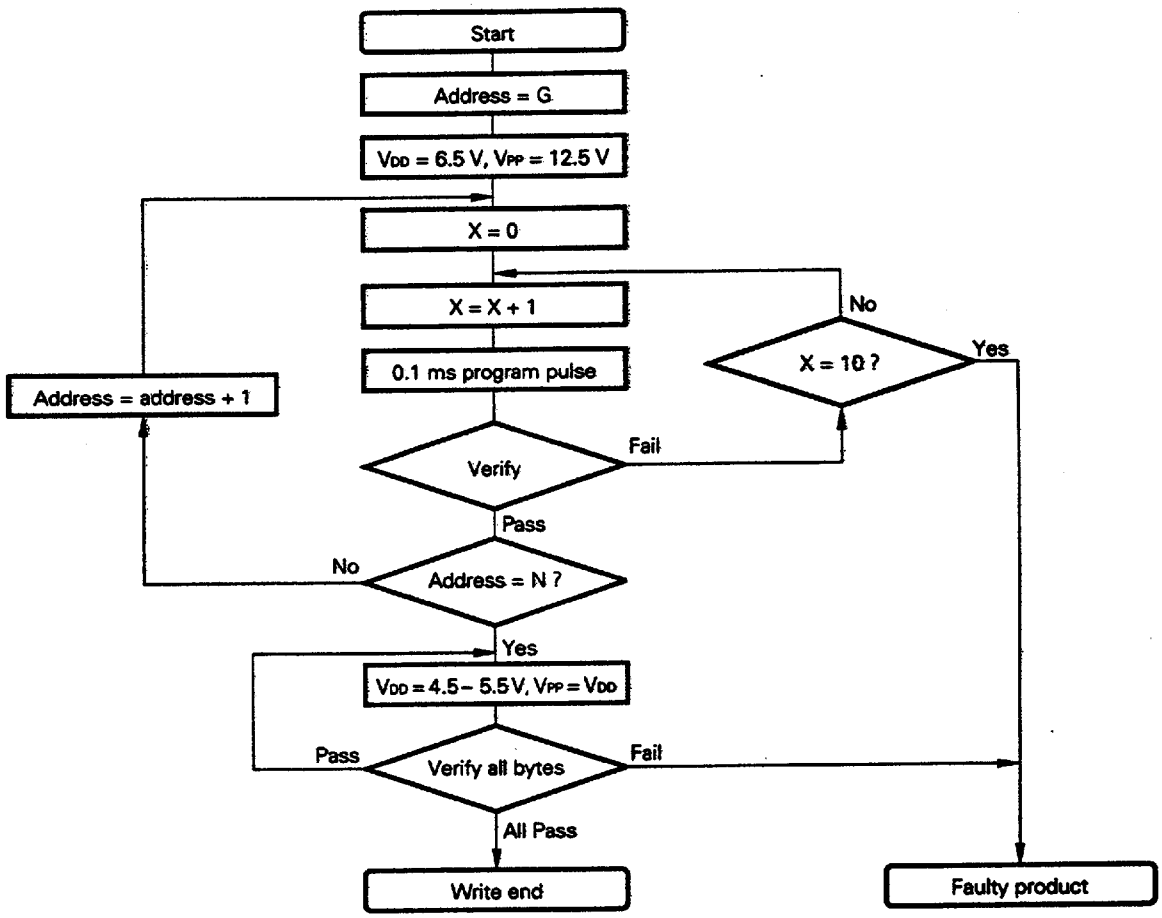
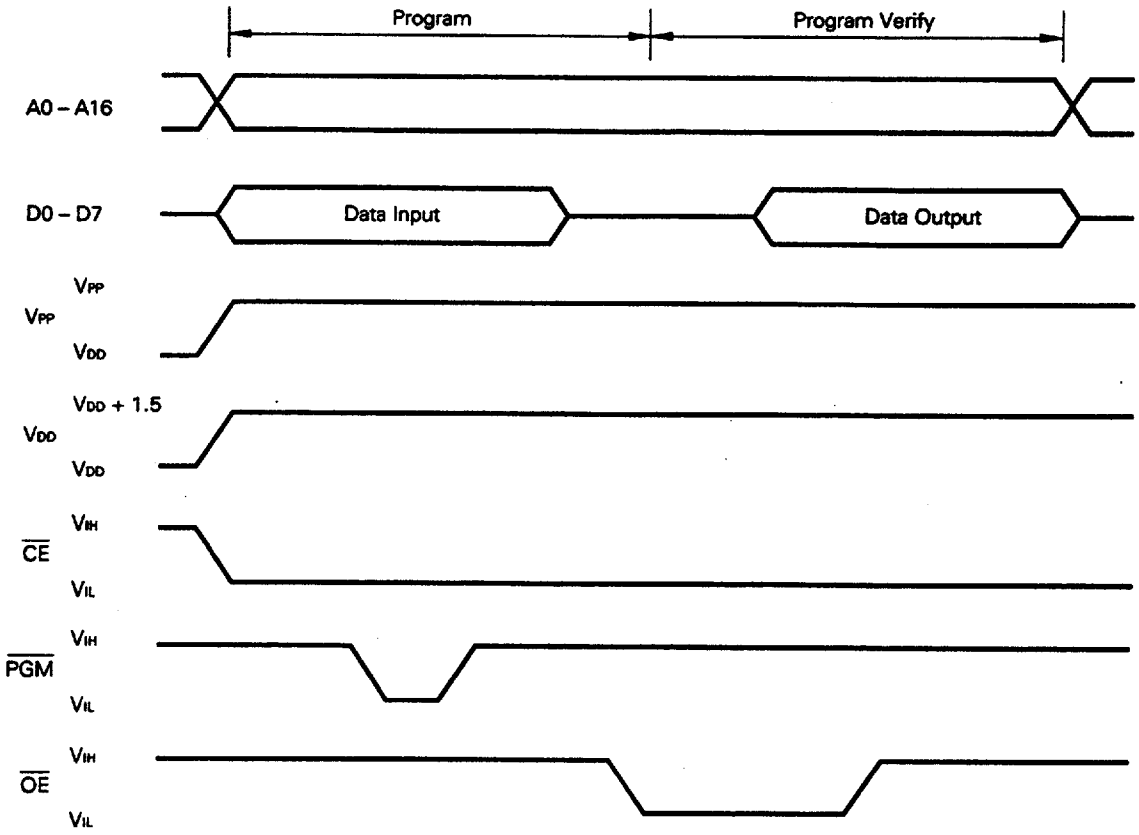


Fig. 4-3 Byte Program Mode Flow Chart



Remarks 1. G = Start address
2. N = Program last address

Fig. 4-4 Byte Program Mode Timing



Note
1. **V_{DD} should be applied before V_{PP} and cut after V_{PP}.**
2. **V_{PP} must not exceed +13.5 V including overshoot.**
3. **Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.**

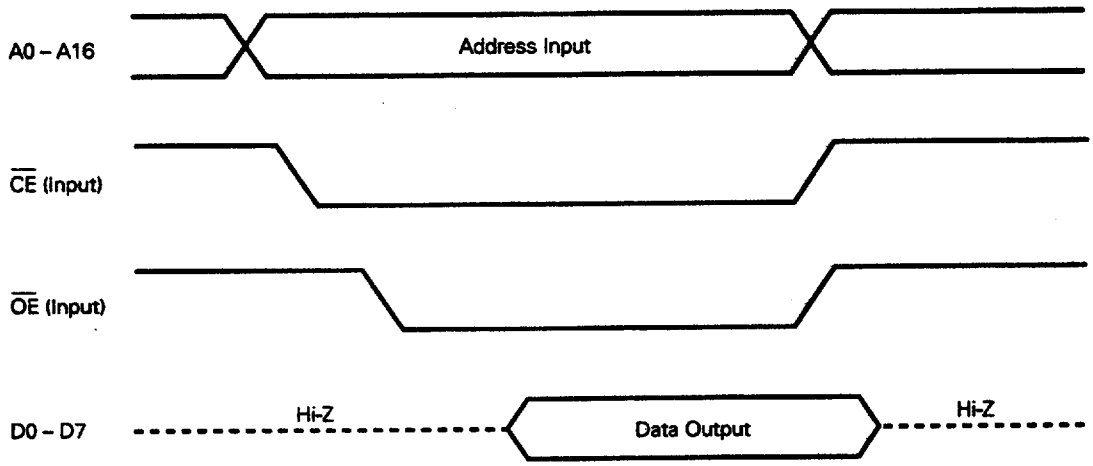
4.3 PROM READ PROCEDURE

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **"Pin Configuration (2) PROM programming mode"**.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of read data into the A0 to A16 pins.
(4) Read mode
(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Fig. 4-5.

Fig. 4-5 PROM Read Timings



5. ERASURE METHOD (μPD78P054YKK-T ONLY)

The μPD78P054YKK-T is capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the contents of data, irradiate light having a wavelength of less than about 400 nm to the erasing window. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of irradiation required to completely erase the contents of data is as follows:

- UV intensity × erasing time : 15 W•s/cm² or more
- Erasing time : 15 to 20 min. (When a UV lamp of 12,000 μW/cm² is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

6. ERASURE WINDOW SEAL (μPD78P054YKK-T ONLY)

To protect from miserasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, stick a protection seal on the erasure window when EPROM contents erasure is not performed.

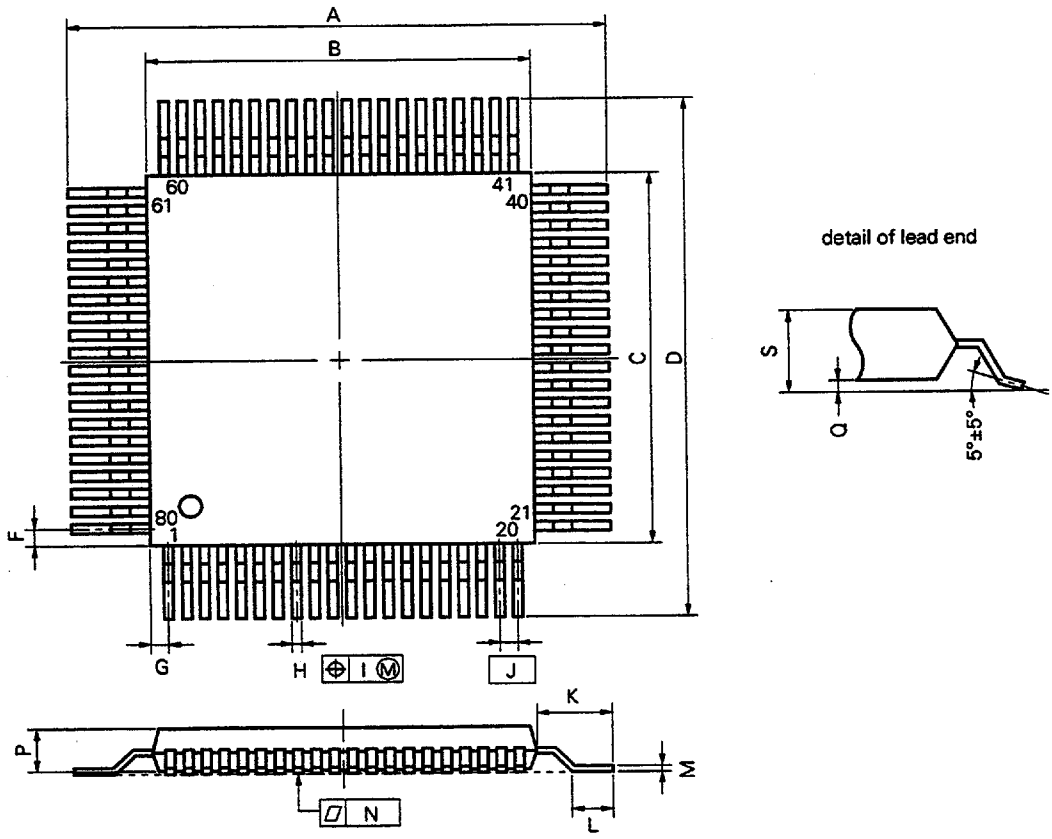
7. ONE-TIME PROM PRODUCTS SCREENING

The one-time PROM product (μPD78P054YGC-3B9, μPD78P054YGK-BE9) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage time
125 °C	24 hours

8. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14)

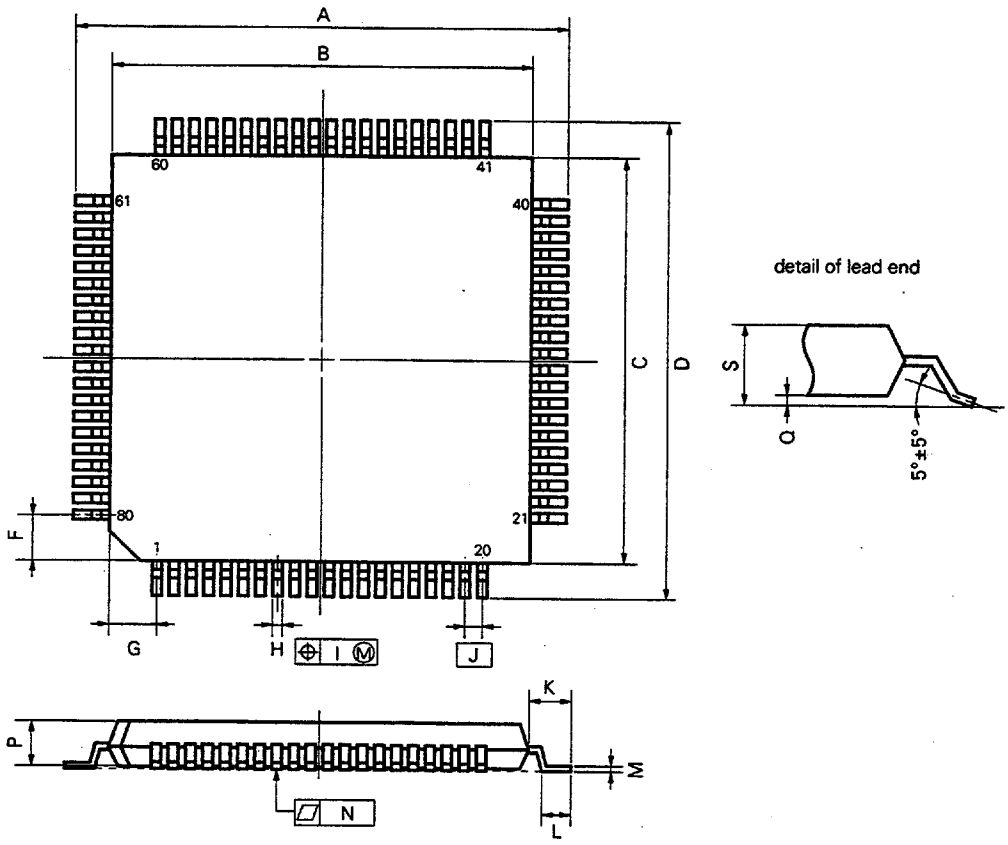


S80GC-65-3B9-3

NOTE
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



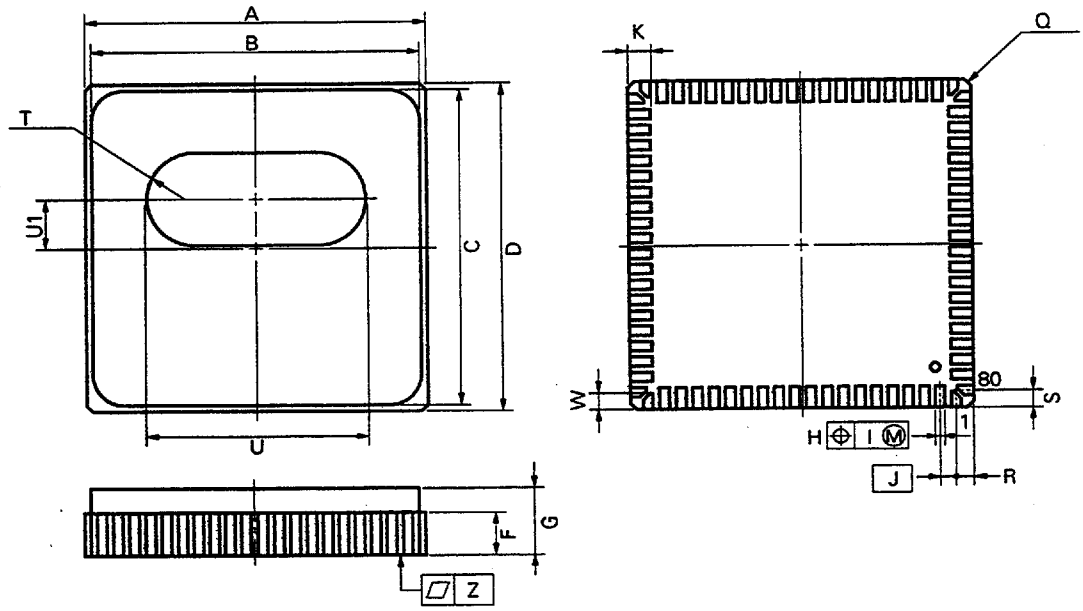
P80GK-50-BE9-3

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.4	0.551±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.4	0.551±0.016
F	1.25	0.049
G	1.25	0.049
H	0.20±0.10	0.008±0.004
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.001}$
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
S	1.27 MAX.	0.05 MAX.

★ 80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE
Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

APPENDIX A. DEVELOPMENT TOOLS

To support development of systems which use the μPD78P054Y, the following development tools are available.

Language Processing Software

RA78K/0 *1,2	78K/0 series common assembler package
CC78K/0 *1,2	78K/0 series common C compiler package
CC78K/0 *1,2	78K/0 series common C compiler library source file

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PROM Write Tools

PG-1500	PROM Programmer
PA-78P054GC PA-78P054GK PA-78P054KK-T	PG-1500 Programmer adapter connected to PG-1500
PG-1500 Controller *1	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulator
IE-78000-R-BK	78/0 series common break board
IE-78064-R-EM	μPD78064 series common emulation board
EP-7230GC-R	μPD78234 series common emulation probe
EV-78054GK-R	μPD78054 series common emulation probe
EV-9200GC-80	Socket to be mounted on user system board created for the 80-pin plastic QFP
EV-9500GK-80	Adapter to be mounted on user system board created for the 80-pin plastic QFP
SD78K/0 *1	IE-78000-R screen debugger
DF78054 *1,3	μPD78054 series common device file

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Real-Time OS

RX78K/0 *1,2	78K/0 series common real-time OS

★

Fuzzy Inference Development Support System

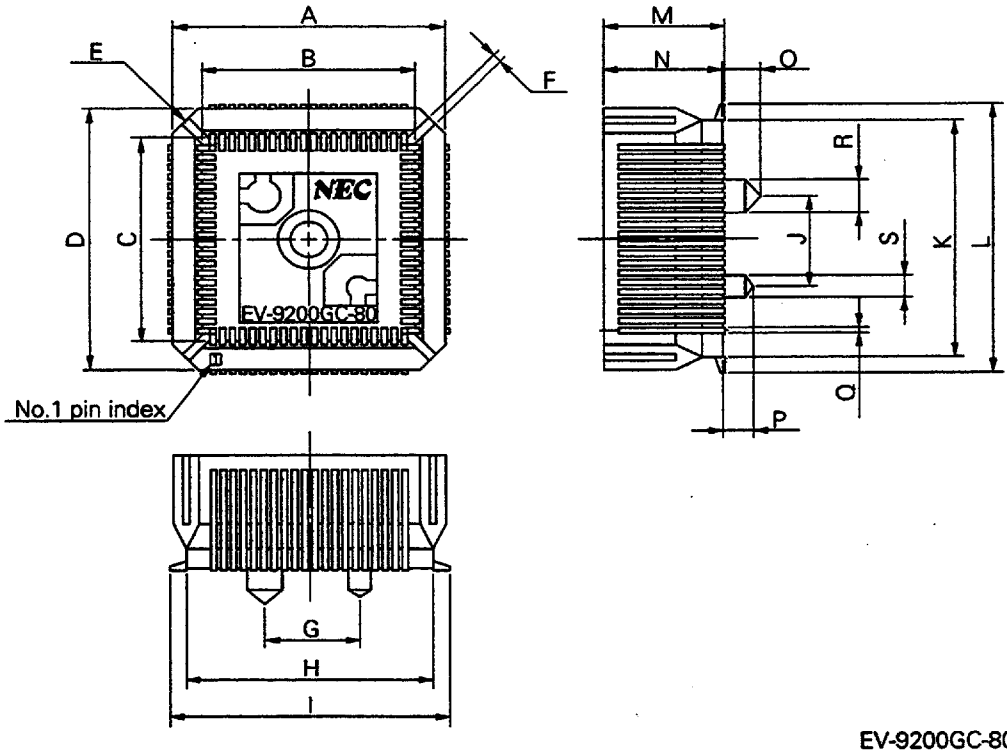
FE9000 *1	Fuzzy knowledge data creation tool
FT9080 *1	Translator
FI78K0 *1	Fuzzy inference module
FD78K0 *1,3	Fuzzy inference debugger

★

* 1. PC-9800 series (MS-DOS™) based, IBM PC/AT™ (PC DOS™) based
2. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series™ (EWS-UX/V™) based
3. Under development

★ **External View of Conversion Socket (EV-9200GC-80) and Recommended Board Mounting Pattern**

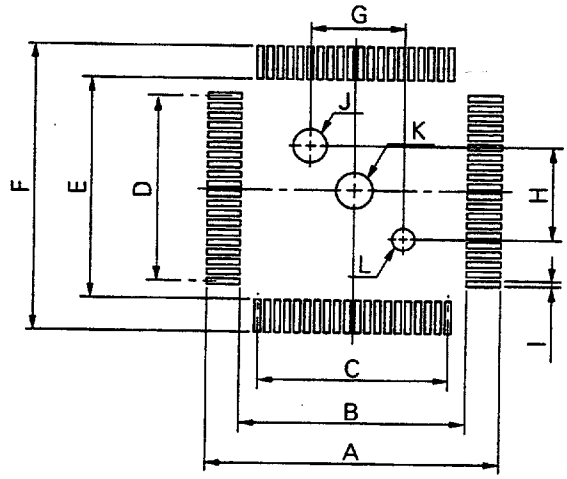
Fig. A-1 EV-9200GC-80 (Reference) (Unit: mm)



EV-9200GC-80-G0

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Fig. A-2 EV-9200GC-80 Recommended Board Mounting Pattern (Reference) (Unit: mm)



EV-9200GC-80-P0

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No.
User's Manual	In preparation
78K/0 Series Instruction Application Table	
78K/0 Series Instruction Set	
μPD78054Y Series Special Function Register Application Table	

Development Tools Related Documents (User's Manual)

Document Name		Document No.
RA78K Series Assembler Package	Operation Volume	
	Language Volume	
RA78K Series Structured Assembler Preprocessor		
CC78K Series C Compiler	Instruction Volume	
	Language Volume	
CC78K Series Library Source File		
PG-1500 PROM Programmer		
IE-78000-R		
IE-78000-R-BK		
IE-78064-R-EM		
SD78K/0 Screen Debugger	Introductory Volume	
	Reference Volume	

Built-In Software Related Documents (User's Manual)

Document Name		Document No.
78K/0 Series Real-Time OS	Introduction Volume	
	Installation Volume	
	Debugging Volume	
	Technical Volume	
Fuzzy Knowledge Data Creation Tool		
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		

Note **The contents of the above related documents are subject to change withoug notice. The latest document should be used for design, etc.**

Other Documents

Document Name	Document No.
Package Manual	
Surface Mount Technology Manual	
Quality Grade on NEC Semiconductor Devices	
NEC Semiconductor Devices	
Electrostatic Discharge (ESD) Test	
Semiconductor Devices Quality Guarantee Guide	
Microcomputer Related Products Guide Others Manufactures Volume	

Note **The contents of the above related documents are subject to change withoug notice. The latest document should be used for design, etc.**