PROCESS CP302

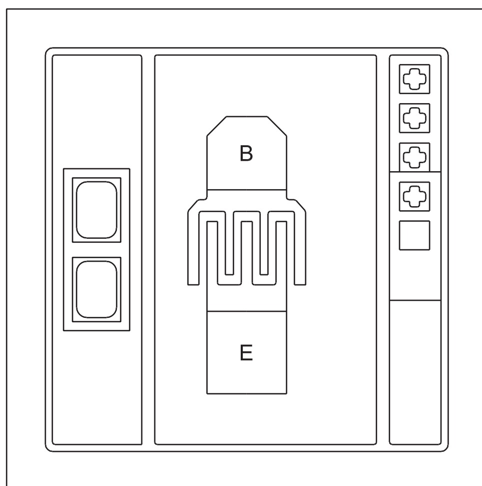
Small Signal Transistor

NPN - Silicon RF Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	14.5 x 14.5 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	2.3 x 2.3 MILS
Emitter Bonding Pad Area	2.5 x 2.3 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R2

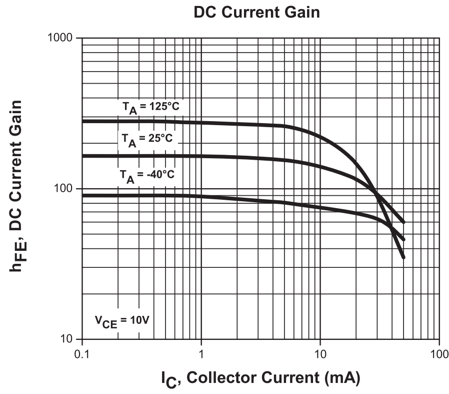
GROSS DIE PER 4 INCH WAFER
53,730

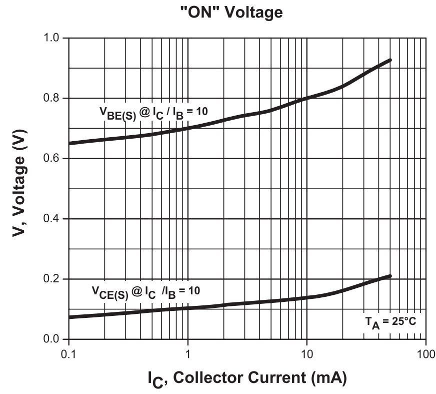
PRINCIPAL DEVICE TYPES
MPSH10
MPSH11
CMPTH10
CMPTH11

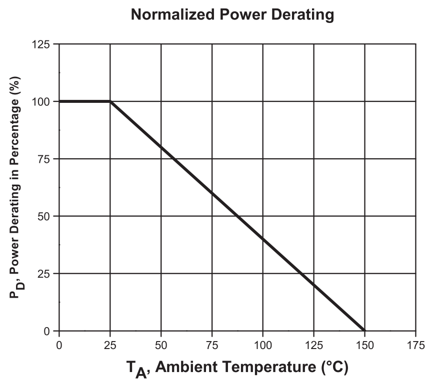
R3 (22-March 2010)

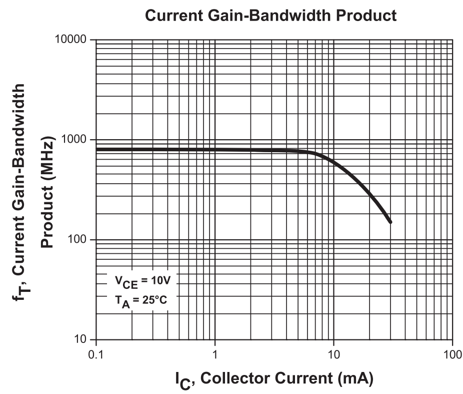
PROCESS CP302

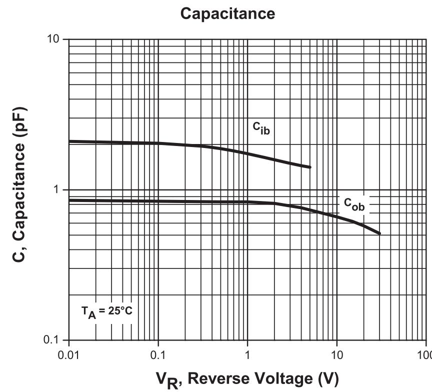
Typical Electrical Characteristics











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