High Reliability Series Serial EEPROMs

WL-CSP EEPROM family
I²C BUS

BRCA016GWZ-W

No.11001EAT23

●Description

BRCA016GWZ-W series is a serial EEPROM of I²C BUS interface method.

●Features

1) Completely conforming to the world standard I²C BUS. All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
2) Other devices than EEPROM can be connected to the same port, saving microcontroller port.
3) 1.7~3.6V single power source action most suitable for battery use.
4) Page write mode useful for initial value write at factory shipment.
5) Highly reliable connection by Au pad and Au wire.
6) Auto erase and auto end function at data rewrite.
7) Low current consumption
   At write operation (5V) : 0.5mA (Typ.)
   At read operation (5V) : 0.2mA (Typ.)
   At standby operation (5V) : 0.1μA (Typ.)
8) Write mistake prevention function
   Write (write protect) function added
   Write mistake prevention function at low voltage
9) UCSP30L1 compact package
10) Data rewrite up to 100,000 times
11) Data kept for 40 years
12) Noise filter built in SCL / SDA terminal
13) Shipment data all address FFh

●BRCA016GWZ-W

Capacity	Bit format	Type	Power source voltage	Package
16kbit	2K×8	BRCA016GWZ-W	1.7~3.6V	UCSP30L1

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Impressed voltage	Vcc	-0.3～+6.5	V
Permissible dissipation	Pd	220(UCSP30L1)*1	mW
Storage temperature range	Tstg	-65 ～ +125	℃
Action temperature range	Topr	-40 ～ +85	℃
Terminal Voltage	—	-0.3～Vcc+1.0	V

* *1 When using at Ta=25℃ or higher, 2.2mW to be reduced per 1℃

●Memory cell characteristics (Ta=25℃,Vcc=1.7V~3.6V)

Parameter	Ratings			Unit
	Min.	Typ.	Max.	
Number of data rewrite times *1	100,000	—	—	Times
Data hold years *1	40	—	—	Years

*1 : Not 100% TESTED

●Recommended operating condition

Parameter	Symbol	Ratings	Unit
Power source voltage	Vcc	1.7～3.6	V
Input voltage	V_{IN}	0～Vcc	

●Electrical characteristics

(Unless otherwise specified, Ta=−40～+85℃, Vcc=1.7～3.6V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ.	Max.		
"H" Input Voltage1	V_{IH1}	0.7Vcc	—	Vcc+1.0	V	
"L" Input Voltage1	V_{IL1}	-0.3	—	0.3Vcc	V	
"L" Output Voltage1	V_{OL1}	−	—	0.4	V	I_{OL}=3.0mA , 2.5V≦Vcc≦3.6V (SDA)
"L" Output Voltage2	V_{OL2}	−	—	0.2	V	I_{OL}=0.7mA , 1.7V≦Vcc≦2.5V (SDA)
Input Leakage Current	I_{LI}	-1	—	1	μA	V_{IN}=0～Vcc
Output Leakage Current	I_{LO}	-1	—	1	μA	V_{OUT}=0～Vcc (SDA)
Current consumption at action	I_{CC1}	—	—	2.0	mA	Vcc=3.6V , f_{SCL} =400kHz, tWR=5ms Byte Write, Page Write BR24S16/32/64-W
	I_{CC2}	—	—	0.5	mA	Vcc=3.6V , f_{SCL} =400kHz Random read, Current read, Sequential read
Standby Current	I_{SB}	—	—	2.0	μA	Vcc=3.6V , SDA・SCL=Vcc A0, A1, A2=GND, WP=GND

○Radiation resistance design is not made.

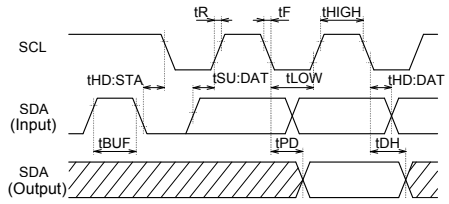
●Action timing characteristics

(Unless otherwise specified, Ta=－40～+85℃, Vcc=1.7~3.6V)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SCL Frequency	fSCL	－	－	400	kHz
Data clock "High" time	tHIGH	0.6	－	－	μs
Data clock "Low" time	tLOW	1.2	－	－	μs
SDA, SCL rise time *1	tR	－	－	0.3	μs
SDA, SCL fall time *1	tF	－	－	0.3	μs
Start condition hold time	tHD:STA	0.6	－	－	μs
Start condition setup time	tSU:STA	0.6	－	－	μs
Input data hold time	tHD:DAT	0	－	－	ns
Input data setup time	tSU:DAT	100	－	－	ns
Output data delay time	tPD	0.1	－	0.9	μs
Output data hold time	tDH	0.1	－	－	μs
Stop condition data setup time	tSU:STO	0.6	－	－	μs
Bus release time before transfer start	tBUF	1.2	－	－	μs
Internal write cycle time	tWR	－	－	5	ms
Noise removal valid period (SDA,SCL terminal)	tI	－	－	0.1	μs
WP hold time	tHD:WP	0	－	－	ns
WP setup time	tSU:WP	0.1	－	－	μs
WP valid time	tHIGH:WP	1.0	－	－	μs

*1 : Not 100% TESTED

●Sync data input/output timing



○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Fig.1-(a) Sync data input / output timing

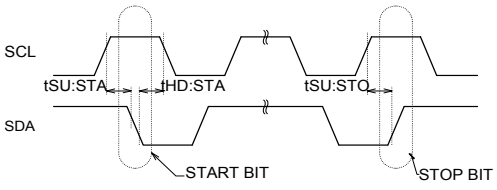


Fig.1-(b) Start - stop bit timing

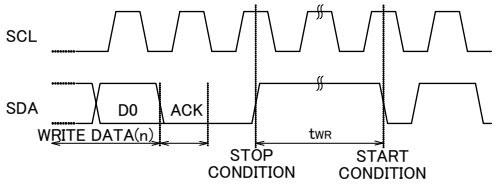


Fig.1-(c) Write cycle timing

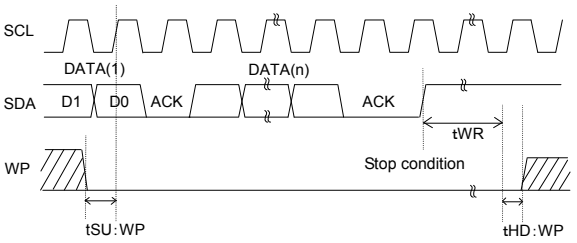
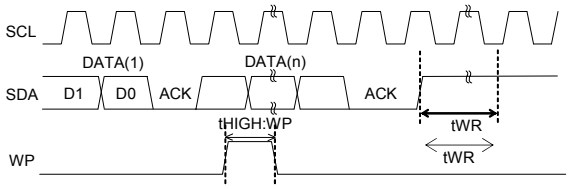


Fig.1-(d) WP timing at write execution



○At write execution, in the area from the D0 taken clock rise of the first DATA(1), to tWR, set WP= 'LOW'.
○By setting WP "HIGH" in the area, write can be cancelled.
When it is set WP = 'HIGH' during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

Fig.1-(e) WP timing at write cancels

●Block diagram

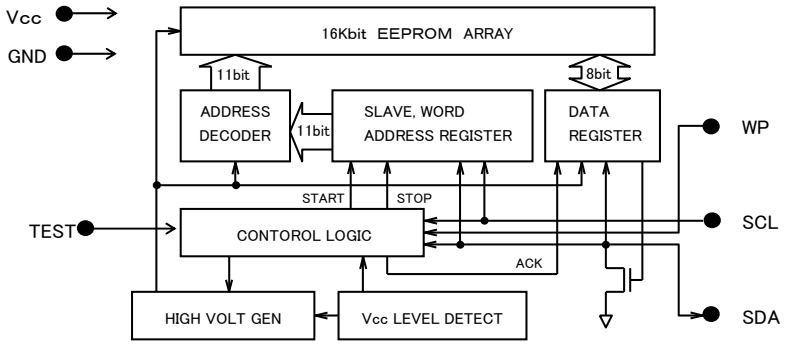
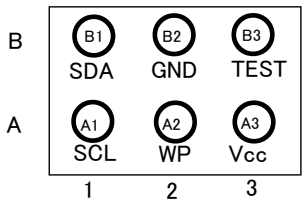


Fig.2 Block diagram

●Pin assignment and description



Land No.	Pin Name	I/O	Function
B3	TEST	input	Please connect GND.
B2	GND	-	Grand (0V)
B1	SDA	input, output	SLAVE,WORD ADDRESS Serial Data Input, Serial Data Output
A3	Vcc	-	Power Supply
A2	WP	input	Write Protect
A1	SCL	input	Serial Clock Input

●Characteristic data (The following values are Typ. ones.)

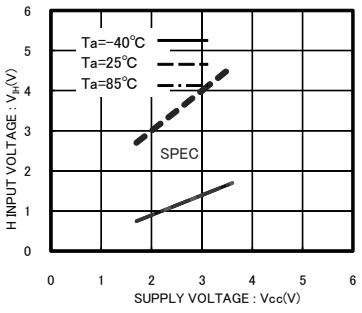


Fig.3 'H' input voltage V_{IH} (SCL,SDA,WP)

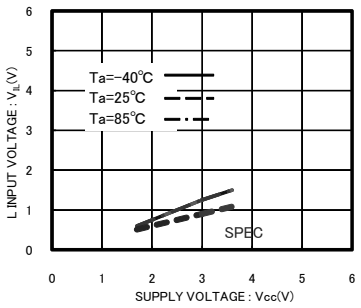


Fig.4 'L' input voltage V_{IL} (SCL,SDA,WP)

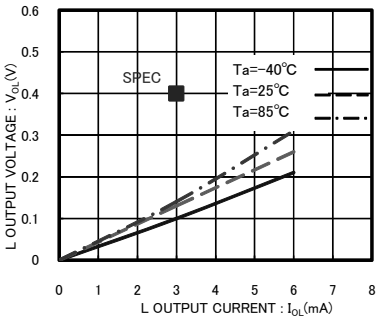


Fig.5 'L' output voltage V_{OL}-I_{OL}(Vcc=2.5V)

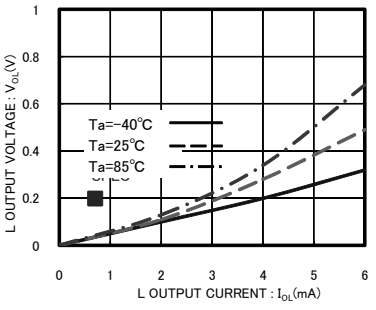


Fig.6 'L' output voltage V_{OL}-I_{OL}(Vcc=2.5V)

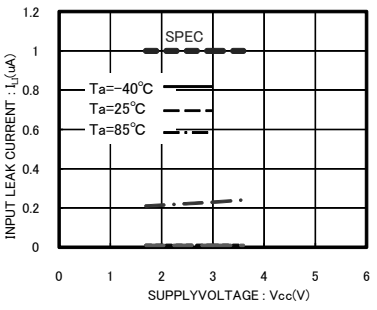


Fig.7 Input leak current I_{LI}(SCL,WP)

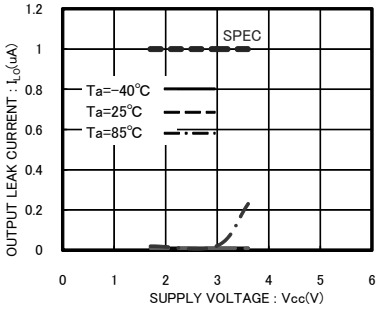


Fig.8 Output leak current I_{LO}(SDA)

●Characteristic data (The following values are Typ. ones.)

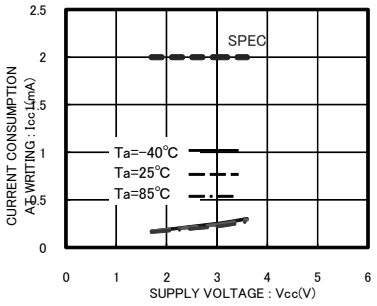


Fig.9 Current consumption at WRITE operation $I_{CC}1$ (fscl=400kHz)

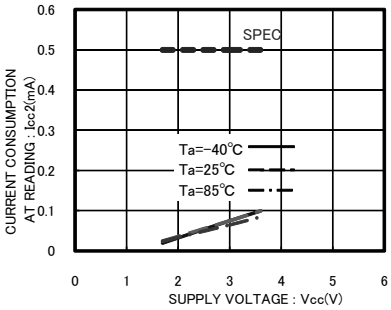


Fig.10 Current consumption at READ operation $I_{CC}2$ (fscl=400kHz)

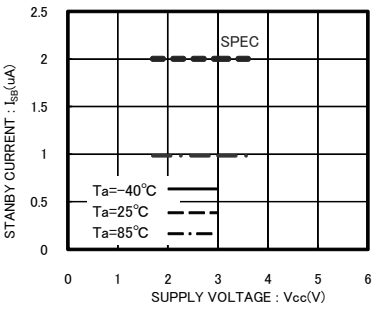


Fig.11 Stanby operation I_{SB}

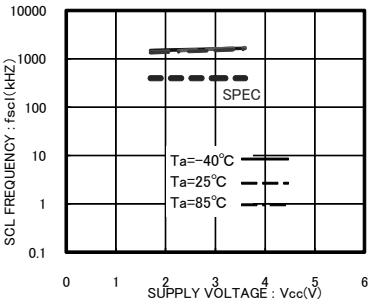


Fig.12 SCL frequency f_{SCL}

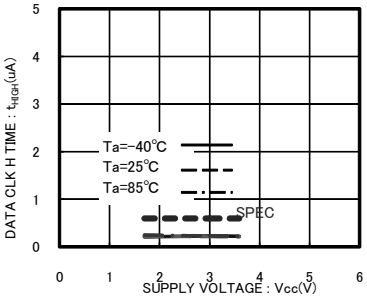


Fig.13 Data clock High Period t_{HIGH}

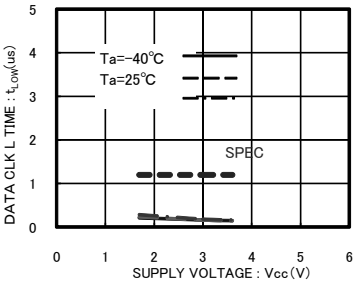


Fig.14 Data clock Low Period t_{LOW}

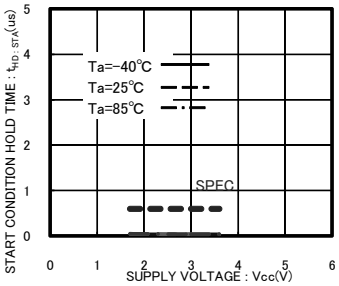


Fig.15 Start Condition Hold Time $t_{HD:STA}$

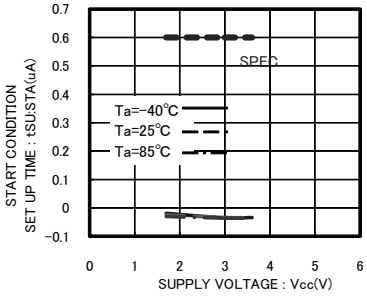


Fig.16 Start Condition Setup Time $t_{SU:STA}$

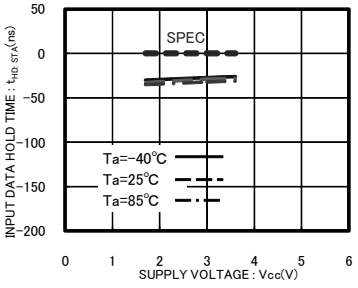


Fig.17 Input Data Hold Time $t_{HD:DAT}$(HIGH)

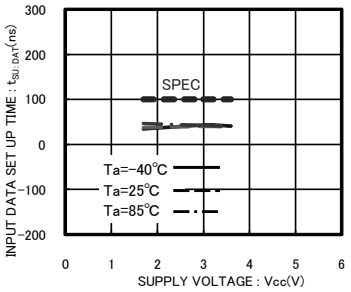


Fig.18 Input Data Setup Time $t_{SU:DAT}$(HIGH)

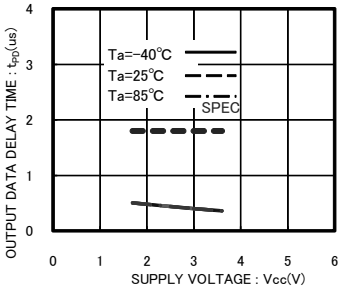


Fig.19 'L' Data output delay time $t_{PD}0$

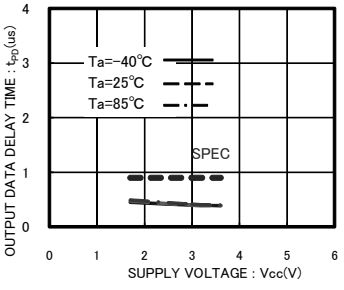


Fig.20 'H' Data output delay time $t_{PD}1$

●Characteristic data (The following values are Typ. ones.)

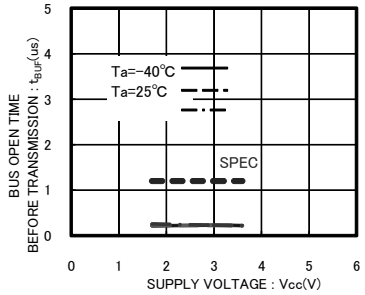


Fig.21 BUS open time before transmission t_{BUF}

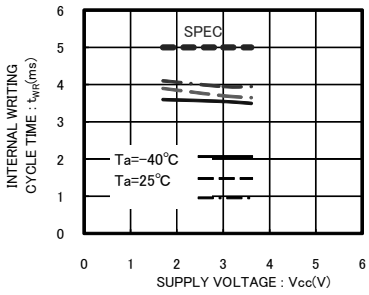


Fig.22 Internal writing cycle time t_{WR}

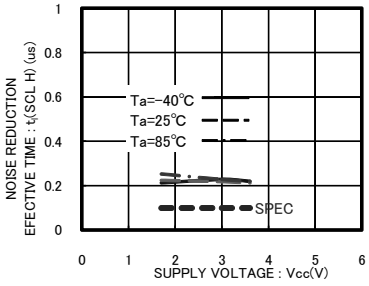


Fig.23 Noise reduction efection time t_I(SCL H)

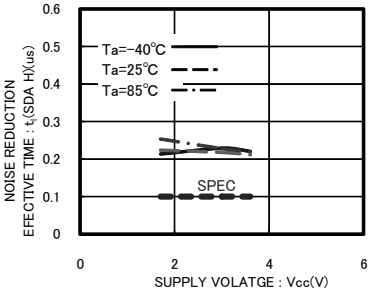


Fig.24 Noise resuction efecctive time t_I(SDA H)

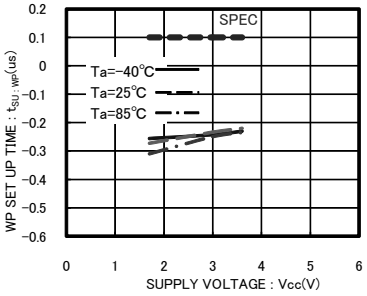


Fig.25 WP setup time $t_{SU:WP}$

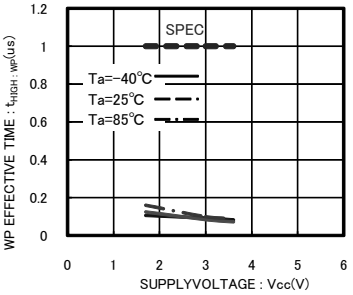


Fig.26 WP efective time $t_{HIGH:WP}$

●I²C BUS communication

○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).
Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by address peculiar to devices. EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

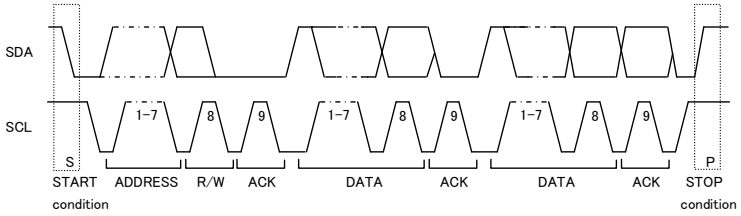


Fig.27 Data transfer timing

○Start condition (Start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this confdition is satisfied, any command is executed.

○Stop condition (stop bit recongnition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

○Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop cindition (stop bit), and ends read action. And this IC gets in status.

○Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type.
  The device code of this IC is fixed to '1010'.
- Next slave addresses (P2 P1 P0) are upper 3bit of word address, and put these and word address (WA0~7) together, 11bit word address (2048byte) of the device specified.
- The most insignificant bit (R / $\overline{W}$ --- READ / WRITE) of slave address is used for designating write or read action, and is as shown below.

  Setting R / $\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
  Setting R / $\overline{W}$ to 1 ------- read

Type	Slave address	Maximum number of Connected buses
BRCA016GWZ-W	1 0 1 0 P2 P1 P0 R / $\overline{W}$	1

P0～P2 are page select bits (Upper 3bit of word address).

●Write Command

○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity. Up to 16 arbitrary bytes can be written.

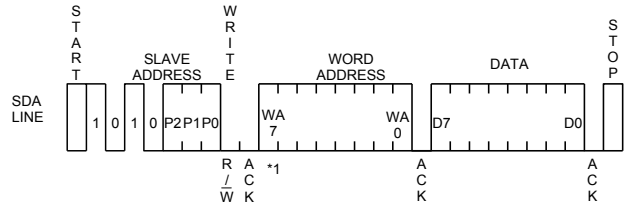


Fig.28 Byte write cy

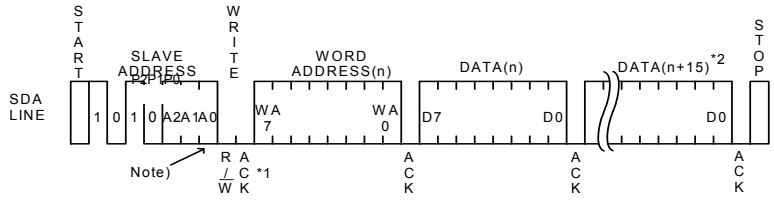


Fig.29 Page write cycle

・Data is written to the address designated by word address (n-th address)
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, the following can be written in bulk : Up to 16bytes
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to "Internal address increment" of "Notes on page write cycle" in P9/32.)

○Notes on write cycle continuous input

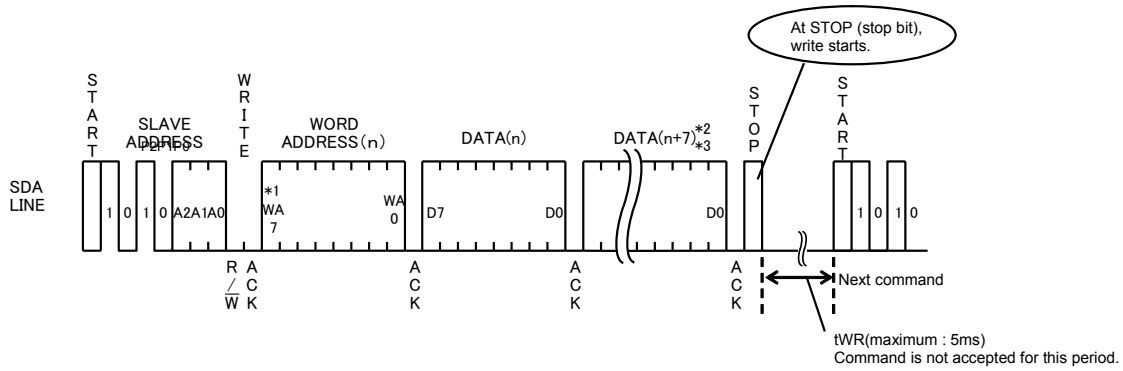


Fig.30 Page write cycle

○Notes on page write cycle

List of numbers of page write

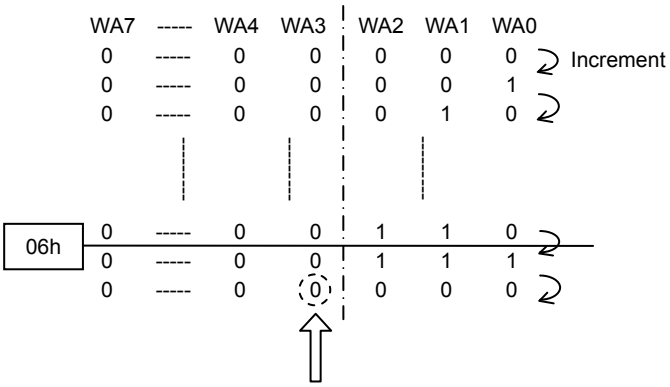
Number of Pages	16Byte
Product number	BRCA016GWZ-W

The above numbers are maximum bytes for respective types.
Any bytes below these can be written.

In the case BRCA016GWZ-W, 1 page=16bytes, but the page write cycle write time is 5ms at maximum for 16byte bulk write. It does not stand 5ms at maximum × 16byte=80ms(Max.)

○Internal address increment

Page write mode



For example, when it is started from address 0Eh,
therefore, increment is made as below,
0Eh → 0Fh → 00h → 01h ---, which please note.

* 0Eh･･･0E in hexadecimal, therefore, 00001110 becomes a binary number.

○Write protect (WP) terminal

・Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.

At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', mistake write can be prevented.

●Read Command

○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

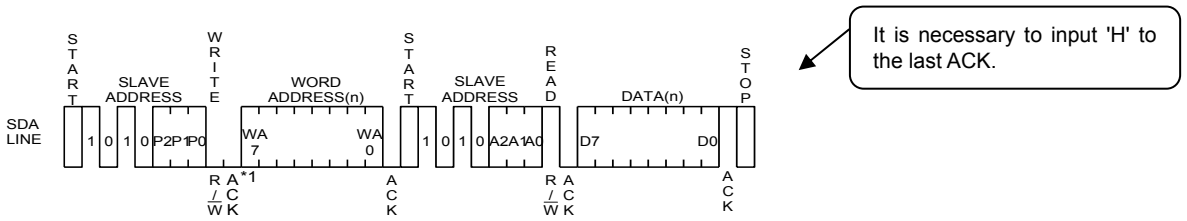


Fig.31 Random read cycle

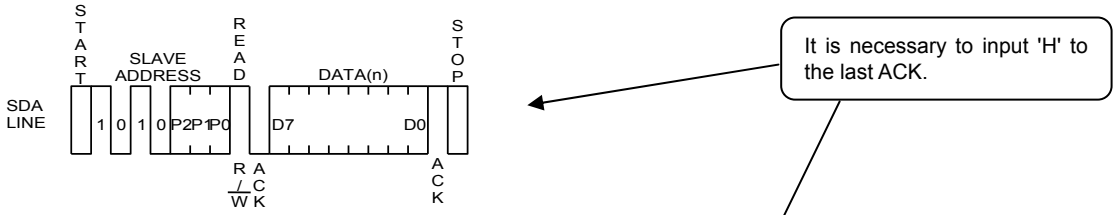


Fig.32 Current read cycle

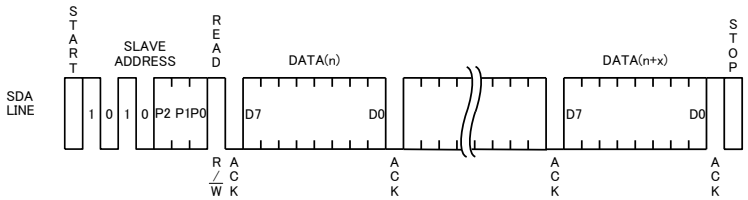


Fig.33 Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H' .
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Fig.34(a), Fig.34(b), and Fig.34(c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

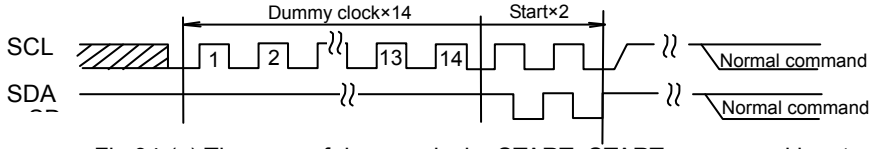


Fig.34-(a) The case of dummy clock +START+START+ command input

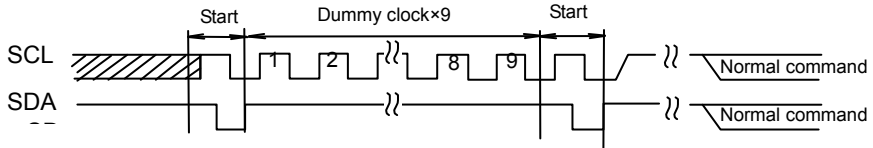


Fig.34-(b) The case of START +9 dummy clocks +START+ command input

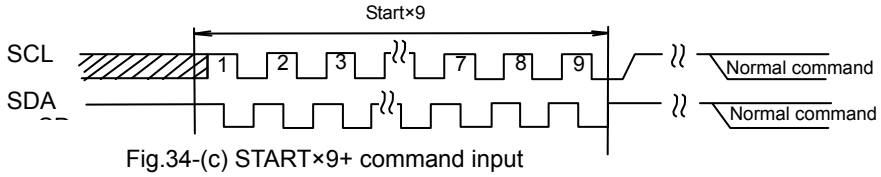


Fig.34-(c) START×9+ command input

※ Start command from START input.

●Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R / $\overline{W}$ = 0, when to carry out current read cycle after write, slave address R / $\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

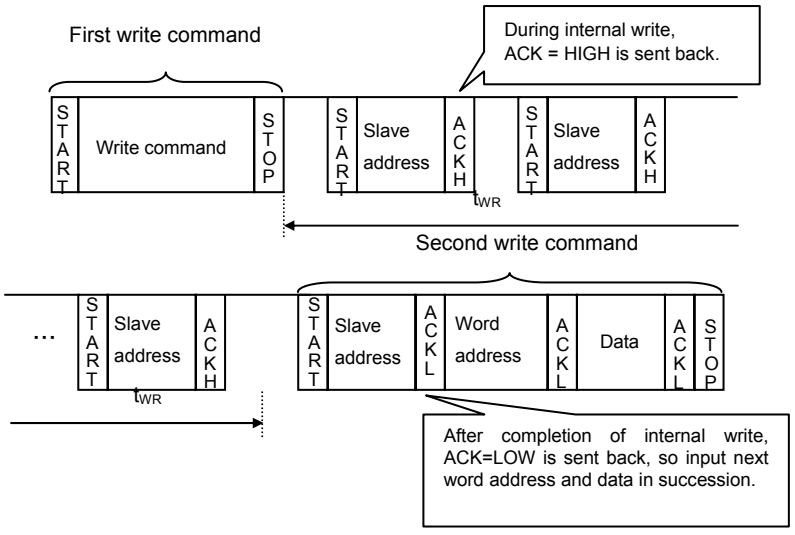


Fig.35 Case to continuously write by acknowledge polling

●WP valid timing (write cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area. WP input in this area becomes Don't care. Set the setup time to rise of D0 taken SCL 100ns or more. The area from the rise of SCL to take in D0 to input the stop condition is cancel valid area. And, after execution of forced end by WP, standby status gets in.

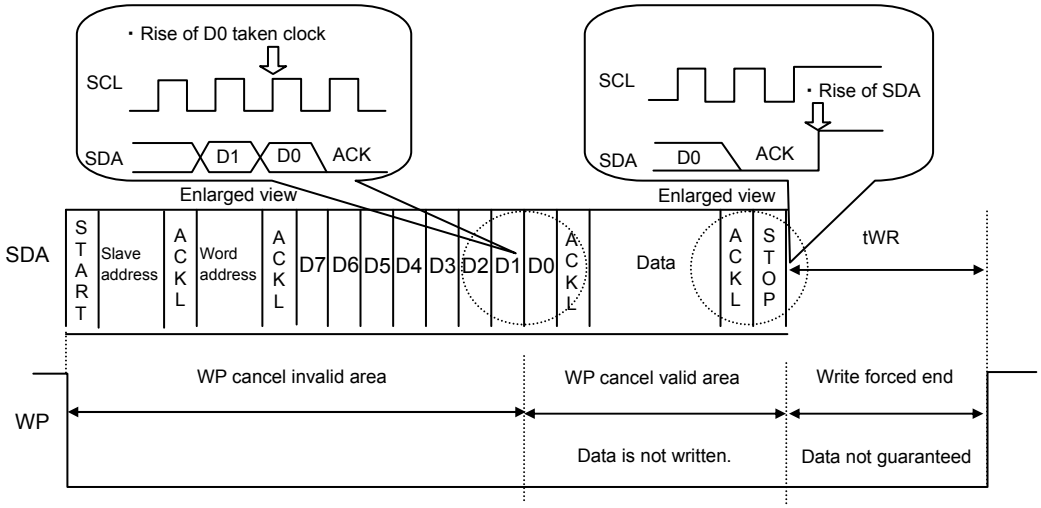


Fig.36 WP valid timing

●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled.
(Refer to Fig. 37.)
However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

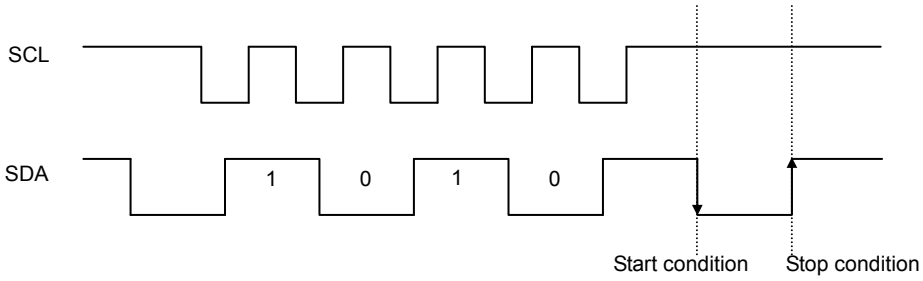


Fig.37 Case of cancel by start, stop condition during slave address input

●I/O peripheral circuit

○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the consumption current at action.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1)SDA rise time to be determined by the capacitance (CBUS) of bus line of R_{PU} and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential A to be determined by input leak total (I_L) of device connected to bus at output of 'H' to SDA bus and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$Vcc - I_L R_{PU} - 0.2Vcc \geqq V_{IH}$$

$$\therefore \quad R_{PU} = \frac{0.8Vcc - V_{IH}}{I_L}$$

Ex.) When V_{CC} =3V, I_L=10 μ A, V_{IH}=0.7 V_{CC},

from (2)

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

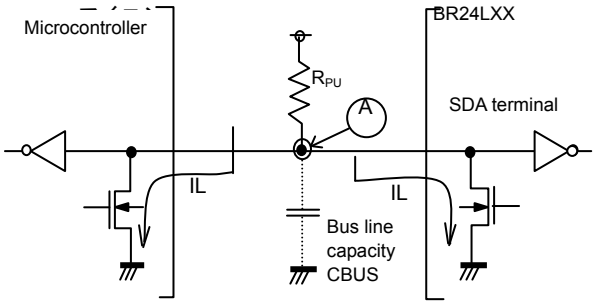


Fig.38 I/O circuit diagram

○Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1)When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL} \qquad \therefore \quad R_{PU} \leqq \frac{V_C - V_{OL}}{I_{OL}}$$

(2)V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$V_{OLMAX} \leqq V_{IL} - 0.1\ V_{CC}$

Ex.) When V_{CC} =3V, V_{OL}=0.4V, I_{OL}=3mA, microcontroller, EEPROM V_{IL}=0.3Vcc

from (1)

$$R_{PU} \geqq \frac{3 - 0.4}{3 \times 10^{-3}}$$

$$\geqq 867\ [\Omega]$$

And

$$V_{OL} = 0.4\ [V]$$

$$V_{IL} = 0.3 \times 3$$

$$= 0.9\ [V]$$

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ ~ several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

○Process of WP terminal

WP terminal is the terminal that prohibits and permits write in hardware manner. In 'H' status, only READ is available and WRITE of all address is prohibited. In the case of 'L', both are available. In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

●Cautions on microcontroller connection

○Rs

In I^2C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

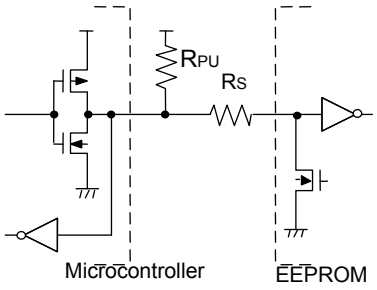


Fig.39 I/O circuit diagram

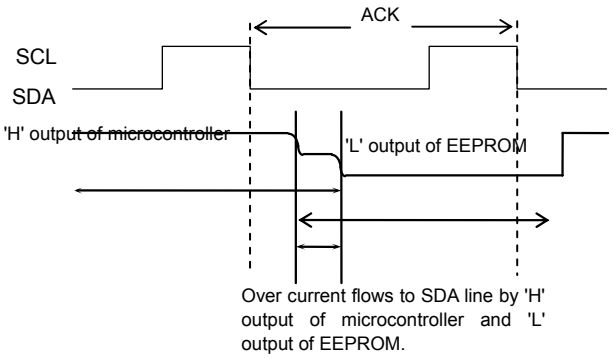


Fig.40 Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1Vcc.

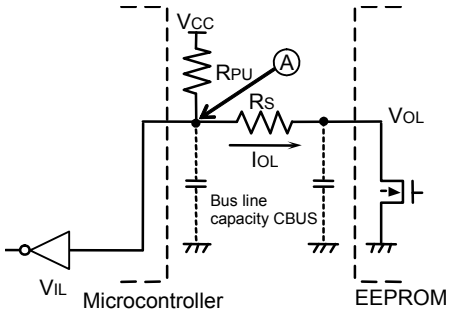


Fig.41 I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ,

$$\text{from(2)}, \quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67[k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

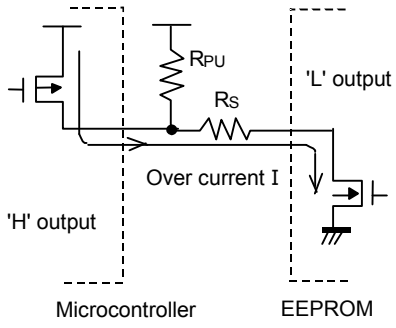


Fig.42 I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Example) When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300[\Omega]$$

●I²C BUS input / output circuit

○Input (WP,SCL)

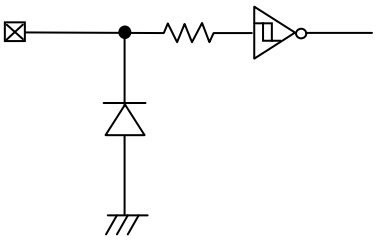


Fig.43 Input pin circuit diagram

○Input / output (SDA)

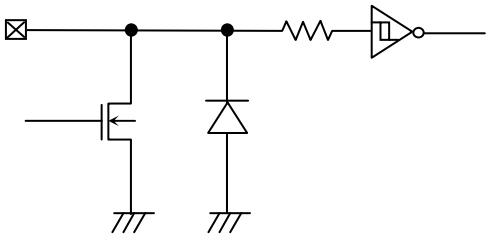


Fig.44 Input / output pin circuit diagram

●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and Vbot for operating POR circuit.

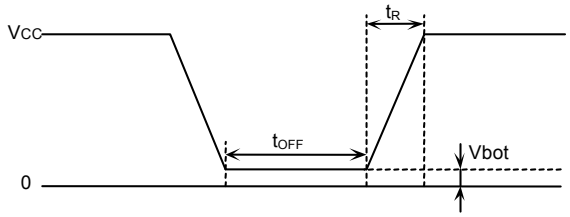


Fig.51 Rise waveform diagram

Recommended conditions of t_R, t_{OFF},Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or longer	0.3V or below
100ms or below	10ms or longer	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

a) In the case when the above condition 1 cannot be observed. When SDA becomes 'L' at power on .

→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

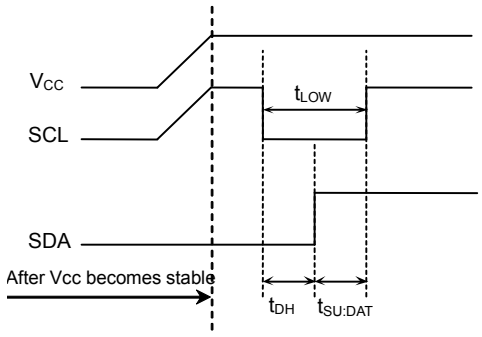


Fig.52 When SCL= 'H' and SDA= 'L'

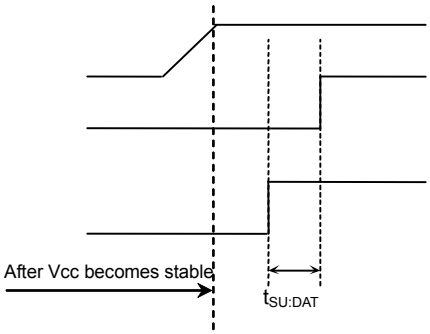


Fig.53 When SCL='L' and SDA='L'

b) In the case when the above condition 2 cannot be observed.

→After power source becomes stable, execute software reset(P11).

c) In the case when the above conditions 1 and 2 cannot be observed.

→Carry out a), and then carry out b).

●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●Vcc noise countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

●Notes for use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

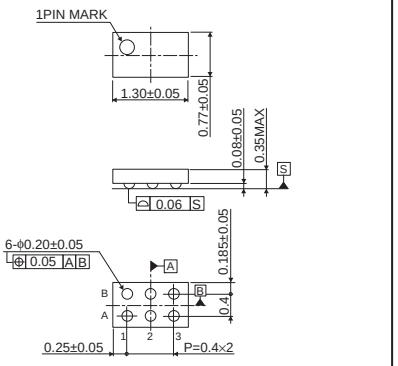
(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

●**Ordering part number**

B	R	C	A	0	1	6	G	W	Z	-	W	E	2

Part No.	Part No.	Package GWZ: UCSP30L1	W-Cell	Packaging and forming specification E2: Embossed tape and reel

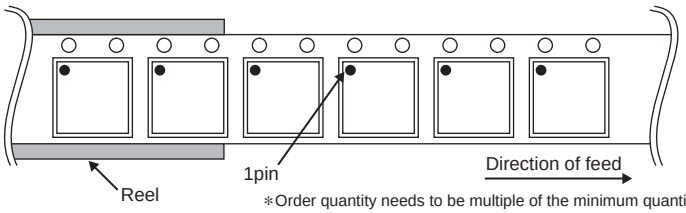
UCSP30L1(BRCA016GWZ-W)



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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