

# ADC1610S series

Single 16-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps;  
CMOS or LVDS DDR digital outputs

Rev. 3 — 25 January 2011

Product data sheet

## 1. General description

---

The ADC1610S is a single-channel 16-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1610S is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode, because of a separate digital output supply. It supports the Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC. The device also includes a programmable full-scale SPI to allow a flexible input voltage range from 1 V to 2 V (peak-to-peak). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1610S is ideal for use in communications, imaging and medical applications.

## 2. Features and benefits

---

- SNR, 72.5 dBFS; SFDR, 88 dBc
- Sample rate up to 125 Msps
- 16-bit pipelined ADC core
- Clock input divided by 2 for less jitter
- Single 3 V supply
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- CMOS or LVDS DDR digital outputs
- HVQFN40 package
- Input bandwidth, 600 MHz
- Power dissipation, 430 mW at 80 Msps
- Serial Peripheral Interface (SPI)
- Duty cycle stabilizer
- Fast Out-of-Range (OTR) detection
- Offset binary, two's complement, gray code
- Power-down and Sleep modes

## 3. Applications

---

- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems
- Software defined radio



### 4. Ordering information

Table 1. Ordering information

| Type number      | f <sub>s</sub> (Msps) | Package |  | Version  |
|------------------|-----------------------|---------|--|----------|
|                  |                       | Name    | Description  |          |
| ADC1610S125HN/C1 | 125                   | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-1 |
| ADC1610S105HN/C1 | 105                   | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-1 |
| ADC1610S080HN/C1 | 80                    | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-1 |
| ADC1610S065HN/C1 | 65                    | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm | SOT618-1 |

### 5. Block diagram

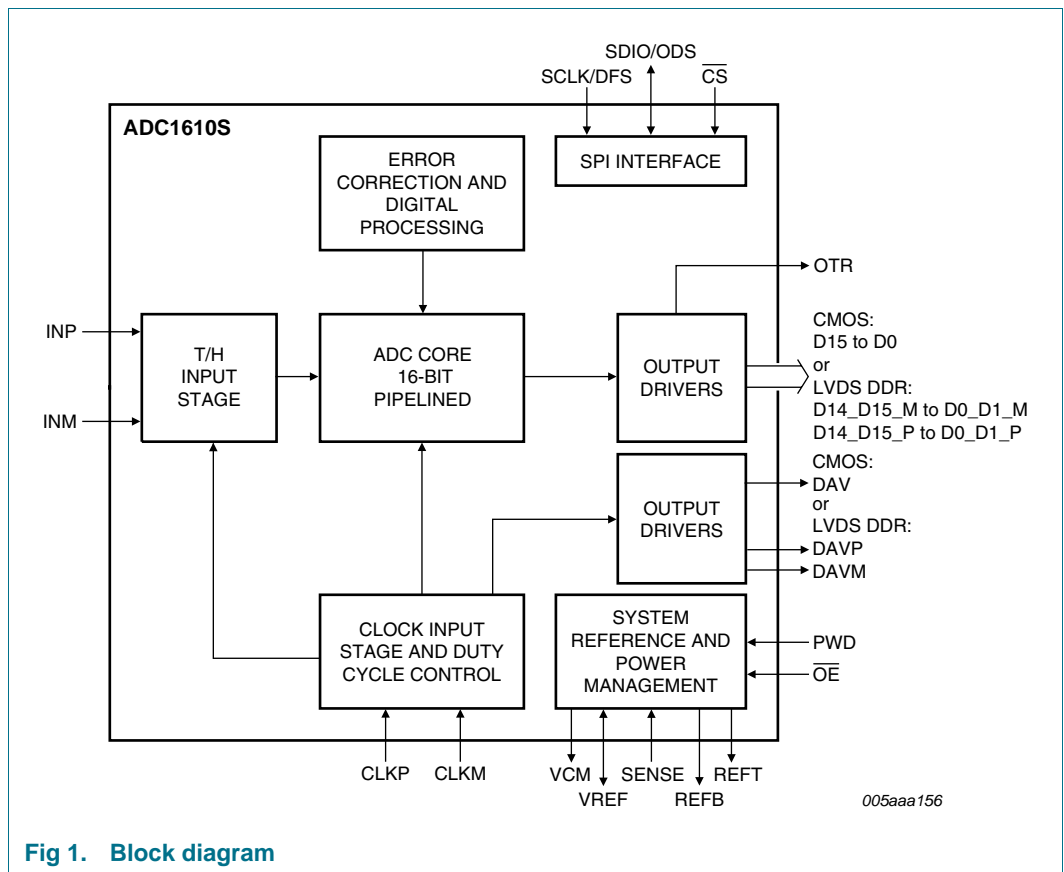


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

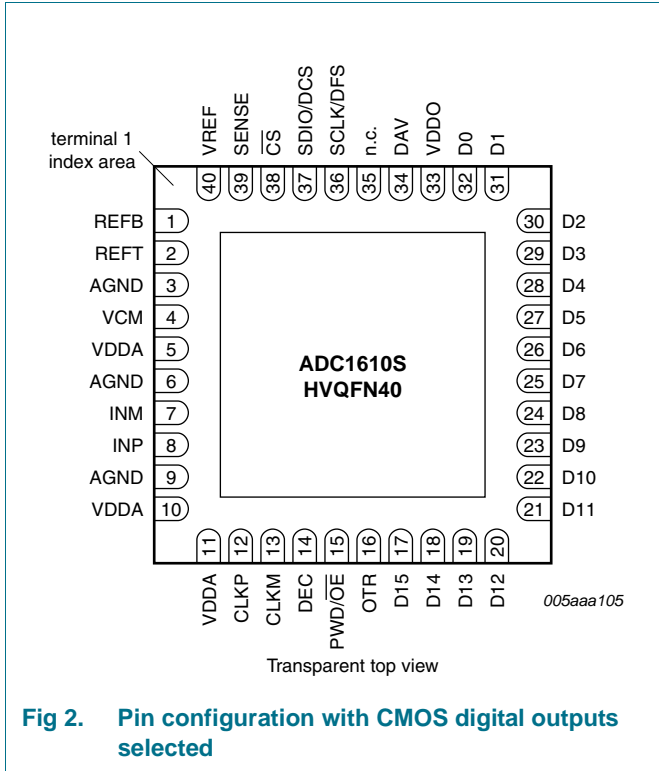


Fig 2. Pin configuration with CMOS digital outputs selected

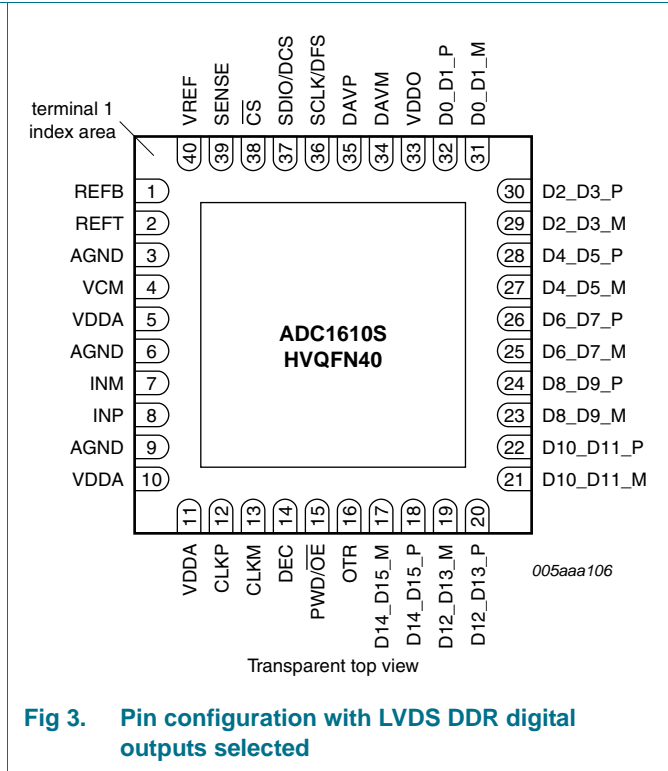


Fig 3. Pin configuration with LVDS DDR digital outputs selected

6.2 Pin description

Table 2. Pin description (CMOS digital outputs)

| Symbol | Pin | Type <sup>[1]</sup> | Description  |
|--------|-----|---------------------|--|
| REFB   | 1   | O                   | bottom reference                                   |
| REFT   | 2   | O                   | top reference                                      |
| AGND   | 3   | G                   | analog ground                                      |
| VCM    | 4   | O                   | common-mode output voltage                         |
| VDDA   | 5   | P                   | analog power supply                                |
| AGND   | 6   | G                   | analog ground                                      |
| INM    | 7   | I                   | complementary analog input                         |
| INP    | 8   | I                   | analog input                                       |
| AGND   | 9   | G                   | analog ground                                      |
| VDDA   | 10  | P                   | analog power supply                                |
| VDDA   | 11  | P                   | analog power supply                                |
| CLKP   | 12  | I                   | clock input  |
| CLKM   | 13  | I                   | complementary clock input                          |
| DEC    | 14  | O                   | regulator decoupling node                          |
| PWD/OE | 15  | I                   | power down, active HIGH; output enable, active LOW |
| OTR    | 16  | O                   | out of range                                       |

Table 2. Pin description (CMOS digital outputs) ...continued

| Symbol                 | Pin | Type <sup>[1]</sup> | Description                                     |
|------------------------|-----|---------------------|---|
| D15                    | 17  | O                   | data output bit 15 (Most Significant Bit (MSB)) |
| D14                    | 18  | O                   | data output bit 14                              |
| D13                    | 19  | O                   | data output bit 13                              |
| D12                    | 20  | O                   | data output bit 12                              |
| D11                    | 21  | O                   | data output bit 11                              |
| D10                    | 22  | O                   | data output bit 10                              |
| D9                     | 23  | O                   | data output bit 9                               |
| D8                     | 24  | O                   | data output bit 8                               |
| D7                     | 25  | O                   | data output bit 7                               |
| D6                     | 26  | O                   | data output bit 6                               |
| D5                     | 27  | O                   | data output bit 5                               |
| D4                     | 28  | O                   | data output bit 4                               |
| D3                     | 29  | O                   | data output bit 3                               |
| D2                     | 30  | O                   | data output bit 2                               |
| D1                     | 31  | O                   | data output bit 1                               |
| D0                     | 32  | O                   | data output bit 0 (Least Significant Bit (LSB)) |
| VDDO                   | 33  | P                   | output power supply                             |
| DAV                    | 34  | O                   | data valid output clock                         |
| n.c.                   | 35  | -                   | not connected                                   |
| SCLK/DFS               | 36  | I                   | SPI clock; data format select                   |
| SDIO/ODS               | 37  | I/O                 | SPI data IO; output data standard               |
| $\overline{\text{CS}}$ | 38  | I                   | SPI chip select                                 |
| SENSE                  | 39  | I                   | reference programming pin                       |
| VREF                   | 40  | I/O                 | voltage reference input/output                  |

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

**Table 3. Pin description (LVDS DDR) digital outputs)**

| Symbol    | Pin <sup>[1]</sup> | Type <sup>[2]</sup> | Description  |
|-----------|--------------------|---------------------|--|
| D14_D15_M | 17                 | O                   | differential output data D14 and D15 multiplexed, complement |
| D14_D15_P | 18                 | O                   | differential output data D14 and D15 multiplexed, true       |
| D12_D13_M | 19                 | O                   | differential output data D12 and D13 multiplexed, complement |
| D12_D13_P | 20                 | O                   | differential output data D12 and D13 multiplexed, true       |
| D10_D11_M | 21                 | O                   | differential output data D10 and D11 multiplexed, complement |
| D10_D11_P | 22                 | O                   | differential output data D10 and D11 multiplexed, true       |
| D8_D9_M   | 23                 | O                   | differential output data D8 and D9 multiplexed, complement   |
| D8_D9_P   | 24                 | O                   | differential output data D8 and D9 multiplexed, true         |
| D6_D7_M   | 25                 | O                   | differential output data D6 and D7 multiplexed, complement   |
| D6_D7_P   | 26                 | O                   | differential output data D6 and D7 multiplexed, true         |
| D4_D5_M   | 27                 | O                   | differential output data D4 and D5 multiplexed, complement   |
| D4_D5_P   | 28                 | O                   | differential output data D4 and D5 multiplexed, true         |
| D2_D3_M   | 29                 | O                   | differential output data D2 and D3 multiplexed, complement   |
| D2_D3_P   | 30                 | O                   | differential output data D2 and D3 multiplexed, true         |
| D0_D1_M   | 31                 | O                   | differential output data D0 and D1 multiplexed, complement   |
| D0_D1_P   | 32                 | O                   | differential output data D0 and D1 multiplexed, true         |
| DAVM      | 34                 | O                   | data valid output clock, complement                          |
| DAVP      | 35                 | O                   | data valid output clock, true                                |

[1] Pins 1 to 16 and pins 36 to 40 are the same for both CMOS and LVDS DDR outputs (see [Table 2](#)).

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol    | Parameter             | Conditions   | Min  | Max  | Unit |
|-----------|-----------------------|--|------|------|------|
| $V_O$     | output voltage        | pins D15 to D0;<br>pins D14_D15_P to D0_D1_P;<br>pins D14_D15_M to D0_D1_M | -0.4 | +3.9 | V    |
| $V_{DDA}$ | analog supply voltage |  | -0.4 | +3.9 | V    |
| $V_{DDO}$ | output supply voltage |  | -0.4 | +3.9 | V    |
| $T_{stg}$ | storage temperature   |  | -55  | +125 | °C   |
| $T_{amb}$ | ambient temperature   |  | -40  | +85  | °C   |
| $T_j$     | junction temperature  |  | -    | 125  | °C   |

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol        | Parameter                                   | Conditions | Typ  | Unit |
|---------------|---|------------|------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | [1]        | 22.5 | K/W  |
| $R_{th(j-c)}$ | thermal resistance from junction to case    | [1]        | 11.7 | K/W  |

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

## 9. Static characteristics

Table 6. Static characteristics<sup>[1]</sup>

| Symbol  | Parameter                        | Conditions   | Min                 | Typ                 | Max                 | Unit |
|---|----------------------------------|--|---------------------|---------------------|---------------------|------|
| <b>Supplies</b>   |                                  |  |                     |                     |                     |      |
| V <sub>DDA</sub>  | analog supply voltage            |  | 2.85                | 3.0                 | 3.4                 | V    |
| V <sub>DDO</sub>  | output supply voltage            | CMOS mode  | 1.65                | 1.8                 | 3.6                 | V    |
|   |                                  | LVDS DDR mode  | 2.85                | 3.0                 | 3.6                 | V    |
| I <sub>DDA</sub>  | analog supply current            | f <sub>clk</sub> = 125 Msps; f <sub>i</sub> = 70 MHz                   | -                   | 210                 | -                   | mA   |
| I <sub>DDO</sub>  | output supply current            | CMOS mode;<br>f <sub>clk</sub> = 125 Msps; f <sub>i</sub> = 70 MHz     | -                   | 14                  | -                   | mA   |
|   |                                  | LVDS DDR mode:<br>f <sub>clk</sub> = 125 Msps; f <sub>i</sub> = 70 MHz | -                   | 43                  | -                   | mA   |
| P   | power dissipation                | ADC1610S125;<br>analog supply only                                     | -                   | 630                 | -                   | mW   |
|   |                                  | ADC1610S105;<br>analog supply only                                     | -                   | 550                 | -                   | mW   |
|   |                                  | ADC1610S080;<br>analog supply only                                     | -                   | 430                 | -                   | mW   |
|   |                                  | ADC1610S065;<br>analog supply only                                     | -                   | 380                 | -                   | mW   |
|   |                                  | Power-down mode  | -                   | 2                   | -                   | mW   |
|   |                                  | Sleep mode   | -                   | 40                  | -                   | mW   |
| <b>Clock inputs: pins CLKP and CLKM</b>                             |                                  |  |                     |                     |                     |      |
| <b>Low-Voltage Positive Emitter-Coupled Logic (LVPECL)</b>          |                                  |  |                     |                     |                     |      |
| V <sub>i(clk)dif</sub>  | differential clock input voltage | peak-to-peak   | -                   | 1.6                 | -                   | V    |
| <b>SINE</b>   |                                  |  |                     |                     |                     |      |
| V <sub>i(clk)dif</sub>  | differential clock input voltage | peak   | -                   | ±3.0                | -                   | V    |
| <b>Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)</b> |                                  |  |                     |                     |                     |      |
| V <sub>IL</sub>   | LOW-level input voltage          |  | -                   | -                   | 0.3V <sub>DDA</sub> | V    |
| V <sub>IH</sub>   | HIGH-level input voltage         |  | 0.7V <sub>DDA</sub> | -                   | -                   | V    |
| <b>Logic inputs, Power-down: pin PWD/OE</b>                         |                                  |  |                     |                     |                     |      |
| V <sub>IL</sub>   | LOW-level input voltage          |  | -                   | 0                   | -                   | V    |
|   |                                  | LOW-medium level   | -                   | 0.3V <sub>DDA</sub> | -                   | V    |
|   |                                  | Medium-HIGH level  | -                   | 0.6V <sub>DDA</sub> | -                   | V    |
| V <sub>IH</sub>   | HIGH-level input voltage         |  | -                   | V <sub>DDA</sub>    | -                   | V    |
| I <sub>IL</sub>   | LOW-level input current          |  | -                   | 55                  | -                   | μA   |
| I <sub>IH</sub>   | HIGH-level input current         |  | -                   | 65                  | -                   | μA   |
| <b>Serial peripheral interface: pins CS, SDIO/ODS, SCLK/DFS</b>     |                                  |  |                     |                     |                     |      |
| V <sub>IL</sub>   | LOW-level input voltage          |  | 0                   | -                   | 0.3V <sub>DDA</sub> | V    |
| V <sub>IH</sub>   | HIGH-level input voltage         |  | 0.7V <sub>DDA</sub> | -                   | V <sub>DDA</sub>    | V    |
| I <sub>IL</sub>   | LOW-level input current          |  | -10                 | -                   | +10                 | μA   |
| I <sub>IH</sub>   | HIGH-level input current         |  | -50                 | -                   | +50                 | μA   |
| C <sub>i</sub>  | input capacitance                |  | -                   | 4                   | -                   | pF   |

Table 6. Static characteristics<sup>[1]</sup> ...continued

| Symbol  | Parameter                      | Conditions                                    | Min          | Typ           | Max          | Unit          |
|---|--------------------------------|---|--------------|---------------|--------------|---------------|
| <b>Digital outputs, CMOS mode: pins D15 to D0, OTR, DAV</b>                                       |                                |   |              |               |              |               |
| Output levels, $V_{DDO} = 3\text{ V}$   |                                |   |              |               |              |               |
| $V_{OL}$  | LOW-level output voltage       |   | OGND         | -             | $0.2V_{DDO}$ | V             |
| $V_{OH}$  | HIGH-level output voltage      |   | $0.8V_{DDO}$ | -             | $V_{DDO}$    | V             |
| $C_O$   | output capacitance             | high impedance; $\overline{OE} = \text{HIGH}$ | -            | 3             | -            | pF            |
| Output levels, $V_{DDO} = 1.8\text{ V}$   |                                |   |              |               |              |               |
| $V_{OL}$  | LOW-level output voltage       |   | OGND         | -             | $0.2V_{DDO}$ | V             |
| $V_{OH}$  | HIGH-level output voltage      |   | $0.8V_{DDO}$ | -             | $V_{DDO}$    | V             |
| <b>Digital outputs, LVDS mode: pins D14_D15_P to D0_D1_P, D14_D15_M to D0_D1_M, DAVP and DAVM</b> |                                |   |              |               |              |               |
| Output levels, $V_{DDO} = 3\text{ V}$ only, $R_L = 100\ \Omega$                                   |                                |   |              |               |              |               |
| $V_{O(\text{offset})}$  | output offset voltage          | output buffer current set to 3.5 mA           | -            | 1.2           | -            | V             |
| $V_{O(\text{dif})}$   | differential output voltage    | output buffer current set to 3.5 mA           | -            | 350           | -            | mV            |
| $C_O$   | output capacitance             |   | -            | 3             | -            | pF            |
| <b>Analog inputs: pins INP and INM</b>  |                                |   |              |               |              |               |
| $I_I$   | input current                  |   | -5           | -             | +5           | $\mu\text{A}$ |
| $R_{i(\text{dif})}$   | differential input resistance  |   | -            | 19.8          | -            | k $\Omega$    |
| $C_{i(\text{dif})}$   | differential input capacitance |   | -            | 2.8           | -            | pF            |
| $V_{I(\text{cm})}$  | common-mode input voltage      | $V_{INP} = V_{INM}$                           | 1.1          | 1.5           | 2.5          | V             |
| $B_i$   | input bandwidth                |   | -            | 650           | -            | MHz           |
| $V_{I(\text{dif})}$   | differential input voltage     | peak-to-peak                                  | 1            | -             | 2            | V             |
| <b>Common-mode output voltage: pin VCM</b>  |                                |   |              |               |              |               |
| $V_{O(\text{cm})}$  | common-mode output voltage     |   | -            | $V_{DDA} / 2$ | -            | V             |
| $I_{O(\text{cm})}$  | common-mode output current     |   | -            | 4             | -            | mA            |
| <b>I/O reference voltage: pin VREF</b>  |                                |   |              |               |              |               |
| $V_{VREF}$  | voltage on pin VREF            | output  | 0.5          | -             | 1            | V             |
|   |                                | input   | 0.5          | -             | 1            | V             |
| <b>Accuracy</b>   |                                |   |              |               |              |               |
| INL   | integral non-linearity         |   | -            | $\pm 4$       | -            | LSB           |
| DNL   | differential non-linearity     | guaranteed no missing codes                   | -0.95        | $\pm 0.5$     | +0.95        | LSB           |
| $E_{\text{offset}}$   | offset error                   |   | -            | $\pm 2$       | -            | mV            |
| $E_G$   | gain error                     | full-scale                                    | -            | $\pm 0.5$     | -            | %             |

Table 6. Static characteristics<sup>[1]</sup> ...continued

| Symbol        | Parameter                    | Conditions                             | Min | Typ | Max | Unit |
|---------------|------------------------------|--|-----|-----|-----|------|
| <b>Supply</b> |                              |  |     |     |     |      |
| PSRR          | power supply rejection ratio | 200 mV (p-p) on $V_{DDA}$ ; $f_i = DC$ | -   | -54 | -   | dB   |

[1] Typical values measured at  $V_{DDA} = 3 V$ ,  $V_{DDO} = 1.8 V$ ,  $T_{amb} = 25 ^\circ C$  and  $C_L = 5 pF$ ; minimum and maximum values are across the full temperature range  $T_{amb} = -40 ^\circ C$  to  $+85 ^\circ C$  at  $V_{DDA} = 3 V$ ,  $V_{DDO} = 1.8 V$ ;  $V_{INP} - V_{INM} = -1 dBFS$ ; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.



## 10. Dynamic characteristics

### 10.1 Dynamic characteristics

Table 7. Dynamic characteristics

| Symbol                          | Parameter                   | Conditions      | ADC1610S065 |      |     | ADC1610S080 |      |     | ADC1610S105 |      |     | ADC1610S125 |      |     | Unit |
|---------------------------------|-----------------------------|-----------------|-------------|------|-----|-------------|------|-----|-------------|------|-----|-------------|------|-----|------|
|                                 |                             |                 | Min         | Typ  | Max | Min         | Typ  | Max | Min         | Typ  | Max | Min         | Typ  | Max |      |
| <b>Analog signal processing</b> |                             |                 |             |      |     |             |      |     |             |      |     |             |      |     |      |
| $\alpha_{2H}$                   | second harmonic level       | $f_i = 3$ MHz   | -           | 89   | -   | -           | 89   | -   | -           | 88   | -   | -           | 90   | -   | dBc  |
|                                 |                             | $f_i = 30$ MHz  | -           | 88   | -   | -           | 88   | -   | -           | 88   | -   | -           | 89   | -   | dBc  |
|                                 |                             | $f_i = 70$ MHz  | -           | 87   | -   | -           | 87   | -   | -           | 86   | -   | -           | 87   | -   | dBc  |
|                                 |                             | $f_i = 170$ MHz | -           | 84   | -   | -           | 84   | -   | -           | 83   | -   | -           | 85   | -   | dBc  |
| $\alpha_{3H}$                   | third harmonic level        | $f_i = 3$ MHz   | -           | 88   | -   | -           | 88   | -   | -           | 87   | -   | -           | 89   | -   | dBc  |
|                                 |                             | $f_i = 30$ MHz  | -           | 87   | -   | -           | 87   | -   | -           | 87   | -   | -           | 88   | -   | dBc  |
|                                 |                             | $f_i = 70$ MHz  | -           | 86   | -   | -           | 86   | -   | -           | 85   | -   | -           | 86   | -   | dBc  |
|                                 |                             | $f_i = 170$ MHz | -           | 83   | -   | -           | 83   | -   | -           | 82   | -   | -           | 84   | -   | dBc  |
| THD                             | total harmonic distortion   | $f_i = 3$ MHz   | -           | 85   | -   | -           | 85   | -   | -           | 84   | -   | -           | 86   | -   | dBc  |
|                                 |                             | $f_i = 30$ MHz  | -           | 84   | -   | -           | 84   | -   | -           | 84   | -   | -           | 85   | -   | dBc  |
|                                 |                             | $f_i = 70$ MHz  | -           | 83   | -   | -           | 83   | -   | -           | 82   | -   | -           | 83   | -   | dBc  |
|                                 |                             | $f_i = 170$ MHz | -           | 80   | -   | -           | 80   | -   | -           | 79   | -   | -           | 81   | -   | dBc  |
| ENOB                            | effective number of bits    | $f_i = 3$ MHz   | -           | 11.7 | -   | -           | 11.7 | -   | -           | 11.7 | -   | -           | 11.6 | -   | bits |
|                                 |                             | $f_i = 30$ MHz  | -           | 11.6 | -   | -           | 11.6 | -   | -           | 11.6 | -   | -           | 11.6 | -   | bits |
|                                 |                             | $f_i = 70$ MHz  | -           | 11.5 | -   | -           | 11.5 | -   | -           | 11.5 | -   | -           | 11.5 | -   | bits |
|                                 |                             | $f_i = 170$ MHz | -           | 11.4 | -   | -           | 11.4 | -   | -           | 11.4 | -   | -           | 11.4 | -   | bits |
| SNR                             | signal-to-noise ratio       | $f_i = 3$ MHz   | -           | 72.3 | -   | -           | 72.2 | -   | -           | 72.0 | -   | -           | 71.6 | -   | dBFS |
|                                 |                             | $f_i = 30$ MHz  | -           | 71.5 | -   | -           | 71.4 | -   | -           | 71.4 | -   | -           | 71.3 | -   | dBFS |
|                                 |                             | $f_i = 70$ MHz  | -           | 70.9 | -   | -           | 70.9 | -   | -           | 70.8 | -   | -           | 70.7 | -   | dBFS |
|                                 |                             | $f_i = 170$ MHz | -           | 70.4 | -   | -           | 70.3 | -   | -           | 70.2 | -   | -           | 70.1 | -   | dBFS |
| SFDR                            | spurious-free dynamic range | $f_i = 3$ MHz   | -           | 88   | -   | -           | 88   | -   | -           | 87   | -   | -           | 89   | -   | dBc  |
|                                 |                             | $f_i = 30$ MHz  | -           | 87   | -   | -           | 87   | -   | -           | 87   | -   | -           | 88   | -   | dBc  |
|                                 |                             | $f_i = 70$ MHz  | -           | 86   | -   | -           | 86   | -   | -           | 85   | -   | -           | 86   | -   | dBc  |
|                                 |                             | $f_i = 170$ MHz | -           | 83   | -   | -           | 83   | -   | -           | 82   | -   | -           | 84   | -   | dBc  |

**Table 7. Dynamic characteristics ...continued**

| Symbol | Parameter                  | Conditions              | ADC1610S065 |     |     | ADC1610S080 |     |     | ADC1610S105 |     |     | ADC1610S125 |     |     | Unit |
|--------|----------------------------|-------------------------|-------------|-----|-----|-------------|-----|-----|-------------|-----|-----|-------------|-----|-----|------|
|        |                            |                         | Min         | Typ | Max | Min         | Typ | Max | Min         | Typ | Max | Min         | Typ | Max |      |
| IMD    | intermodulation distortion | $f_i = 3 \text{ MHz}$   | -           | 89  | -   | -           | 89  | -   | -           | 88  | -   | -           | 89  | -   | dBc  |
|        |                            | $f_i = 30 \text{ MHz}$  | -           | 88  | -   | -           | 88  | -   | -           | 88  | -   | -           | 88  | -   | dBc  |
|        |                            | $f_i = 70 \text{ MHz}$  | -           | 87  | -   | -           | 87  | -   | -           | 86  | -   | -           | 86  | -   | dBc  |
|        |                            | $f_i = 170 \text{ MHz}$ | -           | 84  | -   | -           | 85  | -   | -           | 83  | -   | -           | 84  | -   | dBc  |

[1] Typical values measured at  $V_{DDA} = 3 \text{ V}$ ,  $V_{DDO} = 1.8 \text{ V}$ ,  $T_{amb} = 25 \text{ }^\circ\text{C}$  and  $C_L = 5 \text{ pF}$ ; minimum and maximum values are across the full temperature range  $T_{amb} = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$  at  $V_{DDA} = 3 \text{ V}$ ,  $V_{DDO} = 1.8 \text{ V}$ ;  $V_{INP} - V_{INM} = -1 \text{ dBFS}$ ; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

## 10.2 Clock and digital output timing

**Table 8. Clock and digital output timing characteristics<sup>[1]</sup>**

| Symbol | Parameter | Conditions | ADC1610S065 |     |     | ADC1610S080 |     |     | ADC1610S105 |     |     | ADC1610S125 |     |     | Unit |
|--------|-----------|------------|-------------|-----|-----|-------------|-----|-----|-------------|-----|-----|-------------|-----|-----|------|
|        |           |            | Min         | Typ | Max | Min         | Typ | Max | Min         | Typ | Max | Min         | Typ | Max |      |

### Clock timing input: pins CLKP and CLKM

|                 |                     |                  |    |      |    |    |      |    |    |      |     |     |      |     |               |
|-----------------|---------------------|------------------|----|------|----|----|------|----|----|------|-----|-----|------|-----|---------------|
| $f_{clk}$       | clock frequency     |                  | 40 | -    | 65 | 60 | -    | 80 | 75 | -    | 105 | 100 | -    | 125 | MHz           |
| $t_{lat(data)}$ | data latency time   |                  | -  | 13.5 | -  | -  | 13.5 | -  | -  | 13.5 | -   | -   | 13.5 | -   | clock cycles  |
| $\delta_{clk}$  | clock duty cycle    | DCS_EN = logic 1 | 30 | 50   | 70 | 30 | 50   | 70 | 30 | 50   | 70  | 30  | 50   | 70  | %             |
|                 |                     | DCS_EN = logic 0 | 45 | 50   | 55 | 45 | 50   | 55 | 45 | 50   | 55  | 45  | 50   | 55  | %             |
| $t_{d(s)}$      | sampling delay time |                  | -  | 0.8  | -  | -  | 0.8  | -  | -  | 0.8  | -   | -   | 0.8  | -   | ns            |
| $t_{wake}$      | wake-up time        |                  | -  | 76   | -  | -  | 76   | -  | -  | 76   | -   | -   | 76   | -   | $\mu\text{s}$ |

### CMOS Mode timing output: pins D15 to D0 and DAV

|          |                   |      |                        |      |      |      |      |      |      |      |      |      |     |      |    |
|----------|-------------------|------|------------------------|------|------|------|------|------|------|------|------|------|-----|------|----|
| $t_{pD}$ | propagation delay | DATA | 13.6                   | 14.9 | 16.4 | 11.9 | 12.9 | 14.4 | 8.0  | 10.8 | 12.4 | 8.2  | 9.7 | 11.3 | ns |
|          |                   | DAV  | -                      | 4.2  | -    | -    | 3.6  | -    | -    | 3.3  | -    | -    | 3.4 | -    | ns |
| $t_{su}$ | set-up time       |      | -                      | 12.5 | -    | -    | 9.8  | -    | -    | 6.8  | -    | -    | 5.6 | -    | ns |
| $t_h$    | hold time         |      | -                      | 3.4  | -    | -    | 3.3  | -    | -    | 3.1  | -    | -    | 2.8 | -    | ns |
| $t_r$    | rise time         | DATA | <a href="#">2</a> 0.39 | -    | 2.4  | 0.39 | -    | 2.4  | 0.39 | -    | 2.4  | 0.39 | -   | 2.4  | ns |
|          |                   | DAV  | 0.26                   | -    | 2.4  | 0.26 | -    | 2.4  | 0.26 | -    | 2.4  | 0.26 | -   | 2.4  | ns |
| $t_f$    | fall time         | DATA | <a href="#">2</a> 0.19 | -    | 2.4  | 0.19 | -    | 2.4  | 0.19 | -    | 2.4  | 0.19 | -   | 2.4  | ns |

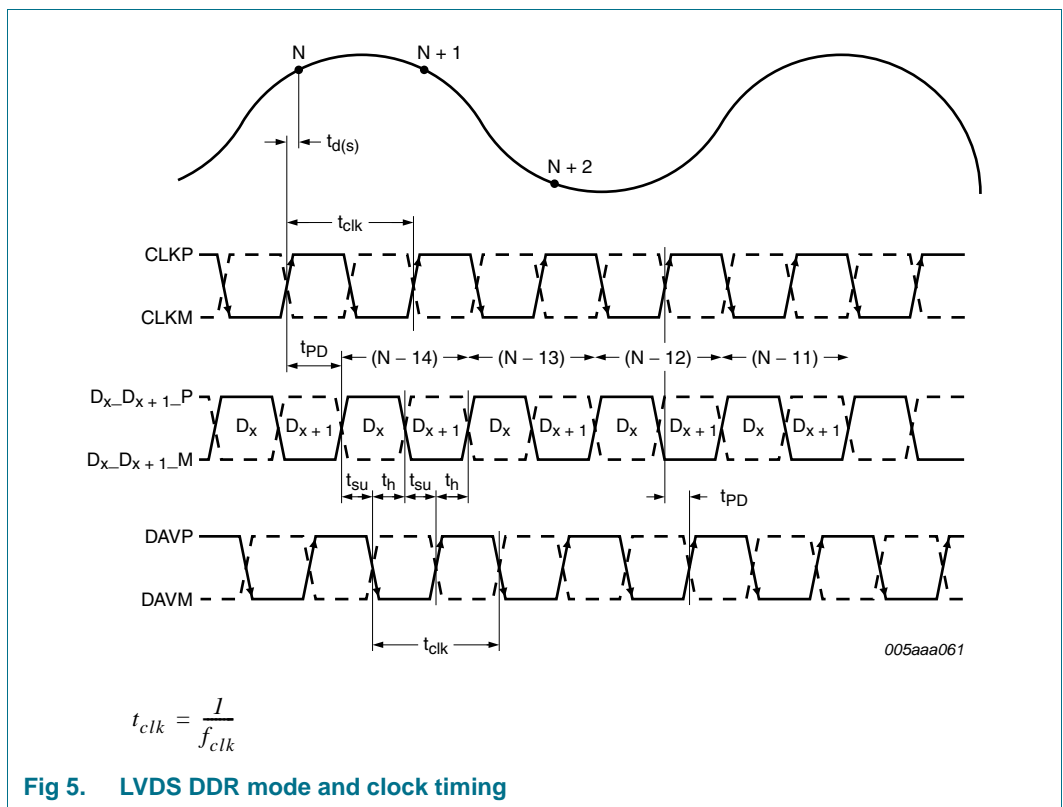
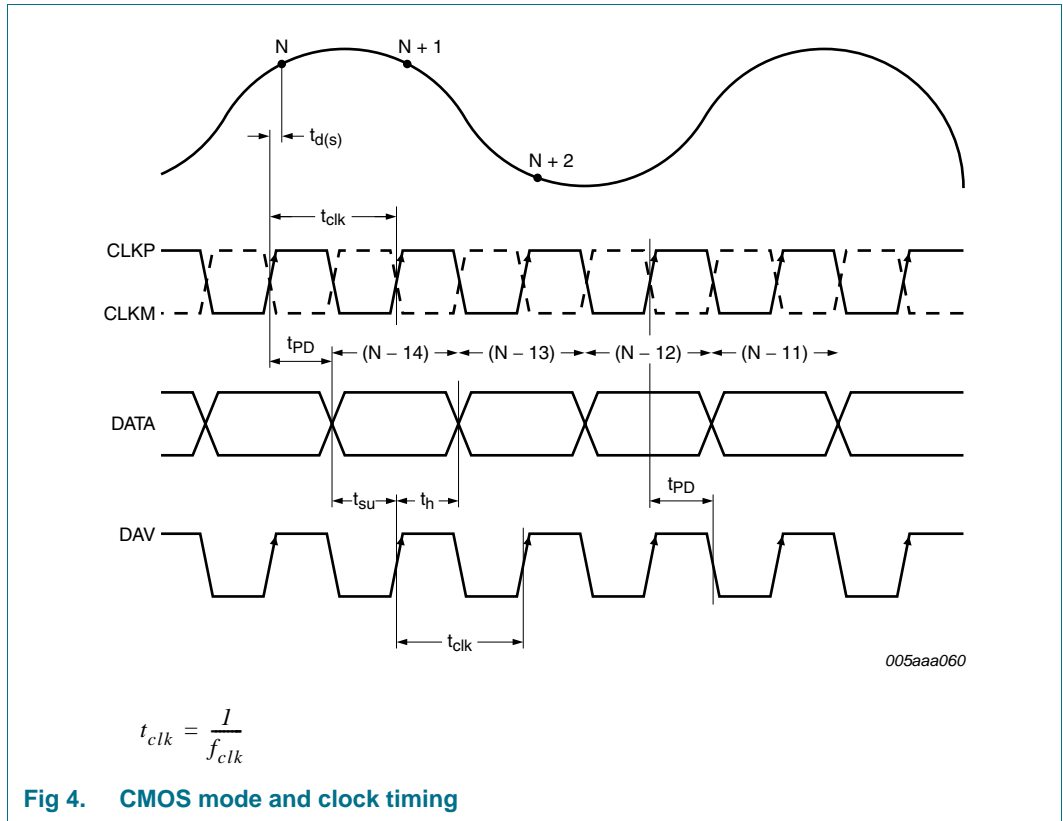
Table 8. Clock and digital output timing characteristics<sup>[1]</sup> ...continued

| Symbol  | Parameter         | Conditions | ADC1610S065         |     |     | ADC1610S080 |     |     | ADC1610S105 |     |     | ADC1610S125 |     |     | Unit |
|---|-------------------|------------|---------------------|-----|-----|-------------|-----|-----|-------------|-----|-----|-------------|-----|-----|------|
|   |                   |            | Min                 | Typ | Max | Min         | Typ | Max | Min         | Typ | Max | Min         | Typ | Max |      |
| LVDS DDR mode timing output: pins D14_D15_P to D0_D1_P, D14_D15_M to D0_D1_M, DAVP and DAVM |                   |            |                     |     |     |             |     |     |             |     |     |             |     |     |      |
| t <sub>PD</sub>   | propagation delay | DATA       | 3.3                 | 5.1 | 7.6 | 2.9         | 4.6 | 7.1 | 2.5         | 4.2 | 6.8 | 2.2         | 4.0 | 6.6 | ns   |
|   |                   | DAV        | -                   | 2.8 | -   | -           | 2.5 | -   | -           | 2.3 | -   | -           | 2.2 | -   | ns   |
| t <sub>su</sub>   | set-up time       |            | -                   | 5.4 | -   | -           | 4.1 | -   | -           | 2.6 | -   | -           | 1.9 | -   | ns   |
| t <sub>h</sub>  | hold time         |            | -                   | 2.2 | -   | -           | 2.0 | -   | -           | 1.8 | -   | -           | 1.7 | -   | ns   |
| t <sub>r</sub>  | rise time         | DATA       | <sup>[3]</sup> 0.5  | -   | 5   | 0.5         | -   | 5   | 0.5         | -   | 5   | 0.5         | -   | 5   | ns   |
|   |                   | DAV        | 0.18                | -   | 2.4 | 0.18        | -   | 2.4 | 0.18        | -   | 2.4 | 0.18        | -   | 2.4 | ns   |
| t <sub>f</sub>  | fall time         | DATA       | <sup>[3]</sup> 0.15 | -   | 1.6 | 0.15        | -   | 1.6 | 0.15        | -   | 1.6 | 0.15        | -   | 1.6 | ns   |

[1] Typical values measured at V<sub>DDA</sub> = 3 V, V<sub>DDO</sub> = 1.8 V, T<sub>amb</sub> = 25 °C and C<sub>L</sub> = 5 pF; minimum and maximum values are across the full temperature range T<sub>amb</sub> = -40 °C to +85 °C at V<sub>DDA</sub> = 3 V, V<sub>DDO</sub> = 1.8 V; V<sub>INP</sub> - V<sub>INM</sub> = -1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

[2] Measured between 20 % to 80 % of V<sub>DDO</sub>.

[3] Rise time measured from -50 mV to +50 mV; fall time measured from +50 mV to -50 mV.



10.3 SPI timings

Table 9. SPI timings characteristics<sup>[1]</sup>

| Symbol         | Parameter               | Conditions                   | Min | Typ | Max | Unit |
|----------------|-------------------------|------------------------------|-----|-----|-----|------|
| $t_{w(SCLK)}$  | SCLK pulse width        |                              | -   | 40  | -   | ns   |
| $t_{w(SCLKH)}$ | SCLK HIGH pulse width   |                              | -   | 16  | -   | ns   |
| $t_{w(SCLKL)}$ | SCLK LOW pulse width    |                              | -   | 16  | -   | ns   |
| $t_{su}$       | set-up time             | data to SCLK HIGH            | -   | 5   | -   | ns   |
|                |                         | $\overline{CS}$ to SCLK HIGH | -   | 5   | -   | ns   |
| $t_h$          | hold time               | data to SCLK HIGH            | -   | 2   | -   | ns   |
|                |                         | $\overline{CS}$ to SCLK HIGH | -   | 2   | -   | ns   |
| $f_{clk(max)}$ | maximum clock frequency |                              | -   | 25  | -   | MHz  |

[1] Typical values measured at  $V_{DDA} = 3\text{ V}$ ,  $V_{DDO} = 1.8\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$  and  $C_L = 5\text{ pF}$ ; minimum and maximum values are across the full temperature range  $T_{amb} = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  at  $V_{DDA} = 3\text{ V}$ ,  $V_{DDO} = 1.8\text{ V}$ .

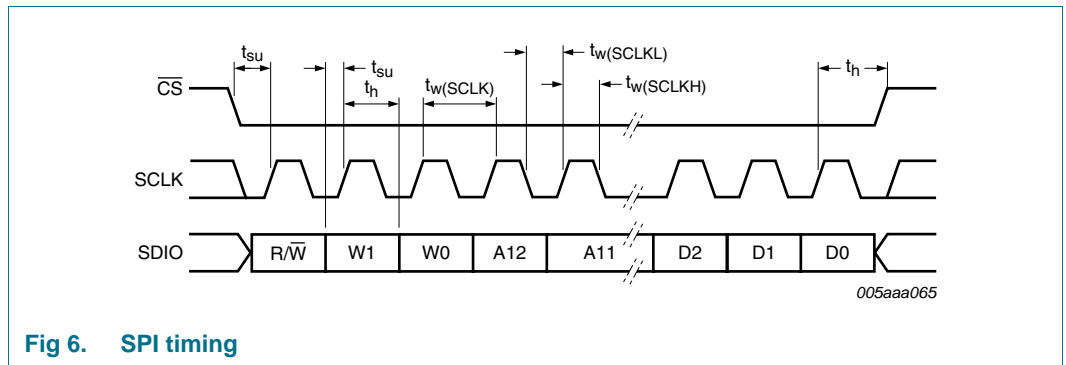


Fig 6. SPI timing

10.4 Typical characteristics

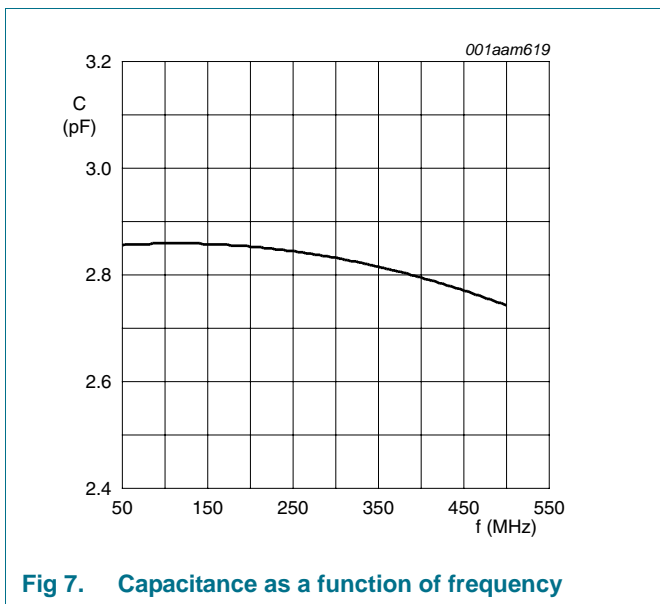


Fig 7. Capacitance as a function of frequency

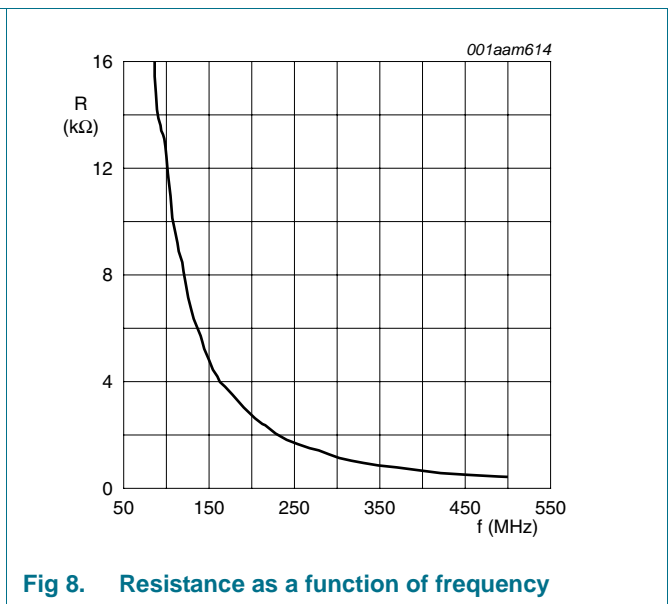
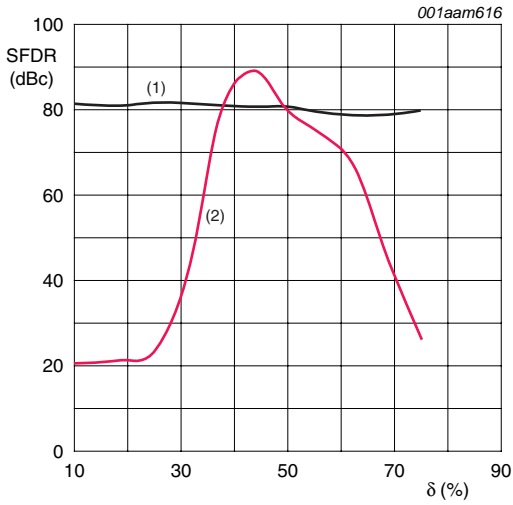
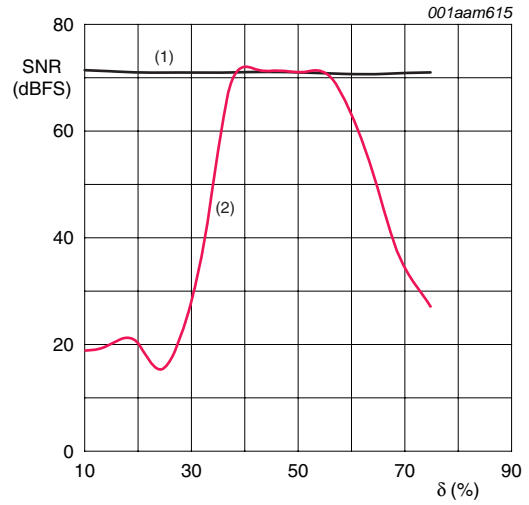


Fig 8. Resistance as a function of frequency



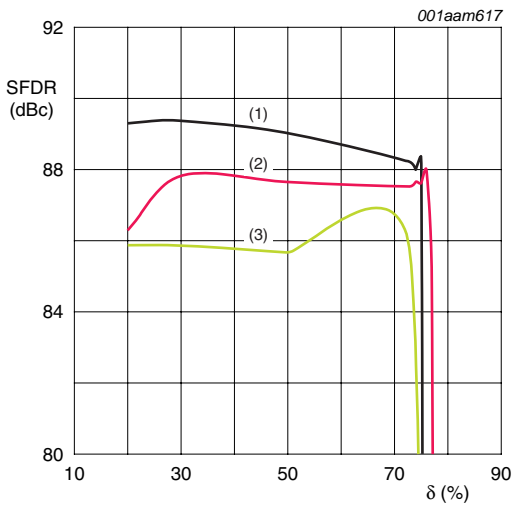
$T = 25\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 3\text{ V}$ ;  $f_i = 170\text{ MHz}$ ;  $f_s = 125\text{ Mpsps}$ .  
 (1) DCS on.  
 (2) DCS off.

Fig 9. SFDR as a function of duty cycle ( $\delta$ )



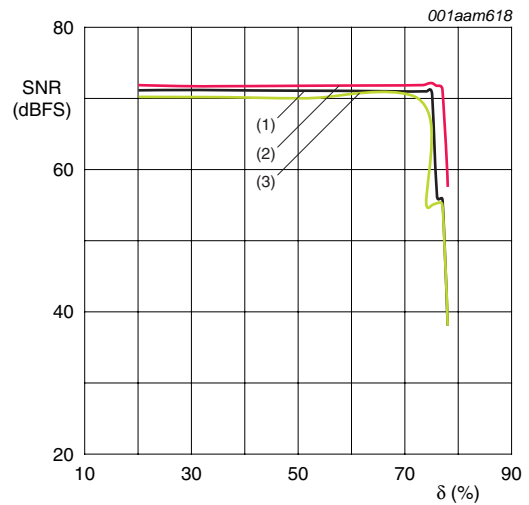
$T = 25\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 3\text{ V}$ ;  $f_i = 170\text{ MHz}$ ;  $f_s = 125\text{ Mpsps}$ .  
 (1) DCS on.  
 (2) DCS off.

Fig 10. SNR as a function of duty cycle ( $\delta$ )



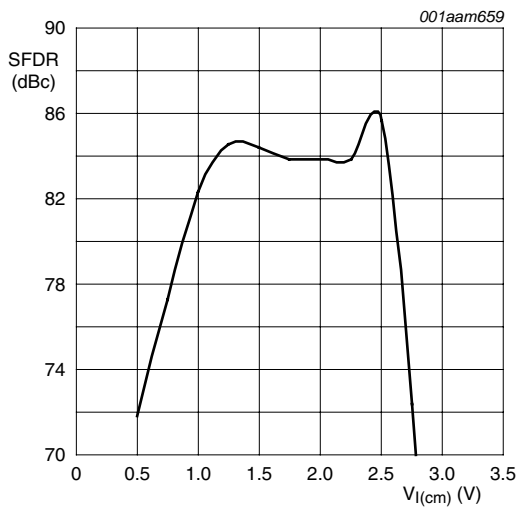
(1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$ /typical supply voltages.  
 (2)  $T_{amb} = +25\text{ }^{\circ}\text{C}$ /typical supply voltages.  
 (3)  $T_{amb} = +90\text{ }^{\circ}\text{C}$ /typical supply voltages.

Fig 11. SFDR as a function of duty cycle ( $\delta$ )

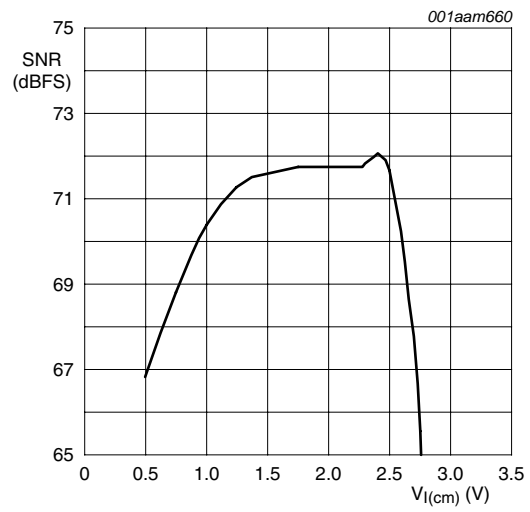


(1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$ /typical supply voltages.  
 (2)  $T_{amb} = +25\text{ }^{\circ}\text{C}$ /typical supply voltages.  
 (3)  $T_{amb} = +90\text{ }^{\circ}\text{C}$ /typical supply voltages.

Fig 12. SNR as a function of duty cycle ( $\delta$ )



**Fig 13. SFDR as a function of common-mode input voltage ( $V_{I(cm)}$ )**



**Fig 14. SNR as a function of common-mode input voltage ( $V_{I(cm)}$ )**

## 11. Application information

### 11.1 Device control

The ADC1610S can be controlled via SPI or directly via the I/O pins (Pin control mode).

#### 11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up, and remains in this mode as long as pin  $\overline{CS}$  is held HIGH. In Pin control mode, the SPI pins SDIO,  $\overline{CS}$  and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin  $\overline{CS}$  LOW. Once SPI control mode has been enabled, the device remains in this mode. The transition from Pin control mode to SPI control mode is illustrated in [Figure 15](#).

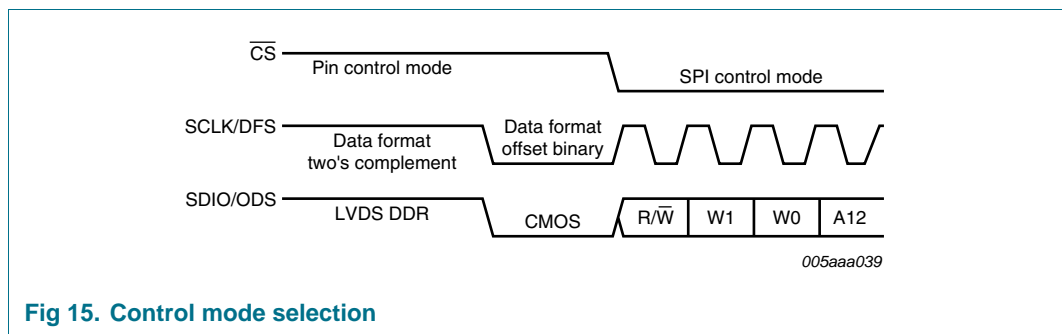


Fig 15. Control mode selection

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO when a transition is triggered by a falling edge on pin  $\overline{CS}$ .

#### 11.1.2 Operating mode selection

The active ADC1610S operating mode (Power-up, Power-down or Sleep) can be selected using bits OP\_MODE[1:0] of the Reset and operating mode register (see [Table 20](#)) or using pins PWD and  $\overline{OE}$  in Pin control mode, as described in [Table 10](#).

Table 10. Operating mode selection pin PWD/ $\overline{OE}$

| Pin PWD/ $\overline{OE}$ | Power mode | Output high-Z |
|--------------------------|------------|---------------|
| GND                      | Power-down | yes           |
| 1/3 V <sub>DDA</sub>     | Sleep      | yes           |
| 2/3 V <sub>DDA</sub>     | Power-up   | yes           |
| V <sub>DDA</sub>         | Power-up   | no            |

#### 11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see [Table 23](#)) or using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.



11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two’s complement or gray code; see [Table 23](#)) or using pin DFS in Pin control mode (offset binary or two’s complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two’s complement is selected.

11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1610S supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ( $V_{I(cm)}$ ) on pins INP and INM set to  $0.5V_{DDA}$ .

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see [Section 11.3](#) and [Table 22](#)).

The equivalent circuit of the sample and hold input stage, including Electrostatic Discharge (ESD) protection and circuit and package parasitics, is shown in [Figure 16](#).

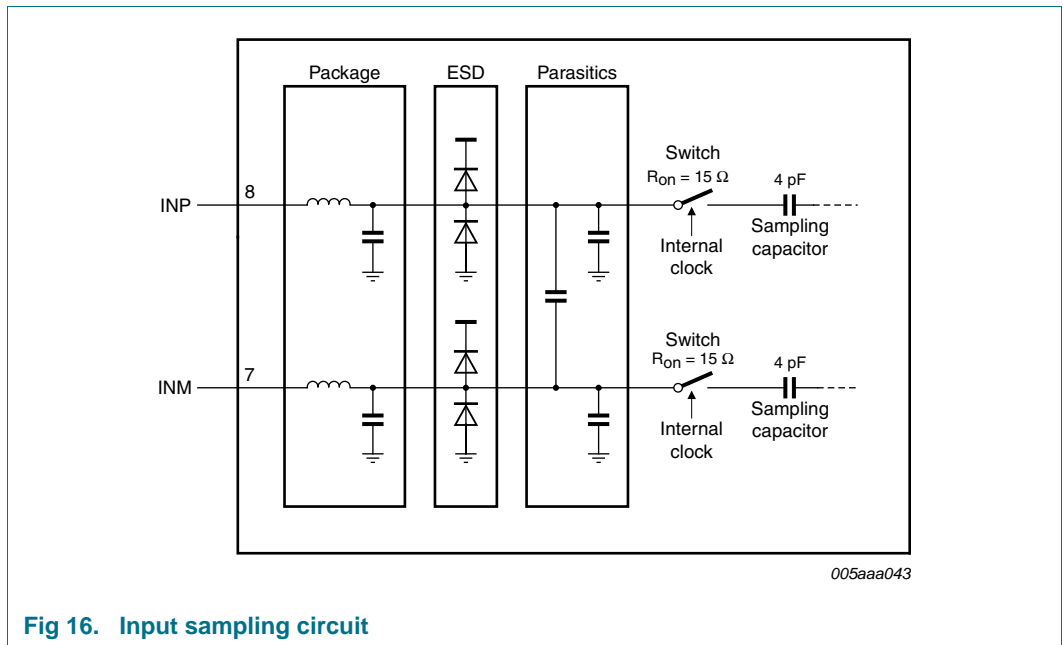


Fig 16. Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.2.2 Anti-kickback circuitry

Anti-kickback circuitry (R-C filter in [Figure 17](#)) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

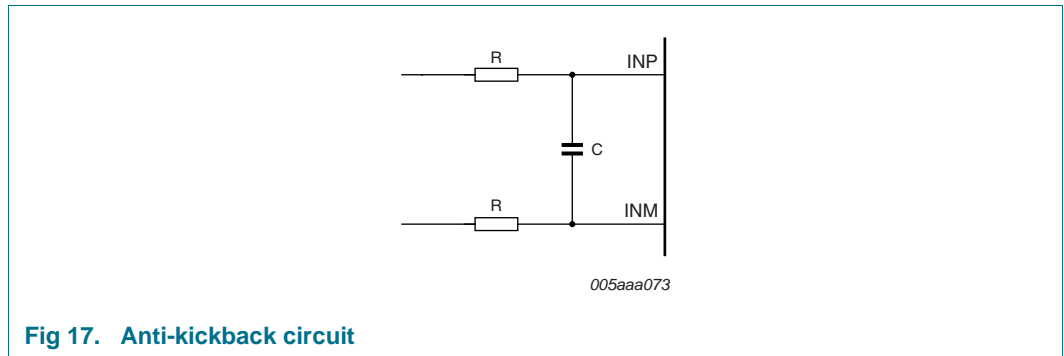


Fig 17. Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 11. RC coupling versus input frequency, typical values

| Input frequency (MHz) | Resistance ( $\Omega$ ) | Capacitance (pF) |
|-----------------------|-------------------------|------------------|
| 3 MHz                 | 25 $\Omega$             | 12 pF            |
| 70 MHz                | 12 $\Omega$             | 8 pF             |
| 170 MHz               | 12 $\Omega$             | 8 pF             |

11.2.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in [Figure 18](#) would be suitable for a baseband application.

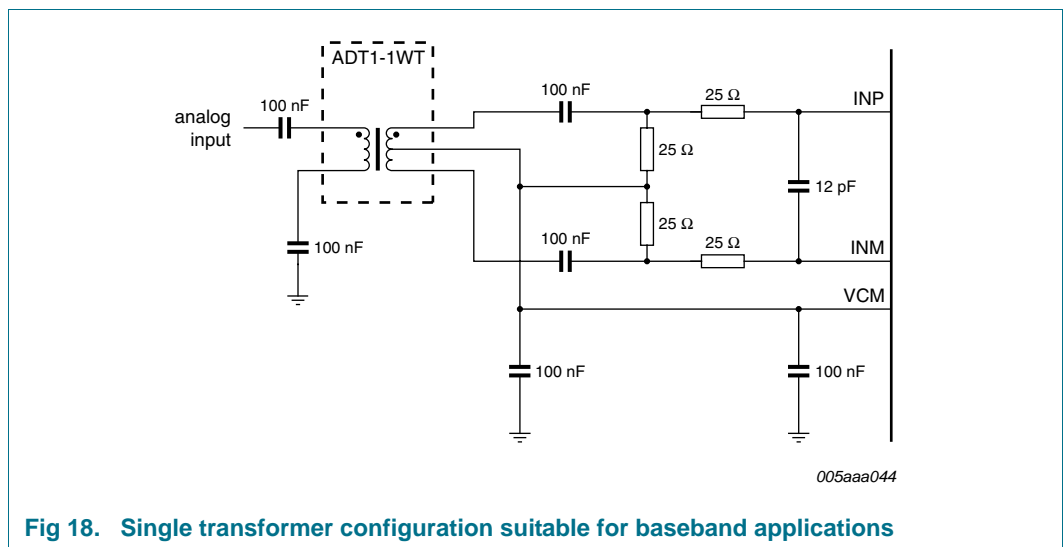
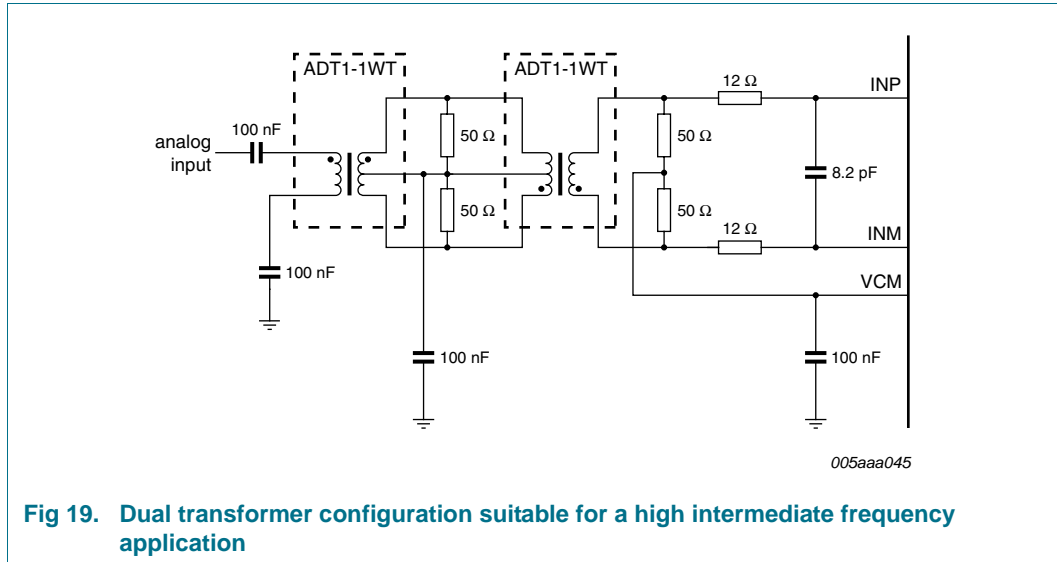


Fig 18. Single transformer configuration suitable for baseband applications

The configuration shown in [Figure 19](#) is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.



**Fig 19. Dual transformer configuration suitable for a high intermediate frequency application**

### 11.3 System reference and power management

#### 11.3.1 Internal/external references

The ADC1610S has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (programmable in 1 dB steps between 0 dB and -6 dB via control bits INTREF[2:0] when bit INTREF\_EN = logic 1; see [Table 22](#)). See [Figure 21](#) to [Figure 24](#). The equivalent reference circuit is shown in [Figure 20](#). An external reference is also possible by providing a voltage on pin VREF as described in [Figure 23](#).

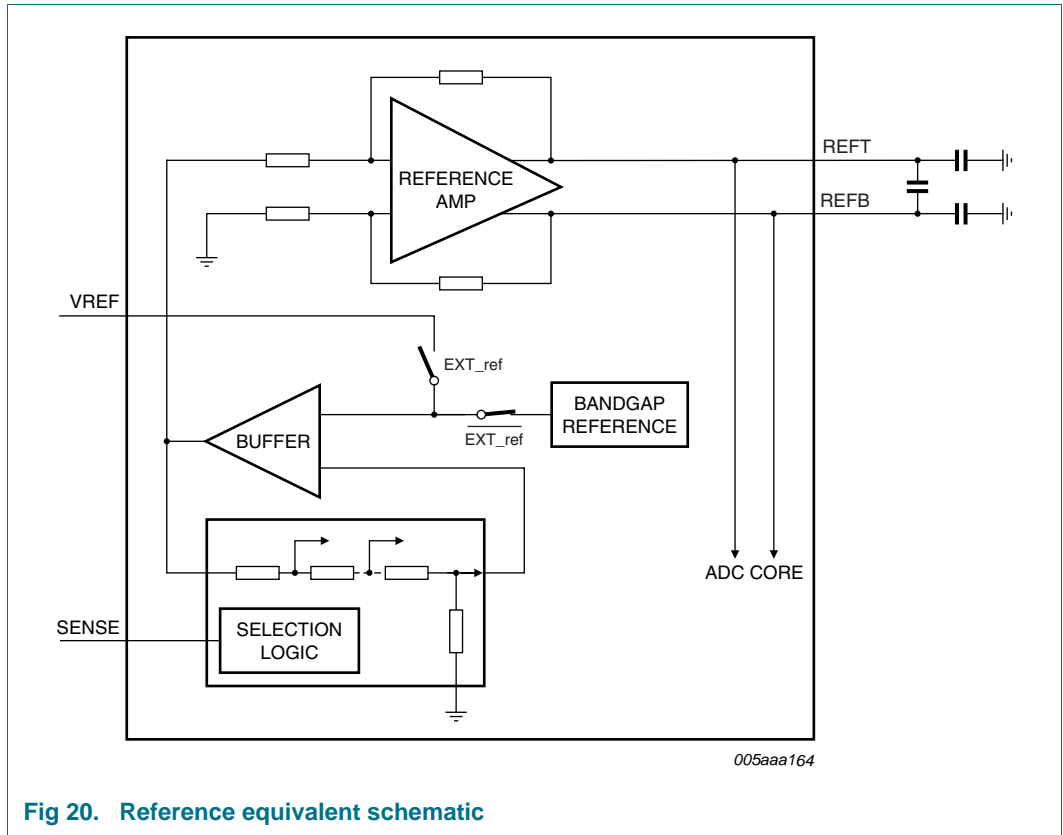


Fig 20. Reference equivalent schematic

If bit INTREF\_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in [Table 12](#).

Table 12. Reference selection

| Selection   | SPI bit INTREF_EN | SENSE pin  | VREF pin  | Full-scale (p-p) |
|---|-------------------|--|---|------------------|
| internal<br>( <a href="#">Figure 21</a> )         | 0                 | AGND   | 330 pF capacitor to AGND                              | 2 V              |
| internal<br>( <a href="#">Figure 22</a> )         | 0                 | pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND |   | 1 V              |
| external<br>( <a href="#">Figure 23</a> )         | 0                 | V <sub>DDA</sub>   | external voltage between 0.5 V and 1 V <sup>[1]</sup> | 1 V to 2 V       |
| internal via SPI<br>( <a href="#">Figure 24</a> ) | 1                 | pin VREF connected to pin SENSE and via 330 pF capacitor to AGND   |   | 1 V to 2 V       |

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

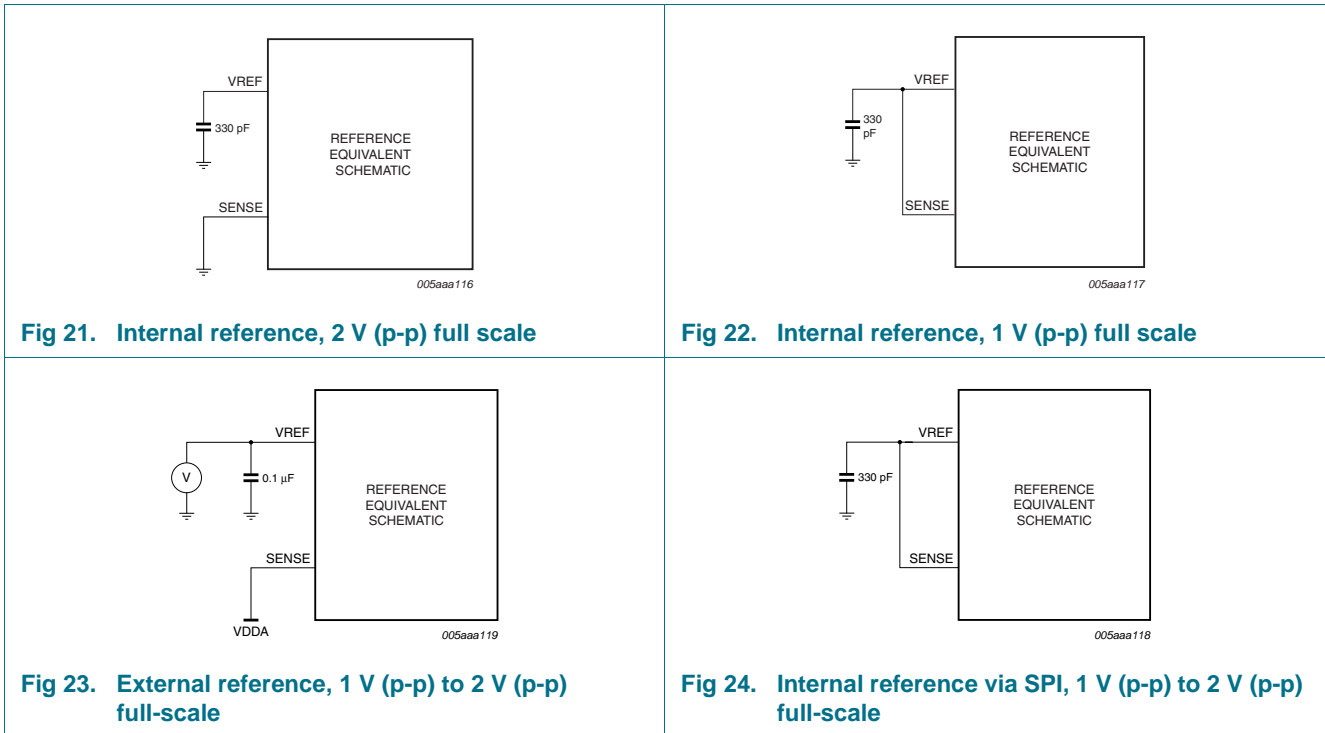


Figure 21 to Figure 24 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

### 11.3.2 Programmable full-scale

The full-scale is programmable between 1 V (p-p) to 2 V (p-p) (see Table 13).

Table 13. Reference SPI gain control

| INTREF[2:0] | Gain (dB) | Full-scale (V (p-p)) |
|-------------|-----------|----------------------|
| 000         | 0         | 2                    |
| 001         | -1        | 1.78                 |
| 010         | -2        | 1.59                 |
| 011         | -3        | 1.42                 |
| 100         | -4        | 1.26                 |
| 101         | -5        | 1.12                 |
| 110         | -6        | 1                    |
| 111         | reserved  | x                    |

11.3.3 Common-mode output voltage ( $V_{O(cm)}$ )

A 0.1  $\mu$ F filter capacitor should be connected between pin VCM and ground to ensure a low-noise common-mode output voltage. When AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

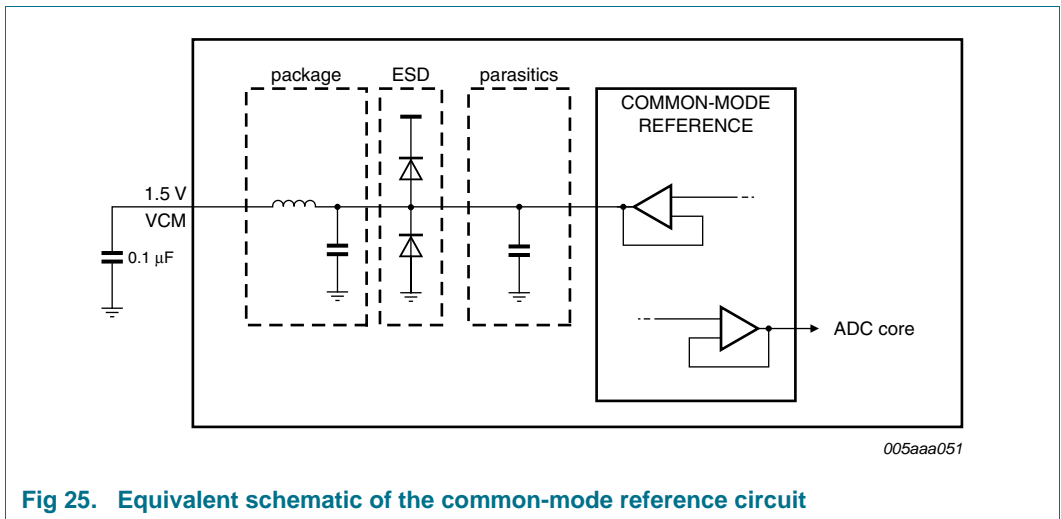


Fig 25. Equivalent schematic of the common-mode reference circuit

11.3.4 Biasing

The common-mode input voltage ( $V_{I(cm)}$ ) on pins INP and INM should be set externally to  $0.5V_{DDA}$  for optimal performance and should always be between 0.9 V and 2 V.

11.4 Clock input

11.4.1 Drive modes

The ADC1610S can be driven differentially (LVPECL). It can also be driven by a single-ended Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or pin CLKM (pin CLKP should be connected to ground via a capacitor).

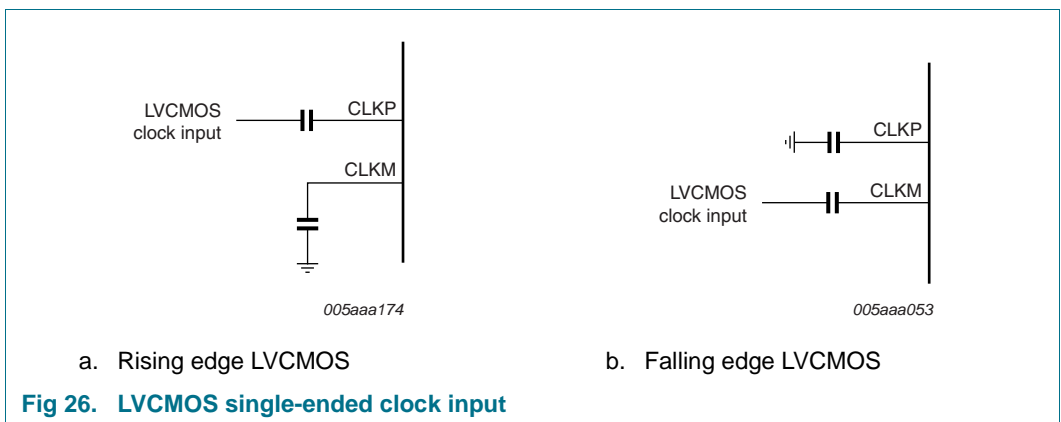
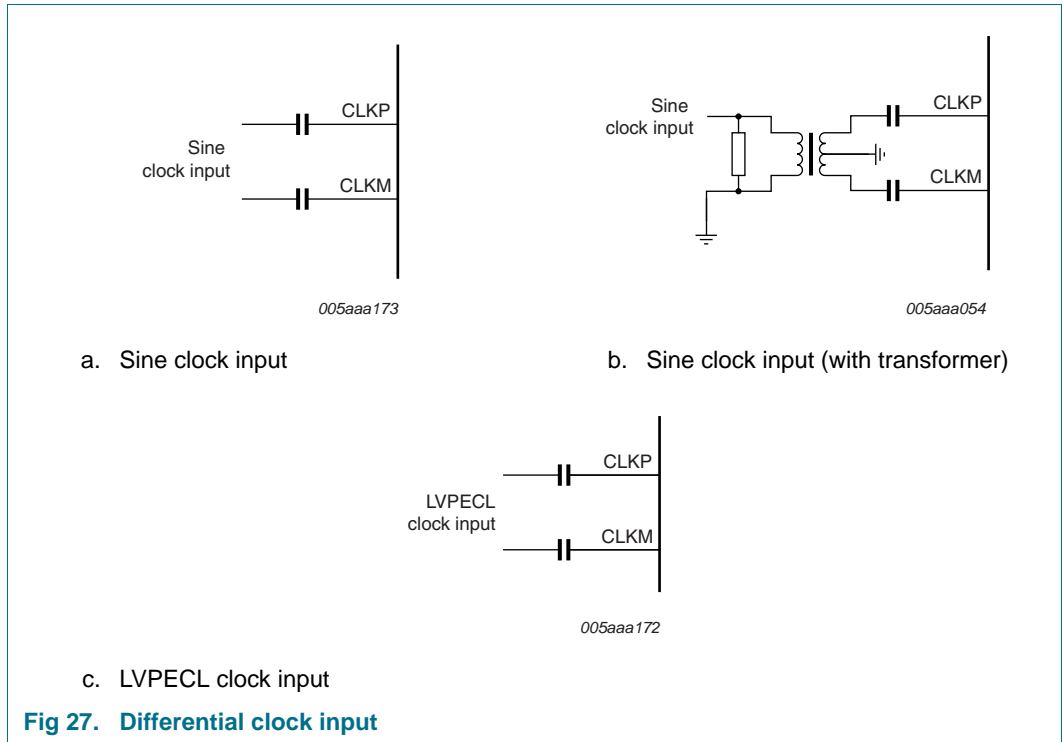
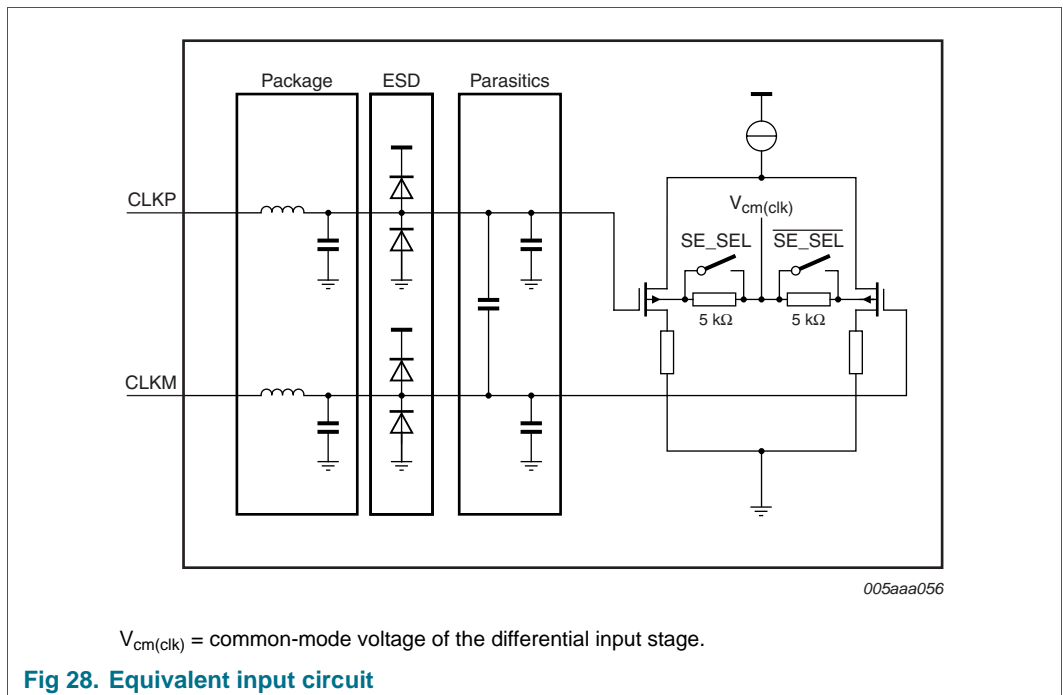


Fig 26. LVCMOS single-ended clock input



11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 29. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.



Single-ended or differential clock inputs can be selected via the SPI interface (see [Table 21](#)). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE\_SEL.

If single-ended is implemented without setting bit SE\_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

**11.4.3 Duty cycle stabilizer**

The duty cycle stabilizer can improve the overall performance of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS\_EN = logic 1; see [Table 21](#)), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS\_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

**11.4.4 Clock input divider**

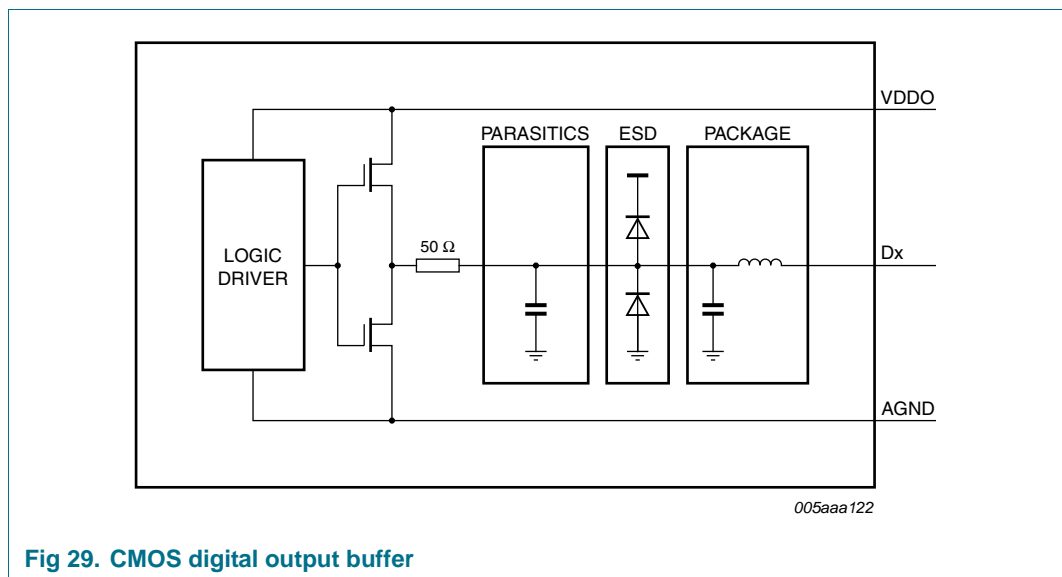
The ADC1610S contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = logic 1; see [Table 21](#)). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

**11.5 Digital outputs**

**11.5.1 Digital output buffers: CMOS mode**

The digital output buffers can be configured as CMOS by setting bit LVDS\_CMOS to logic 0 (see [Table 23](#)).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in [Figure 30](#). The buffer is powered by a separate power supply, pins OGND and VDDO, to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.

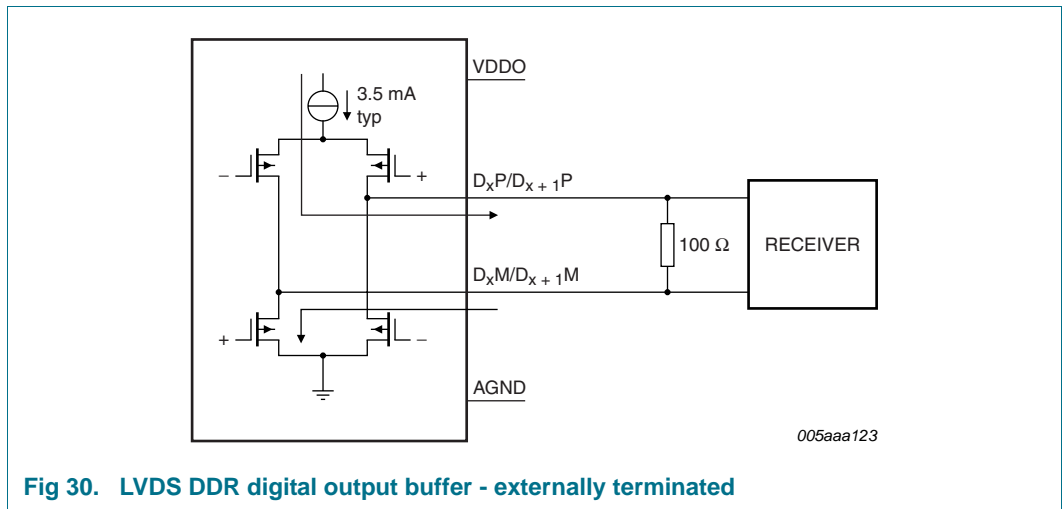




The output resistance is 50 Ω and is the combination of an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see [Table 30](#)):

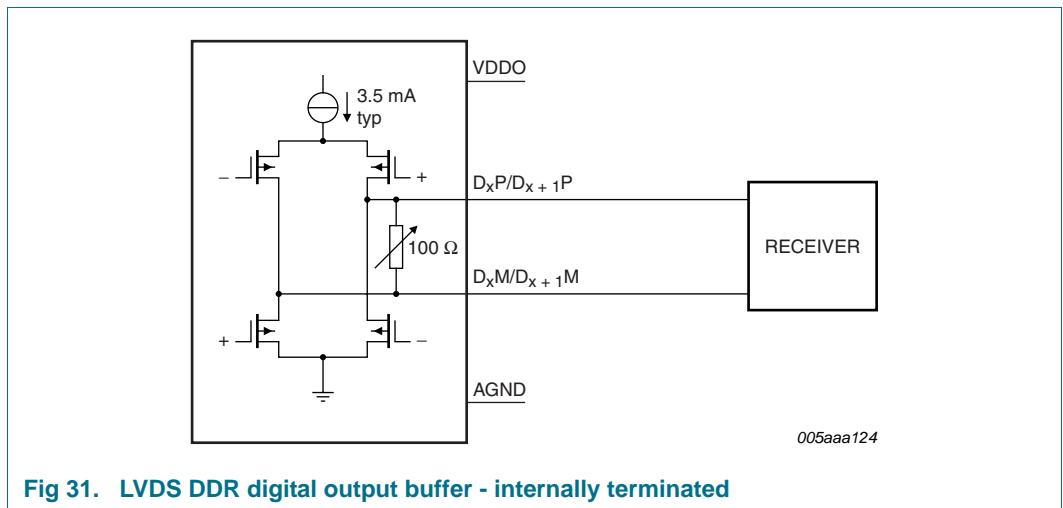
**11.5.2 Digital output buffers: LVDS DDR mode**

The digital output buffers can be configured as LVDS DDR by setting bit LVDS\_CMOS to logic 1 (see [Table 23](#)).



**Fig 30. LVDS DDR digital output buffer - externally terminated**

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side ([Figure 31](#)) or internally via SPI control bits LVDS\_INT\_TER[2:0] (see [Figure 32](#) and [Table 32](#)).



**Fig 31. LVDS DDR digital output buffer - internally terminated**

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI[1:0] and DATAI[1:0]; see [Table 31](#)) in order to adjust the output logic voltage levels.

Table 14. LVDS DDR output register 2

| LVDS_INT_TER[1:0] | Resistor value ( $\Omega$ ) |
|-------------------|-----------------------------|
| 000               | no internal termination     |
| 001               | 300                         |
| 010               | 180                         |
| 011               | 110                         |
| 100               | 150                         |
| 101               | 100                         |
| 110               | 81                          |
| 111               | 60                          |

### 11.5.3 DAta Valid (DAV) output clock

A data valid output clock signal (DAV) can be used to capture the data delivered by the ADC1610S. Detailed timing diagrams for CMOS and LVDS DDR modes are shown in [Figure 4](#) and [Figure 5](#) respectively.

### 11.5.4 Out-of-Range (OTR)

An out-of-range signal is provided on pin OTR. The latency of OTR is fourteen clock cycles. The OTR response can be speeded up by enabling Fast OTR (bit FASTOTR = logic 1; see [Table 29](#)). In this mode, the latency of OTR is reduced to only four clock cycles. The Fast OTR detection threshold (below full-scale) can be programmed via bits FASTOTR\_DET[2:0].

Table 15. Fast OTR register

| FASTOTR_DET[2:0] | Detection level (dB) |
|------------------|----------------------|
| 000              | -20.56               |
| 001              | -16.12               |
| 010              | -11.02               |
| 011              | -7.82                |
| 100              | -5.49                |
| 101              | -3.66                |
| 110              | -2.14                |
| 111              | -0.86                |

### 11.5.5 Digital offset

By default, the ADC1610S delivers output code that corresponds to the analog input. However it is possible to add a digital offset to the output code via the SPI (bits DIG\_OFFSET[5:0]; see [Table 25](#)).

### 11.5.6 Test patterns

For test purposes, the ADC1610S can be configured to transmit one of a number of predefined test patterns (via bits TESTPAT\_SEL[2:0]; see [Table 26](#)). A custom test pattern can be defined by the user (TESTPAT\_USER[15:0]; see [Table 27](#) and [Table 28](#)) and is selected when TESTPAT\_SEL[2:0] = 101. The selected test pattern is transmitted regardless of the analog input.

## 11.5.7 Output codes versus input voltage

Table 16. Output codes

| $V_{INP} - V_{INM}$ | Offset binary              | Two's complement           | OTR pin |
|---------------------|----------------------------|----------------------------|---------|
| < -1                | 0000 0000 0000 0000        | 1000 0000 0000 0000        | 1       |
| -1                  | 0000 0000 0000 0000        | 1000 0000 0000 0000        | 0       |
| -0.99996948         | 0000 0000 0000 0001        | 1000 0000 0000 0001        | 0       |
| -0.99993896         | 0000 0000 0000 0010        | 1000 0000 0000 0010        | 0       |
| -0.99990845         | 0000 0000 0000 0011        | 1000 0000 0000 0011        | 0       |
| -0.99987793         | 0000 0000 0000 0100        | 1000 0000 0000 0100        | 0       |
| ....                | ....                       | ....                       | 0       |
| -0.00006104         | 0111 1111 1111 1110        | 1111 1111 1111 1110        | 0       |
| -0.00003052         | 0111 1111 1111 1111        | 1111 1111 1111 1111        | 0       |
| 0                   | <b>1000 0000 0000 0000</b> | <b>0000 0000 0000 0000</b> | 0       |
| +0.00003052         | 1000 0000 0000 0001        | 0000 0000 0000 0001        | 0       |
| +0.00006104         | 1000 0000 0000 0010        | 0000 0000 0000 0010        | 0       |
| ....                | ....                       | ....                       | 0       |
| +0.99987793         | 1111 1111 1111 1011        | 0111 1111 1111 1011        | 0       |
| +0.99990845         | 1111 1111 1111 1100        | 0111 1111 1111 1100        | 0       |
| +0.99993896         | 1111 1111 1111 1101        | 0111 1111 1111 1101        | 0       |
| +0.99996948         | 1111 1111 1111 1110        | 0111 1111 1111 1110        | 0       |
| +1                  | 1111 1111 1111 1111        | 0111 1111 1111 1111        | 0       |
| > +1                | 1111 1111 1111 1111        | 0111 1111 1111 1111        | 1       |

## 11.6 Serial peripheral interface

### 11.6.1 Register description

The ADC1610S serial interface is a synchronous serial communications port that allows easy interfacing with many commonly-used microprocessors. It provides access to the registers that control the operation of the chip.

This interface is configured as a 3-wire type (SDIO as bidirectional pin)

Pin SCLK is the serial clock input and pin  $\overline{CS}$  is the chip select pin.

Each read/write operation is initiated by a LOW level on pin  $\overline{CS}$ . A minimum of three bytes is transmitted (two instruction bytes and at least one data byte). The number of data bytes is determined by the value of bits W1 and W2 (see [Table 18](#)).

Table 17. Instruction bytes for the SPI

|             | MSB                   |       |       |     |     |     |    | LSB |
|-------------|-----------------------|-------|-------|-----|-----|-----|----|-----|
| Bit         | 7                     | 6     | 5     | 4   | 3   | 2   | 1  | 0   |
| Description | R/ $\overline{W}$ [1] | W1[2] | W0[2] | A12 | A11 | A10 | A9 | A8  |
|             | A7                    | A6    | A5    | A4  | A3  | A2  | A1 | A0  |

[1] Bit  $\overline{R/W}$  indicates whether it is a read (logic 1) or a write (logic 0) operation.

[2] Bits W1 and W0 indicate the number of bytes to be transferred after the instruction byte (see [Table 18](#)).

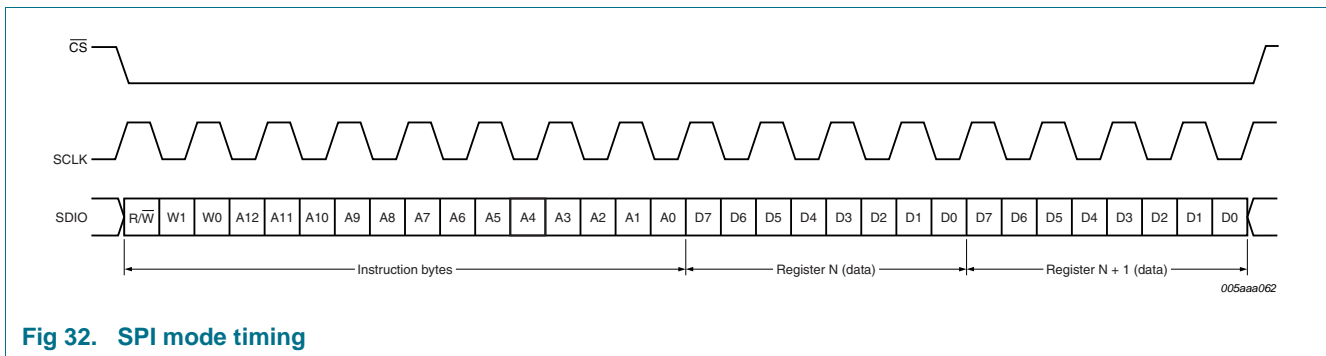
**Table 18. Number of data bytes to be transferred after the instruction bytes**

| W1 | W0 | Number of bytes transmitted |
|----|----|-----------------------------|
| 0  | 0  | 1 byte                      |
| 0  | 1  | 2 bytes                     |
| 1  | 0  | 3 bytes                     |
| 1  | 1  | 4 bytes or more             |

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is increased to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. A falling edge on  $\overline{CS}$  in combination with a rising edge on SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but is always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on  $\overline{CS}$  indicates the end of data transmission.



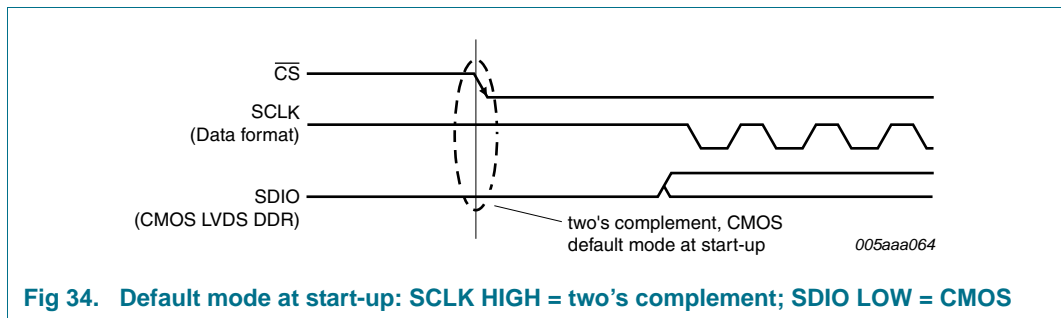
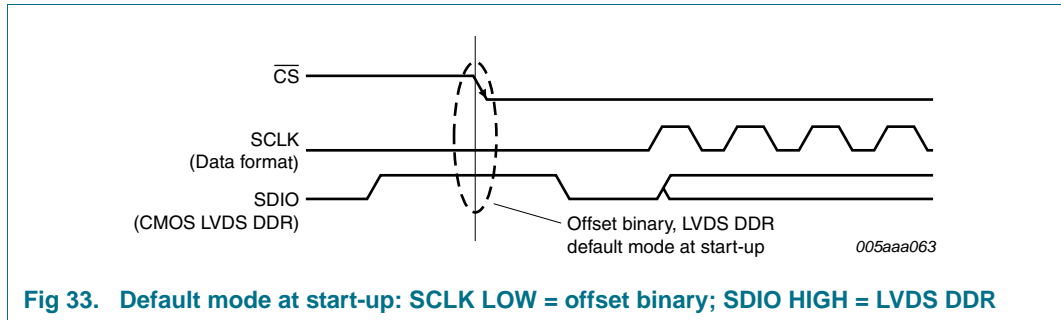
**Fig 32. SPI mode timing**

**11.6.2 Default modes at start-up**

During circuit initialization it does not matter which output data standard has been selected. At power-up, the device enters Pin control mode.

A falling edge on  $\overline{CS}$  triggers a transition to SPI control mode. When the ADC1610S enters SPI control mode, the output data standard (CMOS/LVDS DDR) is determined by the level on pin SDIO (see [Figure 33](#)). Once in SPI control mode, the output data standard can be changed via bit LVDS\_CMOS in [Table 23](#).

When the ADC1610S enters SPI control mode, the output data format (two's complement or offset binary) is determined by the level on pin SCLK (gray code can only be selected via the SPI). Once in SPI control mode, the output data format can be changed via bit DATA\_FORMAT[1:0] in [Table 23](#).



### 11.6.3 Register allocation map

Table 19. Register allocation map

| Addr Hex | Register name            | R/W | Bit definition     |               |                 |           |               |                   |                  |        | Default      |
|----------|--------------------------|-----|--------------------|---------------|-----------------|-----------|---------------|-------------------|------------------|--------|--------------|
|          |                          |     | Bit 7              | Bit 6         | Bit 5           | Bit 4     | Bit 3         | Bit 2             | Bit 1            | Bit 0  | Bin          |
| 0005     | Reset and operating mode | R/W | SW_RST             | RESERVED[2:0] |                 |           | -             | -                 | OP_MODE[1:0]     |        | 0000<br>0000 |
| 0006     | Clock                    | R/W | -                  | -             | -               | SE_SEL    | DIFF_SE       | -                 | CLKDIV           | DCS_EN | 0000<br>0001 |
| 0008     | Internal reference       | R/W | -                  | -             | -               | -         | INTREF_EN     | INTREF[2:0]       |                  |        | 0000<br>0000 |
| 0011     | Output data standard     | R/W | -                  | -             | -               | LVDS_CMOS | OUTBUF        | OUTBUS_SWAP       | DATA_FORMAT[1:0] |        | 0000<br>0000 |
| 0012     | Output clock             | R/W | -                  | -             | -               | -         | DAVINV        | DAVPHASE[2:0]     |                  |        | 0000<br>1110 |
| 0013     | Offset                   | R/W | -                  | -             | DIG_OFFSET[5:0] |           |               |                   |                  |        | 0000<br>0000 |
| 0014     | Test pattern 1           | R/W | -                  | -             | -               | -         | -             | TESTPAT_SEL[2:0]  |                  |        | 0000<br>0000 |
| 0015     | Test pattern 2           | R/W | TESTPAT_USER[15:8] |               |                 |           |               |                   |                  |        | 0000<br>0000 |
| 0016     | Test pattern 3           | R/W | TESTPAT_USER[7:0]  |               |                 |           |               |                   |                  |        | 0000<br>0000 |
| 0017     | Fast OTR                 | R/W | -                  | -             | -               | -         | FASTOTR       | FASTOTR_DET[2:0]  |                  |        | 0000<br>0000 |
| 0020     | CMOS output              | R/W | -                  | -             | -               | -         | DAV_DRV[1:0]  |                   | DATA_DRV[1:0]    |        | 0000<br>1110 |
| 0021     | LVDS DDR O/P 1           | R/W | -                  | -             | DAVI_x2_EN      | DAVI[1:0] |               | DATAI_x2_EN       | DATAI[1:0]       |        | 0000<br>0000 |
| 0022     | LVDS DDR O/P 2           | R/W | -                  | -             | -               | -         | BIT_BYTE_WISE | LVDS_INT_TER[2:0] |                  |        | 0000<br>0000 |

**Table 20. Reset and operating mode control register (address 0005h) bit description***Default values are highlighted.*

| Bit    | Symbol        | Access | Value     | Description                           |
|--------|---------------|--------|-----------|---------------------------------------|
| 7      | SW_RST        | R/W    |           | reset digital section                 |
|        |               |        | <b>0</b>  | <b>no reset</b>                       |
|        |               |        | 1         | performs a reset of the SPI registers |
| 6 to 4 | RESERVED[2:0] |        | 000       | reserved                              |
| 3 to 2 | -             |        | 00        | not used                              |
| 1 to 0 | OP_MODE[1:0]  | R/W    |           | operating mode                        |
|        |               |        | <b>00</b> | <b>normal (power-up)</b>              |
|        |               |        | 01        | power-down                            |
|        |               |        | 10        | sleep                                 |
|        |               |        | 11        | normal (power-up)                     |

**Table 21. Clock control register (address 0006h) bit description***Default values are highlighted.*

| Bit    | Symbol  | Access | Value    | Description                                  |
|--------|---------|--------|----------|--|
| 7 to 5 | -       |        | 000      | not used                                     |
| 4      | SE_SEL  | R/W    |          | single-ended clock input pin select          |
|        |         |        | <b>0</b> | <b>CLKM</b>                                  |
|        |         |        | 1        | CLKP   |
| 3      | DIFF_SE | R/W    |          | differential/single-ended clock input select |
|        |         |        | <b>0</b> | <b>fully differential</b>                    |
|        |         |        | 1        | single-ended                                 |
| 2      | -       |        | 0        | not used                                     |
| 1      | CLKDIV  | R/W    |          | clock input divide by 2                      |
|        |         |        | <b>0</b> | <b>disabled</b>                              |
|        |         |        | 1        | enabled                                      |
| 0      | DCS_EN  | R/W    |          | duty cycle stabilizer                        |
|        |         |        | 0        | disabled                                     |
|        |         |        | <b>1</b> | <b>enabled</b>                               |

**Table 22. Internal reference control register (address 0008h) bit description***Default values are highlighted.*

| Bit    | Symbol      | Access | Value      | Description                            |
|--------|-------------|--------|------------|--|
| 7 to 4 | -           |        | 0          | not used                               |
| 3      | INTREF_EN   | R/W    |            | programmable internal reference enable |
|        |             |        | <b>0</b>   | <b>disable</b>                         |
|        |             |        | 1          | active                                 |
| 2 to 0 | INTREF[2:0] | R/W    |            | programmable internal reference        |
|        |             |        | <b>000</b> | <b>FS = 2 V</b>                        |
|        |             |        | 001        | FS = 1.78 V                            |
|        |             |        | 010        | FS = 1.59 V                            |
|        |             |        | 011        | FS = 1.42 V                            |
|        |             |        | 100        | FS = 1.26 V                            |
|        |             |        | 101        | FS = 1.12 V                            |
|        |             |        | 110        | FS = 1 V                               |
|        |             |        | 111        | reserved                               |

**Table 23. Output data standard control register (address 0011h) bit description***Default values are highlighted.*

| Bit    | Symbol           | Access | Value     | Description   |
|--------|------------------|--------|-----------|---|
| 7 to 5 | -                |        | 000       | not used  |
| 4      | LVDS_CMOS        | R/W    |           | output data standard: LVDS DDR or CMOS                  |
|        |                  |        | <b>0</b>  | <b>CMOS</b>   |
|        |                  |        | 1         | LVDS DDR  |
| 3      | OUTBUF           | R/W    |           | output buffers enable                                   |
|        |                  |        | <b>0</b>  | <b>output enabled</b>                                   |
|        |                  |        | 1         | output disabled (high-Z)                                |
| 2      | OUTBUS_SWAP      |        | 0         | outbus swapping   |
|        |                  |        | <b>0</b>  | <b>no swapping</b>                                      |
|        |                  |        | 1         | output bus is swapping (MSB becomes LSB and vice versa) |
| 1 to 0 | DATA_FORMAT[1:0] | R/W    |           | output data format                                      |
|        |                  |        | <b>00</b> | <b>offset binary</b>                                    |
|        |                  |        | 01        | two's complement  |
|        |                  |        | 10        | gray code   |
|        |                  |        | 11        | offset binary   |



**Table 24. Output clock register (address 0012h) bit description**

Default values are highlighted.

| Bit    | Symbol        | Access | Value      | Description   |
|--------|---------------|--------|------------|---|
| 7 to 4 | -             |        | 0000       | not used  |
| 3      | DAVINV        | R/W    |            | output clock data valid (DAV) polarity                  |
|        |               |        | 0          | normal  |
|        |               |        | <b>1</b>   | <b>inverted</b>   |
| 2 to 0 | DAVPHASE[2:0] | R/W    |            | DAV phase select  |
|        |               |        | 000        | output clock shifted (ahead) by $6/16 \times t_{clk}$   |
|        |               |        | 001        | output clock shifted (ahead) by $5/16 \times t_{clk}$   |
|        |               |        | 010        | output clock shifted (ahead) by $4/16 \times t_{clk}$   |
|        |               |        | 011        | output clock shifted (ahead) by $3/16 \times t_{clk}$   |
|        |               |        | 100        | output clock shifted (ahead) by $2/16 \times t_{clk}$   |
|        |               |        | 101        | output clock shifted (ahead) by $1/16 \times t_{clk}$   |
|        |               |        | <b>110</b> | <b>default value as defined in timing section</b>       |
|        |               |        | 111        | output clock shifted (delayed) by $1/16 \times t_{clk}$ |

**Table 25. Offset register (address 0013h) bit description**

Default values are highlighted.

| Bit    | Symbol          | Access | Value         | Description               |
|--------|-----------------|--------|---------------|---------------------------|
| 7 to 6 | -               |        | 00            | not used                  |
| 5 to 0 | DIG_OFFSET[5:0] | R/W    |               | digital offset adjustment |
|        |                 |        | 011111        | +31 LSB                   |
|        |                 |        | ...           | ...                       |
|        |                 |        | <b>000000</b> | <b>0</b>                  |
|        |                 |        | ...           | ...                       |
|        |                 |        | 100000        | -32 LSB                   |

**Table 26. Test pattern register 1 (address 0014h) bit description**

Default values are highlighted.

| Bit    | Symbol           | Access | Value      | Description                      |
|--------|------------------|--------|------------|----------------------------------|
| 7 to 3 | -                |        | 00000      | not used                         |
| 2 to 0 | TESTPAT_SEL[2:0] | R/W    |            | digital test pattern select      |
|        |                  |        | <b>000</b> | <b>off</b>                       |
|        |                  |        | 001        | mid scale                        |
|        |                  |        | 010        | -FS                              |
|        |                  |        | 011        | +FS                              |
|        |                  |        | 100        | toggle '1111..1111'/'0000..0000' |
|        |                  |        | 101        | custom test pattern              |
|        |                  |        | 110        | '1010..1010.'                    |
|        |                  |        | 111        | '010..1010'                      |

**Table 27. Test pattern register 2 (address 0015h) bit description**

Default values are highlighted.

| Bit    | Symbol             | Access | Value           | Description                                |
|--------|--------------------|--------|-----------------|--|
| 7 to 0 | TESTPAT_USER[15:8] | R/W    | <b>00000000</b> | custom digital test pattern (bits 13 to 6) |

**Table 28. Test pattern register 3 (address 0016h) bit description**

Default values are highlighted.

| Bit    | Symbol            | Access | Value           | Description                               |
|--------|-------------------|--------|-----------------|---|
| 7 to 0 | TESTPAT_USER[7:0] | R/W    | <b>00000000</b> | custom digital test pattern (bits 7 to 0) |

**Table 29. Fast OTR register (address 0017h) bit description**

Default values are highlighted.

| Bit    | Symbol           | Access   | Value      | Description                       |
|--------|------------------|----------|------------|-----------------------------------|
| 7 to 4 | -                |          | 0000       | not used                          |
| 3      | FASTOTR          | R/W      |            | fast OuT-of-Range (OTR) detection |
|        |                  |          | <b>0</b>   | <b>disabled</b>                   |
|        |                  |          | 1          | enabled                           |
| 2 to 0 | FASTOTR_DET[2:0] | R/W      |            | set fast OTR detect level         |
|        |                  |          | <b>000</b> | <b>-20.56 dB</b>                  |
|        |                  |          | 001        | -16.12 dB                         |
|        |                  |          | 010        | -11.02 dB                         |
|        |                  |          | 011        | -7.82 dB                          |
|        |                  |          | 100        | -5.49 dB                          |
|        |                  |          | 101        | -3.66 dB                          |
|        |                  |          | 110        | -2.14 dB                          |
|        | 111              | -0.86 dB |            |                                   |

**Table 30. CMOS output register (address 0020h) bit description**

Default values are highlighted.

| Bit    | Symbol        | Access | Value     | Description                                |
|--------|---------------|--------|-----------|--|
| 7 to 4 | -             |        | 0000      | not used                                   |
| 3 to 2 | DAV_DRV[1:0]  | R/W    |           | drive strength for DAV CMOS output buffer  |
|        |               |        | 00        | low  |
|        |               |        | 01        | medium                                     |
|        |               |        | 10        | high                                       |
|        |               |        | <b>11</b> | <b>very high</b>                           |
| 1 to 0 | DATA_DRV[1:0] | R/W    |           | drive strength for DATA CMOS output buffer |
|        |               |        | 00        | low  |
|        |               |        | 01        | medium                                     |
|        |               |        | <b>10</b> | <b>high</b>                                |
|        |               |        | 11        | very high                                  |

**Table 31. LVDS DDR output register 1 (address 0021h) bit description***Default values are highlighted.*

| Bit    | Symbol      | Access | Value     | Description                              |
|--------|-------------|--------|-----------|--|
| 7 to 6 | -           |        | 00        | not used                                 |
| 5      | DAVI_x2_EN  | R/W    |           | double LVDS current for DAV LVDS buffer  |
|        |             |        | <b>0</b>  | <b>disabled</b>                          |
|        |             |        | 1         | enabled                                  |
| 4 to 3 | DAVI[1:0]   | R/W    |           | LVDS current for DAV LVDS buffer         |
|        |             |        | <b>00</b> | <b>3.5 mA</b>                            |
|        |             |        | 01        | 4.5 mA                                   |
|        |             |        | 10        | 1.25 mA                                  |
|        |             |        | 11        | 2.5 mA                                   |
| 2      | DATAI_x2_EN | R/W    |           | double LVDS current for DATA LVDS buffer |
|        |             |        | <b>0</b>  | <b>disabled</b>                          |
|        |             |        | 1         | enabled                                  |
| 1 to 0 | DATAI[1:0]  | R/W    |           | LVDS current for DATA LVDS buffer        |
|        |             |        | <b>00</b> | <b>3.5 mA</b>                            |
|        |             |        | 01        | 4.5 mA                                   |
|        |             |        | 10        | 1.25 mA                                  |
|        |             |        | 11        | 2.5 mA                                   |

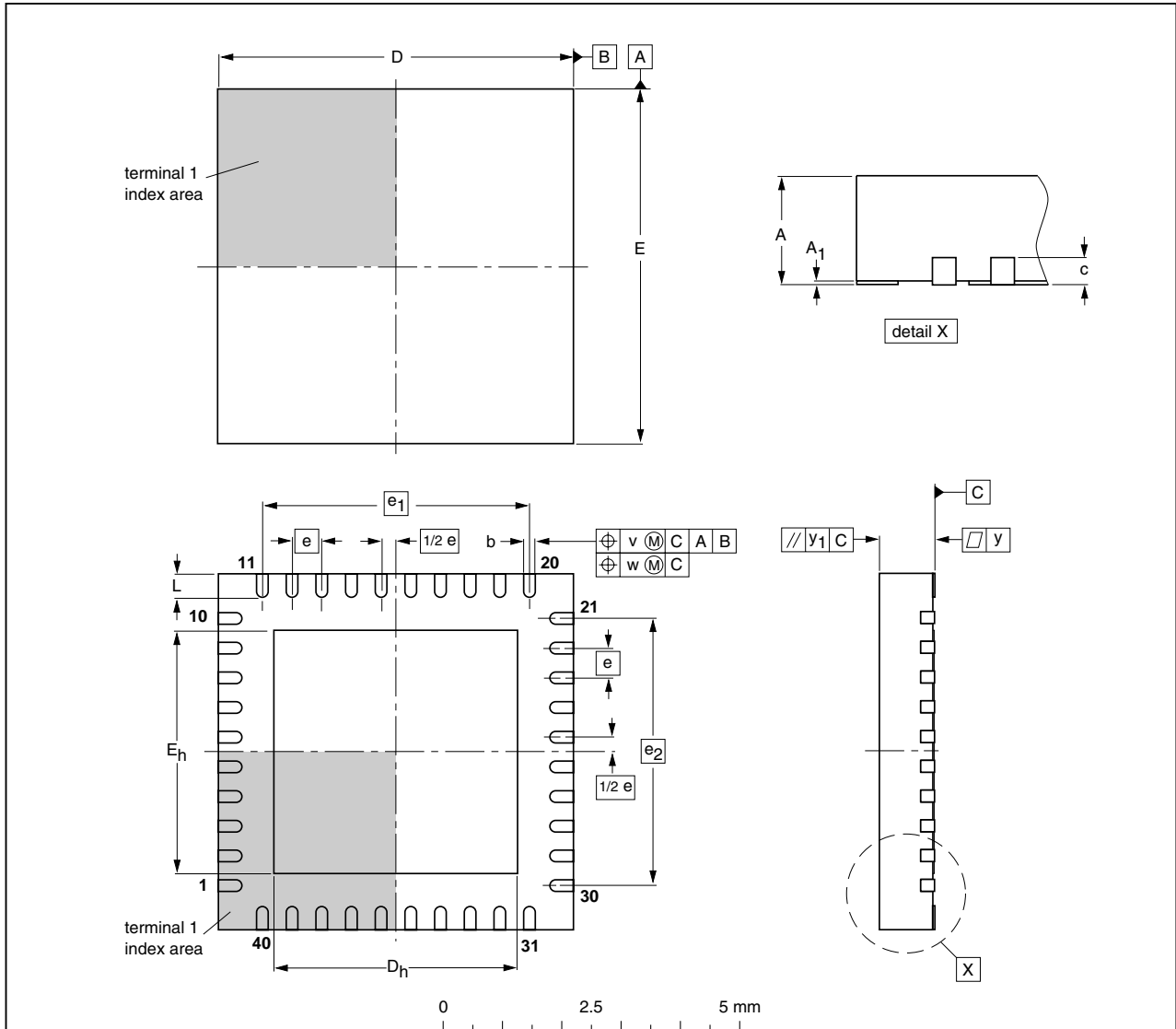
**Table 32. LVDS DDR output register 2 (address 0022h) bit description***Default values are highlighted.*

| Bit    | Symbol            | Access | Value      | Description   |
|--------|-------------------|--------|------------|---|
| 7 to 4 | -                 |        | 0000       | not used  |
| 3      | BIT_BYTE_WISE     | R/W    |            | DDR mode for LVDS output  |
|        |                   |        | <b>0</b>   | <b>bit wise (even data bits output on DAV rising edge/odd data bits output on DAV falling edge)</b> |
|        |                   |        | 1          | byte wise (MSB data bits output on DAV rising edge/LSB data bits output on DAV falling edge)        |
| 2 to 0 | LVDS_INT_TER[2:0] | R/W    |            | internal termination for LVDS buffer (DAV and DATA)   |
|        |                   |        | <b>000</b> | <b>no internal termination</b>  |
|        |                   |        | 001        | 300 Ω   |
|        |                   |        | 010        | 180 Ω   |
|        |                   |        | 011        | 110 Ω   |
|        |                   |        | 100        | 150 Ω   |
|        |                   |        | 101        | 100 Ω   |
|        |                   |        | 110        | 81 Ω  |
|        |                   |        | 111        | 60 Ω  |

12. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

SOT618-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A <sup>(1)</sup> max. | A <sub>1</sub> | b            | c   | D <sup>(1)</sup> | D <sub>h</sub> | E <sup>(1)</sup> | E <sub>h</sub> | e   | e <sub>1</sub> | e <sub>2</sub> | L          | v   | w    | y    | y <sub>1</sub> |
|------|-----------------------|----------------|--------------|-----|------------------|----------------|------------------|----------------|-----|----------------|----------------|------------|-----|------|------|----------------|
| mm   | 1                     | 0.05<br>0.00   | 0.30<br>0.18 | 0.2 | 6.1<br>5.9       | 4.25<br>3.95   | 6.1<br>5.9       | 4.25<br>3.95   | 0.5 | 4.5            | 4.5            | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1            |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |       |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
|                 | IEC        | JEDEC  | JEITA |  |                     |                      |
| SOT618-1        | ---        | MO-220 | ---   |  |                     | 01-08-08<br>02-10-22 |

Fig 35. Package outline SOT618-1 (HVQFN40)

## 13. Revision history

**Table 33. Revision history**

| Document ID      | Release date | Data sheet status  | Change notice | Supersedes     |
|------------------|--------------|--|---------------|----------------|
| ADC1610S_SER v.3 | 20110125     | Product data sheet   | -             | ADC1610S_SER_2 |
| Modifications:   |              | <ul style="list-style-type: none"> <li>• Data sheet status changed from Objective to Product.</li> <li>• Text and drawings updated throughout entire data sheet.</li> <li>• SOT618-6 changed to SOT618-1. See <a href="#">Table 1 "Ordering information"</a> and <a href="#">Figure 35 "Package outline SOT618-1 (HVQFN40)"</a>.</li> <li>• <a href="#">Section 10.4 "Typical characteristics"</a> added to the data sheet.</li> </ul> |               |                |
| ADC1610S_SER_2   | 20100412     | Objective data sheet   | -             | ADC1610S125_1  |
| ADC1610S125_1    | 20090528     | Objective data sheet   | -             | -              |

## 14. Legal information

### 14.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 14.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

16. Contents

|           |  |           |           |                                      |           |
|-----------|--|-----------|-----------|--------------------------------------|-----------|
| <b>1</b>  | <b>General description</b> . . . . .                 | <b>1</b>  | 11.6.2    | Default modes at start-up            | 28        |
| <b>2</b>  | <b>Features and benefits</b> . . . . .               | <b>1</b>  | 11.6.3    | Register allocation map              | 30        |
| <b>3</b>  | <b>Applications</b> . . . . .                        | <b>1</b>  | <b>12</b> | <b>Package outline</b> . . . . .     | <b>36</b> |
| <b>4</b>  | <b>Ordering information</b> . . . . .                | <b>2</b>  | <b>13</b> | <b>Revision history</b> . . . . .    | <b>37</b> |
| <b>5</b>  | <b>Block diagram</b> . . . . .                       | <b>2</b>  | <b>14</b> | <b>Legal information</b> . . . . .   | <b>38</b> |
| <b>6</b>  | <b>Pinning information</b> . . . . .                 | <b>3</b>  | 14.1      | Data sheet status                    | 38        |
| 6.1       | Pinning . . . . .                                    | 3         | 14.2      | Definitions . . . . .                | 38        |
| 6.2       | Pin description . . . . .                            | 3         | 14.3      | Disclaimers . . . . .                | 38        |
| <b>7</b>  | <b>Limiting values</b> . . . . .                     | <b>5</b>  | 14.4      | Trademarks . . . . .                 | 39        |
| <b>8</b>  | <b>Thermal characteristics</b> . . . . .             | <b>5</b>  | <b>15</b> | <b>Contact information</b> . . . . . | <b>39</b> |
| <b>9</b>  | <b>Static characteristics</b> . . . . .              | <b>6</b>  | <b>16</b> | <b>Contents</b> . . . . .            | <b>40</b> |
| <b>10</b> | <b>Dynamic characteristics</b> . . . . .             | <b>9</b>  |           |                                      |           |
| 10.1      | Dynamic characteristics . . . . .                    | 9         |           |                                      |           |
| 10.2      | Clock and digital output timing . . . . .            | 10        |           |                                      |           |
| 10.3      | SPI timings . . . . .                                | 13        |           |                                      |           |
| 10.4      | Typical characteristics . . . . .                    | 13        |           |                                      |           |
| <b>11</b> | <b>Application information</b> . . . . .             | <b>16</b> |           |                                      |           |
| 11.1      | Device control . . . . .                             | 16        |           |                                      |           |
| 11.1.1    | SPI and Pin control modes . . . . .                  | 16        |           |                                      |           |
| 11.1.2    | Operating mode selection . . . . .                   | 16        |           |                                      |           |
| 11.1.3    | Selecting the output data standard . . . . .         | 16        |           |                                      |           |
| 11.1.4    | Selecting the output data format . . . . .           | 17        |           |                                      |           |
| 11.2      | Analog inputs . . . . .                              | 17        |           |                                      |           |
| 11.2.1    | Input stage . . . . .                                | 17        |           |                                      |           |
| 11.2.2    | Anti-kickback circuitry . . . . .                    | 18        |           |                                      |           |
| 11.2.3    | Transformer . . . . .                                | 18        |           |                                      |           |
| 11.3      | System reference and power management . . . . .      | 19        |           |                                      |           |
| 11.3.1    | Internal/external references . . . . .               | 19        |           |                                      |           |
| 11.3.2    | Programmable full-scale . . . . .                    | 21        |           |                                      |           |
| 11.3.3    | Common-mode output voltage ( $V_{O(cm)}$ ) . . . . . | 22        |           |                                      |           |
| 11.3.4    | Biasing . . . . .                                    | 22        |           |                                      |           |
| 11.4      | Clock input . . . . .                                | 22        |           |                                      |           |
| 11.4.1    | Drive modes . . . . .                                | 22        |           |                                      |           |
| 11.4.2    | Equivalent input circuit . . . . .                   | 23        |           |                                      |           |
| 11.4.3    | Duty cycle stabilizer . . . . .                      | 24        |           |                                      |           |
| 11.4.4    | Clock input divider . . . . .                        | 24        |           |                                      |           |
| 11.5      | Digital outputs . . . . .                            | 24        |           |                                      |           |
| 11.5.1    | Digital output buffers: CMOS mode . . . . .          | 24        |           |                                      |           |
| 11.5.2    | Digital output buffers: LVDS DDR mode . . . . .      | 25        |           |                                      |           |
| 11.5.3    | DAta Valid (DAV) output clock . . . . .              | 26        |           |                                      |           |
| 11.5.4    | Out-of-Range (OTR) . . . . .                         | 26        |           |                                      |           |
| 11.5.5    | Digital offset . . . . .                             | 26        |           |                                      |           |
| 11.5.6    | Test patterns . . . . .                              | 26        |           |                                      |           |
| 11.5.7    | Output codes versus input voltage . . . . .          | 27        |           |                                      |           |
| 11.6      | Serial peripheral interface . . . . .                | 27        |           |                                      |           |
| 11.6.1    | Register description . . . . .                       | 27        |           |                                      |           |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011. All rights reserved.

For more information, please visit: <http://www.nxp.com>  
 For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)  
 Date of release: 25 January 2011  
 Document identifier: ADC1610S\_SER