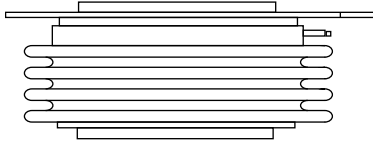


## Phase Control Thyristors (Hockey PUK Version), 1473 A



A-24 (K-PUK)

**FEATURES**

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case A-24 (K-PUK)
- High profile hockey PUK
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
COMPLIANT

**PRODUCT SUMMARY**

$I_{T(AV)}$	1473 A
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**TYPICAL APPLICATIONS**

- DC motor controls
- Controlled DC power supplies
- AC controllers

**MAJOR RATINGS AND CHARACTERISTICS**

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		1473	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		2913	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	20.0	A
	60 Hz	21.2	
$I^2t$	50 Hz	2000	kA <sup>2</sup> s
	60 Hz	1865	
$I^2\sqrt{t}$		20 000	kA <sup>2</sup> √s
$V_{DRM}/V_{RRM}$	Range	1200 to 2600	V
$t_q$	Typical	300	μs
$T_J$	Range	- 40 to 125	°C

**ELECTRICAL SPECIFICATIONS**
**VOLTAGE RATINGS**

TYPE NUMBER	VOLTAGE CODE	$V_{RRM}$ , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}$ MAXIMUM AT $T_J = 125\text{ °C}$ mA
ST1000C..K	12	1200	1300	100
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	
	22	2200	2300	
	24	2400	2500	
	26	2600	2700	



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave Double side (single side) cooled		1473 (630)	A
				55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		6540	A
Maximum peak, one-cycle, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reappplied	20.0	kA
		t = 8.3 ms		21.2	
		t = 10 ms	100 % $V_{RRM}$ reappplied	17.0	
		t = 8.3 ms		18.1	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied	2000	kA <sup>2</sup> s
		t = 8.3 ms		1865	
		t = 10 ms	100 % $V_{RRM}$ reappplied	1445	
		t = 8.3 ms		1360	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		20 000	kA <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		0.950	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > $\pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		1.024	
Low level value of on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		0.283	mΩ
High level value of on-state slope resistance	$r_{t2}$	(I > $\pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		0.265	
Maximum on-state voltage drop	$V_{TM}$	$I_{pk} = 3000$ A, $T_J = 125$ °C, $t_p = 10$ ms sine pulse		1.80	V
Maximum holding current	$I_H$	$T_J = 25$ °C, anode supply 12 V resistive load		600	mA
Typical latching current	$I_L$			1000	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	$di/dt$	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage $\leq 80$ % $V_{DRM}$		1000	A/μs
Typical delay time	$t_d$	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67$ % $V_{DRM}$ , $T_J = 25$ °C		1.9	μs
Typical turn-off time	$t_q$	$I_{TM} = 550$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs		300	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum linear to 80 % rated $V_{DRM}$		500	V/μs
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied		100	mA



<b>TRIGGERING</b>						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		16		W
Maximum peak average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$		3		
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3.0		A
Maximum peak positive gate voltage	$+V_{GM}$			20		
Maximum peak negative gate voltage	$-V_{GM}$			5.0		
DC gate current required to trigger	$I_{GT}$	$T_J = -40$ °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	200	-	mA
		$T_J = 25$ °C		100	200	
		$T_J = 125$ °C		50	-	
DC gate voltage required to trigger	$V_{GT}$	$T_J = -40$ °C		1.4	-	V
		$T_J = 25$ °C		1.1	3.0	
		$T_J = 125$ °C		0.9	-	
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated $V_{DRM}$ anode to cathode applied	10		mA
DC gate voltage not to trigger	$V_{GD}$			0.25		V

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum operating temperature range	$T_J$			- 40 to 125	°C
Maximum storage temperature range	$T_{Stg}$			- 40 to 150	
Maximum thermal resistance, junction to heatsink	$R_{thJ-hs}$	DC operation single side cooled		0.042	K/W
		DC operation double side cooled		0.021	
Maximum thermal resistance, case to heatsink	$R_{thC-hs}$	DC operation single side cooled		0.006	
		DC operation double side cooled		0.003	
Mounting force, $\pm 10$ %				24 500 (2500)	N (kg)
Approximate weight				425	g
Case style		See dimensions - link at the end of datasheet		A-24 (K-PUK)	

<b><math>\Delta R_{thJC}</math> CONDUCTION</b>						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.003	0.003	0.002	0.002	$T_J = T_J$ maximum	K/W
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

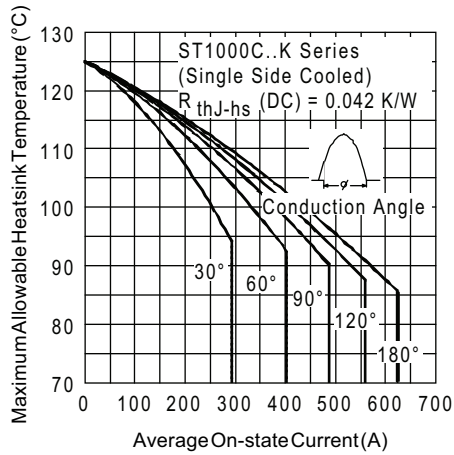


Fig. 1 - Current Ratings Characteristics

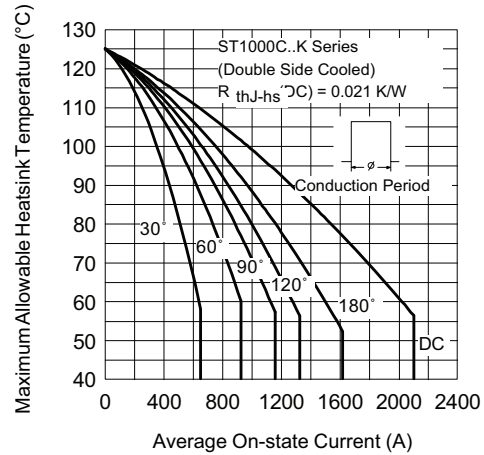


Fig. 4 - Current Ratings Characteristics

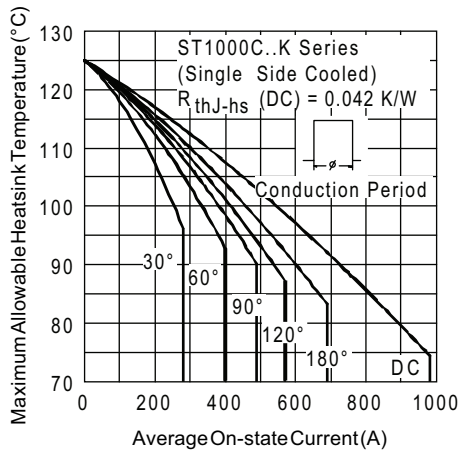


Fig. 2 - Current Ratings Characteristics

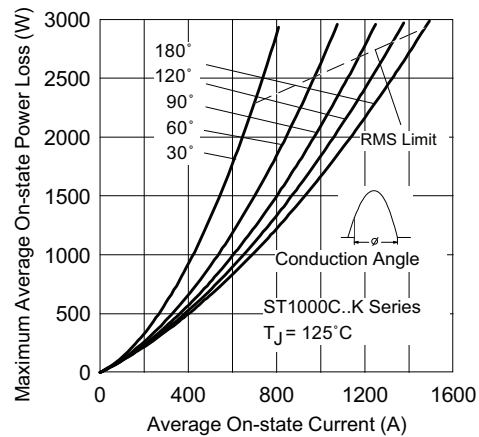


Fig. 5 - On-State Power Loss Characteristics

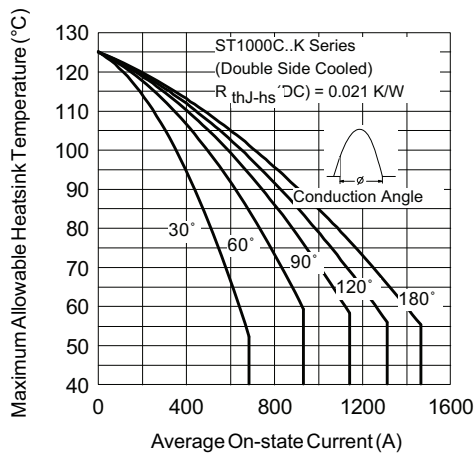


Fig. 3 - Current Ratings Characteristics

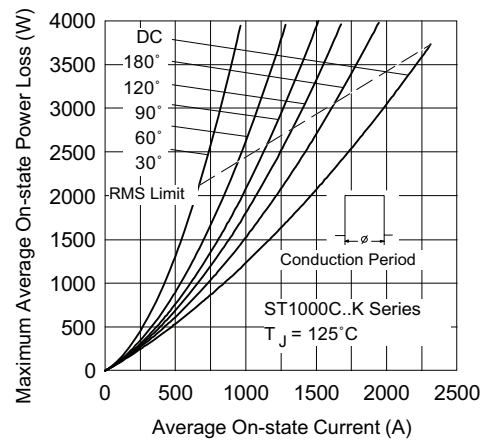


Fig. 6 - On-State Power Loss Characteristics

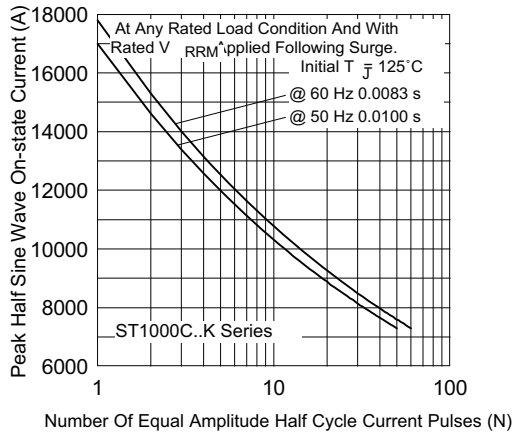


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

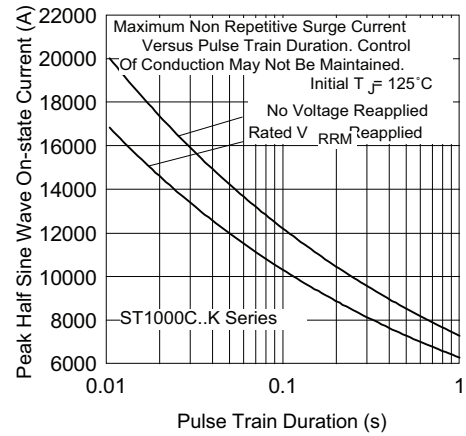


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

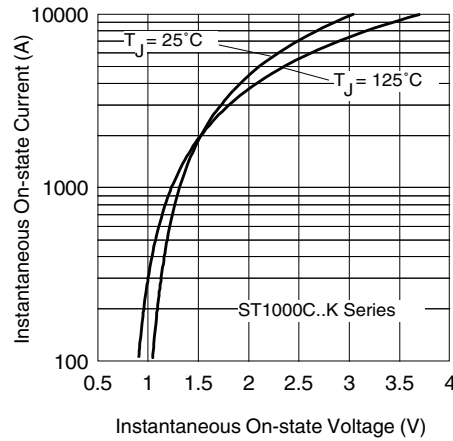


Fig. 9 - On-State Voltage Drop Characteristics

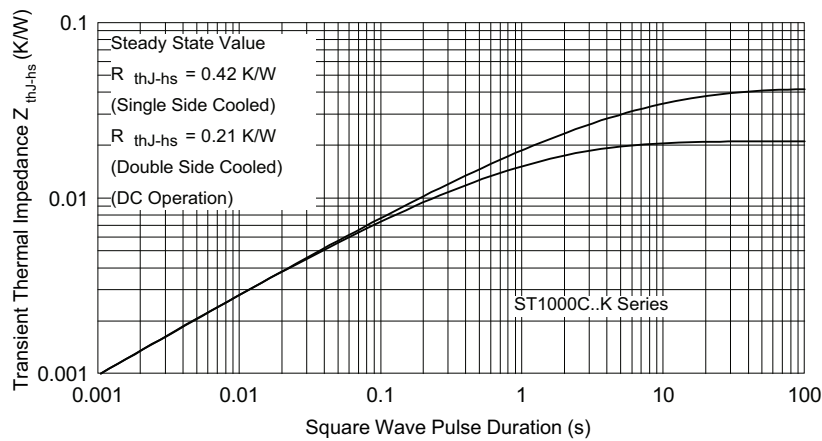


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics

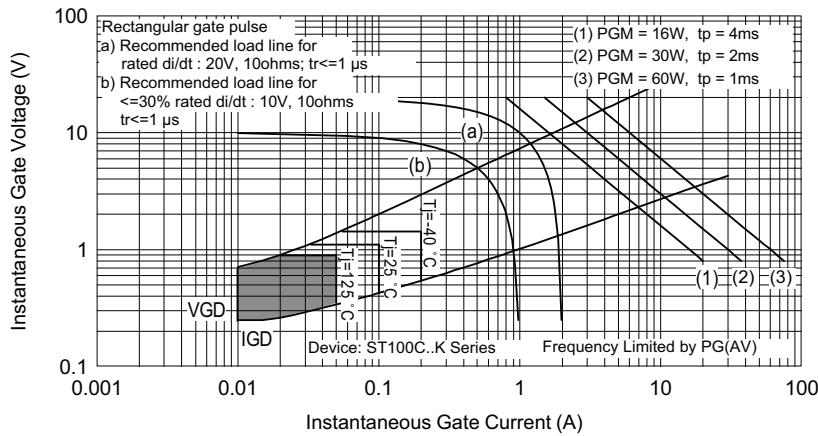


Fig. 11 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	<b>ST</b>	<b>100</b>	<b>0</b>	<b>C</b>	<b>26</b>	<b>K</b>	<b>1</b>	<b>-</b>
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

- 1** - Thyristor
- 2** - Essential part number
- 3** - 0 = Converter grade
- 4** - C = Ceramic PUK
- 5** - Voltage code x 100 =  $V_{RRM}$  (see Voltage Ratings table)
- 6** - K = PUK case A-24 (K-PUK)
- 7** - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)  
 1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)  
 2 = Eyelet terminals (gate and auxiliary cathode soldered leads)  
 3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
- 8** - Critical dV/dt: • None = 500 V/μs (standard selection)  
 • L = 1000 V/μs (special selection)

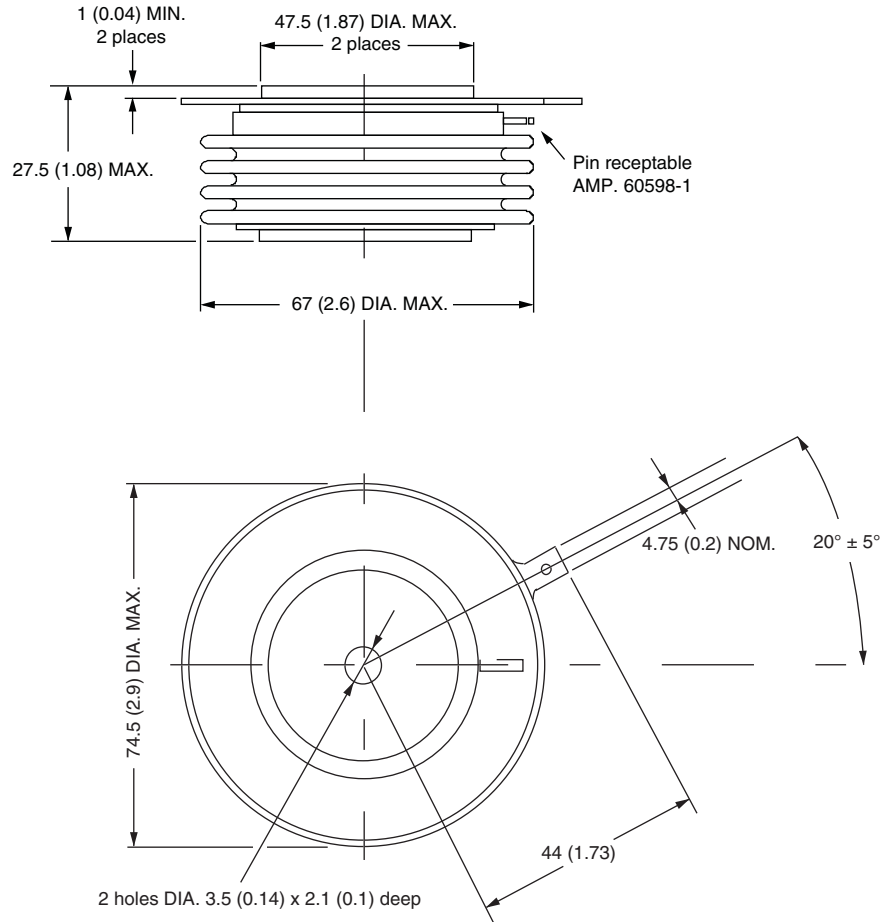
### LINKS TO RELATED DOCUMENTS

Dimensions	<a href="http://www.vishay.com/doc?95081">www.vishay.com/doc?95081</a>
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## A-24 (K-PUK)

**DIMENSIONS** in millimeters (inches)

Creepage distance: 28.88 (1.137) minimum  
 Strike distance: 17.99 (0.708) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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