

## High Voltage Power Operational Amplifiers

### FEATURES

- ◆ HIGH VOLTAGE — 400V (±200V)
- ◆ LOW QUIESCENT CURRENT — 10mA
- ◆ HIGH OUTPUT CURRENT — 8A
- ◆ PROGRAMMABLE CURRENT LIMIT

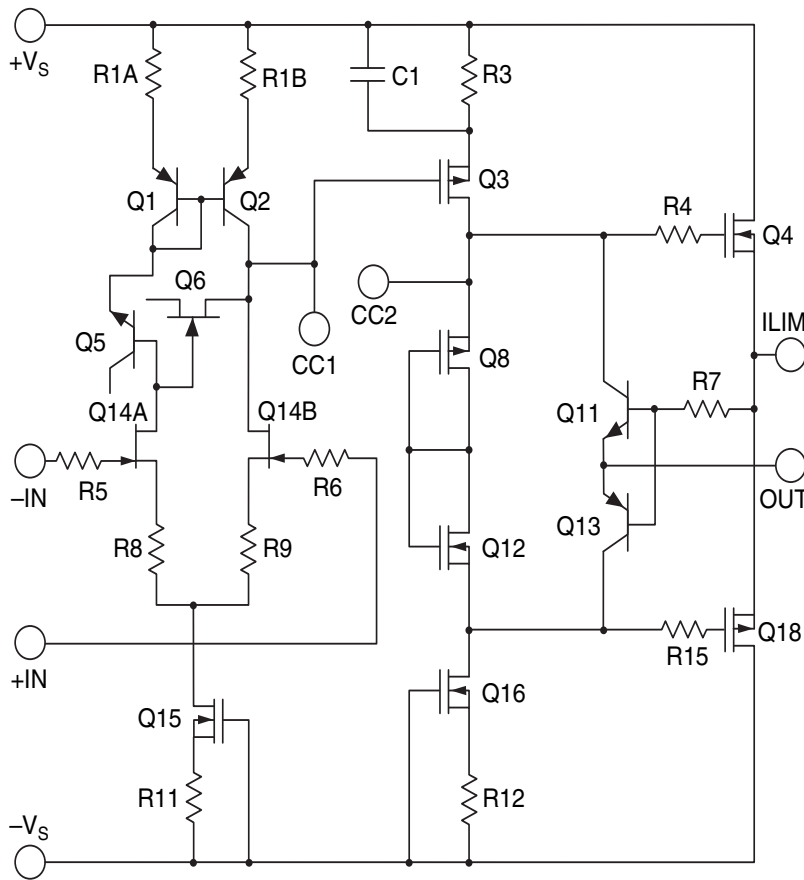
### APPLICATIONS

- ◆ PIEZOELECTRIC POSITIONING
- ◆ HIGH VOLTAGE INSTRUMENTATION
- ◆ ELECTROSTATIC TRANSDUCERS
- ◆ PROGRAMMABLE POWER SUPPLIES UP TO 390V

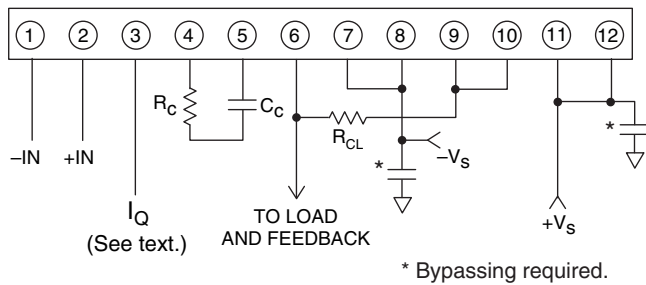
### DESCRIPTION

The PA93/27 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 8A and pulse currents up to 14A. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP package uses a minimum of board space allowing for high density circuit boards. The Power SIP package is electrically isolated.

### EQUIVALENT SCHEMATIC



## EXTERNAL CONNECTIONS



PATENTED

**12-pin SIP  
PACKAGE  
STYLE DP**

Formed leads available  
See package style EE

## 1. CHARACTERISTICS AND SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_s$ to $-V_s$			400	V
OUTPUT CURRENT, source, sink, peak, within SOA			14	A
POWER DISSIPATION, continuous @ $T_c = 25^\circ\text{C}$			125	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode		$-V_s$	$V_s$	V
TEMPERATURE, pin solder, 10s max.			260	$^\circ\text{C}$
TEMPERATURE, junction (Note 2)			150	$^\circ\text{C}$
TEMPERATURE RANGE, storage		-40	85	$^\circ\text{C}$
OPERATING TEMPERATURE RANGE, case		-25	85	$^\circ\text{C}$

**CAUTION** The PA93/27 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of  $850^\circ\text{C}$  to avoid generating toxic fumes.

### SPECIFICATIONS

Parameter	Test Conditions <sup>1</sup>	Min	Typ	Max	Units
<b>INPUT</b>					
OFFSET VOLTAGE, initial			2	10	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	$\mu\text{V}/^\circ\text{C}$
OFFSET VOLTAGE vs. supply			10	25	$\mu\text{V}/\text{V}$
OFFSET VOLTAGE vs. time			75		$\mu\text{V}/\text{kHz}$
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			$10^{11}$		$\Omega$
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)		$\pm V_s \mp 15$			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90\text{V}$	80	98		dB
NOISE	100kHz bandwidth, $R_s = 1\text{K}\Omega$ , $C_c = 10\text{pF}$		1		$\mu\text{V RMS}$

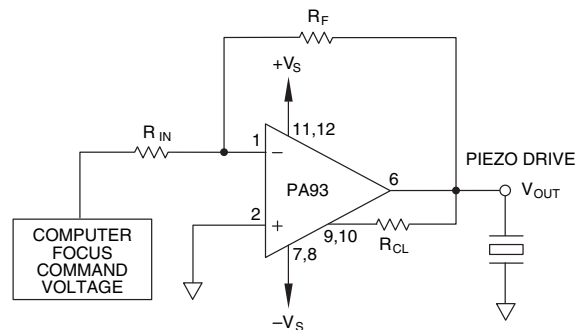
Parameter	Test Conditions <sup>1</sup>	Min	Typ	Max	Units
<b>GAIN</b>					
OPEN LOOP, @ 15Hz	$R_L = 2K\Omega, C_C = 10pF$	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$R_L = 2K\Omega, C_C = 10pF$		12		MHz
POWER BANDWIDTH	$R_L = 2K\Omega, C_C = 10pF$		30		kHz
PHASE MARGIN	Full temp range		60		°
<b>OUTPUT</b>					
VOLTAGE SWING (Note 3)	$I_o = 8A$	$\pm V_s \mp 12$	$\pm V_s \mp 10$		V
CURRENT, continuous		8			A
SLEW RATE, $A_v = 100$	$C_C = 10pF$		50		V/ $\mu$ S
CAPACITIVE LOAD, $A_v = +1$	Full temp range	1			nF
SETTLING TIME to 0.1%	$C_C = 10pF, 2V$ step		1		$\mu$ S
RESISTANCE, no load			10		$\Omega$
<b>POWER SUPPLY</b>					
VOLTAGE (Note 5)		$\pm 40$	$\pm 150$	$\pm 200$	V
CURRENT, quiescent		9.5	11	14	mA
<b>THERMAL</b>					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, $F > 60Hz$			0.7	°C/W
RESISTANCE, DC, junction to case	Full temp range, $F < 60Hz$			1	°C/W
RESISTANCE, junction to air	Full temp range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	°C

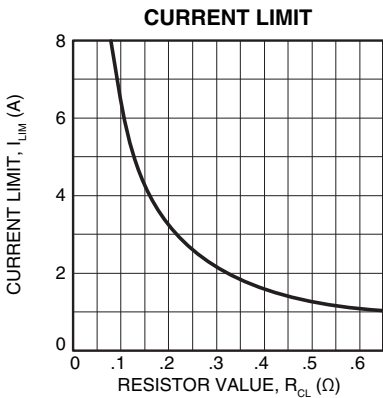
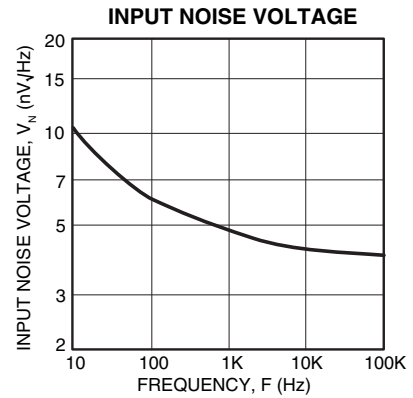
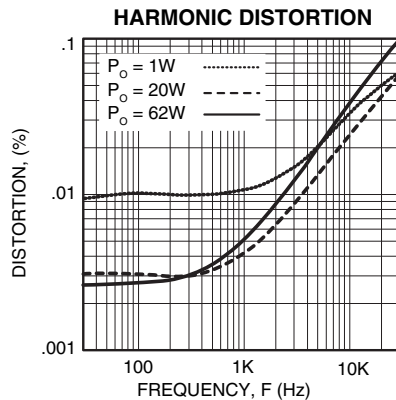
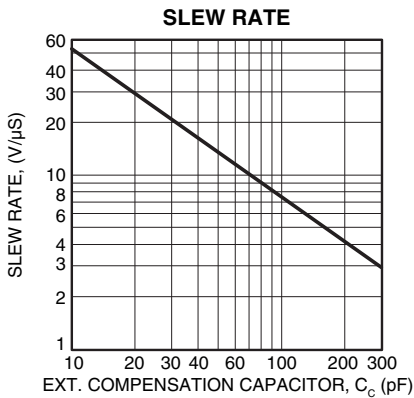
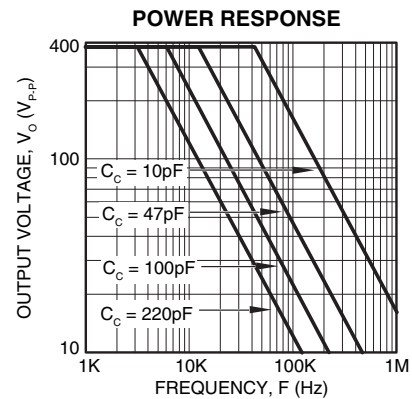
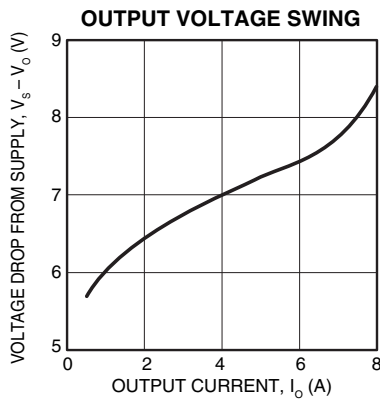
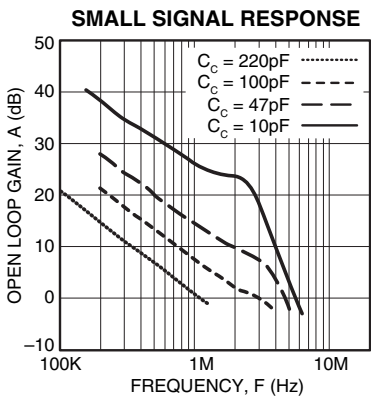
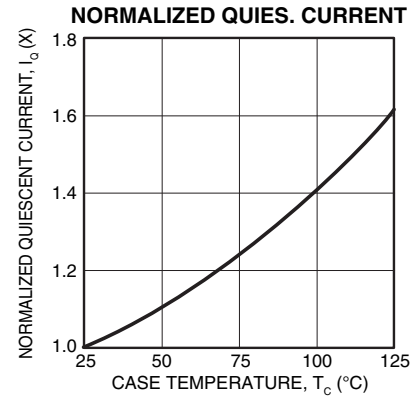
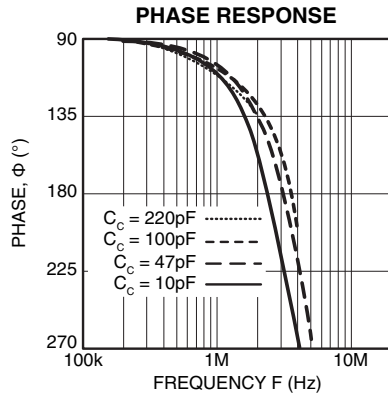
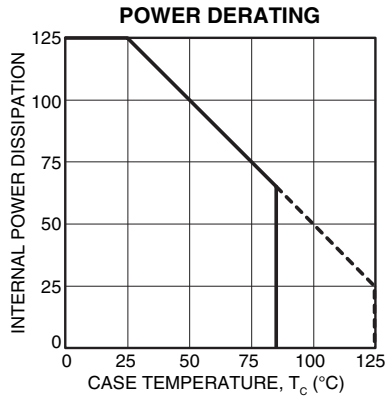
- NOTES: 1. Unless otherwise noted:  $T_C = 25^\circ C$ , DC input specifications are  $\pm$  value given. Power supply voltage is typical rating.  $R_C = 100 \Omega, C_C = 220pF$ .
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3.  $+V_s$  and  $-V_s$  denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

## TYPICAL APPLICATION

### LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA93/27 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.





## PHASE COMPENSATION

GAIN	C <sub>c</sub> *	R <sub>c</sub>
≥1	220pF	100Ω
≥2	100pF	100Ω
≥4	47pF	0Ω
≥17	10pF	0Ω

\*C<sub>c</sub> Never to be <10pF. C<sub>c</sub> to be rated for the full supply voltage +V<sub>s</sub> to -V<sub>s</sub>. Use ceramic NPO (COG) type.

## GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.cirrus.com](http://www.cirrus.com) for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

## CURRENT LIMIT

For proper operation, the current limit resistor (R<sub>CL</sub>) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 16 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

## SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

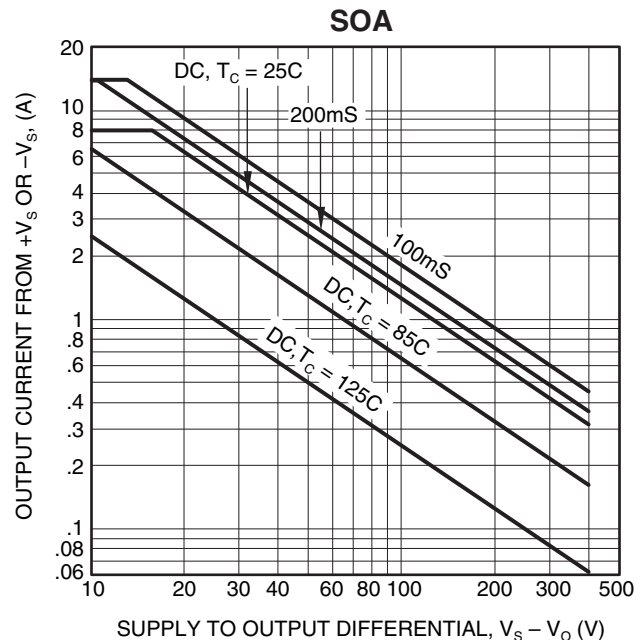
NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

## SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.

## INPUT PROTECTION

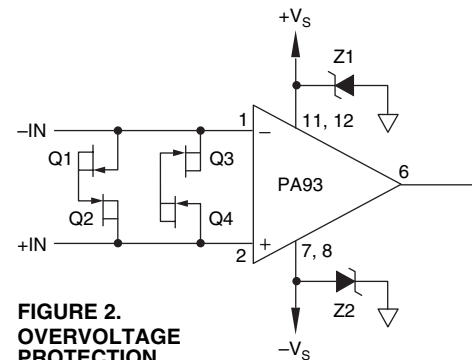
Although the PA93/27 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.



## POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzors prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.



**FIGURE 2.**  
**OVERVOLTAGE**  
**PROTECTION**

## STABILITY

The PA93/27 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor  $C_c$  must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network  $C_c R_c$  must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

## QUIESCENT CURRENT REDUCTION

When pin 3 ( $I_Q$ ) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

## CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.

For inquiries via email, please contact [tucson.support@cirrus.com](mailto:tucson.support@cirrus.com).

International customers can also request support by contacting their local Cirrus Logic Sales Representative.

To find the one nearest to you, go to [www.cirrus.com](http://www.cirrus.com)

### IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs, Apex Precision Power, Apex and the Apex Precision Power logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.