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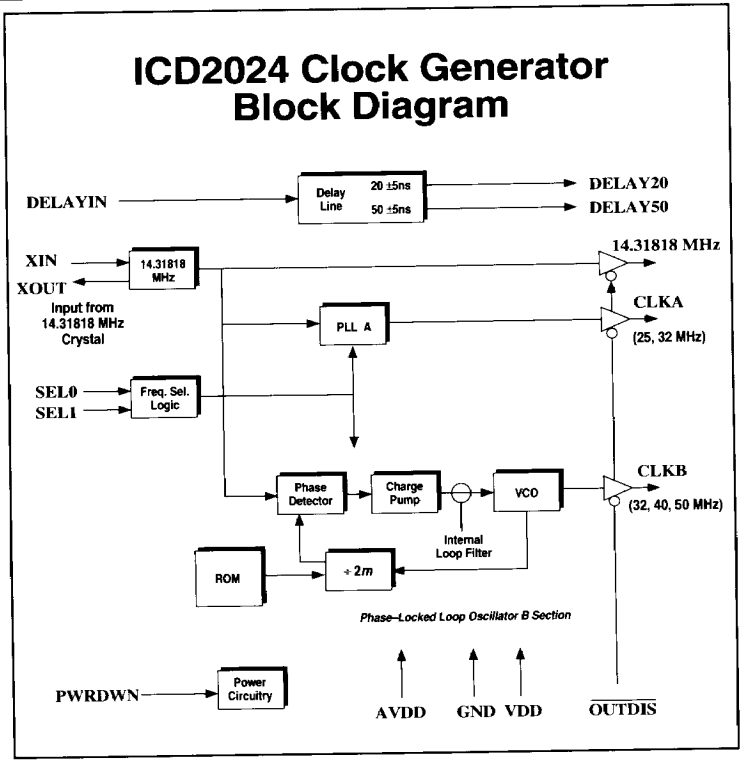
ICD2024

AMD286™ LX / AMD286™ ZX Clock Generator

Supports AMD's "AT-on-a-Chip" Microprocessors

- 1 Fixed, 2 Selectable Clock Outputs
- Dual-Tapped Delay Line Supports both Memory Refresh and DMA Timing
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Ideally Suited for use with AMD286™ LX / AMD286™ ZX Integrated Processors
- Tri-State Oscillator Control Disables Outputs for Test Purposes
- Power-Down Circuitry Disables Unnecessary Clock Outputs to Reduce Power Consumption
- Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 5 Volt Operation
- Low-Power, High-Speed 1.25µ CMOS Technology
- Available in 16–Pin DIP or SOIC Package Configuration

ICD2024 Clock Generator Block Diagram



NOTE:
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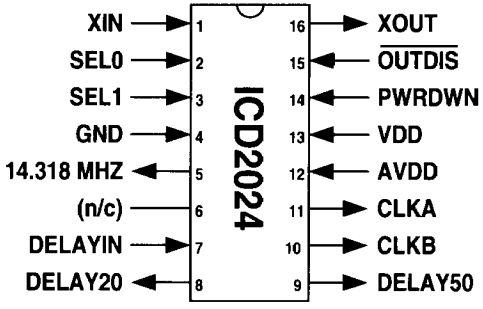
Pin Descriptions



Signal Descriptions

Signal	Pin #	Signal Function
XIN	1	Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available.
SEL0	2	Bit 0 (LSB) of the frequency select logic, used to set oscillator frequencies
SEL1	3	Bit 1 (MSB) of the frequency select logic, used to set oscillator frequencies
GND	4	Ground
14.318 MHz	5	14.31818 MHz output
(n/c)	6	No connection
DELAYIN	7	Input to Delay Line
DELAY20	8	20 nsec delay, ±5 nsec
DELAY50	9	50 nsec delay, ±5 nsec
CLKB	10	Oscillator B output (32, 40 or 50 MHz)
CLKA	11	Oscillator A output (25 or 32 MHz)
AVDD	12	+5 volts to Analog Core
VDD	13	+5 volts to I/O Ring
PWRDWN	14	Power Down Mode active when signal pulled high. (Internal pull-up allows Power Down Mode if no active device is driving this pin.)
OUTDIS–	15	Output Disable (Tri-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if tri-state operation not needed.)
XOUT	16	Oscillator Output to a 14.31818 MHz Series-Resonant Crystal. (Not used if the PC System Bus Clock Signal is utilized.)

General

A new family of single-chip multi-function microprocessors allows unparalleled flexibility in designing personal computer systems, particularly those in which size and power are primary constraints. A new generation of frequency synthesis parts from IC DESIGNS is designed to mate with these microprocessors and supply necessary timing functions (clocks and delay lines). These parts synthesize all the required frequencies in a single monolithic device, lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2024 Clock Generator offers 1 oscillator, 2 phase-locked loops, and a two-output delay line in a single package. The oscillators may be changed "on the fly" to any one of four preset frequency pairs (40 & 32 MHz, 40 & 25 MHz, 50 & 32 MHz, 32 & 25 MHz). The ICD2024 is ideally suited for use in existing designs which utilize the AMD286™LX / AMD286™ZX "AT-on-a-Chip" microprocessors.

CLKA & CLKB Selectable Oscillator Operation

The CLKA & CLKB Oscillator Outputs may be set via the select lines SEL0 & SEL1 to one of four preset frequency pairs, as detailed in the table below:

CLKA & CLKB Output Selection

SEL1	SEL0	CLKA	CLKB
0	0	32 MHz	40 MHz
0	1	25 MHz	40 MHz
1	0	32 MHz	50 MHz
1	1	25 MHz	32 MHz

Tri-State Output Operation

The OUTDIS– signal, when pulled low, will tri-state all the clock output lines (but not the delay line outputs). This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OUTDIS– signal contains an internal pull-up; it can be left unconnected if tri-state operation is not required.

Dual-Tap Delay Line

The ICD2024 contains a voltage and temperature stabilized delay line with two fixed delays of 20 ns and 50 ns (±5 ns).

Power-Down Circuitry

When the PWRDWN signal is pulled high, the ICD2024 enters its power-down mode of operation. During power-down mode, the CLKB output and CLKB phase-locked loop are shut down, thereby reducing power consumption.

No External Components Required

Under normal conditions no external components other than the crystal are required for proper operation of any of the internal circuitry of the ICD2024.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout in order to accommodate a single source of all clocks.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µf multi-layer ceramic capacitor and a 2.2µf/10V tantalum capacitor wired in parallel and connected to the system power (+5V) through a 22Ω resistor. Both capacitors should be placed within 0.15" of the power pin.

The designer should also avoid routing any of the output traces of the ICD2024 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2024 closest to the device requiring the highest frequency.

For more details concerning layout and power considerations, please see the IC DESIGNS Application Notes *Power Feed and Board Layout Issues* and *Minimizing Radio Frequency Emissions*.

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is 14.31818 MHz, and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for motherboard designs.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2024 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2024, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

Ordering Information

Part Number	Package Type	Temperature Range
ICD2024	P = 16–Pin Plastic DIP	C = Commercial (0°C – +70°C)
	C = 16–Pin Ceramic DIP	
	S = 16–Pin SOIC	

Example: order *ICD2024PC* for the ICD2024, 16–pin plastic DIP, commercial temperature range device.

Electrical Data

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input Voltage with respect to GND	–0.5	VDD + 0.5	Volts
T_{OPER}	Operating Temperature	0	+70	°C
T_{STOR}	Storage Temperature	–65	+150	°C
T_{SOL}	Max Soldering Temperature (10 sec)		+260	°C
T_J	Junction Temperature		+125	°C
P_{DISS}	Power Dissipation		350	mWatts

DC Characteristics

VDD = +5V ±5%
0°C ≤ T_{CASE} ≤ +70°C

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level output voltage	2.4		Volts	I_{OH} = –4.0ma
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0ma
V_{BATT}	Backup battery voltage	2.0	5.0	Volts	
I_{IH}	Input high current		100	µa	V_{IH} = 5.25V
I_{IL}	Input low current		–250	µa	V_{IL} = 0V
I_{OZ}	Output leakage current		10	µa	(tri-state)
I_{DD}	Power supply current	25	45	ma	
I_{DD-PD}	Power-down supply current		15	ma	
C_{IN}	Input Capacitance		10	pf	

AC Characteristics

VDD = +5V ±5%
0°C ≤ T_{CASE} ≤ +70°C

Symbol	Name	Description	Min	Max	Units
t_1	ref freq	Reference Oscillator nominal value		14.31818	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as t_2/t_1	45%	55%	
t_3	rise time	Rise time for the output oscillators into a 25pf load		3	ns
t_4	fall time	Fall time for the output oscillators into a 25pf load		3	ns
t_5	clk unstable	Time the output oscillators remain valid after the S0, S1 select signals change value		0	ns
t_6	clk stable	Time required for the output oscillators to become valid after the S0, S1 select signals change value		10	msec
t_7	tri-state	Time for the output oscillators to go into tri-state mode after OUTDIS– signal assertion		12	ns
t_8	clk valid	Time for the output oscillators to recover from tri-state mode after OUTDIS– signal goes high		12	ns
t_9	DELAY20	20ns-delayed output	15	25	ns
t_{10}	DELAY50	50ns-delayed output	45	55	ns