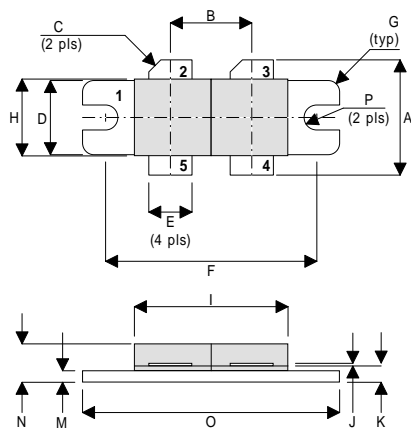


MECHANICAL DATA



DR

PIN 1	SOURCE (COMMON)	PIN 2	DRAIN 1
PIN 3	DRAIN 2	PIN 4	GATE 2
PIN 5	GATE 1		

DIM	Millimetres	Tol.	Inches	Tol.
A	19.05	0.50	0.75	0.020
B	10.77	0.13	0.424	0.005
C	45°	5°	45°	5°
D	9.78	0.13	0.385	0.005
E	5.71	0.13	0.225	0.005
F	27.94	0.13	1.100	0.005
G	1.52R	0.13	0.060R	0.005
H	10.16	0.13	0.400	0.005
I	22.22	MAX	0.875	MAX
J	0.13	0.02	0.005	0.001
K	2.72	0.13	0.107	0.005
M	1.70	0.13	0.067	0.005
N	5.08	0.50	0.200	0.020
O	34.03	0.13	1.340	0.005
P	1.61R	0.08	0.064R	0.003

**GOLD METALLISED
MULTI-PURPOSE SILICON
DMOS RF FET
350W – 50V – 175MHz
PUSH-PULL**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 13 dB MINIMUM

APPLICATIONS

- VHF/UHF COMMUNICATIONS
from 1 MHz to 200 MHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	438W
BV_{DSS}	Drain – Source Breakdown Voltage*	125V
BV_{GSS}	Gate – Source Breakdown Voltage*	±20V
$I_{D(sat)}$	Drain Current*	21A
T_{stg}	Storage Temperature	-65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

* Per Side

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
PER SIDE							
B _V DSS	Drain–Source Breakdown Voltage	V _{GS} = 0	I _D = 100mA	125			V
I _D DSS	Zero Gate Voltage Drain Current	V _{DS} = 50V	V _{GS} = 0			7	mA
I _G DSS	Gate Leakage Current	V _{GS} = 20V	V _{DS} = 0			1	μA
V _{GS(th)}	Gate Threshold Voltage*	I _D = 10mA	V _{DS} = V _{GS}	1		7	V
g _{fs}	Forward Transconductance*	V _{DS} = 10V	I _D = 3.5A	5.6			mhos
V _{GS(th)match}	Gate Threshold Voltage Matching Between Sides	I _D = 10mA	V _{DS} = V _{GS}			0.1	V
TOTAL DEVICE							
G _{PS}	Common Source Power Gain	P _O = 350W		13			dB
η	Drain Efficiency	V _{DS} = 50V I _{DQ} = 1.4A		50			%
VSWR	Load Mismatch Tolerance	f = 175MHz		20:1			—
PER SIDE							
C _{iss}	Input Capacitance	V _{DS} = 50V	V _{GS} = -5V f = 1MHz			420	pF
C _{oss}	Output Capacitance	V _{DS} = 50V	V _{GS} = 0 f = 1MHz			175	pF
C _{rss}	Reverse Transfer Capacitance	V _{DS} = 50V	V _{GS} = 0 f = 1MHz			10.5	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 0.4°C / W
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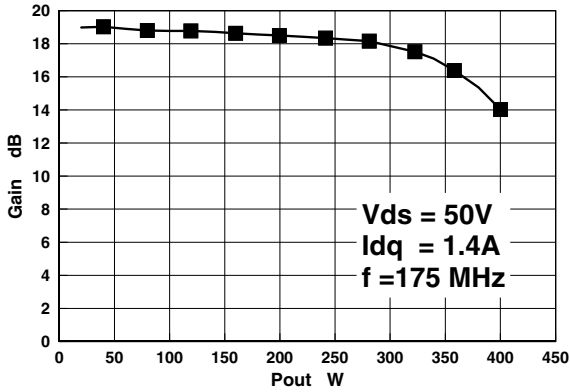


Figure 1 – Gain vs. Output Power.

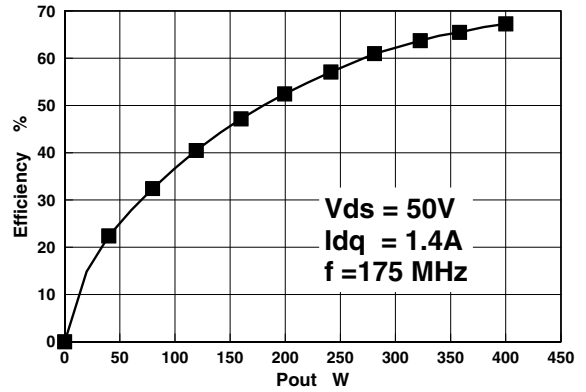


Figure 2 – Efficiency vs. Output Power.

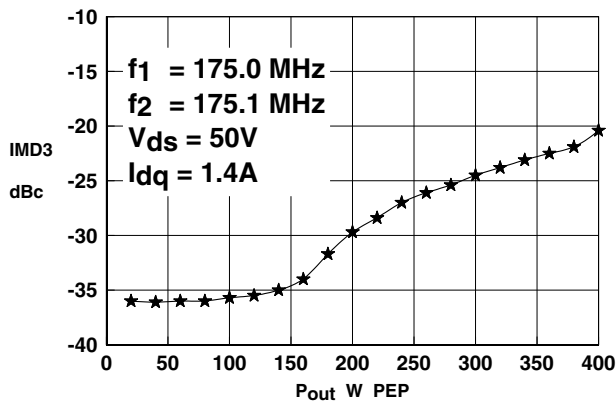


Figure 3 – IMD vs. Output Power.

D5029UK OPTIMUM SOURCE AND LOAD IMPEDANCE @ 350W / 50V

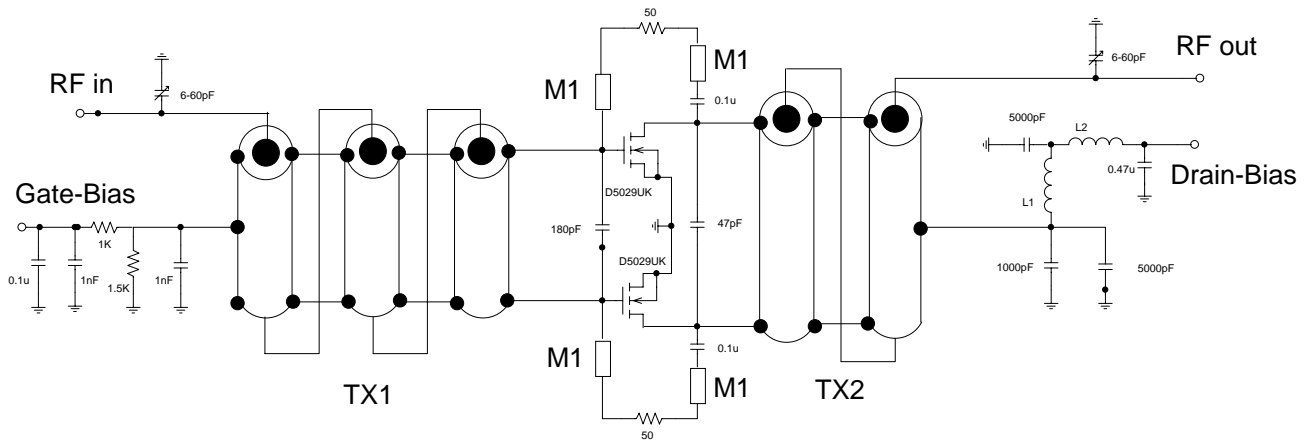
Frequency MHz	Z _S Ω	Z _L Ω
175	1.0 + j1.2	2.6 + j1.3

Typical S Parameters

! V_{DS} = 50V, I_{DQ} = 1.4A
MHz S MA R 50

Freq MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
50	0.83	-165.3	20.29	69.4	0.007	-9.2	0.63	-150.7
100	0.89	-170.0	8.28	48.6	0.004	-6.0	0.78	-156.6
150	0.93	-173.2	4.42	35.6	0.003	50.0	0.86	-162.0
200	0.95	-175.7	2.71	27.2	0.005	82.4	0.91	-166.2
250	0.97	-177.8	1.82	21.3	0.008	88.8	0.94	-169.4
300	0.98	-179.7	1.30	17.0	0.011	90.0	0.95	-171.9
350	0.98	-178.7	0.97	13.8	0.014	89.6	0.97	-174.0
400	0.98	-177.3	0.76	11.4	0.017	88.9	0.97	-175.7
450	0.99	-175.9	0.61	9.5	0.020	87.9	0.98	-177.3
500	0.99	-174.7	0.50	8.1	0.023	86.9	0.98	-178.6
550	0.99	-173.5	0.42	7.1	0.026	85.9	0.98	-179.8
600	0.99	-172.3	0.35	6.5	0.028	84.9	0.99	-179.0

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TX1 9:1 transformer. 3 turns of 062-25 semi-rigid coax around 75-26 powdered iron core

TX2 4:1 transformer. 2 turns of 090-25 semi-rigid coax around 100-8 powdered iron core

L1 10 turns 16 awg enamelled wire, 5mm internal diameter

L2 0.5 turns 16 awg enamelled wire on A1 x 1 2-hole core

M1 microstrip line, 20mm long, 1mm wide on 0.062in thick G10 substrate

D5029UK 175MHz TEST FIXTURE