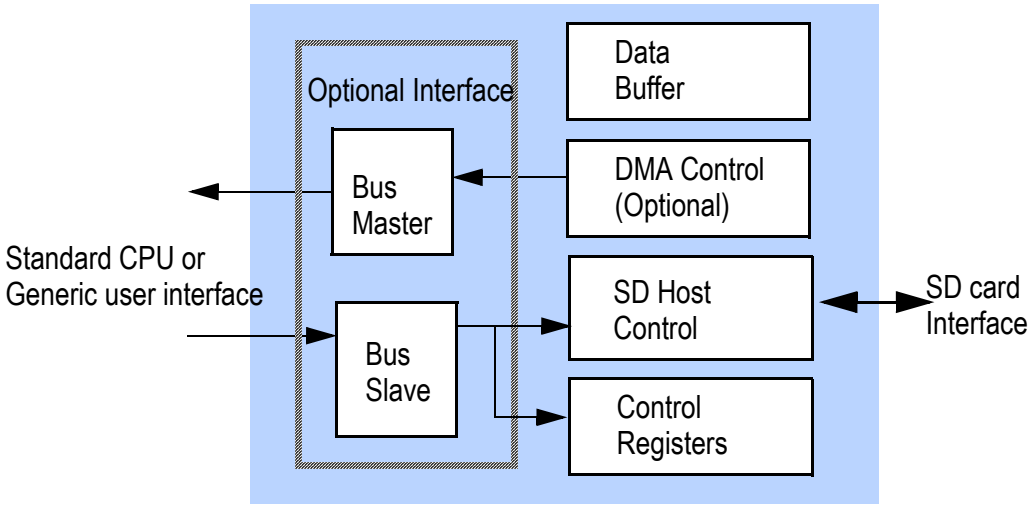
EP550 SDIO/SD Memory/MMC Host Controller

FEATURES

- Host controller for Secure Digital (SD), SDIO, SD combo, and MultiMedia Card (MMC) bus.
- Allows host CPU to access SD and MMC devices.
- Compatible with SD 2.0, including high capacity (SDHC) and 8-bit MMC 4.2 specifications.
- Many choices of CPU interfaces, including AHB, APB, SH4, Wishbone, PCI and generic user interface.
- Supports SDMA operation with option to remove SDMA for very small gate count implementation.
- Selectable data buffer size from 512 to 16Kbytes.
- Hardware support of CRC error detection and interrupt generation.
- Supports multi-function SD cards including command suspend, resume, and read wait.
- Option to operate user interface and card control at different clock domains.
- Supports all SD-enabled operating systems including Windows.
- Free source code included for bus driver development.
- Fully sythesizable code ideal for ASIC and FPGA implementations.
- Fully static design with edge triggered flip-flops.

BLOCK DIAGRAM



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EP550 SD/SDIO/MMC Host Controller

Description

The EP550 is a host controller for SD memory, SDIO, SD combo and MMC interface. The core connects the host CPU of the system to the SD card socket. External SD cards can be accessed by the host CPU through the EP550 controller IP core.

SD memory and SDIO are low cost, high speed interfaces designed for removable mass storage and IO devices. It is a very flexible architecture supporting variable clock rate and 1 to 4-bit SD data width. Data rate up to 25Mbyte/sec (200Mbs) can be realized with SD interface. The MMC standard allows up to 8-bit of parallel data to be transferred with data rate of 50Mbyte/sec. Features such as plug and play, auto-detection, error correction, write protection are standard with SD card interface and supported by the EP550.

The EP550 SD card host controller core is designed according to the SD Association's latest SD host controller specification (version 2.0). The core presents itself as a standard register set to the OS and application software. To access the SD card, the host CPU simply issue read/write access to the control registers in the core. The controllers core handles all the SD card protocol automatically including data shifting, timing and CRC generation. The core has an optional DMA controller so that data can be automatically transferred between the system and the SD card without CPU intervention. Because it supports the standard SD register set, the EP550 is automatically recognized by any operating systems that supports the SD bus. No driver development is needed. In applications where there is no operating system of the OS does not have built-in SD support, Eureka provides free source code to help user develop the bus driver.

There are several options for user hardware interface to the controller core. The controller supports generic user interface optimized for on-chip logic interface as well as embedded CPU interface such as AMBA AHB and APB bus, Wishbone, SH4, PCI and generic address/data interface.

With the EP550, SD card interface can be realized with very little development cost and effort. Designer can add SD memory and SDIO interface to the system by simply adding the EP550 module without impacting the rest of the system architecture.

Free Source Code

The EP550 implements the standard SD host controller register set which supports any standard operating systems that supports SD bus. For applications where the user need to develop its own SD driver software, Eureka provides free source code for driver development.

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Optional Features

The EP550 standard core features a simple generic user interface which can be connected easily into any design. In addition, Eureka also offer the EP550 with AHB, APB, SH4, Wishbone and PCI bus interface. For certain interfaces, the bus interface may operate at a different clock domain from the SD host controller. The core is also available with and without DMA.

ACTEL DEVICE UTILIZATION DATA

Family	Device	Utilization				Performance
	(-speed grade)	SEQ	COMB	Total	RAM	
ProASIC3	A3P1000-2	900	3392	17%	2	53Mhz
Axcelerator	AX1000-2	894	2090	16%	2	59Mhz
IGLOO	AGL600V5	996	3633	33%	2	34Mhz
Fusion	AFS1500	900	3429	11%	2	56Mhz

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