

ASM2012CB

DATA SHEET

APLUS INTEGRATED CIRCUITS INC.

Address:

3 F-10, No. 32, Sec. 1, Chenggung Rd., Taipei,
Taiwan 115, R.O.C.
(115)台北市南港區成功路一段 32 號 3 樓之 10.

TEL: 886-2-2782-9266

FAX: 886-2-2782-9255

WEBSITE : <http://www.aplusinc.com.tw>

Sales E-mail: Mr. Jason

sales@plusinc.com.tw

Technology E-mail: Mr. George

service@plusinc.com.tw

ASM2012CB – VERY LOW-COST VOICE SYNTHESIZER WITH 4-BIT MICROPROCESSOR**1.0 General Description**

The AM4DD0207 is very low cost voice synthesizer with 4-bit microprocessor. It has various features including 4-bit ALU, ROM, RAM, I/O ports, timers, clock generator, watchdog timer(WDT), voice synthesizer, etc. It consists of 22 instructions in the device. With CMOS technology and halt function can minimize power dissipation. Its architecture is similar to RISC, with two stages of instruction pipeline. It allows all instructions to be executed in a single cycle, except for program branches and data table read instructions (which need two instruction cycles).

1.1 Feature

- ◆ Single power supply can operate from 2.4V through 5V
- ◆ Internal Program ROM: 4K x 10-bit
- ◆ 1 sets of 16-bit DPR can access up to 64K x 10 bits data memory space
- ◆ Data Registers:
 - 96 x 4-bit data RAM (00-1Fh plus 40h-7Fh)
 - Unbanked special function registers (SFR) range: 20h-3Fh
- ◆ I/O Ports:
 - PRA: 4-bit I/O Port A (2Bh)
 - PRB: 4-bit Output Port B (2Dh)
 - PRC: 4-bit Input Port C (2Fh)
- ◆ On-chip clock generator: Resistive Clock Drive(**RM**)
- ◆ Timer: 1
 - Timer0: a 9-bit auto-reload timer/counter
- ◆ Stack: 2-level subroutine nesting
- ◆ HALT and Release from HALT function to reduce power consumption
- ◆ Watch Dog Timer (**WDT**)
- ◆ Instruction: 1-cycle instruction except for table read and program branches which are 2-cycles
- ◆ Number of instruction: 22
- ◆ The Voice function can be implemented by microprocessor instruction
 - One 8-bit COUT output for ASM2012CB

FIGURE 1.1 : Block Diagram of ASM2012CB

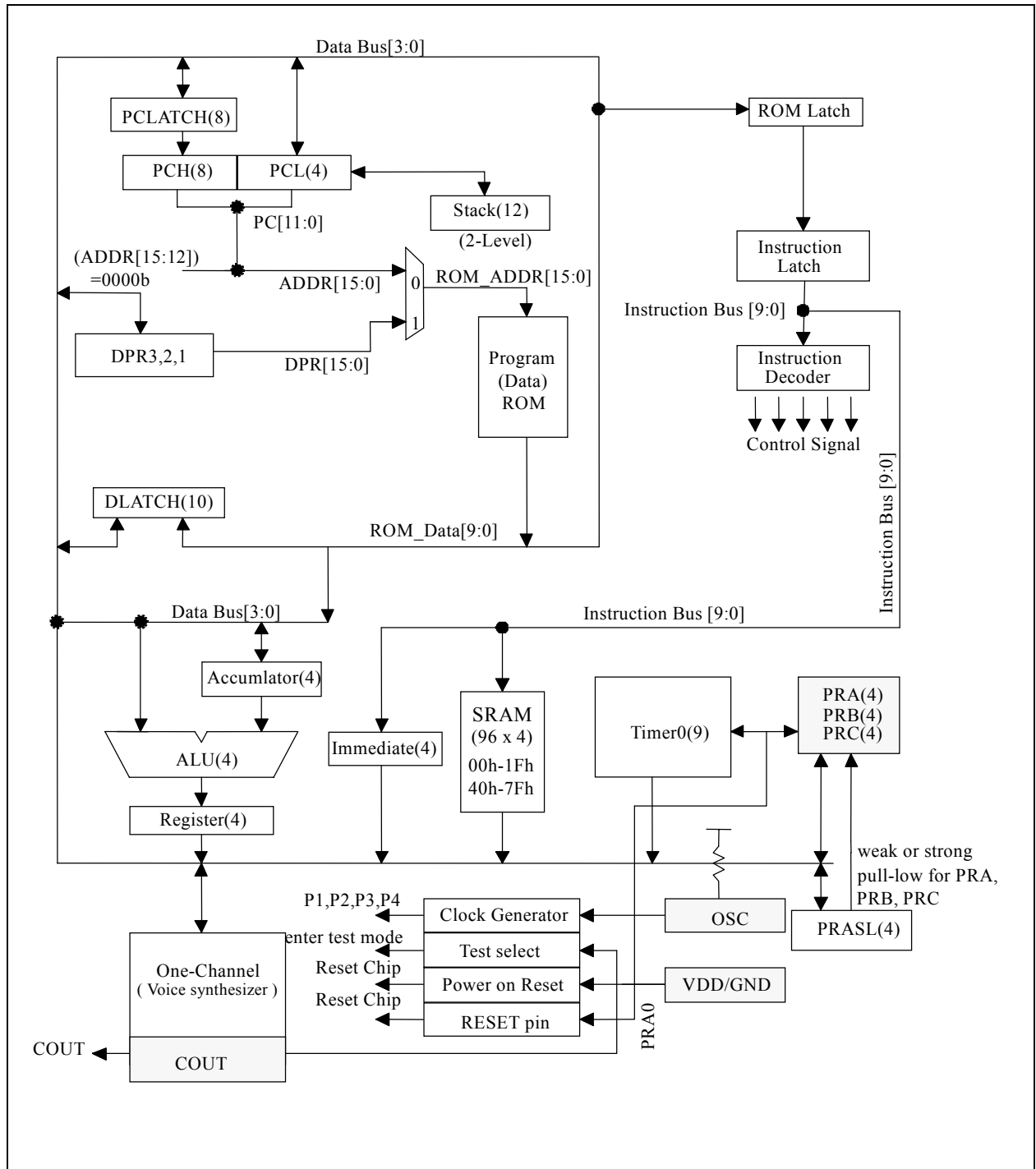
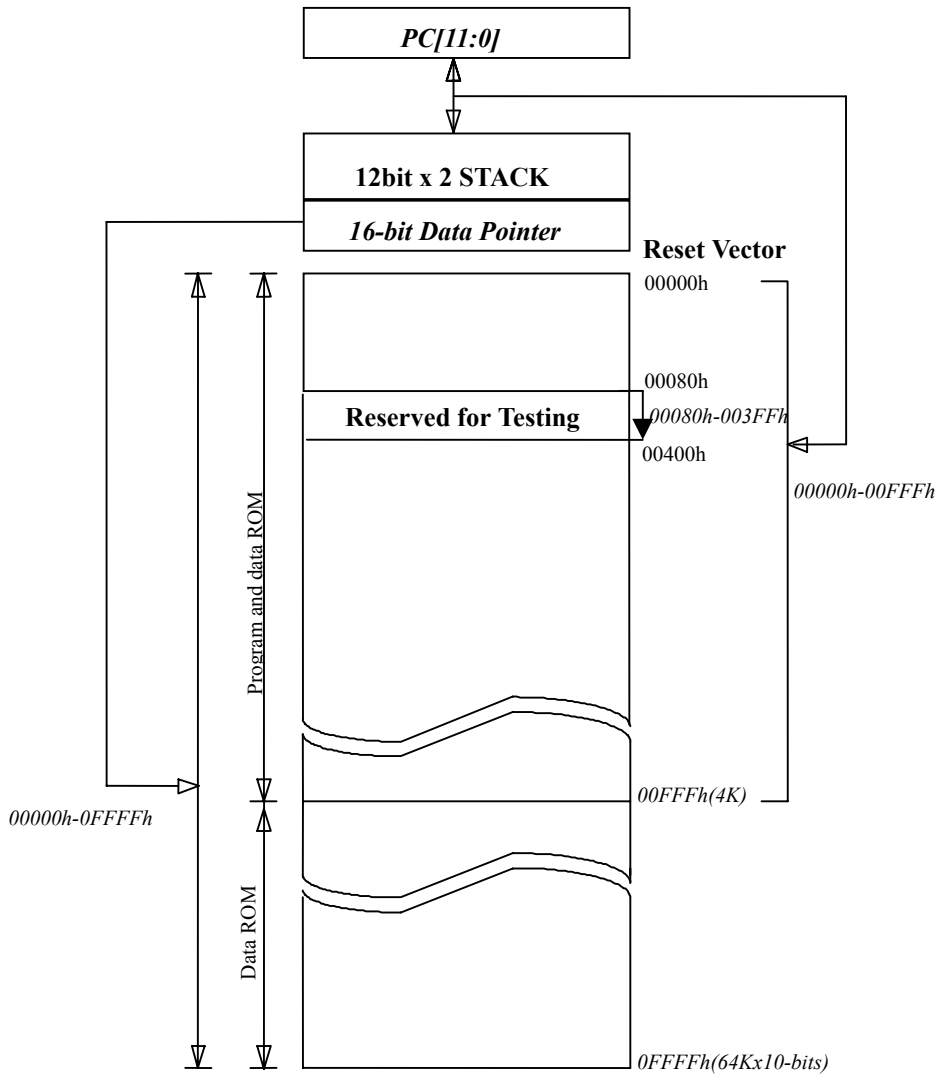


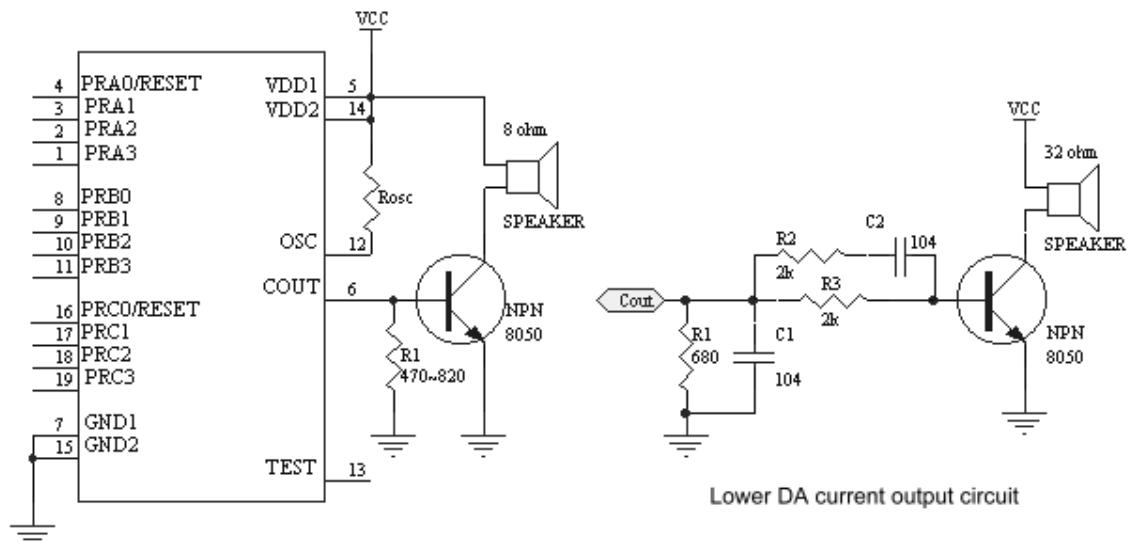
FIGURE 1.2 : External ROM Map of ASM2012CB



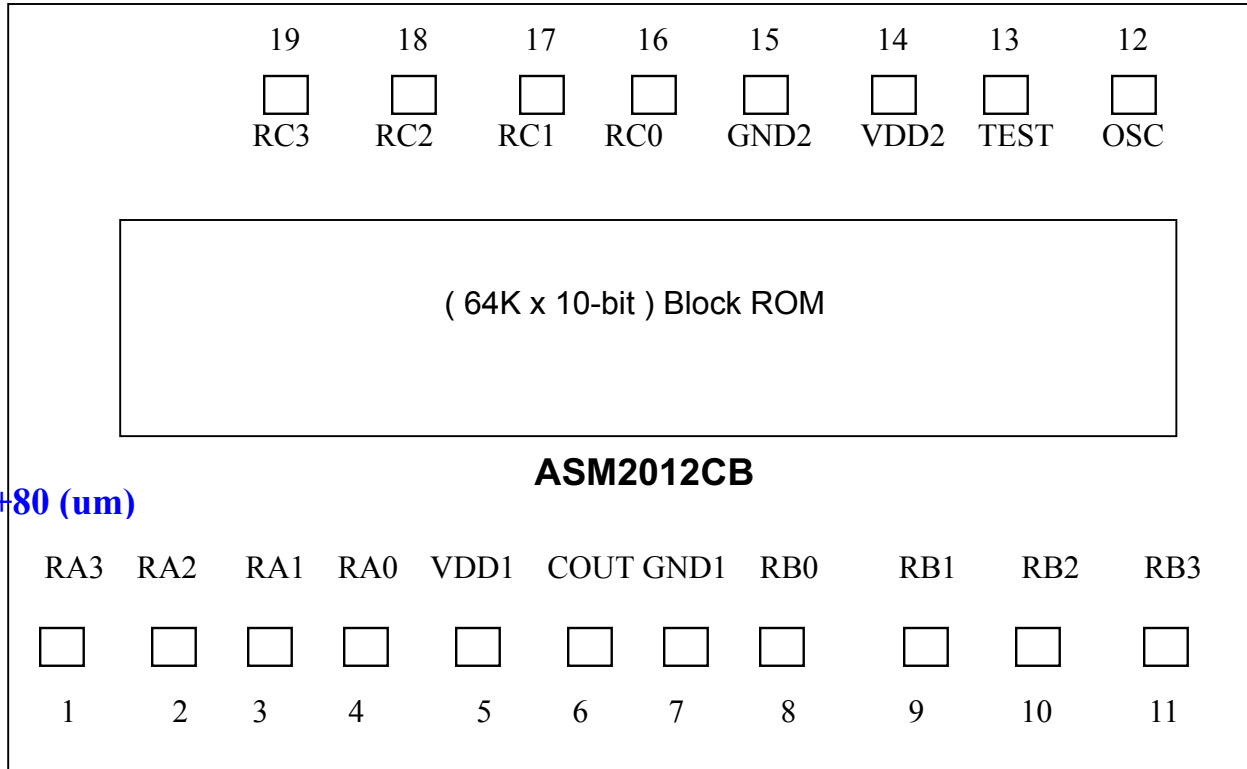
1.2 Pin-Out

ASM2012CB Pin-Out			
PRC1	I	STI Std./O.D.	Input port with programmable strong pull-low or weak pull-low or fix-input-floating capability
PRC0/RESET	I	STI Std./O.D.	Input port with programmable strong pull-low or weak pull-low or fix-input-floating capability <i>Mask option selected as an external RESET pin with weak pull-low capability</i>
PRA3-1	I/O	STI Std./O.D.	I/O port with programmable strong pull-low or weak pull-low or fix-input-floating capability Output type with standard or Open-Drain output
PRA0/RESET	I/O	STI Std./O.D.	I/O port with programmable strong pull-low or weak pull-low or fix-input-floating capability Output type with standard or Open-Drain output <i>Mask option selected as an external RESET pin with weak pull-low capability</i>
OSC	I	-	RM mode Oscillator input
VDD1	I	-	First Power supply during operation
COUT	O	-	Current Output of Audio
GND1	I	-	First Circuit Ground Potential
GND2	I	-	Second Circuit Ground Potential
TEST	O	-	Enter Test Mode. (TEST = High)
VDD2	I	-	Second Power supply during operation
PRB0-3	O	Std./O.D.	Output type with standard or Open-Drain output
PRC2-3	I	STI Std./O.D.	Input port with programmable strong pull-low or weak pull-low or fix-input-floating capability

1.3 Application circuit



1.4 Bonding Diagram



Y=1780+80 (um)

X= 1540+80 (um)

Substrate must be connected to GND.

ASM2012CB Pad Location				Chip Size: X= 1540+80 (um), Y=1780+80 (um)			
PAD #	PAD Name	X	Y	PAD #	PAD Name	X	Y
1	RA3	-682.16	-772.68	11	RB3	674.88	-772.68
2	RA2	-559.84	-772.68	12	OSC	633.56	804
3	RA1	-437.52	-772.68	13	TEST	432.48	804
4	RA0	-315.2	-772.68	14	VDD2	273.16	804
5	VDD1	-191.28	-772.68	15	GND2	134.68	804
6	COUT	71.12	-772.68	16	RC0	-51.76	804
7	GND1	189.52	-772.68	17	RC1	-248.4	804
8	RB0	307.92	-772.68	18	RC2	-454.24	804
9	RB1	430.24	-772.68	19	RC3	-650.88	804
10	RB2	552.56	-772.68				

1.5 DC Characteristics for ASM2012CB

SYMBOL	PARAMETER		VDD	MIN.	TYP.	MAX.	UNIT	CONDITION
VDD	OPERATING VOLTAGE			2.4	3	5.5	V	depending on Freq.
Isb	SUPPLY CURRENT	STANDBY	3			1	uA	4MHz, RM in HALT Mode
			5			1		
Iop		OPERATING	3		2		mA	4MHz, RM IO Floating
			5		7			
Iih	INPUT CURRENT /Internal pull low		3		3		uA	4MHz, RM in HALT Mode (IO Ports with weak pull-high pull-low)
			5		9			
			5		-5.2			
Ioh	OUTPUT HIGH CURRENT		3		-3		mA	4MHz, RM (IO ports)
			5		-8			
Iol	OUTPUT LOW CURRENT		3		7			
			5		20			
Cout	DA CURRENT OUT (FULL SCALE)		3		4			
			5		5.2			
dF/F	FREQUENCY STABILITY			-10		10	%	$\frac{F_{osc}(3v-2.4v)}{F_{osc}(3v)}$
dF/F	Fosc VARIATION			-20		20	%	VDD=3V, Rosc=200k, 4MHz

FIGURE 1.3 : Frequency Range for Rosc in RM mode

Resistor(k ohm)	300	200	130	110
3v Freq.(MHz)	2.56	3.92	5.48	7.11

