Device Overview

The IDT 89HP0604SB (P0604SB) is a 6Gbps SAS/SATA® Repeater device featuring IDT EyeBoost™ technology that compensates for cable and board trace attenuations and ISI jitter, thereby extending connection reach. The device is optimized for SAS/SATA high speed serial data streams and contains four data channels, each able to process 6Gbps transmission rates. Each channel consists of an input equalizer and amplifier, signal detection with glitch filter, as well as programmable output swing and de-emphasis. Allowing for application specific optimization, the P0604SB, with its configurable receiver and transmitter features, is ideal for SAS/SATA applications using a wide combination of cables and board trace materials.

All modes of active data transfer are designed with minimized power consumption. In full shutdown mode, the part consumes less than 40mW in worst case environmental conditions.

Applications

- Blade servers, rack servers
- SAS/SATA instrumentation
- Storage systems
- Cabled SAS/SATA devices

Features

- Compensates for cable and PCB trace attenuation and ISI jitter
- Programmable receiver equalization up to 24db
- Programmable transmitter swing and de-emphasis
- Recovers data stream even when the differential signal eye is completely closed due to trace attenuation and ISI jitter
- Full SAS/SATA protocol support
- Configurable via external pins
- Leading edge power minimization in active and shutdown modes
- No external bias resistors or reference clocks required
- Channel mux mode, demux mode, 1 to 2 channels multicast, and Z-switch function mode
- Available in a 36-pin QFN package (4.0 x 7.5mm with 0.5mm pitch)

Benefits

- Extends maximum cable length to over 8 meters and trace length over 48 inches in SAS/SATA applications
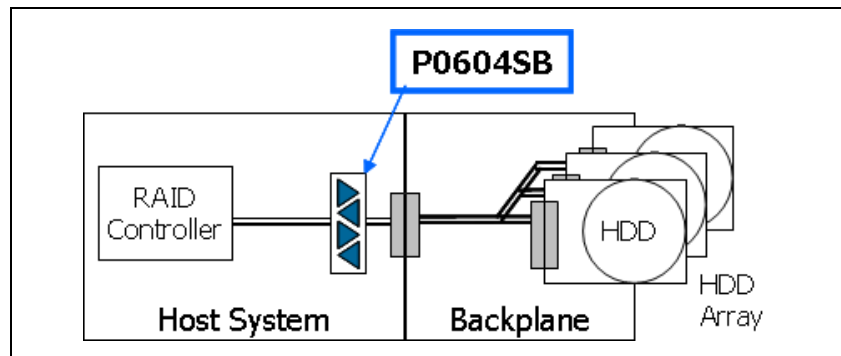- Minimizes BER

Typical Application

Figure 1 IDT Repeaters in Blade Servers

IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc.

SAS/SATA Compliance

The device was designed to provide end users with features needed to comply with SAS/SATA system application requirements:

- – SAS/SATA Out-of-Band (OOB) Support
- – Jitter, eye opening, and all other AC and DC specifications.

Block Diagram

The P0604SB contains four high speed channels as shown in Figure 2. Each channel can be routed to different outputs. Depending on user configuration via mode selections, input traffic can be muxed or demuxed. Powerdown (PDB) is provided for state and channel control.
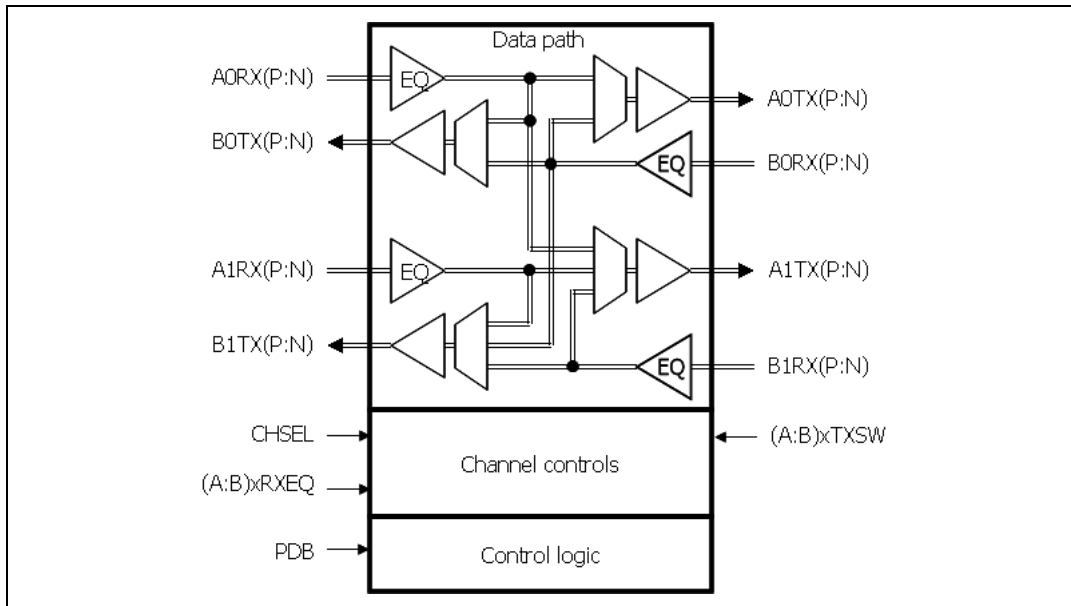

Figure 2 Block Diagram

Table of Contents

PAGE INTENTIONALLY LEFT BLANK

Functional Description

The P0604SB has 4 channels, each with the individually programmable features listed below. Figure 3 diagrams the channel and Table 1 summarizes key configuration options.
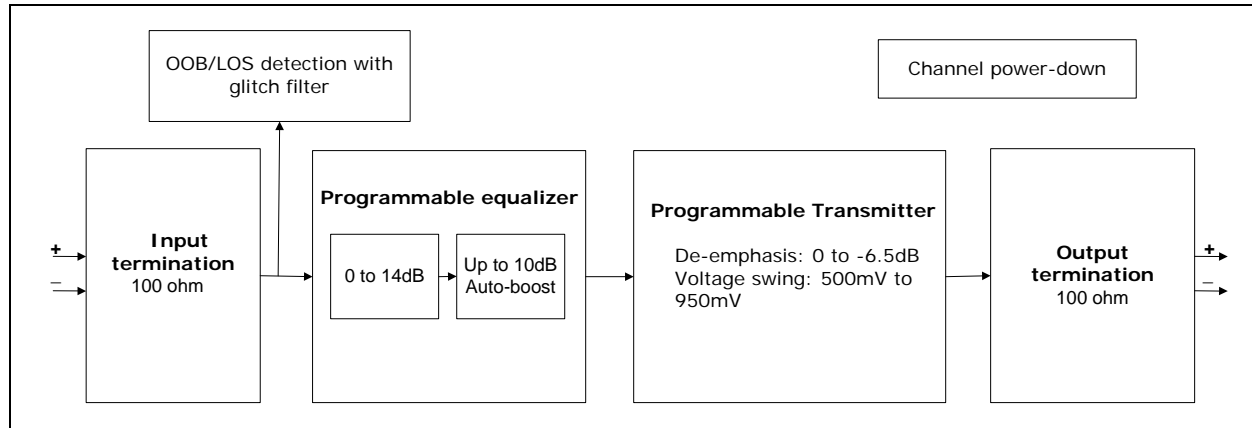

Figure 3 Channel Block Diagram with Channel Features

◆ Per-channel programmable features used at the Receive side.
  – Input equalization with 3 levels: 2 to 14dB compensation for high frequency signal attenuation due to cables and board traces. Additionally, up to 10dB boost is added automatically by the equalizer for applications using long cables. The total equalization range is between 2dB and 24dB.
  – Input high impedance control via channel enable: disabled (active mode) and hi-Z (power-down).
◆ Per-channel programmable features used at the Transmit side.
  – Output de-emphasis with 8 levels: 0 to -6.5dB. The de-emphasis boosts the magnitude of higher frequencies sent by the transmitter to compensate for high frequency losses travelling through output side cable or output side board traces. This ensures that the final received signal has a wider eye opening.
  – Output differential swing with 3 levels: 0.5V to 0.95V (peak-to-peak).
  – Loss of signal detection: When the incoming differential peak-peak amplitude falls below 110mV, the device enters loss of signal mode and the corresponding transmitter stops toggling, maintains its common mode voltage level, and meets all loss of signal specifications described in the AC Specifications section of this data sheet.

In addition, the device contains global configuration of the data path:
  – Transfer modes: direct connect, cross-connect, multicast.

Power-Up

After the power supplies reach their minimum required levels, the P0604SB powers up by setting all input and output pins to known states:

- ◆ All the device's input configuration pins are set internally to VSS or VDD for 2-level pins and to VDD/2 for 3-level pins.
- ◆ High speed differential input and output pins depend on various conditions described below:
  - − High speed differential input and output pins are in high impedance if any of the following conditions is true:
    - • Powerdown is set (PDB pin = 0V) or
    - • No receiver termination was detected at TX outputs

    In all other cases, high speed differential input and output pins are set to 50 ohms per pin, with 100 ohms differential impedance. Also refer to Table 2, Power Reducing Modes.

The power ramp up time for the P0604SB should be less than 1ms.

Power Sequencing

There are no power sequencing constraints for the P0604SB.

IDT EyeBoost™ Technology

IDT EyeBoost™ technology is a method of data stream recovery even when the differential signal eye is completely closed due to cable or trace attenuation and ISI jitter. With IDT EyeBoost™, the system designer can both recover the incoming data and retransmit it to target device with a maximized eye width and amplitude. An example of IDT EyeBoost™ usage in a system application and eye diagram results are shown in Figure 4. In this figure, the (a) diagram shows incoming differential signal (closed eye) after 62 inch FR4 connection from signal source and the (b) diagram shows differential signal at the output of repeater maximized eye opening with IDT EyeBoost™.
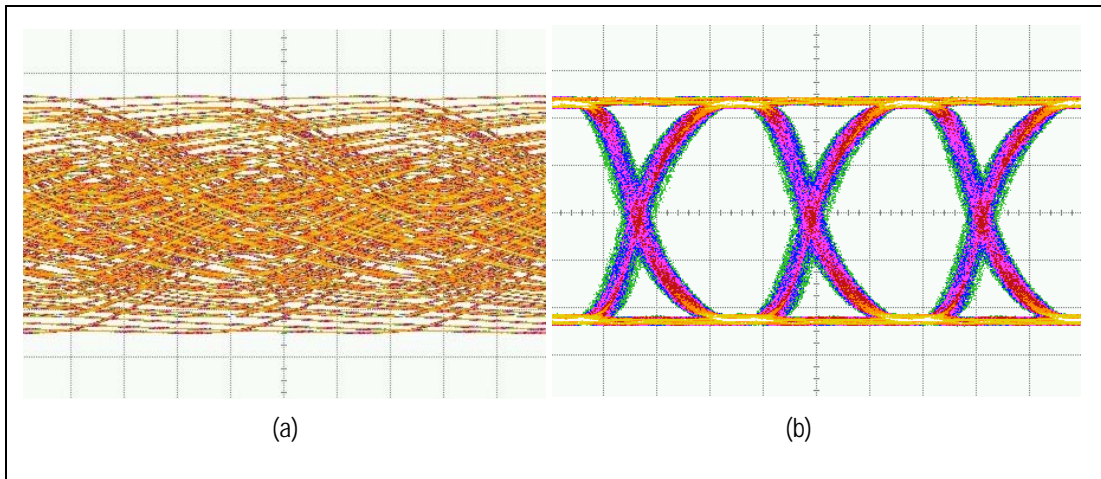

(a)   (b)

Figure 4   Eye Diagram

Eye Diagram Parameters

Feature	Feature Type	Parameter Names for Programming via Pins
Input equalization	Main eye optimization	A0RXEQ, A1RXEQ, B0RXEQ, B1RXEQ Range: 0dB to 14dB (plus additional auto-boost up to 10dB for long connections)
Output differential signal swing (peak-to-peak) and output de-emphasis	Main eye optimization	A0TXSW, A1TXSW, B0TXSW, B1TXSW Range: 0.5V to 0.95V for swing Range: 0 to -6.5dB for de-emphasis

Table 1 Quick Reference: Parameters Used for Eye Optimization

Modes of Operation

The device supports several data transfer modes, loss of signal mode, and one power reducing mode.

Loss of Signal Mode

When the input signal is lost, the transmitter stops toggling and maintains its common-mode voltage level. The device detects loss-of-signal (LOS) when the envelope of the incoming signal on a given channel has fallen below a programmable threshold level.

Power Reducing Modes

The Repeater supports five power-down states and one active state as shown in Table 2. The user can choose between full chip power-down or channel based power-down. Power reducing modes are selected via PDB and channel enable pins (A0EN, A1EN, etc.).

Power Reducing Mode	Required Signal Values	State Description
	PDB	
Full IC power-down	0	All channels are powered-down Rx termination is set to Hi-Z Tx termination is set to 1kΩ Tx common-mode is at VDD
Channel enabled and active. No power-down	1	Tx output is active Receiver terminations set to 50Ω Transmitter terminations set to 50Ω

Table 2 Power Reducing Modes

Channel Muxing

The P0604SB repeater permits a variety of muxing, demuxing, and switching configurations, and it can mux/de-mux 1 or 2 bi-directional SAS/SATA lanes (4 SAS/SATA channels) into 2 target devices. These configurations require the selection of specific pins for input and output ports. In the following sections, each configuration is described in terms of pin connectivity to external upstream and downstream devices. The configurations shown are those often used in system designs:

- – Uni-directional 2:1 Mux (1 or 2 instances)
- – Uni-directional 1:2 De-Mux (1 or 2 instances)
- – Bi-directional 2:1 Mux/De-Mux
- – Bi-directional Z-function (also called Partial Cross Function)

The P0604SB supports channel muxing in both upstream and downstream channel directions via the CHSEL pin, as shown below. Figure 5 shows the channel/reference muxing modes and Table 3 shows how CHSEL (Channel transfer selection) pin allows for various modes of data transfers: Multicast mode, Direct-connect, and Cross-connect. Both Direct-connect, and Cross-connect modes are used to build uni-directional and bi-directional 2:1 mux and Z-switch functions.
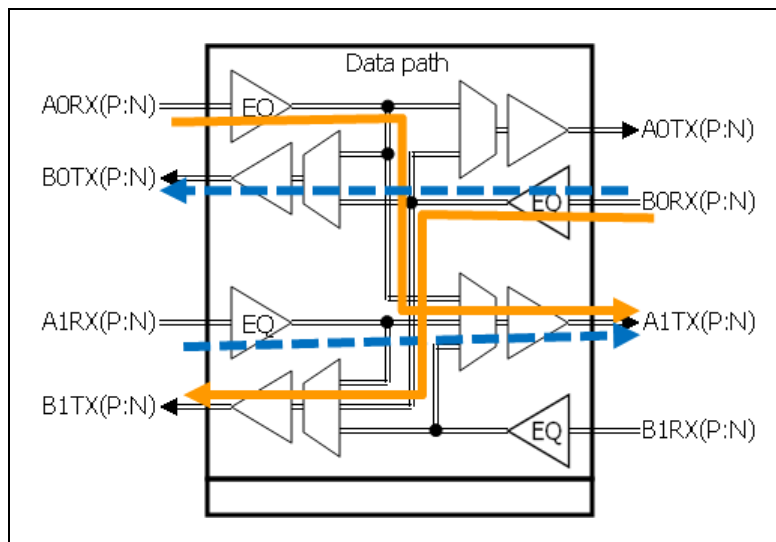

Figure 5 Diagram of Channel/Reference Muxing Modes

Input Pins				Output Pins			
CHSEL	A0RX[P,M]	A1RX[P,M]	B0RX[P,M]	B1RX[P,M]	A0TX[P,M]	A1TX[P,M]	B0TX[P,M]	B1TX[P,M]
CHSEL=VSS (Multicast Mode)	A0 DATA	X	B0 DATA	X	A0 DATA	A0 DATA	B0 DATA	B0 DATA
CHSEL=Open (Direct-Connect Mode)	A0 DATA	A1 DATA	B0 DATA	B1 DATA	A0 DATA	A1 DATA	B0 DATA	B1 DATA
CHSEL=VDD (Cross-Connect Mode)	A0 DATA	X	B0 DATA	X	Squelched	A0 DATA	Squelched	B0 DATA

Table 3 Description of Channel Muxing/De-Muxing Functionality

February 8, 2011

Uni-directional 2:1 Mux or Two Instances of Unidirectional 2:1 Mux

This function can be achieved by using the CHSEL pin as a mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 6.
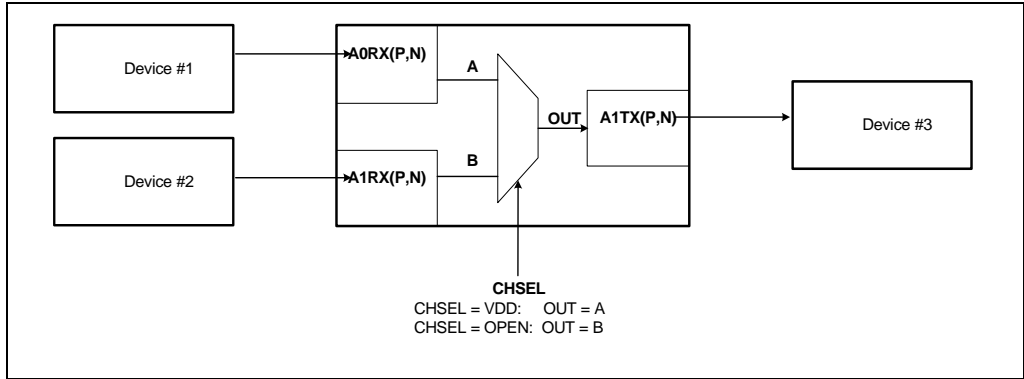

Figure 6 Implementation of Unidirectional 2:1 Mux

As an alternative, different chip channels can also be selected as shown in Figure 7. This solution can be combined with the previous one to obtain two instances of Uni-directional 2:1 Mux.
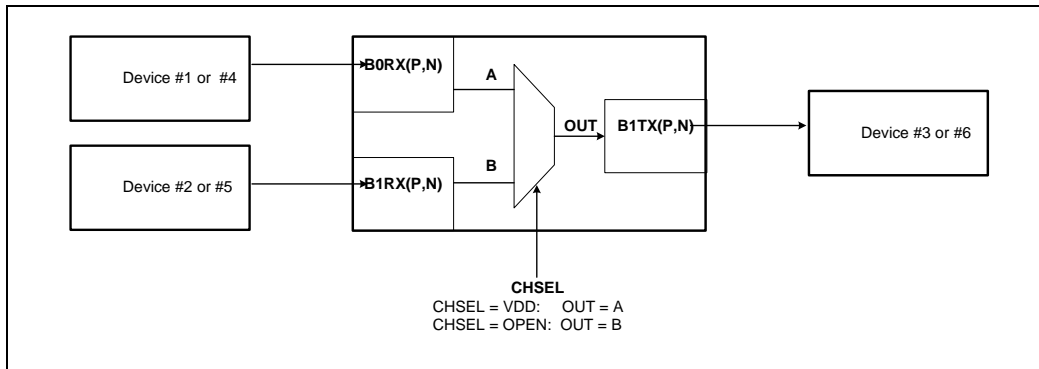

Figure 7 Implementation of Second Instance of Unidirectional 2:1 Mux

Uni-directional 1:2 De-Mux or Two Instances of Unidirectional 1:2 De-Mux

This function can be achieved by using CHSEL pin as a de-mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 8.
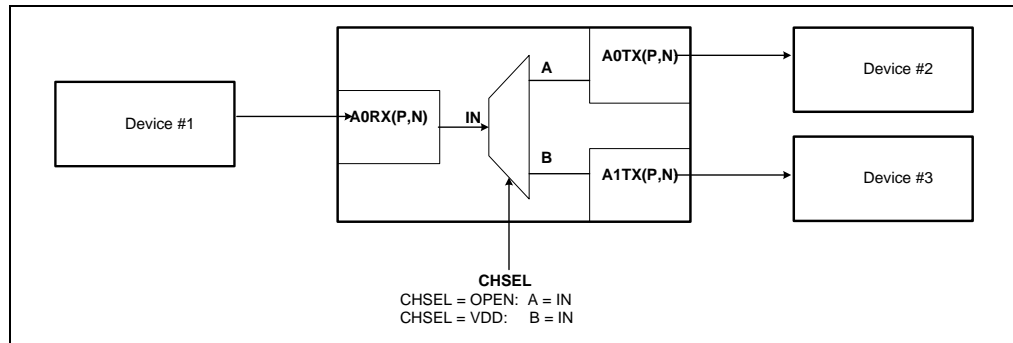

Figure 8 Implementation of Unidirectional 1:2 De-Mux

As an alternative, different chip channels can also be selected as shown in Figure 9. This solution can be combined with the previous one to obtain two instances of Uni-directional 1:2 De-Mux.
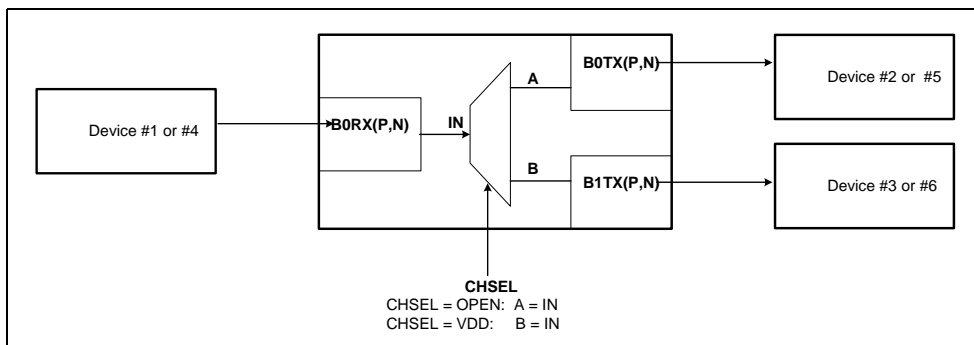

Figure 9 Implementation of Second Instance of Unidirectional 1:2 De-Mux

Bi-directional 2:1 Mux/De-Mux

The bi-directional Mux and De-Mux function can also be achieved by using the CHSEL pin as a mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 10.
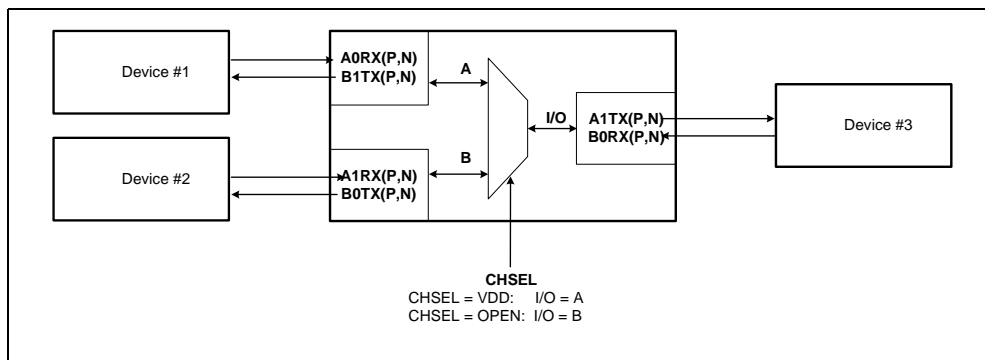

Figure 10 Implementation of Bi--directional 2:1 Mux/De-Mux

Bi-directional Z-function (also called Partial Cross Function)

This function can also be achieved by using the CHSEL pin as a flow control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 11.
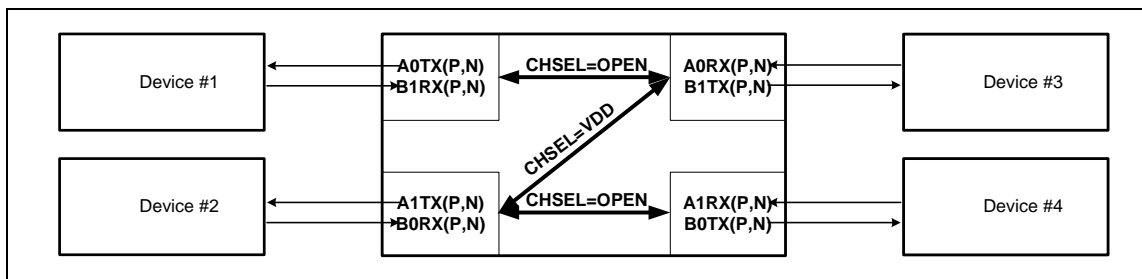

Figure 11 Implementation of Z-function

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range VDD	−0.5 to 1.35	V
Voltage range Differential I/O	−0.5 to VDD +0.5	V
Control I/O	−0.5 to VDD + 0.5	V
ESD requirements: Electrostatic discharge Human body model	±2000	V
ESD requirements: Charged-Device Model (CDM)	±500	V
ESD requirements: Machine model	±125	V
Storage ambient temperature	-55 to 150	°C

Table 4 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Notes	Min	Typical	Max	Unit
Power Supply Pin Requirements					
VDD	1.2V DC analog supply voltage (specified at bump pins)	1.14	1.2	1.26	V
Temperature Requirements					
TA	Ambient operating temperature - Commercial	0	—	70	°C
	Ambient operating temperature - Industrial	-40	—	85	°C
TJUNCTION	Junction operating temperature	0	—	125	°C

Table 5 P0604SB Operating Conditions

Power Consumption

Table 6 below lists power consumption values under typical and maximum operating conditions.

Parameter	Notes	Min	Typical	Max	Unit
Active Mode					
I$_{VDD}$	Current into VDD supply	—	330	500	mA
P$_D$	Full chip power[1]		400	600	mW
P$_{D-ch}$	Power per channel[1]		100	150	mW
Standby Mode	Full chip standby		30	40	mW

Table 6 Power Consumption

[1.] Maximum power under all conditions. Power is reduced by selecting smaller de-emphasis settings (closer or equal to 0dB).

Package Thermal Considerations

The data in Table 7 below contains information that is relevant to the thermal performance of the 36-pin QFN package.

Symbol	Parameter	Value	Conditions	Units
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	49.8	Zero air flow	°C/W
		44.8	1 m/S air flow	°C/W
		42.2	2 m/S air flow	°C/W
θ_{JB}	Thermal Resistance, Junction-to-Board	39.3	NA	°C/W
θ_{JC}	Thermal Resistance, Junction-to-Case	34.5	NA	°C/W

Table 7 Thermal Specifications for 36-QFN Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 7. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 7), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board).

DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IL}	Digital Input Signal Voltage Low Level[1]	-0.3	—	0.25*VDD-0.1	V
V_{IM}	Digital Input Signal Voltage Mid Level[2]	0.25*VDD+ 0.1		0.75*VDD-0.1	V
V_{IH}	Digital Input Signal Voltage High Level[1]	0.75*VDD+ 0.1		VDD+ 0.3	V
V_{HYS}	Hysteresis of Schmitt Trigger Input	0.1		—	V
I_{IL}	Input Current[3]	—		100	µA
I_{IH}	Input Current[4]	—		100	µA
I_{IL1}	Input Current[2]	—		180	µA
I_{IH1}	Input Current[2]	—		180	µA
$R_{WEAK\_PD\_2L}$	Internal weak pull-down resistor at 2-level input pads[4]	11		—	K ohm
$R_{WEAK\_PU\_2L}$	Internal weak pull-up resistor at 2-level input pads[3]	11		—	K ohm
$R_{WEAK\_PD\_3L}$	Internal weak pull-down resistor at all 3-level input pads	6.3		—	K ohm
$R_{WEAK\_PU\_3L}$	Internal weak pull-up resistor at all 3-level input pads	6.3		—	K ohm

Table 8 DC Specification

[1.] Applies to all input pins.

[2.] Applies to all 3-level input pins.

[3.] Applies only to 2-level input pins with default values set to VDD in the Pin Description table (Table 12).

[4.] Applies only to 2-level input pins with default values set to VSS in the Pin Description table (Table 12).

AC Specifications

Latency Specification

Parameter	Description	Min	Typical	Max	Unit
T_{PD}	Input to output signal propagation device	—	300	—	ps
$T_{SIGDET-ATTACK}$	Signal Detect Valid Signal Attack Time (Turn-on time)	—	—	15	ns
$T_{SIGDET-DECAY}$	Signal Detect Valid Signal Decay Time (Turn-off time)	—	—	15	ns
$T_{SIGDET-ATT-DECAY-MIS}$	Signal Detect Attack / Decay Time Mismatch	—	—	5	ns

Table 9 P0604SB Latency Specification

Receiver Specifications

Parameter	Description	Min	Typical	Max	Unit
Receiver Input Jitter Specification					
T_{RX-DJ}	Receive input, Data Dependant Jitter (Inter-Symbol-Interference)	—	—	>1	UI
T_{RX-TJ}	Receive input, Total Jitter	—	—	>1	UI
T_{RX-EYE}	Receiver eye time opening (can recover from closed eye due to trace/cable jitter)	0	—	—	UI

Table 10 P0604SB Receiver Electrical Specifications (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Unit
Receiver Input Eye Specification					
$V_{DIFF-RX}$	Receiver Differential Peak-Peak Voltage[1]	0	—	2000	mV
$t_{skew-RX}$	RX Differential Skew	—	—	30	ps
$V_{CM-AC-RX}$	Receiver AC Common Mode Voltage	—	—	100	mVp-p
V_{thresh}	OOB Signal Detection Threshold	50	110	160	mVppd
Receiver Return Loss					
$RL_{DD11,RX}$	RX Differential Mode Return Loss				
	0 MHz - 150 MHz	18	—	—	dB
	150 MHz - 300 MHz	18	—	—	
	300 MHz - 600 MHz	14	—	—	
	600 MHz - 1.2 GHz	10	—	—	
	1.2 GHz - 2.4 GHz	8	—	—	
	2.4 GHz - 3.0 GHz	3	—	—	
	3.0 GHz - 5.0 GHz	1	—	—	
$RL_{RXslope}$	Slope of RX Differential Mode Return Loss (From 300MHz)	—	-13	—	dB/dec
$RL_{RX-freq-max}$	RX Differential Mode Return Loss Max Frequency	—	6	—	GHz
$RL_{CC11,RX}$	RX Common Mode Return Loss				
	0 MHz - 300 MHz	5	—	—	dB
	300 MHz - 600 MHz	5	—	—	
	600 MHz - 1.2 GHz	2	—	—	
	1.2 GHz - 2.4 GHz	1	—	—	
	2.4 GHz - 3.0 GHz	1	—	—	
	3.0 GHz - 5.0 GHz	—	—	—	
Receiver DC Impedance					
$Z_{DIFF-RX}$	Differential impedance , RX pair	85	—	115	Ohm
Z_{CM-RX}	Common-Mode Receive Impedance	20	—	40	Ohm

Table 10 P0604SB Receiver Electrical Specifications (Part 2 of 2)

[1] The minimum value of 0 mV represents the case when Eye is completely closed.

Transmitter Specifications

Parameter	Description	Min	Typical	Max	Unit
Output Eye and Common Voltage Specification					
$V_{TX-DIFF-PP}$	Differential Transmitter swing [A:B]xTXSW=1 [A:B]xTXSW=open	800 700	950 800	1100 950	mV
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Transmitter swing [A:B]xTXSW=0	400	500	650	mV

Table 11 P0604SB Transmitter Electrical Requirements (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Unit
$V_{TX\text{-}DE\text{-}RATIO}$	Tx de-emphasis level ratio	-6.5		0	dB
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	Tx de-emphasis level ratio [A:B]xTXSW=open	-4.0	—	-3.0	dB
$V_{TX\text{-}DE\text{-}RATIO\text{-}6dB}$	Tx de-emphasis level [A:B]xTXSW=1	-6.5	—	-5.5	dB
$T_{RES\text{-}DJ\text{-}6.25GBPS\text{-}1}$	Residual Deterministic Jitter at output pins (1 inch FR4 trace before receiver input pins, 6.25Gbps)[1]	—	—	<0.1	UI
$T_{RES\text{-}DJ\text{-}6.25GBPS\text{-}2}$	Residual Deterministic Jitter at output pins (40 inch FR4 trace before receiver input pins, 6.25Gbps)[1]	—	0.18	0.25	UI
$T_{20\text{-}80TX}$	TX Rise/Fall Time (20-80%)	33	—	90	ps
T_{skewTX}	TX Differential Skew	—	—	20	ps
R/F_{bal}	TX Rise/Fall Imbalance	—	—	20	%
AMP_{bal}	TX Amplitude Balance	—	—	10	%
$V_{CM,AC\text{-}TX\text{-}PP}$	Tx AC Common Mode Voltage (Peak to peak)	—	—	50	mVp-p
$V_{TX\text{-}CM\text{-}RMS\text{-}AC}$	RMS AC Common Mode Voltage Variation	—	—	20	mV
C_{TX}	AC Coupling Capacitor	12	—	200	nF
Transmitter DC Impedance					
$Z_{TX\text{-}DIFF\text{-}DC}$	Transmitter Output Differential DC Impedance	85	100	115	Ohm
$I_{TX\text{-}SHORT}$	Transmitter short-circuit current limit	—	—	90	mA
Transmitter Return Loss					
$RL_{DD11,TX}$	DC TX Differential Mode Return Loss	14	—	—	dB
	DC TX Differential Mode Return Loss ($F_{BAUD/2}$)	6	—	—	
$RL_{TXslope}$	Slope of TX Differential Mode Return Loss (From 300MHz)	—	-13	—	dB/dec
$RL_{CC11,TX}$	TX Common Mode Return Loss (measured at 3.0 Gbps)				
	0 MHz - 300 MHz	8	—	—	dB
	300 MHz - 600 MHz	5	—	—	
	600 MHz - 1.2 GHz	2	—	—	
	1.2 GHz - 2.4 GHz	1	—	—	
	2.4 GHz - 3.0 GHz	1	—	—	
	3.0 GHz - 5.0 GHz	1	—	—	
Lane Skew					
$L_{TX\text{-}SKEW}$	Lane-to-Lane Output Skew	—	5	10	ps

Table 11 P0604SB Transmitter Electrical Requirements (Part 2 of 2)
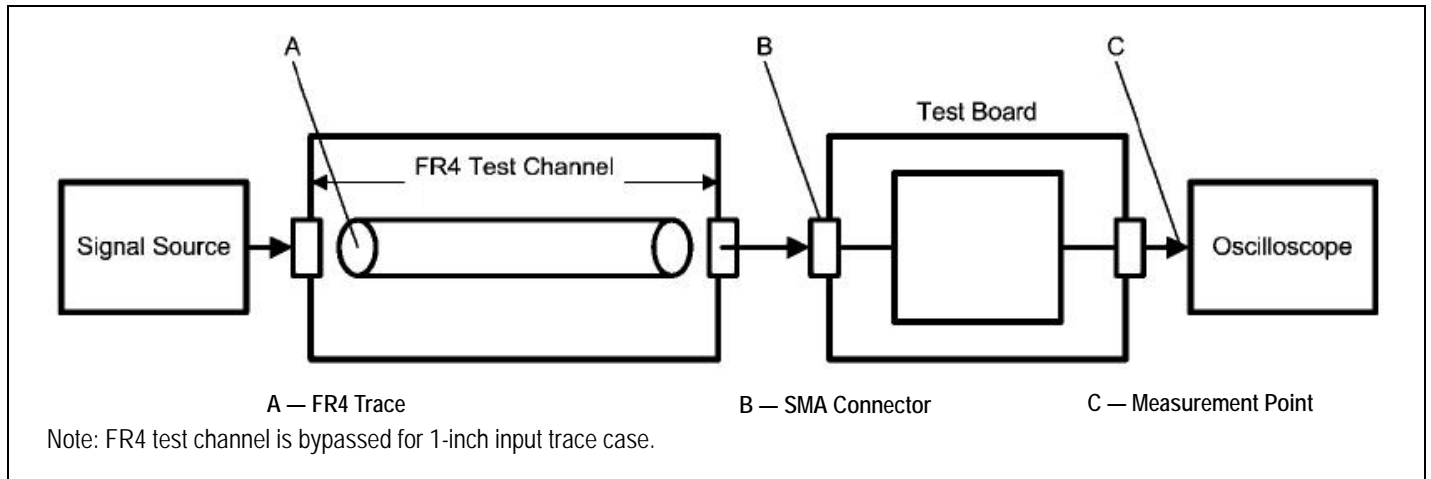
[1.] Refer to Figure 12.

Figure 12 Residual Jitter Characterization Test Setup

Pin Description

Note: Unused pins can be left floating.

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
Power			
VDD	5, 8, 11, 21, 24, 27	1.2V (typ) Power supply for Repeater high speed channels and internal logic. Each VDD pin should be connected to the VDD plane through a low inductance path, with a via located as close as possible to the landing pad of VDD pins. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each VDD pin to ground plane.	Power
VSS	Center Pad	VSS reference. VSS should be connected to the ground plane through a low inductance path, with a via located as close as possible to the landing pad.	Power
Data Signals			
A0RXN A0RXP	4 3	Channel A0 Receive Data Ports	Input
A0TXN A0TXP	28 29	Channel A0 Transmit Data Ports	Output
B0RXN B0RXP	25 26	Channel B0 Receive Data Ports	Input
B0TXN B0TXP	7 6	Channel B0 Transmit Data Ports	Output
A1RXN A1RXP	10 9	Channel A1 Receive Data Ports	Input
A1TXN A1TXP	22 23	Channel A1 Transmit Data Ports	Output
B1RXN B1RXP	19 20	Channel B1 Receive Data Ports	Input
B1TXN B1TXP	13 12	Channel B1 Transmit Data Ports	Output
Channel Control and Status			
A0RXEQ (Channel A0) B0RXEQ (Channel B0) A1RXEQ (Channel A1) B1RXEQ (Channel B1)	15 17 36 33	Receiver Equalization at F=3GHz (6Gbps). Programming of channel A0 via pins is shown below. To program other channels, use pins for those channels. A0RXEQ Setting VSS 2dB (3GHz) Open 6dB (3GHz) (Default) VDD 14dB (3GHz)	Input - 3 level

Table 12 Pin Description (Part 1 of 2)

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
A0TXSW (Channel A0) B0TXSW (Channel B0) A1TXSW (Channel A1) B1TXSW (Channel B1)	1 32 14 18	Transmitter Voltage Swing (pk-pk). Programming of channel A0 via pins is shown below. To program other channels, use pins for those channels. A0TXSW Swing De-Emphasis VSS 0.5Vdiff-pkpk 0dB Open 0.8Vdiff-pkpk (Default) -3.5dB VDD 0.95Vdiff-pkpk -6.5dB	Input - 3 level
Other Control Signals			
PDB	35	Power-down Enable. PDB Setting VSS Powerdown IC. RX terminations are in Hi-Z, TX is disabled VDD Normal operation (internal 11K ohm minimum pull-up applied)	Input - 2 level
CHSEL	30	Channel Transfer Mode. CHSEL Setting VSS Multi-cast mode Open Direct-connect mode (default) VDD Cross-connect mode	Input - 3 level
RSVD	2,16,31,34	Reserved. Do not connect.	

Table 12 Pin Description (Part 2 of 2)

Package Pinout — 36-QFN Signal Pinout

Table 13 lists the pin numbers and signal names for the P0604SB device.

Function	Pin	Function	Pin	Function	Pin
A0RXEQ	15	A1TXP	23	B1RXP	20
A0RXN	4	A1TXSW	14	B1TXN	13
A0RXP	3	B0RXEQ	17	B1TXP	12
A0TXN	28	B0RXN	25	B1TXSW	18
A0TXP	29	B0RXP	26	CHSEL	30
A0TXSW	1	B0TXN	7	PDB	35
A1RXEQ	36	B0TXP	6	RSVD	2,16,31,34
A1RXN	10	B0TXSW	32	VDD	5,8,11,21,24,27
A1RXP	9	B1RXEQ	33		
A1TXN	22	B1RXN	19		

Table 13 Alphabetical Pin List

Pin Diagram

The following figure lists the pin numbers and the signal names for the 36-QFN package.
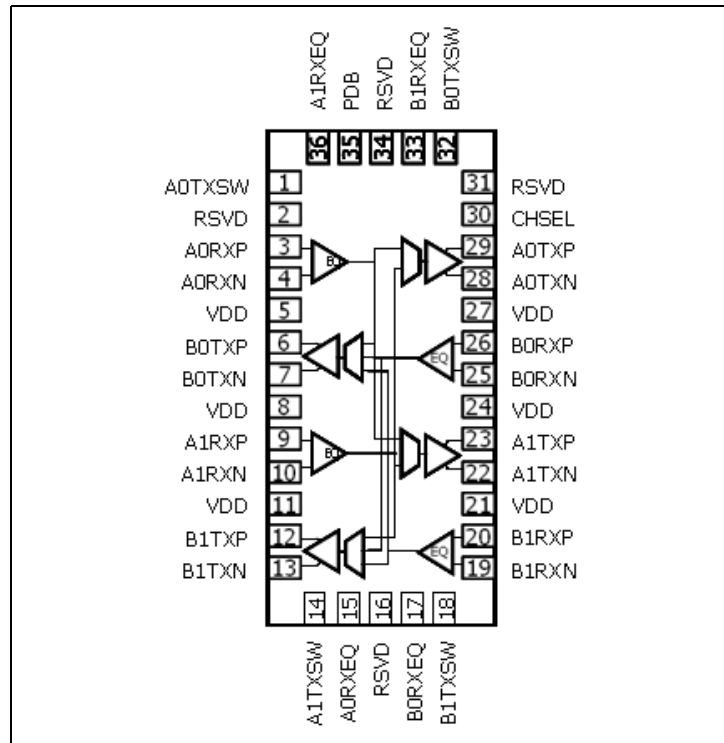
Figure 13 Pin Diagram — Top View

QFN Package Dimension

Revision History

November 2, 2010: Initial publication of final datasheet.

February 8, 2011: Removed black packaging options from Order page.

Ordering Information

NN	A	A	NN	NN	AA	AA	AAA	A	N
Product Family	Operating Voltage	Product Detail	Speed	Chnls	Protocol	Device Revision	Pkg	Temp Range	Tape & Reel
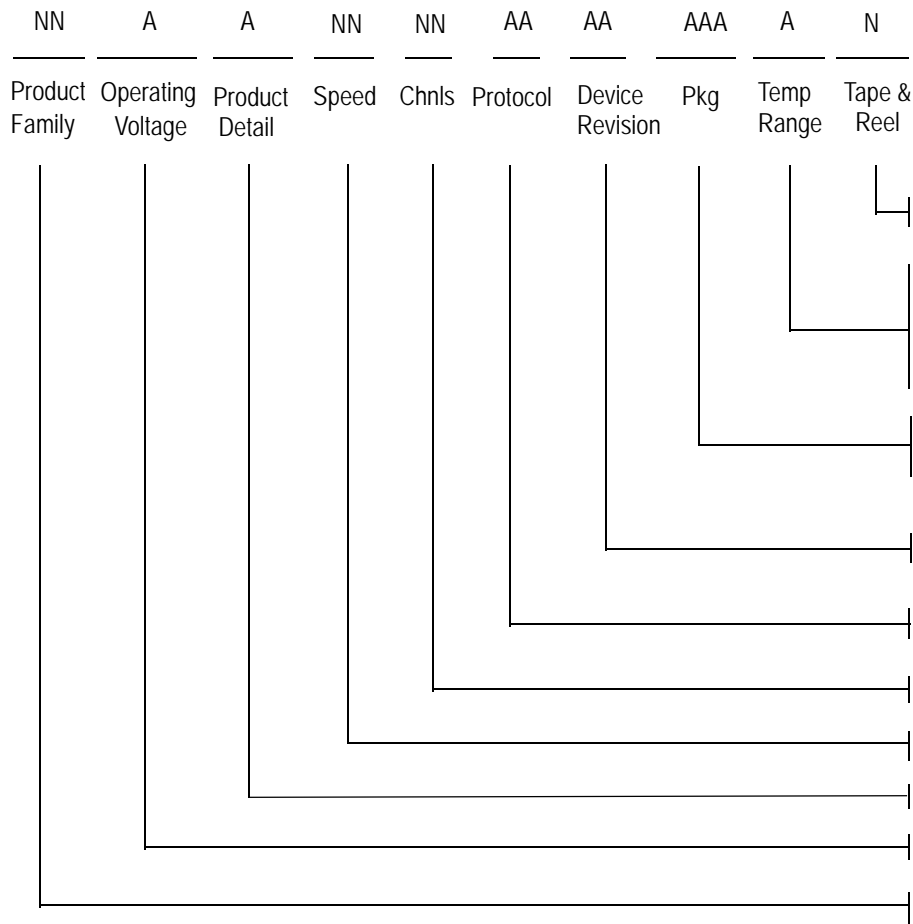
Legend
A = Alpha Character
N = Numeric Character

8	Tape & Reel
Blank	Commercial Temperature (0°C to +70°C Ambient)
I	Industrial Temperature (-40° C to +85° C Ambient)
NRG	NRG36 36-pin QFN, Green
ZB	ZB revision
SB	SAS/SATA Interface, "B" version
04	4 Channels
06	6Gbps
P	rePeater
H	1.2V +/- 5%
89	Signal Integrity Product

Valid Combinations

89HP0604SBZBNRG8   36-pin Green QFN package, Commercial Temperature

89HP0604SBZBNRGI8   36-pin Green QFN package, Industrial Temperature

IDT®

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: siphelp@idt.com
phone: 408-284-8208