Ordering number : EN*A1514A

Preliminary

SANYO Semiconductors
DATA SHEET

CMOS IC

LE24CBK22 — Two Wire Serial Interface EEPROM (2K+2K EEPROM)

Overview

The dual port EEPROM series consists of two independent banks, and each bank can be controlled separately using dedicated control pins. The two banks can each be controlled separately, but share the internal power supply system. In addition, this product uses a 2-wire serial interface, and is the optimal device for realizing substantial reductions in system cost and mounting area, as well as low power consumption.
The dual port EEPROM series also has a combined mode that allows the two-bank configuration (2K bits + 2K bits) to be used as a pseudo one-bank configuration (4K bits) by setting the $\overline{\text{COBM}}$ pin low. Together with the 16-byte page write function, this enables a reduction in the number of factory write processes.
This product incorporates SANYO's high performance CMOS EEPROM technology and realizes high-speed operation and high-level reliability. The interface of this product is compatible with the I^2C bus protocol, making it ideal as a nonvolatile memory for small-scale parameter storage.
In addition, this product also supports DDC2™, so it can also be used as an EDID data storage memory for display equipment.

Functions

- Capacity : 2K bits (256 × 8 bits) + 2K bits (256 × 8 bits), 4K bits in total
- Bank structure : 2 banks (2K bits + 2K bits)
- Single supply voltage : 2.5V to 5.5V
- Interface : Two wire serial interface (I^2C Bus*), VESA DDC2™ compliant**
- Operating clock frequency : 400kHz (max)
- Low power consumption : Standby: 5μA (max)
  : Active (Read): 0.5mA (max)

Continued on next page.

* : I^2C Bus is a trademark of Philips Corporation.
** : DDC and EDID are trademarks of Video Electronics Standard Association (VESA).

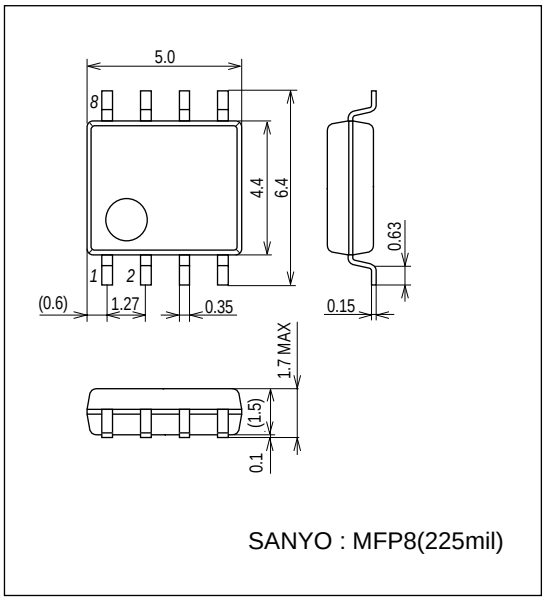
* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

Continued from preceding page.

- Automatic page write mode: 16 bytes
- Read mode : Sequential read and random read
- Erase/Write cycles : 10^6 cycles
- Data Retention : 20 years
- High reliability : Adopts SANYO's proprietary symmetric memory array configuration (USP6947325)
  Noise filters connected to SCL1, SDA2, SCL2 and SDA2 pins
  Incorporates a feature to prohibit write operations under low voltage conditions.
- Package : LE24CBK22M MFP8 (225mil)
  : LE24CBK22TT MSOP8 (150mil)

Package Dimensions

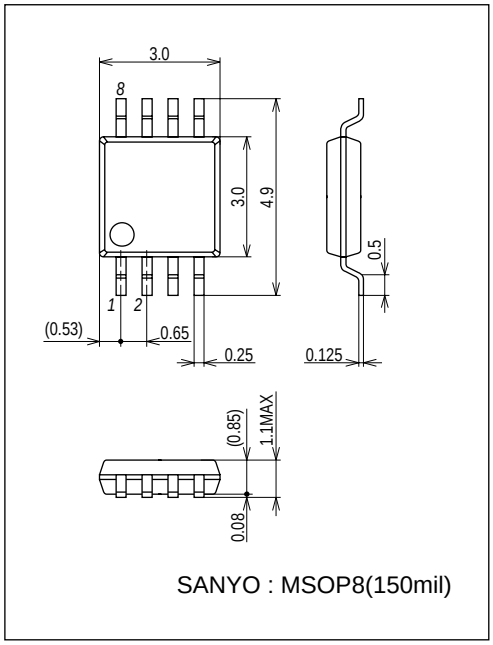
unit:mm (typ)
3032E [LE24CBK22M]



SANYO : MFP8(225mil)

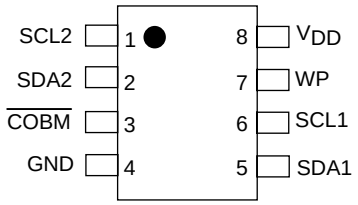
Package Dimensions

unit:mm (typ)
3245B [LE24CBK22TT]



SANYO : MSOP8(150mil)

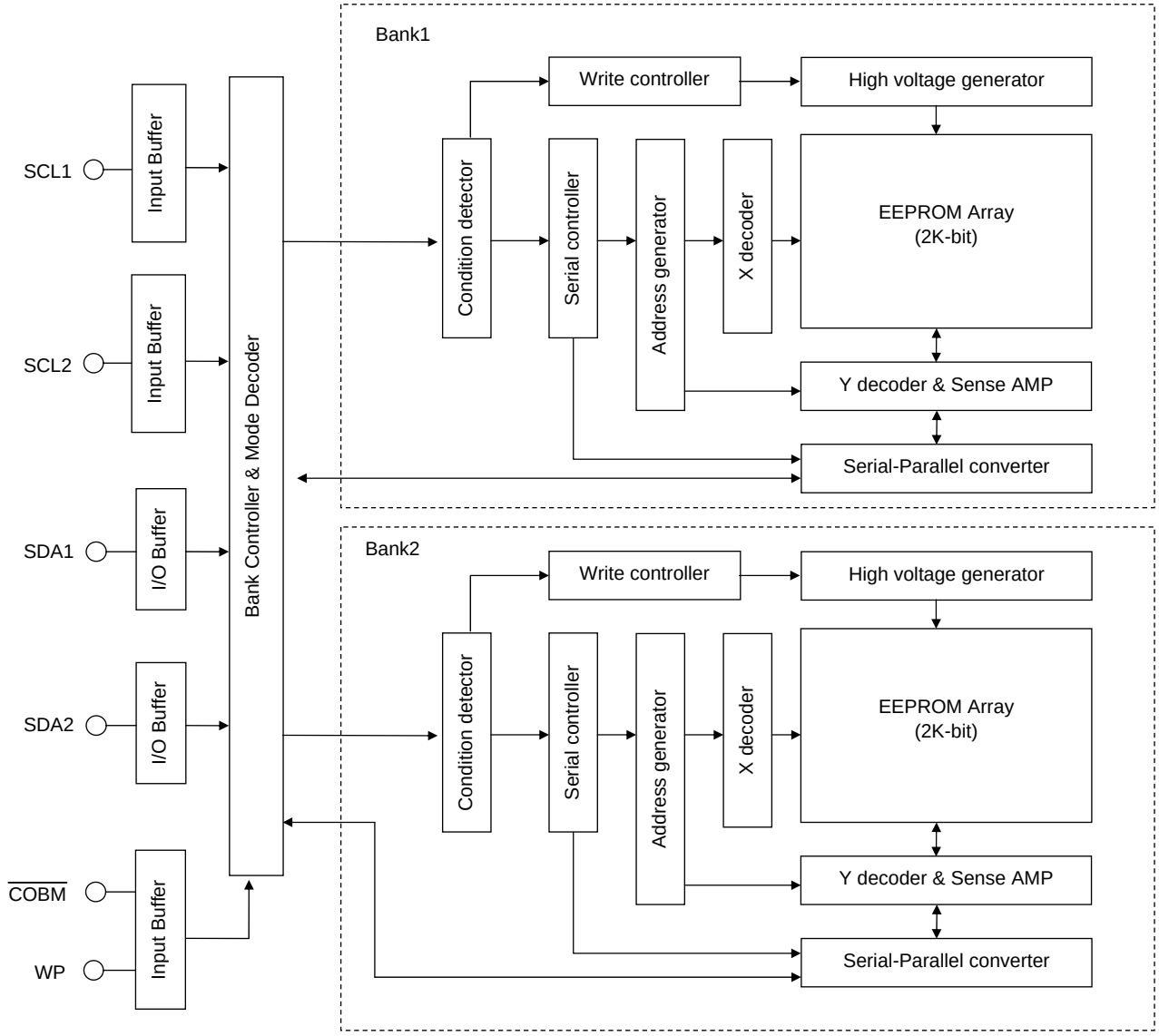
Pin Assignment



Pin Descriptions

PIN.1	SCL2	Serial clock input	(For Bank2)
PIN.2	SDA2	Serial data input/output	
PIN.3	$\overline{\text{COBM}}$	Bank/combine mode switching	
PIN.4	GND	Ground	
PIN.5	SDA1	Serial data input/output	(For Bank1)
PIN.6	SCL1	Serial clock input	
PIN.7	WP	Write protect	
PIN.8	V_{DD}	Power supply	

Block Diagram



Description of Operation

The Bank1 control signals are SCL1 and SDA1, and the Bank2 control signals are SCL2 and SDA2. The control signals for each bank can be controlled separately, regardless of the other bank's status. This enables behavior like two separate EEPROM mounted in a single package, enabling the Bank1 and Bank2 sides to be used simultaneously for two independent systems.

Bank mode (2K bits + 2K bits) and combined mode (internally treated as 4K bits) can be switched using the $\overline{\text{COBM}}$ pin. In combined mode, the Bank1 control signals (SCL1, SDA1) are used, and both Bank1 and Bank2 are accessed. This enables the two-bank configuration (2K bits + 2K bits) to be used as a pseudo one-bank configuration (4K bits), which allows access to both the Bank1 and Bank2 areas using a single system of control signals (SCL1, SDA1). Data correlation is guaranteed between combined mode and bank mode, enabling operation while switching the mode, such as performing write in combined mode and read in bank mode.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage			-0.5 to +6.5	V
DC input voltage			-0.5 to +5.5	V
Over-shoot voltage		Below 20ns	-1.0 to +6.5	V
Storage temperature	Tstg		-65 to +150	°C

Note: If an electrical stress exceeding the maximum rating is applied, the device may be damaged.

Operating Conditions

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage			2.5 to 5.5	V
Operating temperature			-40 to +85	°C

DC Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD}=2.5V to 5.5V			Unit
			min	typ	max	
Supply current at reading (when either Bank1 or Bank2 is read)	$I_{CC}11$	f=400kHz			0.5	mA
Supply current at reading (when both Bank1 and Bank2 are read simultaneously)	$I_{CC}12$	f=400kHz			0.8	mA
Supply current at writing (when either Bank1 or Bank2 is written)	$I_{CC}21$	f=400kHz, t_{WC}=5ms			5	mA
Supply current at writing (when both Bank1 and Bank2 are written simultaneously)	$I_{CC}22$	f=400kHz, t_{WC}=5ms			8	mA
Standby current	I_{SB}	V_{IN}=V_{DD} or GND		0.7	5	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{DD}	-2.0		+2.0	μA
Output leakage current (SDA)	I_{LO}	V_{OUT}=GND to V_{DD}	-2.0		+2.0	μA
Input low voltage	V_{IL}				V_{DD}*0.3	V
Input high voltage	V_{IH}		V_{DD}*0.7			V
Output low voltage	V_{OL}	I_{OL}=0.7mA, V_{DD}=2.5V			0.2	V
		I_{OL}=3.0mA, V_{DD}=2.5V			0.4	V
		I_{OL}=3.0mA, V_{DD}=5.5V			0.4	V
		I_{OL}=6.0mA, V_{DD}=4.5V			0.6	V

Capacitance/Ta=25°C, f=100kHz

Parameter	Symbol	Conditions	min	typ	max	Unit
In/Output capacitance	$C_{I/O}$	$V_{I/O}$=0V (SDA)		2	5	pF
Input capacitance	C_I	V_{IN}=0V (other than SDA)		2	5	pF

Note: This parameter is sampled and not 100% tested.

AC Electric Characteristics

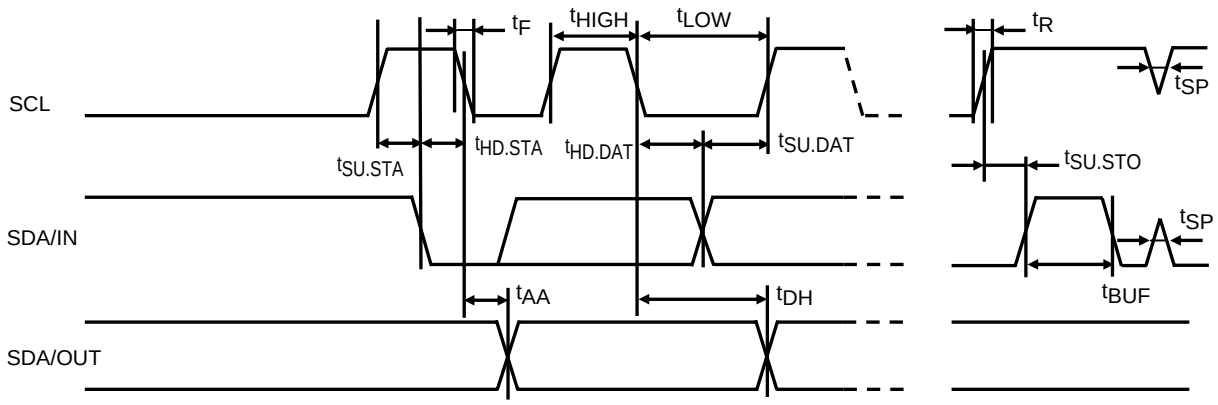
Fast Mode

Parameter	Symbol	V_{DD}=2.5V to 5.5V			unit
		min	typ	max	
Slave mode SCL clock frequency	f_{SCLS}	0		400	kHz
SCL clock low time	t_{LOW}	1200			ns
SCL clock high time	t_{HIGH}	600			ns
SDA output delay time	t_{AA}	100		900	ns
SDA data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	600			ns
Start condition hold time	$t_{HD.STA}$	600			ns
Data in setup time	$t_{SU.DAT}$	100			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	600			ns
SCL, SDA rise time	t_R			300	ns
SCL, SDA fall time	t_F			300	ns
Bus release time	t_{BUF}	1200			ns
Noise suppression time	t_{SP}			100	ns
Write cycle time	t_{WC}			5	ms

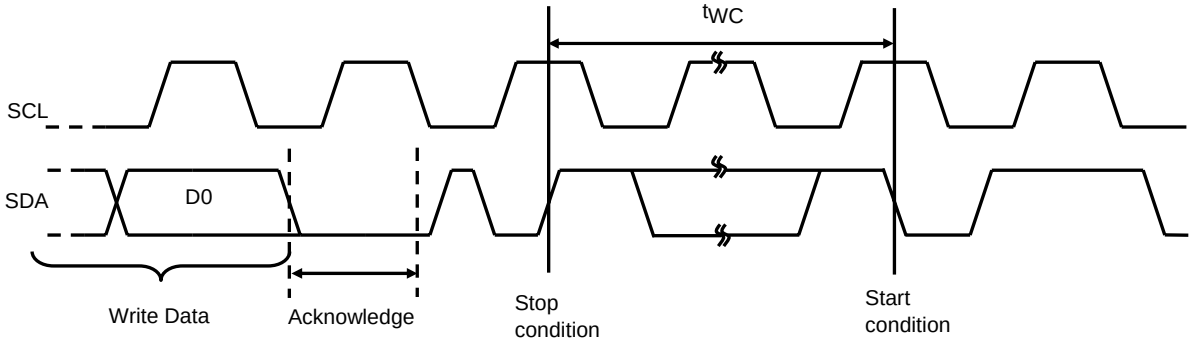
Standard Mode

Parameter	Symbol	V_{DD}=2.5V to 5.5V			unit
		min	typ	max	
Slave mode SCL clock frequency	f_{SCLS}	0		100	kHz
SCL clock low time	t_{LOW}	4700			ns
SCL clock high time	t_{HIGH}	4000			ns
SDA output delay time	t_{AA}	100		3500	ns
SDA data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	4700			ns
Start condition hold time	$t_{HD.STA}$	4000			ns
Data in setup time	$t_{SU.DAT}$	250			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	4000			ns
SCL, SDA rise time	t_R			1000	ns
SCL, SDA fall time	t_F			300	ns
Bus release time	t_{BUF}	4700			ns
Noise suppression time	t_{SP}			100	ns
Write cycle time	t_{WC}			5	ms

Bus Timing



Write Timing



Pin Functions

(For Bank1)

SCL1 (serial clock input) pin

The SCL1 pin is the serial clock input pin used to access the Bank1 area, and processes signals at the rising and falling edges of the SCL1 clock signal.

This pin must be pulled up by a resistor to the V_{DD} level, and wired-ORed with another open drain (or open collector) output device for use.

In combined mode, the SCL1 pin is serial clock input pin controlled both Bank1 and Bank2.

SDA1 (serial data input/output) pin

The SDA1 pin is used to transfer serial data to the input/output of the Bank1 side area and it consists of a signal input pin and n-channel transistor open drain output pin.

Like the SCL1 line, the SDA1 line must be pulled up by a resistor to the V_{DD} level and wired-ORed with another open drain (or open collector) output device for use.

In combined mode, the SDA1 pin is serial data input/output pin controlled both Bank1 and Bank2.

(For Bank2)

SCL2 (serial clock input) pin

The SCL2 pin is the serial clock input pin used to access the Bank2 area, and processes signals at the rising and falling edges of the SCL2 clock signal.

This pin must be pulled up by a resistor to the V_{DD} level, and wired-ORed with another open drain (or open collector) output device for use.

In combined mode, the SCL2 pin is invalid.

SDA2 (serial data input/output) pin

The SDA2 pin is used to transfer serial data to the input/output of the Bank2 side area and it consists of a signal input pin and n-channel transistor open drain output pin.

Like the SCL2 line, the SDA2 line must be pulled up by a resistor to the V_{DD} level and wired-ORed with another open drain (or open collector) output device for use.

In combined mode, the SDA2 pin is invalid.

(Shared pins)

WP (write protect) pin

When the WP pin is high, write protect is enabled, and write is prohibited to all memory areas within both Bank1 and Bank2. Read operation can access all memory areas regardless of the WP pin status.

$\overline{\text{COBM}}$(combined Mode) pin

The $\overline{\text{COBM}}$ pin is used to switch the EEPROM internal operation between bank mode and combined mode. The EEPROM operates in bank mode when the $\overline{\text{COBM}}$ pin is high, and in combined mode when low.

Note that in combined mode, the SCL2 and SDA2 pins are treated as don't care.

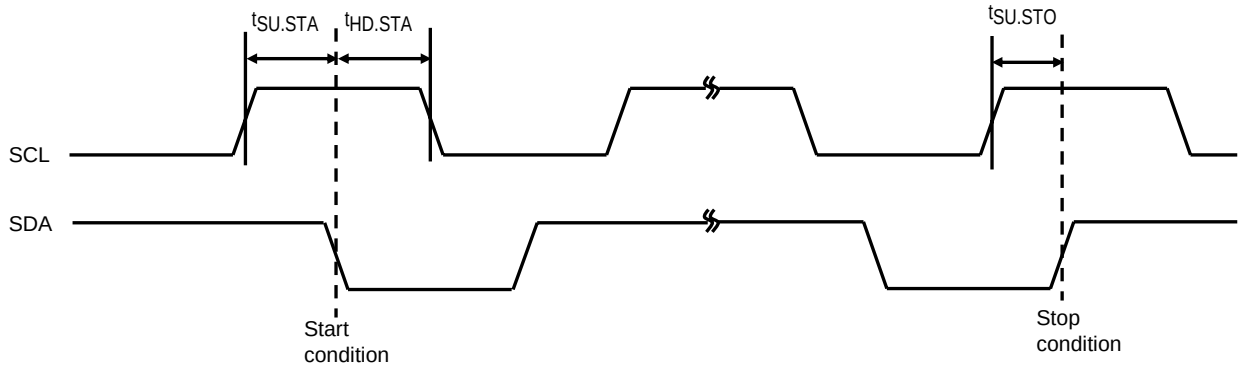
Functional Description

1. Start condition

When the SCL line is at the high level, the start condition is established by changing the SDA line from high to low. The operation of the EEPROM as a slave starts in the start condition.

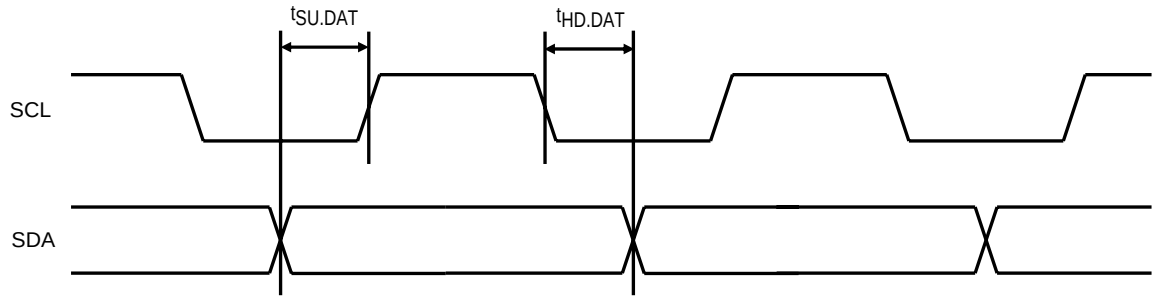
2. Stop condition

When the SCL line is at the high level, the stop condition is established by changing the SDA line from low to high. When the device is set up for the read sequence, the read operation is suspended when the stop condition is received, and the device is set to standby mode. When it is set up for the write sequence, the capture of the write data is ended when the stop condition is received, and the EEPROM internal write operation is started.



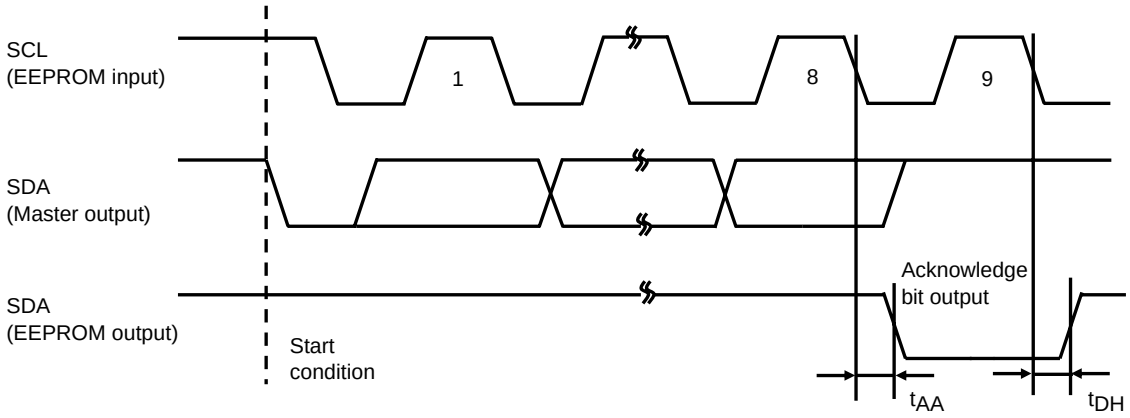
3. Data transfer

Data is transferred by changing the SDA line while the SCL line is low. When the SDA line is changed while the SCL line is high, the resulting condition will be recognized as the start or stop condition.



4. Acknowledge

During data transfer, 8 bits are transferred in succession, and then in the ninth clock cycle period the device on the system bus receiving the data sets the SDA line to low, and sends the acknowledge signal indicating that the data has been received. The acknowledge signal is not sent during an EEPROM internal write operation.

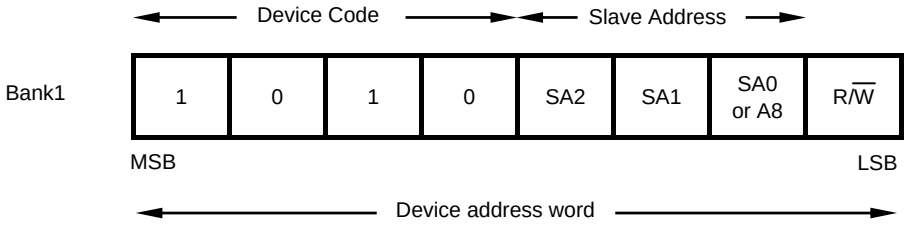


5. Device addressing

For the purposes of communication, the master device in the system generates the start condition for the slave device. Communication with a particular slave device is enabled by sending along the SDA bus the device address, which is 7 bits long, and the read/write command code, which is 1 bit long, immediately following the start condition.

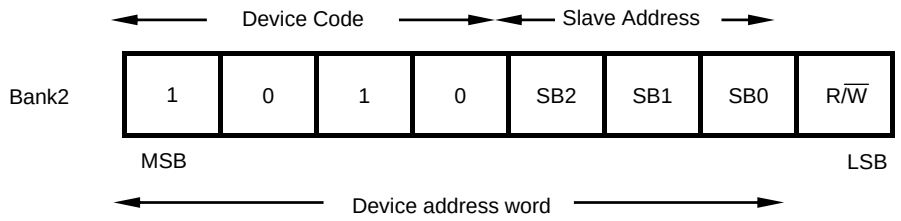
The upper four bits of the device address are called the device code which, for this product, is fixed as “1010.” This device has the upper 3-bit of the Slave Device address as the Slave address (Bank1: SA2, SA1, SA0 and Bank2: SB2, SB1, SB0), which fixed internally. The value of Slave address are SA2=0, SA1=0, SA0=0 and SB2=0, SB1=0, B0=0

When the device code input from SDA and the slave addresses are compared with the product’s device code and slave addresses that were set at the mounting stage and found to match, the product sends the acknowledge signal during the ninth clock cycle period, and initiates the read or write operation in accordance with the read or write command code. If they do not match, the EEPROM returns to standby mode. When a read operation is performed immediately after the slave device has been switched, the random read command must be used.



* The default internal slave address is set to SA2 = 0, SA1 = 0, SA0 = 0.
* In bank mode (2K bits), the valid address is A7 to A0, and the valid slave address is SA2, SA1 and SA0.
* In combined mode (4K bits), the valid address is A8 to A0, and the slave address SA2 and SA1 is don’t care.
  A8 = 0: Selects the Bank1 area, A8 = 1: Selects the Bank2 area.

	Valid Address	Slave Address
Bank mode ($\overline{\text{COBM}}$='H')	A7-A0	SA2, SA1, SA0
Combine mode ($\overline{\text{COBM}}$='L')	A8-A0 A8=0: Selects the Bank1 area A8=1: Selects the Bank2 area	SA2, SA1 But SA2 and SA1 are don’t care.



* The default internal slave address is set to SB2 = 0, SB1 = 0, SB0 = 0.
* In combine mode (4K bits), communication in Bank2 side is invalid.

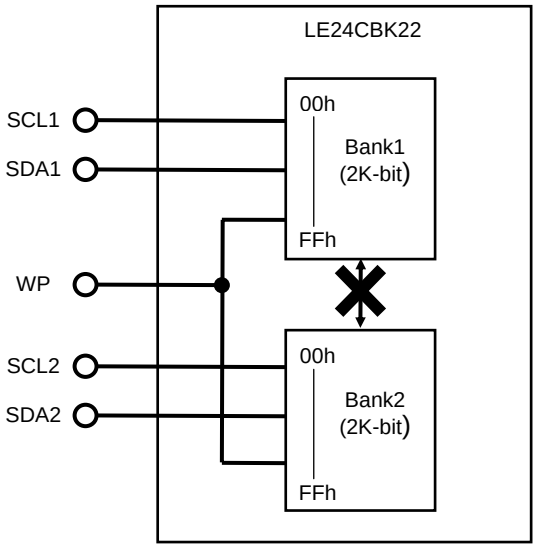
	Valid Address	Slave Address
Bank mode ($\overline{COBM}$='H')	A7-A0	SB2, SB1, SB0
Combine mode ($\overline{COBM}$='L')	-	-

6. Internal mode

The EEPROM functions in bank mode when the $\overline{COBM}$ pin is high, or in combined mode when the $\overline{COBM}$ pin is low.

6-1. Bank mode

The EEPROM functions in bank mode when the $\overline{COBM}$ pin is high. In bank mode, each bank (Bank1, Bank2) is controlled separately using dedicated control signals. The two banks are independent, and can be controlled separately regardless of the other bank's status. This enables treatment like two separate EEPROM mounted in a single package, which means that the Bank1 and Bank2 sides can be connected to the MCU of separate systems.

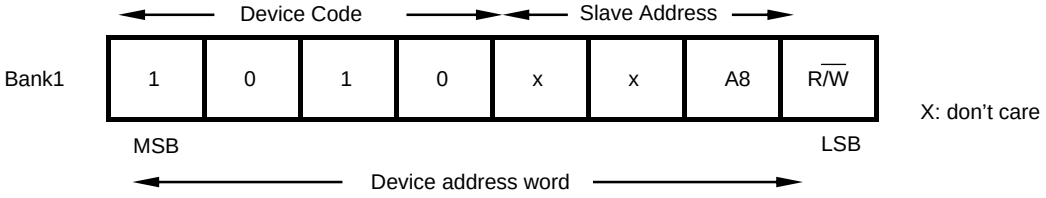


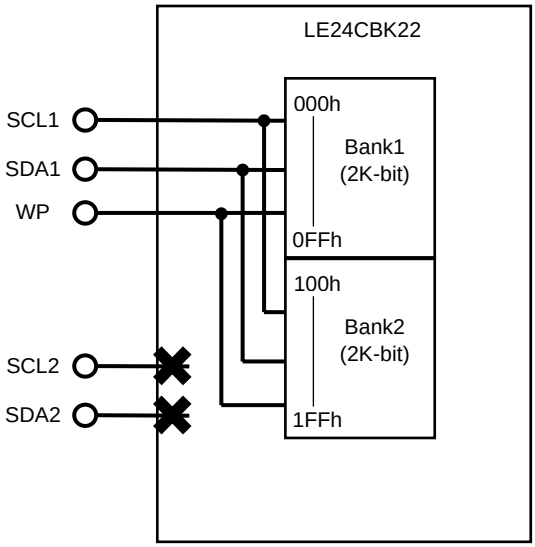
6-2. Combine mode

The EEPROM functions in combined mode when the $\overline{\text{COBM}}$ pin is low. In combined mode, The Bank1 control signals SCL1 and SDA1 are used to control both Bank1 and Bank2. Combined mode uses the two-bank configuration (2K bits + 2K bits) as a pseudo one-bank configuration (4K bits). In combined mode, the Bank2 control signals SCL2 and SDA2 are treated as don't care.

In combined mode, the memory area is processed as a 4K-bit single bank, so the MSB address changes from A7 to A8, and A8 becomes a valid address. Set A8 = 0 to control the Bank1 area, or A8 = 1 to control the Bank2 area.

Data correlation is guaranteed between combined mode and bank mode, enabling operation while switching the mode, such as performing write in combined mode and read in bank mode.

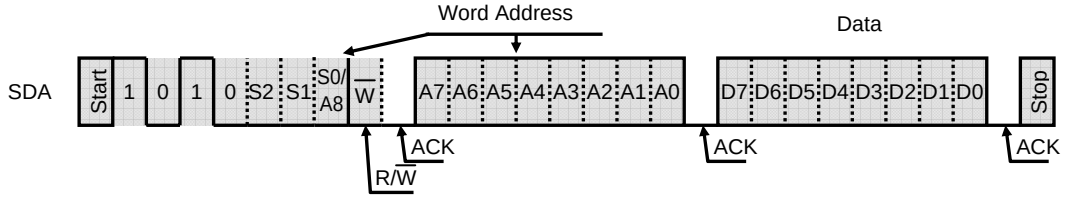




7 EEPROM write operation

7-1. Byte writing

When the EEPROM receives the 7-bit device address and write command code "0" after the start condition, it generates an acknowledge signal. After this, if it receives the 8-bit word address, generates an acknowledge signal, receives the 8-bit write data, generates an acknowledge signal and then receives the stop condition, the internal write operation of the EEPROM in the designated memory address will start. Rewriting is completed in the t_{WC} period after the stop condition. During an EEPROM internal write operation, no input is accepted and no acknowledge signals are generated.



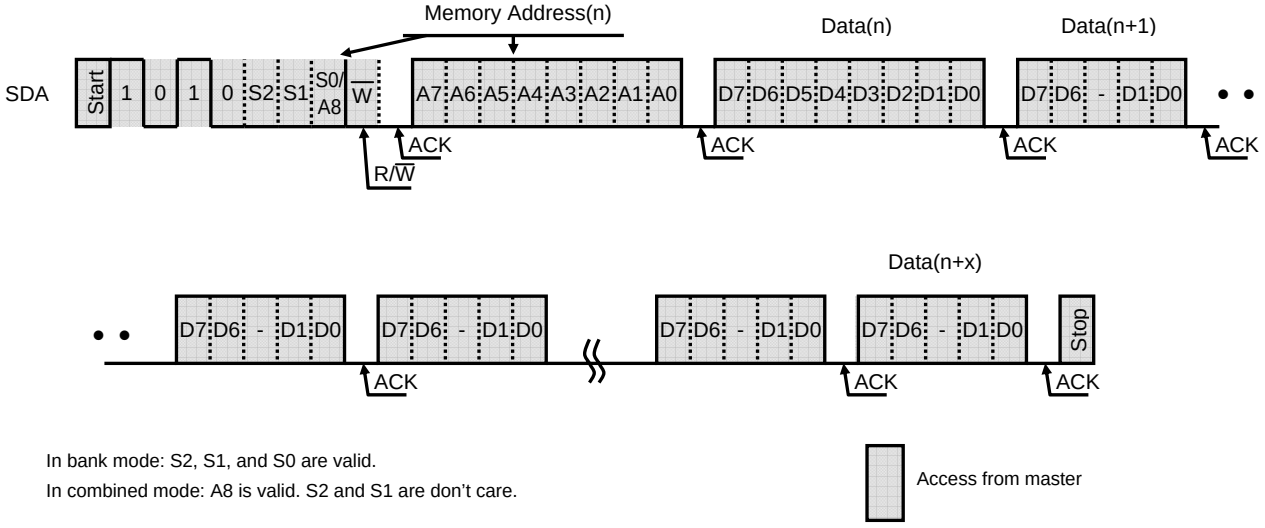
In bank mode: S2, S1, and S0 are valid.
In combined mode: A8 is valid. S2 and S1 are don't care.

Access from master

7-2. Page writing

This product enables pages with up to 16 bytes to be written. The basic data transfer procedure is the same as for byte writing: Following the start condition, the 7-bit device address and write command code “0,” word address (n), and data (n) are input in this order while confirming acknowledge “0” every 9 bits. The page write mode is established if, after data (n) is input, the write data (n+1) is input without inputting the stop condition. After this, the write data equivalent to the largest page size can be received by a continuous process of repeating the receiving of the 8-bit write data and generating the acknowledge signals.

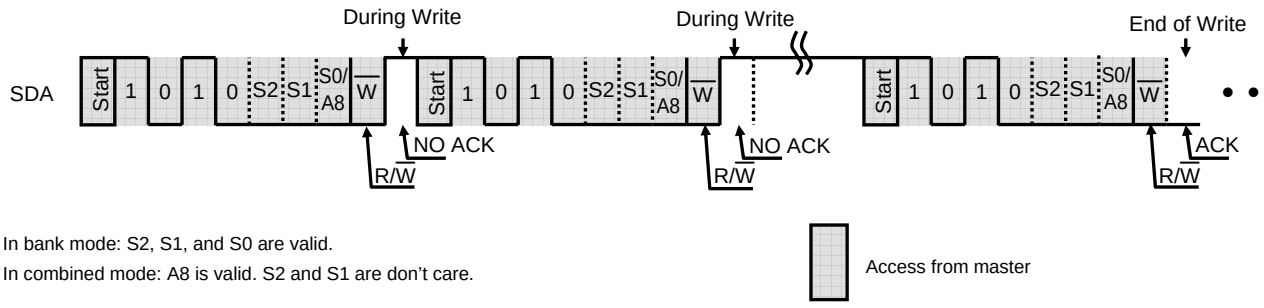
At the point when the write data (n+1) has been input, the lower 4 bits (A0-A3) of the word addresses are automatically incremented to form the (n+1) address. In this way, the write data can be successively input, and the word address on the page is incremented each time the write data is input. If the write data exceeds 16 bytes or the last address of the page is exceeded, the word address on the page is rolled over. Write data will be input into the same address two or more times, but in such cases the write data that was input last will take effect. Finally, the EEPROM internal write operation corresponding to the page size for which the write data is received starts from the designated memory address when the stop condition is received.



7-3. Acknowledge polling

Acknowledge polling is used to find out when the EEPROM internal write operation is completed. When the stop condition is received and the EEPROM starts rewriting, all operations are prohibited, and no response can be given to the signals sent by the master device. Therefore, in order to find out when the EEPROM internal write operation is completed, the start condition, device address and write command code are sent from the master device to the EEPROM (slave device), and the response of the slave device is detected.

In other words, if the slave device does not send the acknowledge signal, it means that the internal write operation is in progress; conversely, if it does send the acknowledge signal, it means that the internal write operation has been completed.



8 EEPROM read operations

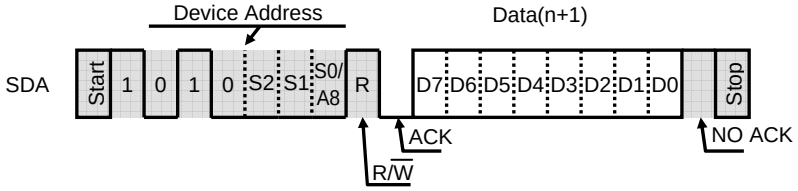
8-1. Current address reading

The address equivalent to the memory address accessed last +1 is held as the internal address of the EEPROM for both write* and read operations. Therefore, provided that the master device has recognized the position of the EEPROM address pointer, data can be read from the memory address with the current address pointer without specifying the word address.

As with writing, current address reading involves receiving the 7-bit device address and read command code “1” following the start condition, at which time the EEPROM generates an acknowledge signal. After this, the 8-bit data of the (n+1) address is output serially starting with the highest bits. After the 8 bits have been output, by not sending an acknowledge signal and inputting the stop condition, the EEPROM completes the read operation and is set to standby mode.

If the previous read address is the last address, the address for the current address reading is rolled over to become address 0.

*: If the last address (A3-A0=1111b) on the page has been designated at the write operation as the word address, the first address (A3-A0=0000b) on the page serves as the internal address after writing.



In bank mode: S2, S1, and S0 are valid.
In combined mode: A8 is valid. S2 and S1 are don’t care.

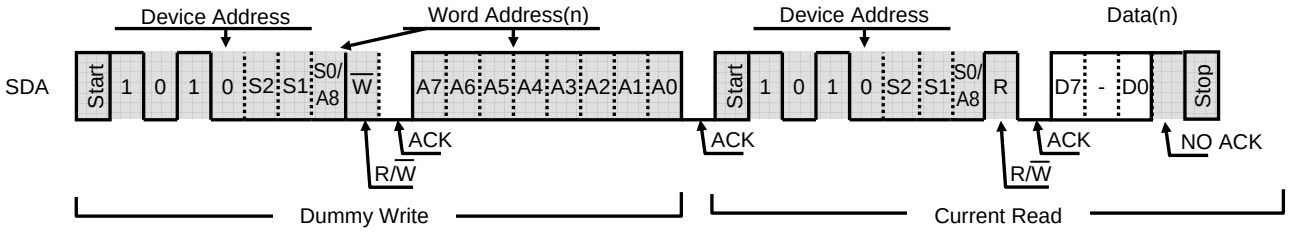
Access from master

8-2. Random read

Random read is a mode in which any memory address is specified and its data read. The address is specified by a dummy write input.

First, when the EEPROM receives the 7-bit device address and write command code “0” following the start condition, it generates an acknowledge signal. It then receives the 8-bit word address, and generates an acknowledge signal. Through these operations, the word address is loaded into the address counter inside the EEPROM.

Next, the start condition is input again and the current read is initiated. This causes the data of the word address that was input using the dummy write input to be output. If, after the data is output, an acknowledge signal is not sent and the stop condition is input, reading is completed, and the EEPROM returns to standby mode.

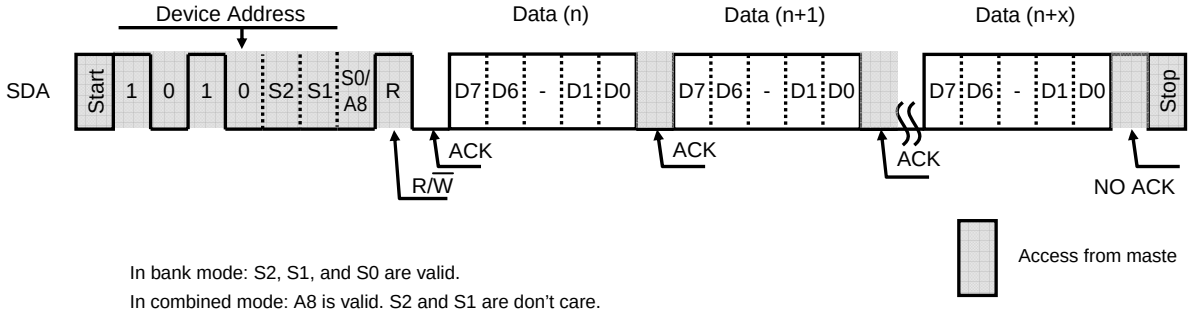


In bank mode: S2, S1, and S0 are valid.
In combined mode: A8 is valid. S2 and S1 are don’t care.

Access from maste

8-3. Sequential read

In this mode, the data is read continuously, and sequential read operations can be performed with both current address read and random read. If, after the 8-bit data has been output, acknowledge “0” is input and reading is continued without issuing the stop condition, the address is incremented, and the data of the next address is output.
If acknowledge “0” continues to be input after the data has been output in this way, the data is successively output while the address is incremented. When the last address is reached, it is rolled over to address 0, and the data continues to be read. As with current address read and random read, the operation is completed by inputting the stop condition without sending an acknowledge signal.



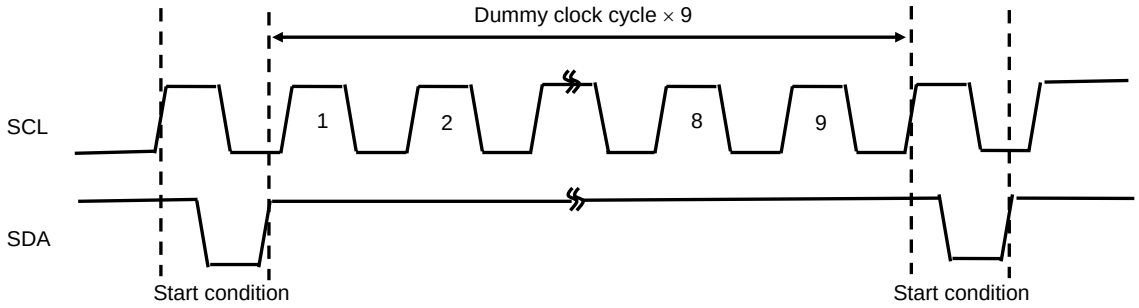
In bank mode: S2, S1, and S0 are valid.
In combined mode: A8 is valid. S2 and S1 are don’t care.

Application Notes

1) Software reset function

Software reset (start condition + 9 dummy clock cycles + start condition), shown in the figure below, is executed in order to avoid erroneous operation after power-on and to reset while the command input sequence. During the dummy clock input period, the SDA bus must be opened (set to high by a pull-up resistor). Since it is possible for the ACK output and read data to be output from the EEPROM during the dummy clock period, forcibly entering H will result in an overcurrent flow.

Note that this software reset function does not work during the internal write cycle.



2) Pull-up resistor of SDA pin

Due to the demands of the I^2C bus protocol function, the SDA pin must be connected to a pull-up resistor (with a resistance from several kΩ to several tens of kΩ) without fail. The appropriate value must be selected for this resistance (R_{PU}) on the basis of the V_{IL} and I_{IL} of the microcontroller and other devices controlling this product as well as the V_{OL}–I_{OL} characteristics of the product. Generally, when the resistance is too high, the operating frequency will be restricted; conversely, when it is too low, the operating current consumption will increase.

R_{PU} maximum resistance

The maximum resistance must be set in such a way that the bus potential, which is determined by the sum total (I_L) of the input leaks of the devices connected to the SDA bus and by R_{PU}, can completely satisfy the input high level (V_{IH} min) of the microcontroller and EEPROM. However, a resistance value that satisfies SDA rise time t_R and fall time t_F must be set.

R_{PU} maximum value = $(V_{DD} - V_{IH})/I_L$

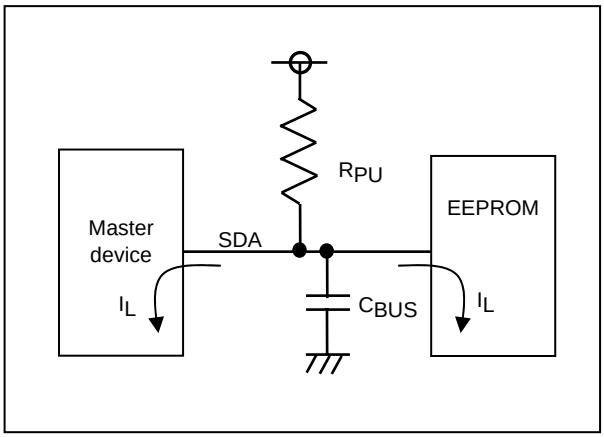
Example: When V_{DD}=3.0V and I_L= 2μA
R_{PU} maximum value = (3.0V – 3.0V × 0.8)/2μA = 300kΩ

R_{PU} minimum value

A resistance corresponding to the low-level output voltage (V_{OL} max) of SANYO's EEPROM must be set.

R_{PU} minimum value = $(V_{DD} - V_{OL})/I_{OL}$

Example: When V_{DD}=3.0V, V_{OL} = 0.4V and I_{OL} = 1mA
R_{PU} minimum value = (3.0V – 0.4)/1mA = 2.6kΩ

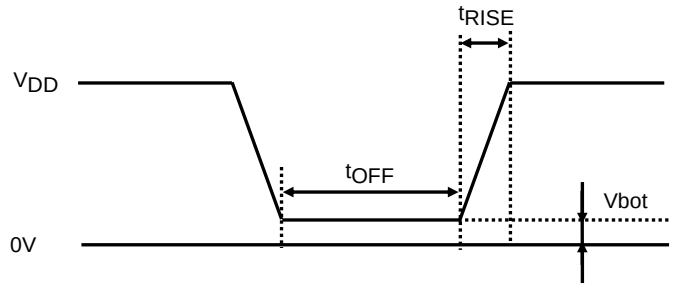


Recommended R_{PU} setting

R_{PU} is set to strike a good balance between the operating frequency requirements and power consumption. If it is assumed that the SDA load capacitance is 50pF and the SDA output data strobe time is 500ns, R_{PU} will be about R_{PU} = 500ns/50pF = 10kΩ.

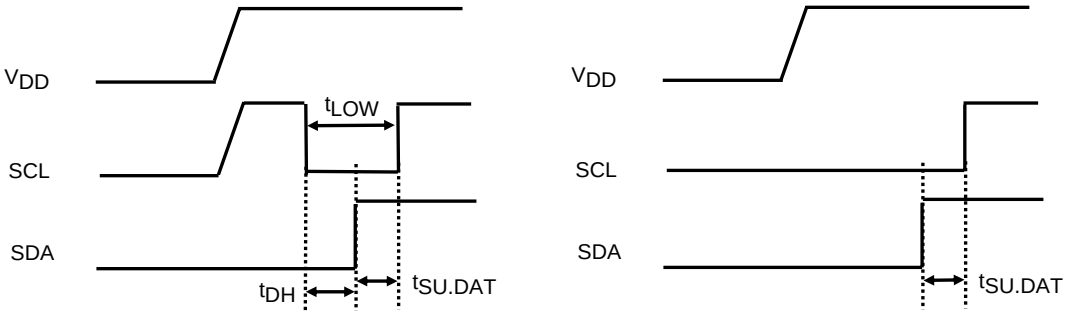
3) Precautions when turning on the power
This product contains a power-on reset circuit for preventing the inadvertent writing of data when the power is turned on. The following conditions must be met in order to ensure stable operation of this circuit. No data guarantees are given in the event of an instantaneous power failure during the internal write operation.

Item	Symbol	V_{DD}=2.5 to 5.5V			unit
		min	typ	max	
Power rise time	t_{RISE}			100	ms
Power off time	t_{OFF}	10			ms
Power bottom voltage	V_{bot}			0.2	V



Notes:
1) The SDA pin must be set to high and the SCL pin to low or high.
2) Steps must be taken to ensure that the SDA and SCL pins are not placed in a high-impedance state.

A. If it is not possible to satisfy the instruction 1 in Note above, and SDA is set to low during power rise
After the power has stabilized, the SCL and SDA pins must be controlled as shown below, with both pins set to high.



B. If it is not possible to satisfy the instruction 2 in Note above
After the power has stabilized, software reset must be executed.

C. If it is not possible to satisfy the instructions both 1 and 2 in Note above
After the power has stabilized, the steps in A must be executed, then software reset must be executed.

4) Noise filter for the SCL and SDA pins
This product contains a filter circuit for eliminating noise at the SCL and SDA pins. Pulses of 100ns or less are not recognized because of this function.

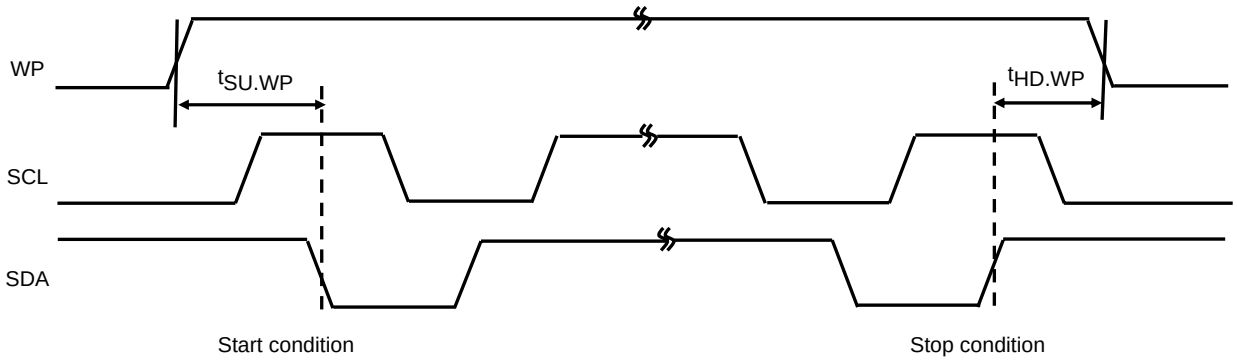
5) Function to inhibit writing when supply voltage is low
This product contains a supply voltage monitoring circuit that inhibits inadvertent writing below the guaranteed operating supply voltage range. The data is protected by ensuring that write operations are not started at voltages (typ.) of 1.3V and below.

6) Slave address settings
This product does not come with any slave address pins, but the information of the Bank1: SA2, SA1, SA0 and Bank2: SB2, SB1, SB0 slave addresses is held internally. SA2=0, SA1=0, SA0=0 and SB2=0, SB1=0, SB0=0 were set for the slave addresses before shipment. During device addressing, these slave address codes must be executed following the device code.

7) Note on Write Protect Operation

This product prohibits writing to all memory areas when the WP pin is high. To ensure full write protection, the WP pin is set high for all periods from the start condition to the stop condition, and the condition below must be satisfied.

Item	Symbol	V_{DD}=2.5 to 5.5V			unit
		min	typ	max	
WP Setup time	$t_{SU.WP}$	600			ns
WP Hold time	$t_{HD.WP}$	600			ns

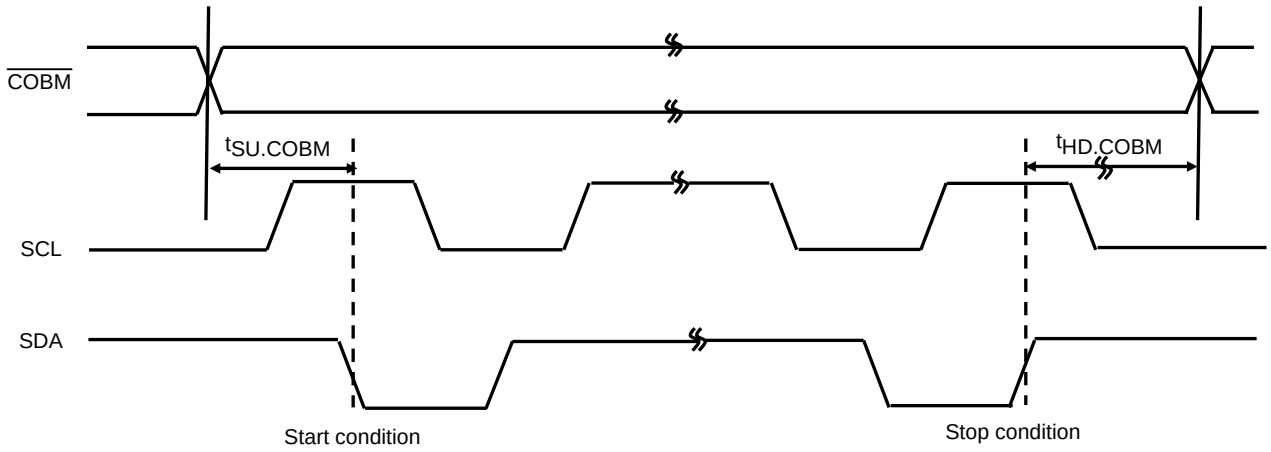


8) Notes on Mode Switching

This product selects bank mode operation or combined mode operation according to the $\overline{COBM}$ pin status. Changing the $\overline{COBM}$ pin status while this product is active (during access to Bank1 or Bank2, including during the write period) is prohibited.

The following conditions must be observed to ensure reliable access functions in each mode.

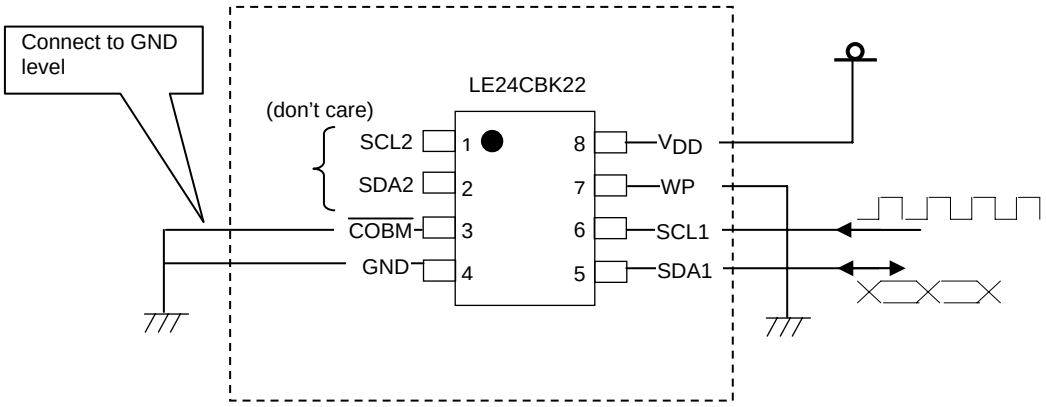
Item	Symbol	V_{DD}=2.5 to 5.5V			unit
		min	typ	max	
$\overline{COBM}$ Setup time	t_{SU}.COBM	10			μs
$\overline{COBM}$ Hold time (Write cycle time)	t_{HD}.COBM	5			ms

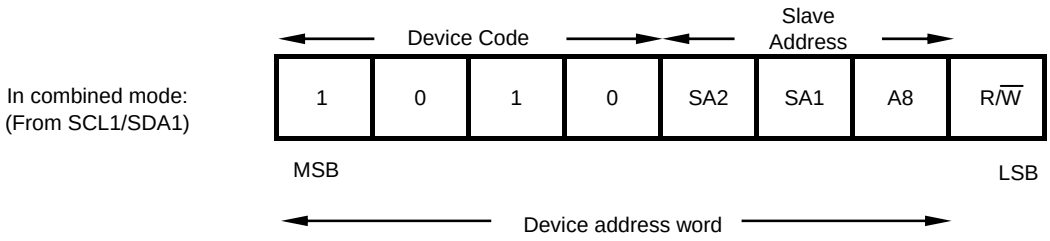


9) Write using a ROM writer in combined mode
This product enters combined mode by setting the $\overline{\text{COBM}}$ pin (Pin 3) low, which allows the two-bank configuration (2K bits + 2K bits) to be used as a pseudo one-bank configuration (4K bits). This enables write using a ROM writer in the manner of a typical 4k-bit EEPROM.

Pin 3 of standard 4K-bit EEPROM products is assigned a slave pin (S2), but Pin 3 of the LE24CBK22 is assigned the $\overline{\text{COBM}}$ pin. Combined mode is entered by setting the $\overline{\text{COBM}}$ pin low. In combined mode, the state of the SCL2 pin and SDA2 pin is "don't care" (may be either high, low, or open).

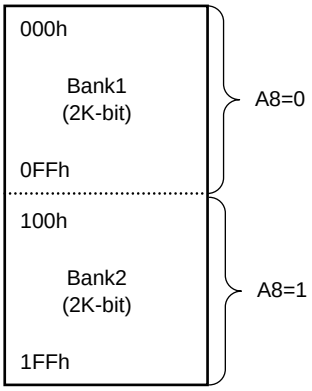
ROM writer connection example





In combined mode, the slave address (SA2, SA1) is don't care, and any combination can be entered (SA2 = 1, SA1 = 1 or SA2 = 1, SA1 = 0 or SA2 = 0, SA1 = 1 or SA2 = 0, SA1 = 0).

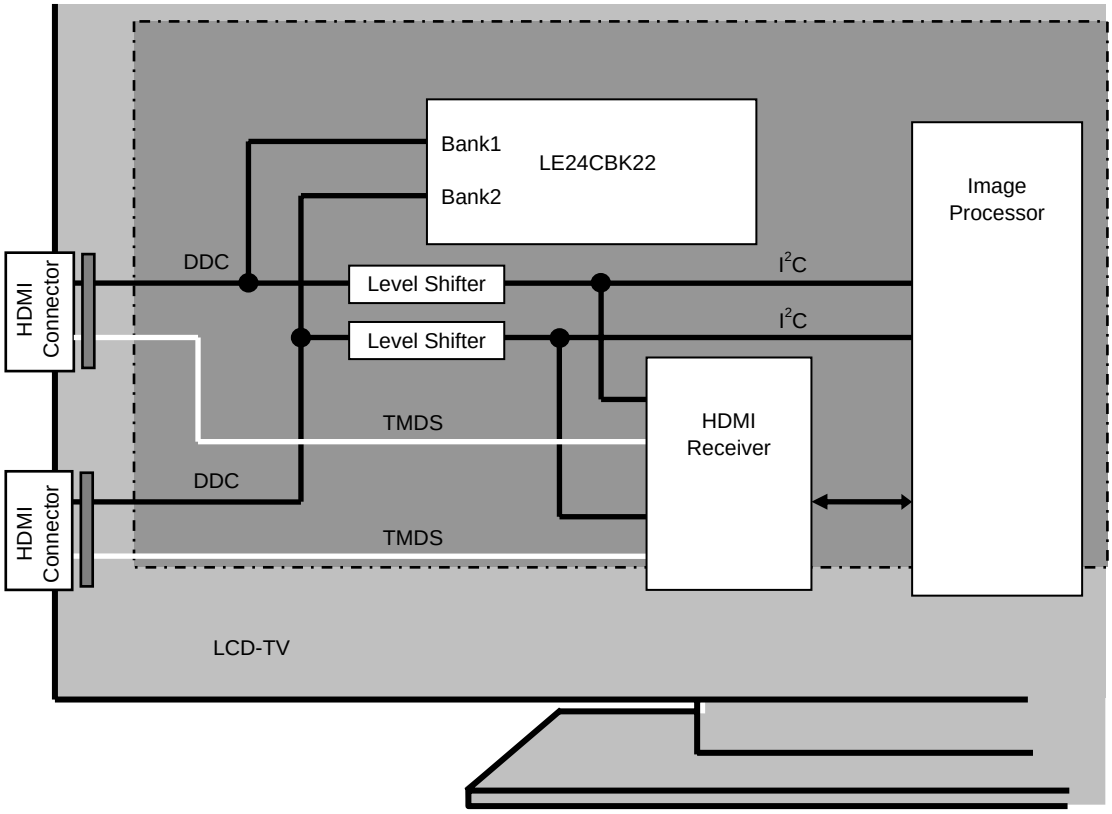
Memory Area (4K-bit)



The MSB address in combined mode is A8. A8 is used to select the Bank1 or Bank2 area. Set A8 = 0 to control the Bank1 area, or A8 = 1 to control the Bank2 area.

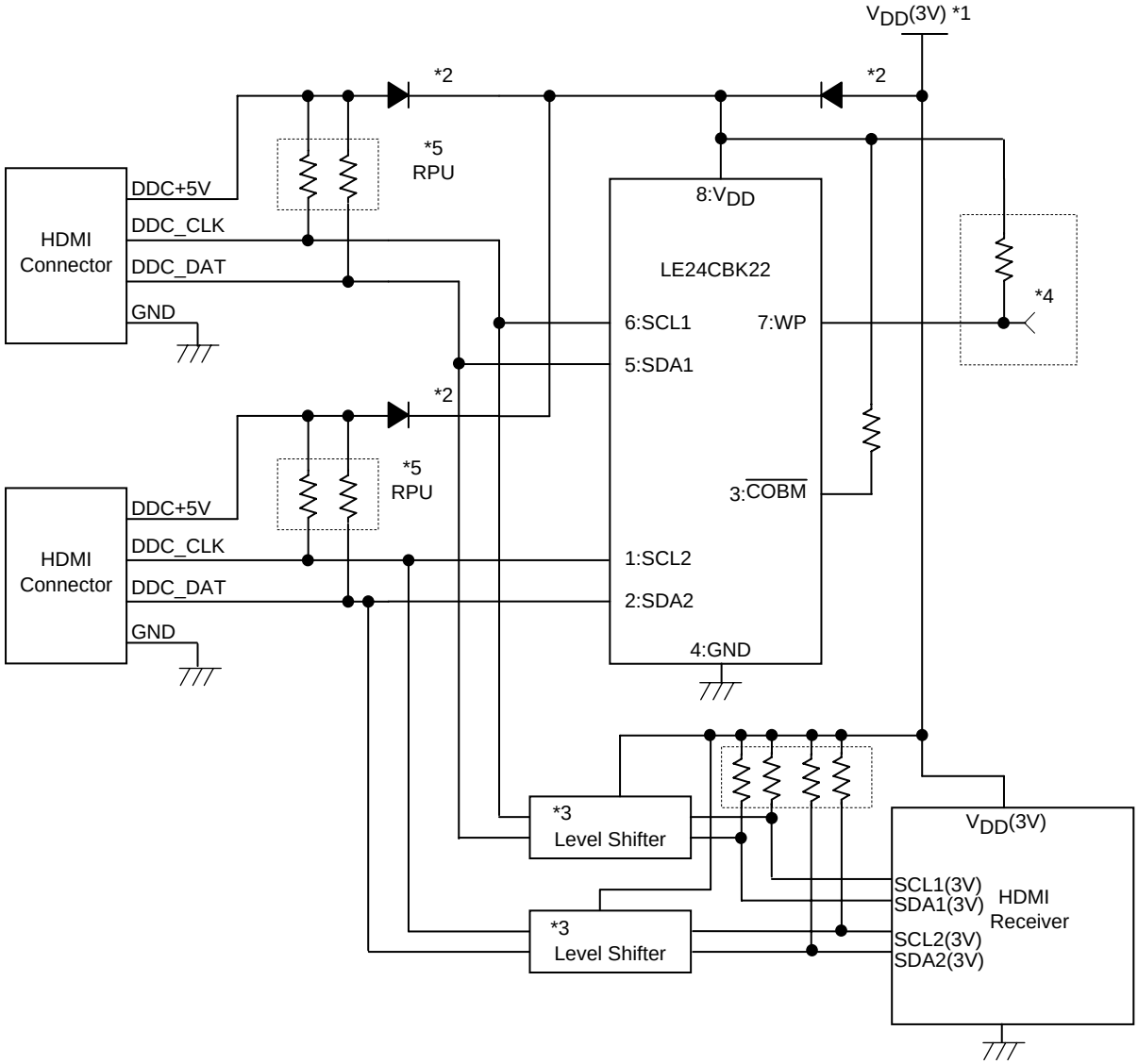
10) System Configuration Image
(HDMI System)

This product can support two HDMI ports simultaneously. Each port can be accessed (read operation, write operation) constantly, regardless of the other port's status.



11) Peripheral Circuit Diagram

Example of connection with HDMI receiver



*1: System power supply (3V) for HDMI receiver, etc.

*2: Reverse-current preventing diode

This device can be operated by supplying power from any of the connected HDMI connectors (DDC + 5V) or the system power supply (3V). However, the supply voltage must be set so that the voltage stepped-down by the reverse-current preventing diode is within the guaranteed operation voltage range of this device.

*3: Level shifter

When connecting the 5V HDMI connector side with a 3V system, level shifters must generally be inserted. However, this is not necessary when the HDMI receiver supports 5V input signals.

*4: Write protect

In general after implementation, use with HDMI applications presumes that this device performs read-only operation. The write protect function is enabled to prevent write due to mistaken access, by setting the WP pin to the same level as the power supply (8: V_{DD}) for this device.

Note that the WP pin is connected to the power supply via a resistor, and that when re-settings, etc., is necessary, write operation is enabled by connecting the WP pin to GND level using jumpers, etc.

*5: Pull-up resistors for the I^2C and DDC interfaces.

See item 2) in the Application Notes for the resistance value settings.