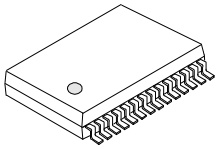
16-BIT CCD/CIS ANALOG SIGNAL PROCESSOR



TSSOP-28

■ DESCRIPTION

The **M1008** is a 16-bit CCD/CIS analog signal processor for imaging applications. A 3-channel architecture is designed to sample and control the outputs of tri-linear color CCD arrays. Each channel processes one color analog signal and includes an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), and a 16-bit A/D converter.

If there are sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, the CDS amplifiers are not necessary.

The 16-bit digital output is composed of high and low 8-bit output and is assessed by two reading cycles. The internal registers are programmed by a 3-wire serial interface which provides gain, offset and operating mode adjustments.

The typical operation power of **M1008** is 400mW in 5V power supply.

■ FEATURES

* 400mW In 5V Operation Supply
* Under 2mA Power-Down Mode
* Built-In16-Bit 30 Msps A/D Converter
* No Missing Codes
* Input Clamp Circuitry
* Correlated Double Sampling
* Programmable Gain
* 250mV Programmable Offset
* Built-In Voltage Reference
* Programmable 3-Wire Serial Interface
* 3V/5V Digital I/O Compatibility
* Up To 25 Msps In 1-Channel Operation
* Up To 30 Msps In 2-Channel (Even-Odd) Operation
* Up To 30 Msps In 3-Channel Operation

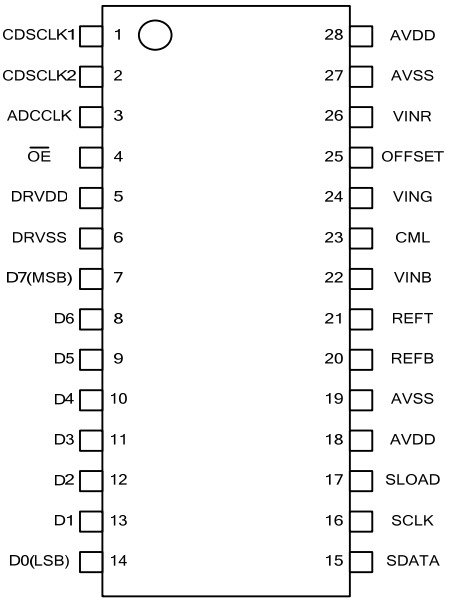
■ ORDERING INFORMATION

Ordering Number	Package	Packing
M1008G-P28-T	TSSOP-28	Tube
M1008G-P28-R	TSSOP-28	Tape Reel

M1008G-P28-T
(1) Packing Type
(2) Package Type
(3) Halogen Free

(1) T: Tube, R: Tape Reel
(2) P28: TSSOP-28
(3) G: Halogen Free

■ PIN CONFIGURATIONS

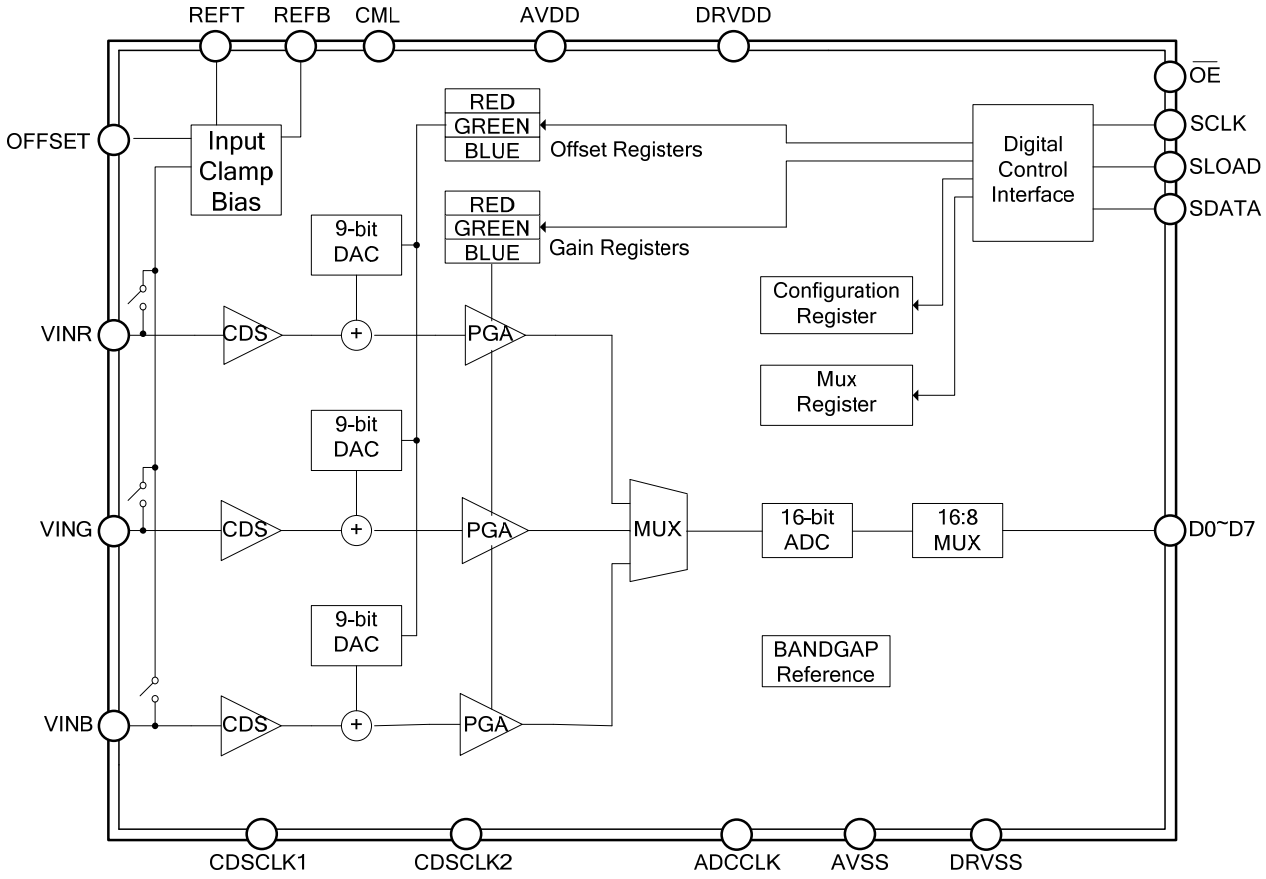


■ PIN DESCRIPTION

PIN NO.	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	CDSCLK1	DI	CDS reference clock pulse input
2	CDSCLK2	DI	CDS data clock pulse input
3	ADCCLK	DI	A/D sample clock input for 3-channels mode
4	$\overline{OE}$	DI	Output enable, active low
5	DRV_{DD}	P	Digital driver power
6	DRV_{SS}	P	Digital driver ground
7~14	D7~D0	DO	Digital data output
15	SDATA	DI/DO	Serial data input/output
16	SCLK	DI	Clock input for serial interface
17	SLOAD	DI	Serial interface load pulse
18,28	AV_{DD}	P	Analog supply
19,27	AV_{SS}	P	Analog ground
20	REFB	AO	Reference decoupling
21	REFT	AO	Reference decoupling
22	VINB	AI	Analog input, blue
23	CML	AO	Internal reference output
24	VING	AI	Analog input, green
25	OFFSET	AO	Clamp bias level decoupling
26	VINR	AI	Analog input, red

Note: I=input, O=output, I/O=input/output, P=power supply, G=ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.3 to V_{SS}+5.5	V
Input Voltage	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	V
Ambient Operation Temperature	T_{OPR}	-25 ~ +75	°C
Storage Temperature	T_{STG}	-50 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (AV_{DD}=5V, DV_{DD}=3V, T_A=25°C. Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Analog Power Supply	V_{ADD}		4.75	5	5.25	V
Digital Power Supply	V_{DRDD}		3	5	5.25	V
3-Channel Mode with CDS	t_{MAX3}		30			MSPS
2-Channel Mode with CDS	t_{MAX2}		30			MSPS
1-Channel Mode with CDS	t_{MAX1}		25			MSPS
ADC Resolution				16		Bits
Integral Nonlinear (INL)				±32		LSB
Differential Nonlinear (DNL)			-1		1	LSB
Offset Error			-100		100	mV
Gain Error				5		%FSR
Full-Scale Input Range	R_{FS}			2.0		V_{P-P}
Input Limits	$V_{I(LIMIT)}$		A_{VSS}-0.3	5	A_{VDD}+0.3	V
Input Current	I_{IN}			10		nA
PGA Gain at Minimum				1		V/V
PGA Gain at Maximum				5.85		V/V
PGA Gain Resolution				6		Bits
Programmable Offset at Minimum				-250		mV
Programmable Offset at Maximum				250		mV
Offset Resolution				9		Bits
Operating	T_A		0		70	°C
Total Power Consumption	P_{tot}			400		mW
High Level Input Voltage (CDSCLK1, CDSCLK2, ADCCLK, $\overline{OE}$, SCK, SLOAD)	V_{IH}		0.8*V_{DD}			V
Low Level Input Voltage (CDSCLK1, CDSCLK2, ADCCLK, $\overline{OE}$, SCK, SLOAD)	V_{IL}				0.2*V_{DD}	V
High Level Input Voltage (SDATA)	V_{IH1}		0.8*V_{DD}			V
Low Level Input Voltage (SDATA)	V_{IL1}				0.2*V_{DD}	V
High Level Input Current	I_{IH}			10		uA
Low Level Input Current	I_{IL}			10		uA
Input Capacitance	C_{IN}			10		pF
High Level Output Voltage (SDATA, D0~D7)	V_{OH}		V_{DD}-0.5			V
Low Level Output Voltage (SDATA, D0~D7)	V_{OL}				0.5	V
High Level Output Current	I_{OH}			1		mA
Low Level Output Current	I_{OL}			1		mA

■ TIMING SPECIFICATION

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
3-Channel Pixel Rate	t_{PRA}		100			ns
2-Channel Pixel Rate	t_{PRB}		66			ns
1-Channel Pixel Rate	t_{PRC}		40			ns
ADCCLK Pulse Width	t_{ADCLK}		16			ns
CDSCLK1 Pulse Width	t_{C1}		12			ns
CDSCLK2 Pulse Width	t_{C2}		12			ns
CDSCLK1 Falling to CDSCLK2 Rising	t_{C1C2}		0			ns
ADCCLK Rising to CDSCLK1 Falling	t_{ADC1}		0			ns
ADCCLK Rising to CDSCLK2 Falling	t_{ADC2}		0			ns
Analog Sampling Delay	t_{AD}		5			ns
3-CHANNEL Mode Only						
CDSCLK2 Falling to CDSCLK1 Rising	ta_{C2C1}		30			ns
CDSCLK2 Falling to ADCCLK Rising	ta_{C2ADR}		30			ns
2-CHANNEL Mode Only						
CDSCLK2 Falling to ADCCLK Rising	tb_{C2ADR}		30			ns
CDSCLK1 Rising to ADCCLK Rising	tb_{C1ADR}		15			ns
CDSCLK2 Falling to CDSCLK1 Rising	tb_{C2C1}		15			ns
1-CHANNEL Mode Only						
CDSCLK2 Falling to ADCCLK Rising	tc_{C2ADR}		20			ns
CDSCLK1 Rising to ADCCLK Falling	tc_{C1ADF}		0			ns
CDSCLK2 Falling to CDSCLK1 Rising	tc_{C2C1}		15			ns
SERIAL INTERFACE						
Maximum SCLK Frequency	f_{SCLK}		10			MHz
SLOAD to SCLK Setup Time	t_{LS}		10			ns
SCLK to SLOAD Hold Time	t_{LH}		10			ns
SDATA to SCLK Rising Setup Time	t_{DS}		10			ns
SCLK Rising to SDARA Hold Time	t_{DH}		10			ns
Falling to SDATA Valid	t_{RDV}		10			ns
DATA OUTPUT						
Output Delay	t_{OD}			8		ns
Latency(Pipeline Delay)				9		Cycles

■ FUNCTIONAL DESCRIPTION

Offset Error

At a level of 1/2 LSB above the nominal zero scale voltage, the first ADC code transition should come. The offset error is defined as the deviation between the actual first code transition level with the ideal level.

Gain Error

At a level of 1/2 LSB below the nominal full-scale voltage, the last code transition should come. Gain error is defined as the deviation of the actual difference between the first and the last code transitions and the ideal difference between the first and the last code transitions.

Internal Register Descriptions

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	0	1	3-CH	CDS on	Clamp Voltage	Enable Power Down	Output Delay	1 byte out
MUX	0	0	1	0	RGB/ BGR	Red	Green	Blue	Delay enable	CDSCLK1 Delay	CDSCLK 2 Delay	ADCCLK Delay
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Internal Register Map

Configuration Register

The configuration register sets the **M1008**'s operating mode and bias levels. Bits D6 should always hold high. Bit D5 configures the **M1008** for the 3-channel(high) operation mode. Bit D4 will be set high to implement the CDS mode operation, and be set low to implement the SHA mode operation.

Bit D3 controls the dc bias level of the **M1008**'s input clamp. This bit should hold high for the 4V clamp bias, unless a CCD with a reset feed through transient exceeding 2V is applied. The clamp voltage is 3V with this bit low.

Bit D2 controls the power-down mode. With bit D2 high, the **M1008** will come to a very low power "sleep" mode, in which all register contents are retained. Bit D1 is set high for the digital output (D0~D7) delay 2ns. Bit D0 configures the output mode of the **M1008**. Setting the bit high can implement a single byte output mode in which only one byte of the 16b ADC is output. Inversely, the 16b ADC output is multiplexed into two bytes.

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	3-Channels	CDS Operation	Clamp Bias	Power-Down	Output Delay	High Byte Out
			1=on (Note)	1=CDS mode (Note)	1=4V (Note)	1=on	1=on	1=on
			0=off	0=SHA mode	0=3V	0=off (Note)	0=off (Note)	0=off

Configuration Register Settings

Note: Power-on default value

MUX Register

The sampling channel order and 2-channel mode configuration in the **M1008** are both controlled by the MUX register. Bits D8 should hold low. Bit D7 goes into effect in the 3-channel mode or the 2-channel mode of operation. Setting it high will sequence the MUX to sample the red channel first, then the green channel, and the last blue channel. In the 3-channel mode, the CDSCLK2 rising edge always resets the MUX to sample the red channel first (see timing diagrams). When bit D7 is set low, the channel order is reversed to blue first, green second, and red third, the CDSCLK2 rising edge will always reset the MUX to sample the blue channel first. Bits D6, D5, and D4 go into effect when operating in 1 or 2-channel mode. Bit D6 is set high to sample the red channel. Bit D5 is set high to sample the green channel. Bit D4 is set high to sample the blue channel. The MUX remains stationary during 1-channel mode. Setting two of Bits D4~D6 high to configure the two channel mode, and the sequence of sampling is selected by bit D7. Bits D0~D3 are applied to controlling CDSCLK1, CDSCLK2 and ADCCLK internal delay.

■ FUNCTIONAL DESCRIPTION (Cont.)

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	MUX order	Channel Select			Enable Delay	CDS1 Delay	CDS2 Delay	ADCK Delay
	1=R-G-B (Note) 0=B-G-R	1=Red (Note) 0=off	1=Green 0=off (Note)	1=Blue 0=off (Note)	1=on (Note)	1=4ns	1=4ns	1=2ns
					0=off	0=2ns (Note)	0=2ns (Note)	0=0ns (Note)

MUX Register Settings

Note: Power-on default value

PGA Gain Registers

There are three PGA registers for use in respectively programming the gain of the red, green and blue channels. Bits D8, D7 and D6 in each register must hold low, and bits D5 through D0 control the gain range in 64 increments. The coding for the PGA registers is a straight binary. An all zero word corresponds to the minimum gain setting (1x) and an all one word corresponds to the maximum gain setting (5.85x).

The **M1008** distributes one Programmable Gain Amplifier (PGA) for each channel. Each PGA has a gain range from 1x (0dB) to 5.85x (15.3dB), adjustable in 64 steps. Although the gain curve is approximately linear in dB, the gain in V/V varies in nonlinear proportion with the register code, according to the following the equation:

$$\text{Gain} = \frac{5.85}{1 + 4.85 * (\frac{63 - G}{63})}$$

Where G is the decimal value of the gain register contents, and varies from 0 to 63.

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain(V/V)	Gain(dB)
0	0	0	MSB					LSB		
0	0	0	0	0	0	0	0	0 (Note)	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
0	0	0	1	1	1	1	1	0	5.43	14.7
0	0	0	1	1	1	1	1	1	5.85	15.3

Note: Power-on default value

Offset Registers

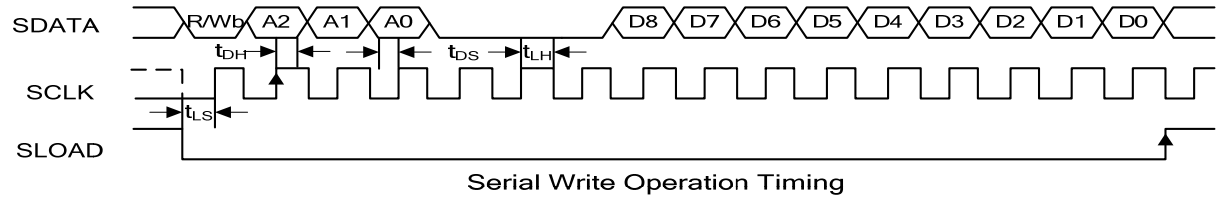
There are three PGA registers for use in respectively programming the offset of the red, green, and blue channels. Bits D8 through D0 control the offset range from -250mV to 250mV in 512 increments.

The coding for the offset registers is sign magnitude, with D8 as the sign bit. The following table shows the offset range as a function of the bits D8 through D0.

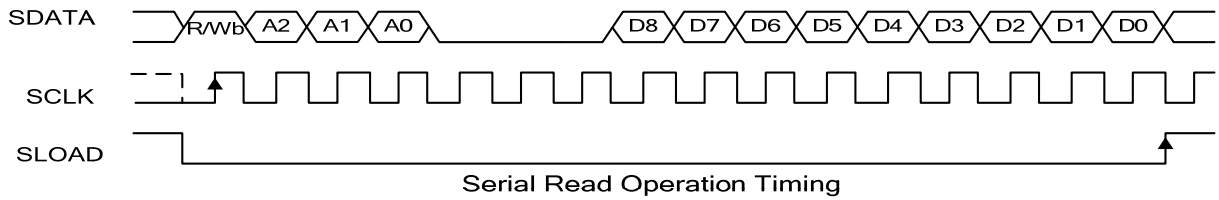
D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset(mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0 (Note)	0
0	0	0	0	0	0	0	0	1	0.98
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	1	250
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	-0.98
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	-250

Note: Power-on default value

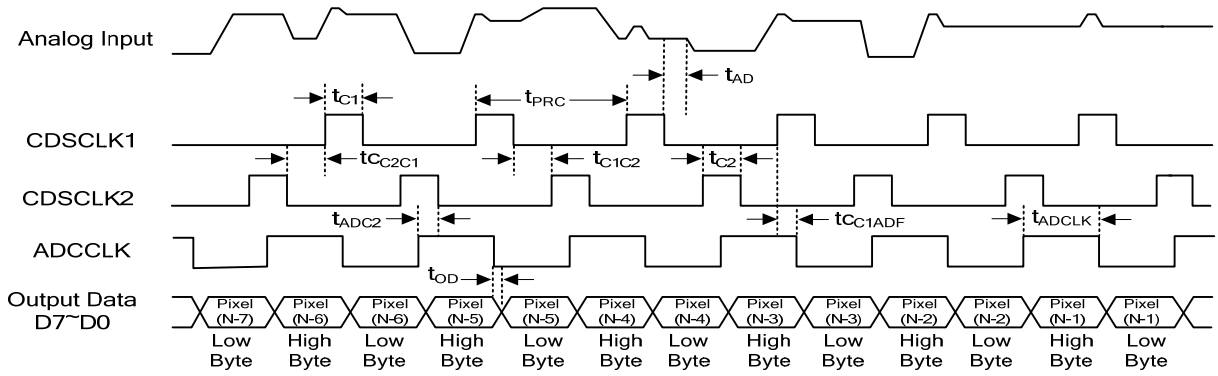
■ TIMING DIAGRAMS



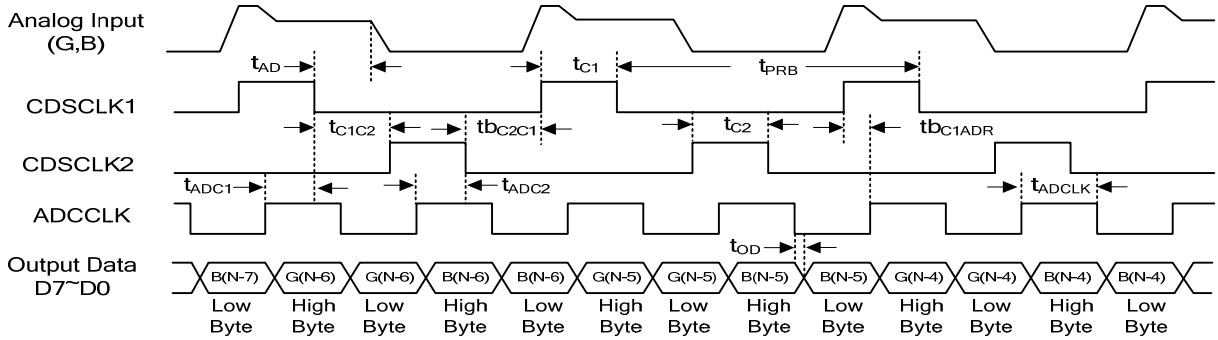
Serial Write Operation Timing



Serial Read Operation Timing

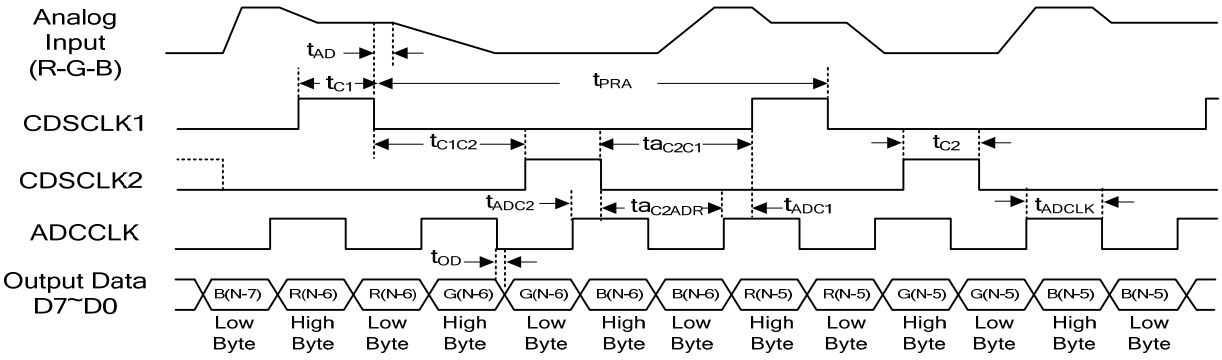


1-Channel CCD Mode Timing

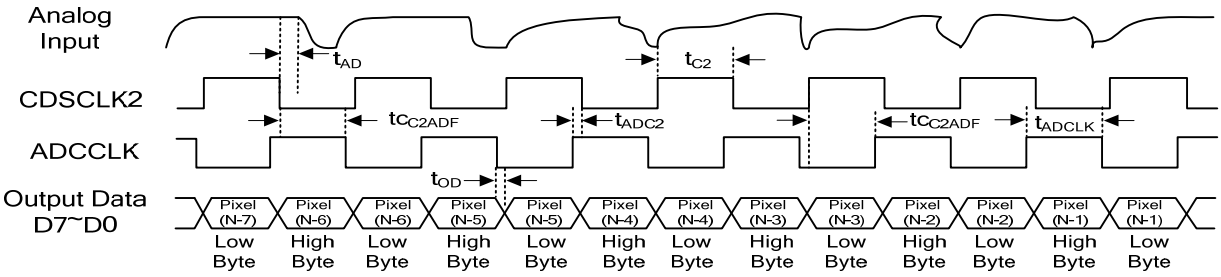


2-Channel CCD Mode Timing (Select G-B Mode)

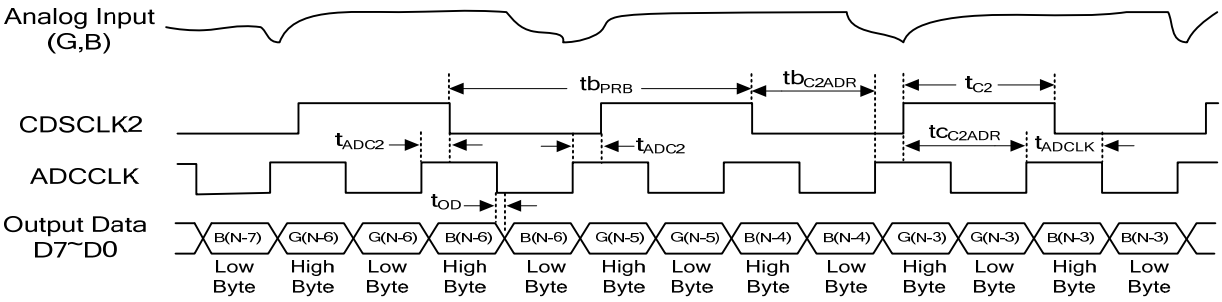
■ TIMING DIAGRAMS (Cont.)



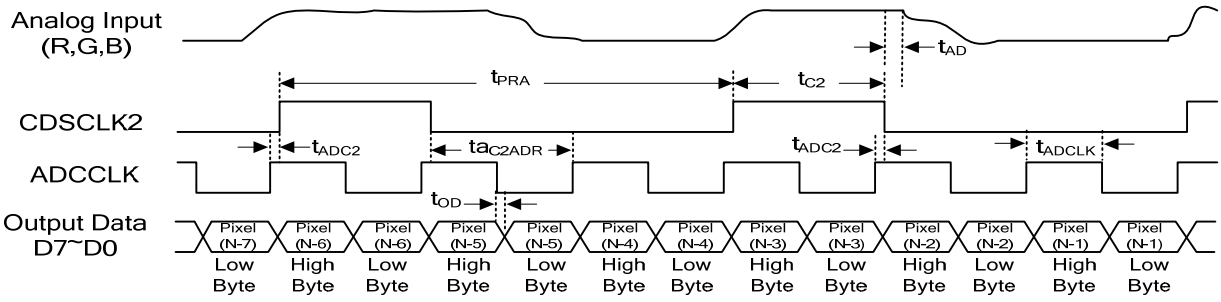
3-Channel CCD Mode Timing (Select R-G-B Mode)



1-Channel SHA Mode Timing



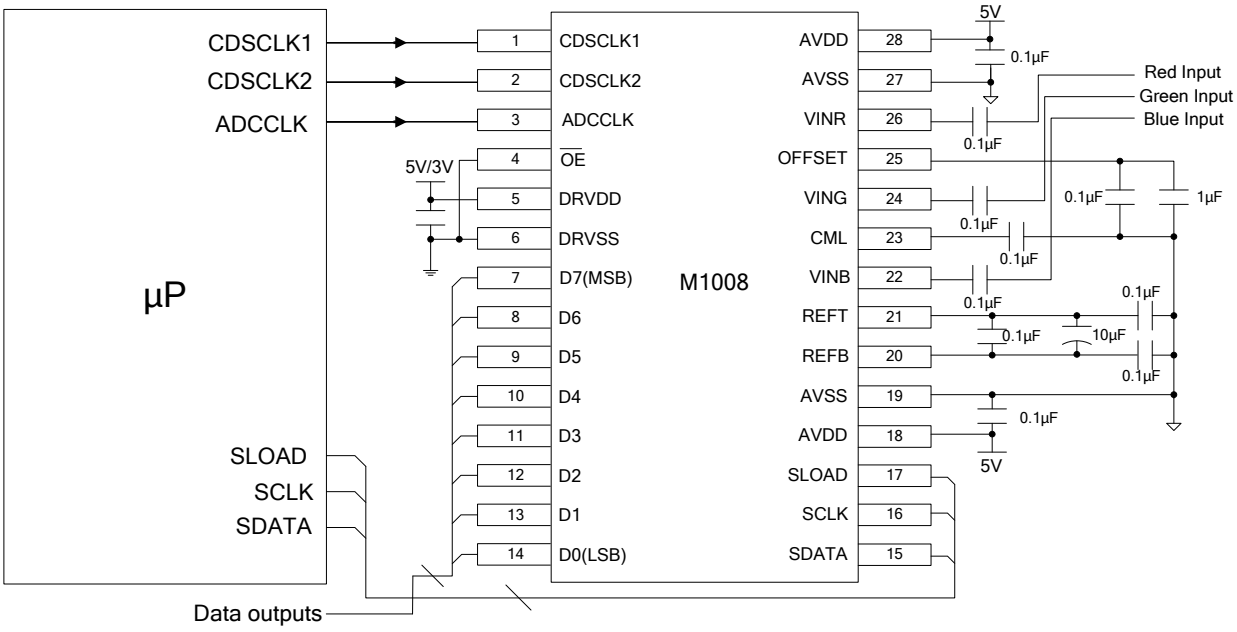
2-Channel SHA Mode Timing (Select G-B Mode)



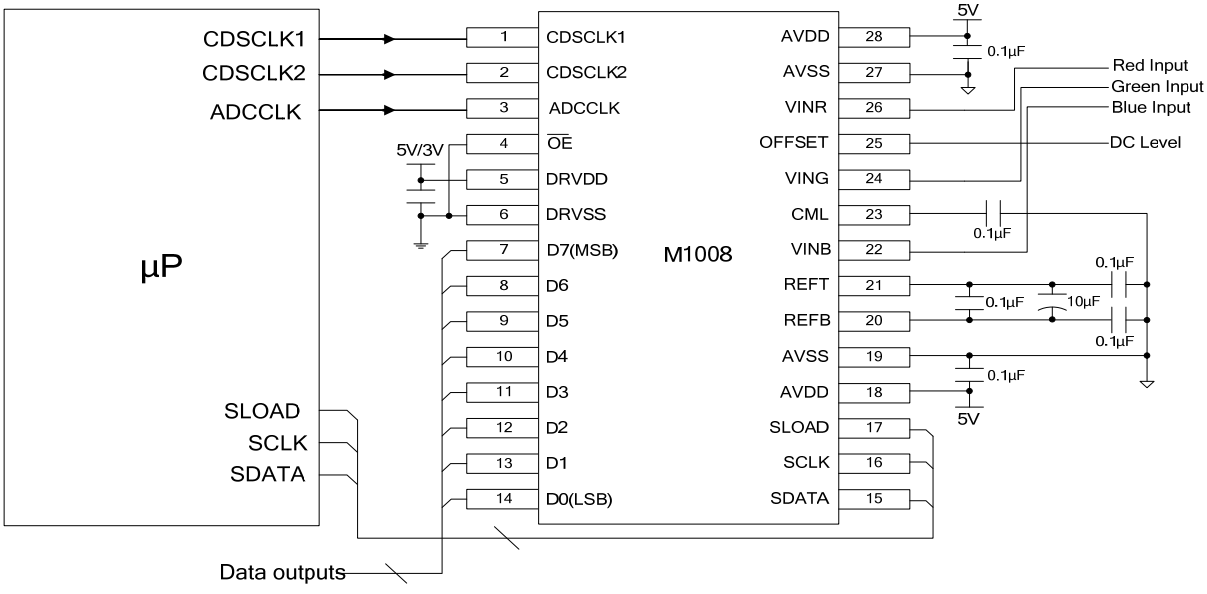
3-Channel SHA Mode Timing (Select R-G-B Mode)

■ TYPICAL APPLICATIONS CIRCUIT

CDS Mode



SHA Mode



■ APPLICATION CONSIDERATIONS

The digital outputs load should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. In order to minimize the number of code conversion in the main output of the impact of transients, which should happen in the coincidences CDSCLK2 falling on or before ADCCLK rising edge. All 0.1μF decoupling capacitor should be located as close as possible to the M1008 pins. When operating in a single channel mode, the unused analog inputs should be grounded.

For the 3-channel SHA mode, all of the above considerations also apply for this configuration, except that the analog input signals are directly connected to the M1008 without the use of coupling capacitors. The OFFSET pin should be grounded if the inputs to the M1008 are to be referenced to ground, or a DC offset voltage should be applied to the OFFSET pin in the case where a coarse offset needs to be removed from the inputs. The analog input signals must already be dc-biased between 0V and 2V, if OFFSET is connected to ground.