ML2724

2.4GHz Low-IF 1.5Mbps FSK Transceiver

Final Datasheet

GENERAL DESCRIPTION

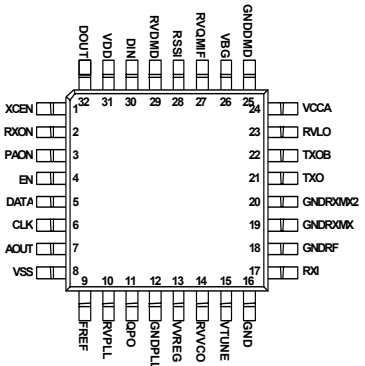
The ML2724 is a fully integrated 1.5Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 2.4GHz ISM frequency band. The device has been optimized for digital cordless telephone applications and includes all the frequency generation, receive and transmit functions. Automatically adjusted filters eliminate mechanical tuning. Closed loop modulation eliminates frequency drift and permits practically unlimited TX duration. The transmitter generates a 3dBm FSK output signal.

The 1.5Mbps data rate permits data spreading, such as Direct Sequence Spread Spectrum (DSSS) modulation, which improves range. The dual conversion Low-IF receiver has all of the sensitivity and selectivity advantages of a traditional super-heterodyne without requiring costly, bulky external filters, while providing the integration advantages of direct conversion.

The phase locked loop (PLL) synthesizer is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator. This allows the ML2724 to be used in frequency hopped spread spectrum (FHSS) applications.

The ML2724 contains internal voltage regulation. It also contains PLL and transmitter configuration registers. The device can be placed in a low power standby mode for current sensitive applications. It is packaged in a 32TQFP.

PIN CONFIGURATION



ORDERING INFORMATION

PART #	TEMP RANGE	PACKAGE	SPEC
ML2724DH	-10°C to +60°C	32 Pin TQFP 7mmx7mm	DS2724-F-01

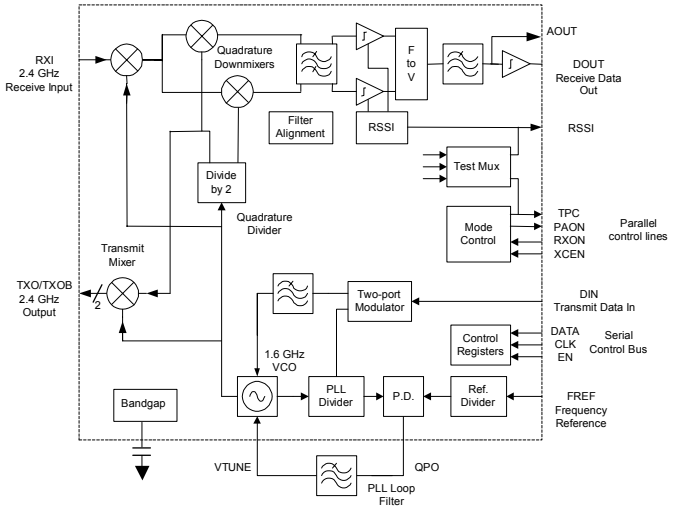
FEATURES

- Complete 2.4GHz FSK Transceiver
  - High data rate (1.5Mbps)
  - -90dBm sensitivity (DSSS modulation)
  - 3dBm Output Power (differential, typical)
- Closed Loop TX Modulation
- Low IF Receiver: No external IF filters required.
- Fully Integrated frequency synthesizer:
  - No external resonator required.
- Sigma-Delta Fractional-N two-port modulator
- Automatic Filter Alignment
  - No manufacturing adjustments required.
- No external data slicer components required
- Control outputs correctly sequence and control PA
- 3-wire control interface
- Analog RSSI output

APPLICATIONS

- 2.4GHz FSK Data Transceivers
  - Digital Cordless Telephones
  - Wireless PC Peripherals
  - Wireless Game Controllers
  - Wireless Streaming Media

BLOCK DIAGRAM



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CHANGE LOG

VERSION	DATE	AUTHOR	CHANGES/COMMENTS
DS2724-F-01	4/23/03	mlj	Originate Final Datasheet

SIMPLIFIED APPLICATIONS DIAGRAM

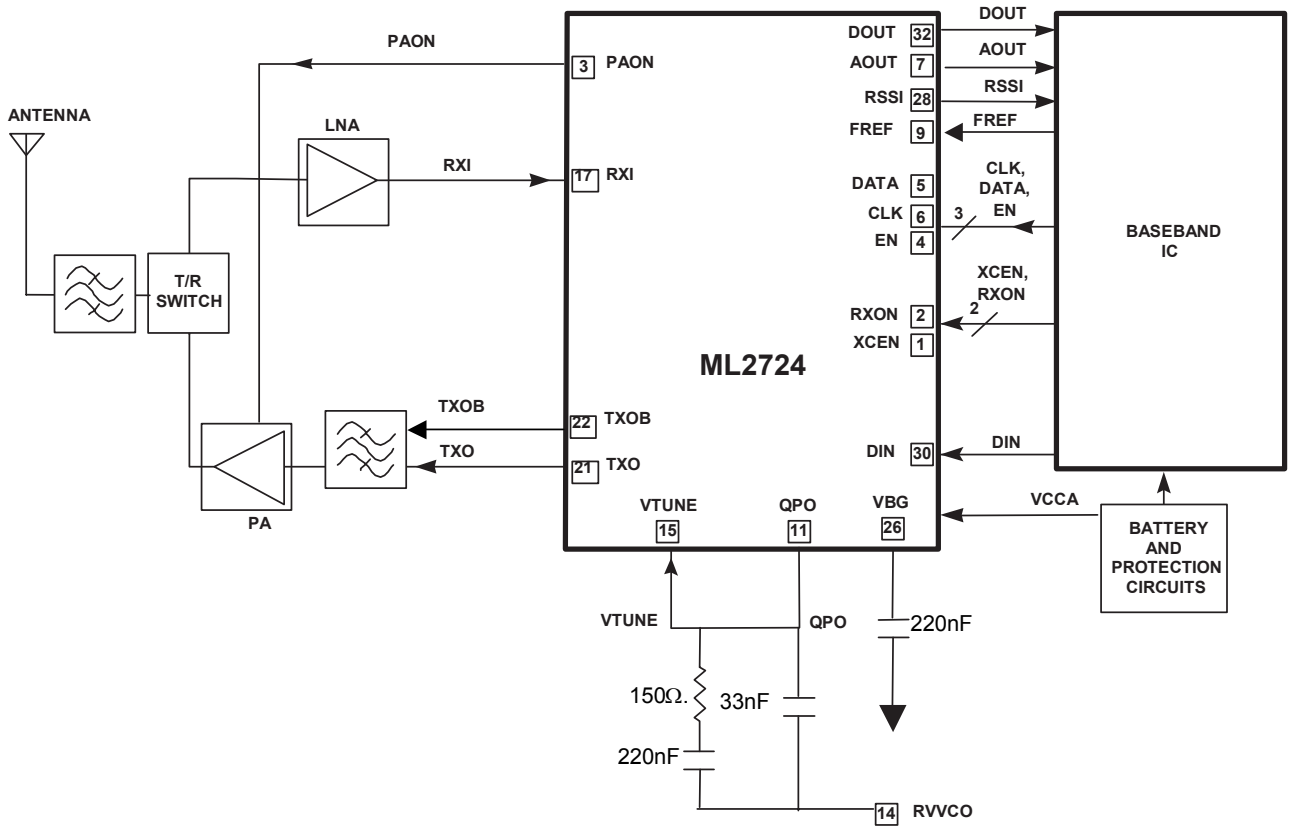


Figure 1: Typical ML2724 Application Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VCCA, VDD ..... 5.5 V
Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10s) ..... 260°C

OPERATING CONDITIONS

Normal Temperature Range ..... -10°C to 60°C
VCCA Range ..... 2.7V to 4.5V
VDD Range ..... 2.7V to 3.3V
Thermal Resistance (θ_{JA}) ..... 70°C/W

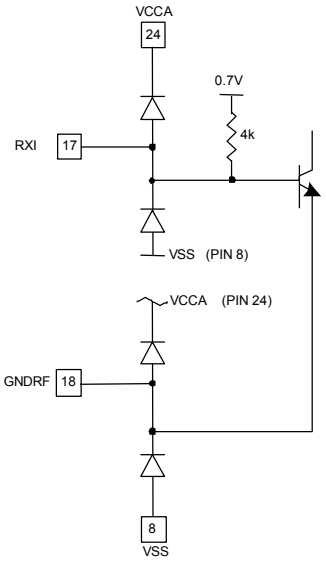
Unless otherwise specified, VCCA=VDD=3.3V, T_A=25°C, f_{REF}=6.144MHz, Data Rate=1.536Mbps, 13KHz Loop Filter as shown in **Figure 1.**

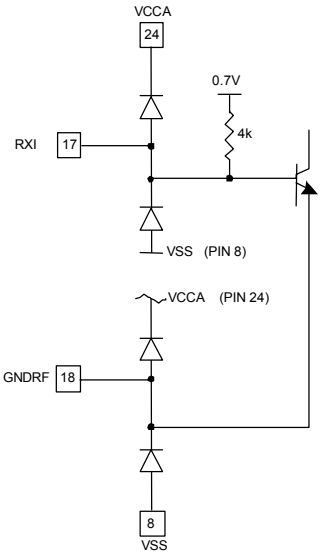
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER CONSUMPTION						
VCCA	Analog supply (VCCA)		2.7	3.3	3.8	V
VDD	Digital Supply voltage	VDD pin (VCCA ≥ VDD always)	2.7		VCCA	V
V_{BG}	Bandgap Voltage	VBG pin 26, I_O=0µA		1.23		V
I_{STBY}	Supply current, STANDBY mode	DC supply connected, XCEN low		10	120	µA
I_{RX}	Supply current, RECEIVE mode	RX chain active, data being received		55	76	mA
I_{TX}	Supply current, TRANSMIT mode	P_{OUT}=3dBm		50	76	mA
SYNTHESIZER						
f_C	Carrier frequency range		2.4		2.485	GHz
δf	Channel Spacing			2048		kHz
I_P	Charge Pump sink/source current			+/-5.5		mA
Φ_N	Phase noise at TXO 1.2MHz 3MHz >7MHz	Closed loop, loop filter bandwidth 13KHz (See **Figure 1**)		 -95 -115 -125		dBc/Hz
t_{FH}	Lock time for channel switch	From EN asserted to RX valid data(RX), or PAON high (TX) 1 Channel 5 Channels Full Range		 110 185 250	 125 220 300	 µs µs µs
t_{TX2RX}	Lock time for TX/RX	RXON High to Valid RX data		70	120	µs
t_{RX2TX}	Lock time for RX/TX	RXON Low to PAON high		63	75	µs
t_{WAKE}	Lock up time from standby	XCEN high to Valid RX data, XCEN low period >120 seconds		240	325	µs

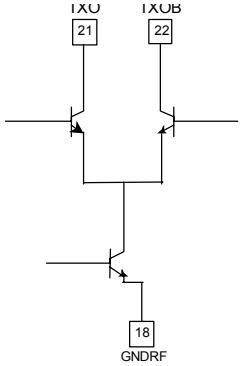
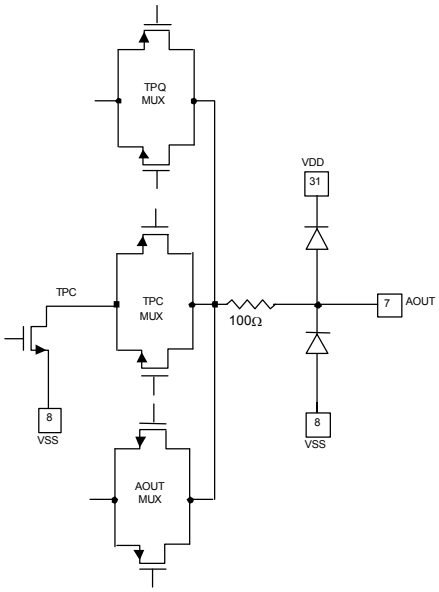
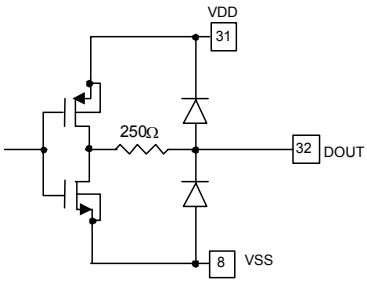
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{FREF}	Reference signal frequency			6.144 12.288		MHz MHz
V_{FREF}	Reference signal input level	6.144MHz or 12.288MHz sine wave, capacitively coupled	2.0		VCCA	V_{PP}
RECEIVER						
Z_{IN}	Receiver input impedance	f_c=2445MHz		2.2+j0		Ω
NF	Receiver noise figure	f_c=2445MHz		16.5		dB
DR_{RX}	Data Rate	FSK modulation, f_{dev}=+/-512KHz		1.536		Mbps
S	Input Sensitivity	<12.5% CER at 1.536Mchip/s <10e-3 BER at 1.536Mbps	-82	-90 -81		dBm dBm
BW_{RX}	Bandwidth	3dB Bandwidth		770		kHz
P_{IMAX}	Maximum RX RF input	<12.5% CER at 1.536Mchip/s <10e-3 BER at 1.536Mb/s	+5 -4			dBm dBm
I_{IP3}	Receiver Input IP3	Test tones 2 and 4 channels away		-15		dBm
	LO leakage at RXI			-60		dBm
IRR	Mixer Image Rejection Ratio	Measured at 3.5MHz offset		35		dB
	Adjacent channel rejection	-80dBm wanted signal <10^{-3} BER Single 2GFSK modulated interferer with a 1.5MHz –20dBc bandwidth 1 channel away 2 channels away 3 or more channels away		 6 31 36		 dB dB dB
IF FILTERS						
f_{IFC}	IF filter center frequency	After Automatic Filter Alignment		1.024		MHz
BW_{IF}	IF filter 3dB bandwidth	After Automatic Filter Alignment		1405		kHz
LIMITER, AGC, AND FM DEMODULATOR						
t_{OVLD}	Recovery from overload	From +15dBm at input		5	12	µs
	Eb/No	For 10^{-3} BER		10.5		dB
	Co-Channel rejection, 10^{-3} BER	-80 dBm, modulated with 1.536Mbps GFSK, BT=0.5, PRBS data		10.5		dB
V_{ODC}	Quiescent voltage @ AOUT			1.1		V
V_{OPK}	Output voltage swing AOUT		0.55		1.1	V_{PP}
V_{OL}	AOUT open-drain voltage	I_O=100µA, TPC Mode			0.4	V
RSSI PERFORMANCE						
t_{RRSSI}	RSSI rise time No Signal to -15dBm into the IF mixer	20 pF load, 20% to 80%		4.5		µs
t_{FRSSI}	RSSI fall time, < -15dBm to No Signal into the IF mixer	20 pF load, 20% to 80%		3.0		µs
G_{RSMID}	RSSI sensitivity	$(V_{-40dBm} – V_{-60dBm})/20dB$	28	36	42	mV/dB
V_{RSMX}	RSSI maximum voltage	See Figure 3	1.8	2.3		V
V_{RSMD}	RSSI midrange voltage	-40 dBm into RXI	1.4	1.7	2.0	V

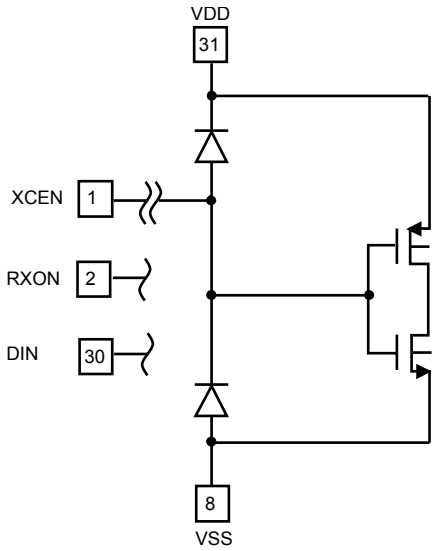
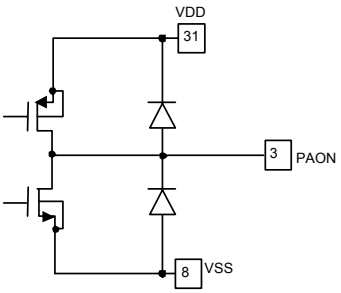
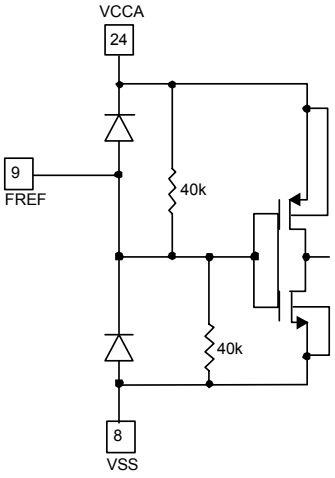
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{RSMN}	RSSI minimum voltage	No signal into RXI		75		mV
V_{RSMXC}	RSSI maximum voltage (clipped)	-10 dBm into RXI	1.6	1.95		V
TRANSMIT RF MIXER						
P_{OSE}	Output power, single ended	TRXO or TRXOB, f_C=2.445 GHz	-3	1	5	dBm
P_{ODIF}	Output power, differential	$P_{(TRXO,TRXOB)}$, f_C=2.445 GHz	-1	3	6	dBm
Z_{OUT}	Output impedance	TRXO or TRXOB, f_C=2.445 GHz		12+j0		Ω
TRANSMIT MODULATION						
f_{DEV}	Modulation Deviation, @2.4GHz	200us of consecutive '1's or '0's	500	512	524	kHz
f_{OS}	Modulation center frequency offset	50us after RXON low	-50		+50	kHz
TRANSMIT DATA FILTER						
BW_{TX}	Transmit Data Filter Bandwidth	3dB Bandwidth		1.4		MHz
	TX spurious Image			-25 -20		dBc dBc
INTERFACE LOGIC LEVELS						
INPUTS (DIN, XCEN, RXON, DATA, CLK, EN)						
V_{IH}	Input high voltage	(never exceed VDD)	0.75*VDD		VDD	V
V_{IL}	Input low voltage		0		0.25*VDD	V
I_B	Input bias current		-5	0	5	µA
C_{IN}	Input capacitance	(measured at 1MHz)		4		pF
OUTPUTS (DOUT, PAON)						
V_{OH}	DOUT high voltage	I_o=0.1mA	VDD-0.4			V
V_{OL}	DOUT low voltage	I_o=-0.1mA			0.4	V
I_o	DOUT sink/source current		0.1			mA
V_{OH}	PAON output high voltage	Sourcing 0.5 mA	VDD-0.4			V
V_{OL}	PAON output low voltage	Sinking 0.5 mA			0.4	V
I_o	PAON source/sink current		0.5			mA
3 WIRE SERIAL BUS TIMING						
t_r	CLK input rise time	**See Figure 4**			15	ns
t_f	CLK input fall time				15	ns
t_{ck}	CLK period		50			ns
t_{ew}	CLK pulse width		100			ns
t_l	Delay from last CLK falling edge		15			ns
t_{se}	EN setup time to ignore next rising CLK		15			ns
t_s	DATA-to-CLK setup time		15			ns
t_h	DATA-to-CLK hold time		15			ns

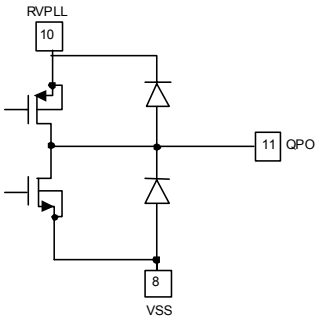
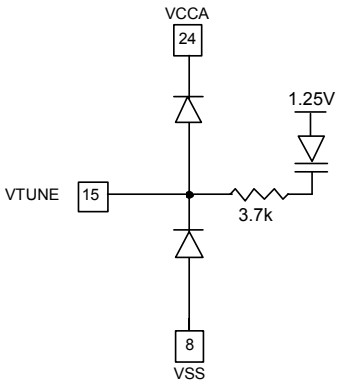
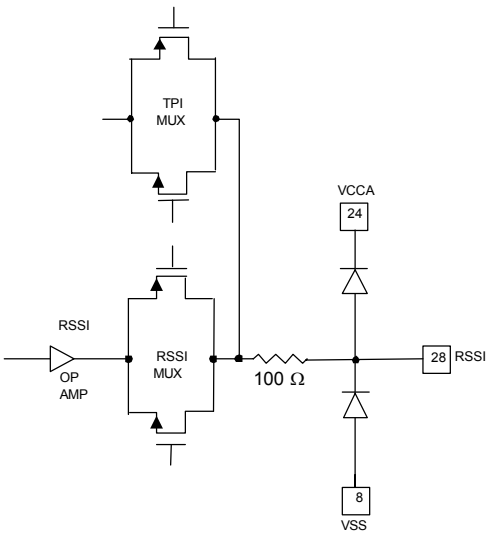
PIN DESCRIPTIONS

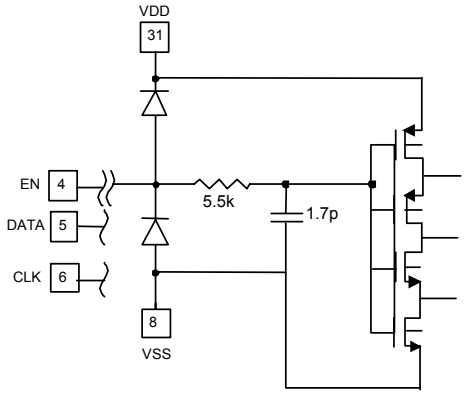
PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
POWER & GROUND				
8	VSS	GND	Digital Ground. Ground for digital I/O circuits and control logic.	**N/A**
10	RVPLL	PWR	PLL Supply. DC power supply decoupling point for the PLL dividers, phase detector, and charge pump. This pin is connected to the output of the regulator and to the PLL supplies. There must be a 220nF capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator.	See Pin 11 below.
12	GNDPLL	GND	Ground for the PLL dividers, phase detector, and charge pump.	**N/A**
13	VVREG	PWR	DC Power Supply Input to the VCO voltage regulator. Must be connected to RVQMIF (pin 27) or RVDMD (pin 29) via decoupling network.	**N/A**
14	RVVCO	PWR	DC power supply decoupling point for the VCO. Connected to the output of the VCO regulator. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
16	GND	GND	DC ground for VCO and LO circuits.	**N/A**
18	GNDRF	GND	Ground return for the Receive RF input and Transmit RF output.	
19	GNDRXMX	GND	Signal ground for the Receive mixers.	**N/A**
20	GNDRXMX2	GND	Signal ground for the Receive mixers.	**N/A**
23	RVLO	PWR	DC power supply decoupling point for the LO Chain. Connected to the output of a regulator. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
24	VCCA	PWR	DC power supply Input to Voltage Regulators and unregulated loads: 2.7 to 3.8V. VCCA is the main (or master) analog VCC pin. There must be capacitors to ground from this pin to decouple (bypass) supply noise.	**N/A**
25	GNDDMD	GND	DC ground to IF, Demodulator, and Data Slicer circuits.	**N/A**
27	RVQMIF	PWR	DC power supply decoupling point for Quadrature Mixer and IF filter circuits. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
29	RVDMD	PWR	DC power supply decoupling point for IF, Demodulator, and Data Slicer circuits. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
31	VDD	PWR	DC power supply input to the interface logic and control registers. This supply is not connected internally to any other supply pin, but its voltage must be less than or equal to the VCCA supply and greater than 2.7V. A capacitor must be tied between this pin and ground to decouple (bypass) noise.	**N/A**
TRANSMIT/RECEIVE				
17	RXI	I (analog)	Receive RF Input. Nominal impedance at 2445 MHz is 2.6-j2.6 with a simple matching network required for optimum noise figure. This input connects to the base of an NPN transistor and should be AC coupled.	
21	TXO	O (analog)	TX RF open-collector output. This output requires a DC path to VCCA.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
22	TXOB	O (analog)	Complementary TX RF open-collector output. This output requires a DC path to VCCA. For single-ended output applications, this pin should be connected to a dummy load that includes a DC path to VCCA.	
DATA				
7	AOUT	A (analog)	Multi-function Output. In Analog output mode this is output drives an off chip data slicer. In Transmit power control mode this is an open drain output, which is pulled low when the TPC bit is serial register #1, is clear. Transitions on TPC are synchronized to the falling edge of RXON. In analog test modes this pin and the RSSI output become test access points controlled by the serial control bus.	
30	DIN	I (CMOS)	Transmit Data Input. Drives the transmit pulse shaping circuits. Serial digital data on this pin becomes FSK modulation on the Transmit RF output. The logic timing on this pin controls data timing. Internal circuits determine the modulation deviation. This is a standard CMOS input referenced to VDD and VSS.	See Pin 1 below.
32	DOUT	O (CMOS)	Serial digital output after demodulation, chip rate filtering and center data slicing. A CMOS level output (VSS to VDD) with controlled slew rates. A low drive output designed to drive a PCB trace and a CMOS logic input while generating minimal RFI. In digital test modes this pin becomes a test access port controlled by the serial control bus.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
MODE CONTROL AND INTERFACE LINES				
1	XCEN	I (CMOS)	Enables the bandgap reference and voltage regulators when high. Consumes only leakage current in STANDBY mode when low. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
2	RXON	I (CMOS)	TX/RX Control Input. Switches the transceiver between TRANSMIT and RECEIVE modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
3	PAON	O (CMOS)	PA Control Output. Enables the off-chip PA at the correct times in a Transmit slot. Goes high when transmit RF is present at TXO; goes low 5µs before transmit RF is removed from TXO. Has interlock logic to shut down the PA if the PLL does not lock.	
9	FREF	I	Input for the 12.288 MHz or 6.144 MHz reference frequency. This input is used as the reference frequency for the PLL and as a calibration frequency for the on-chip filters. An AC-coupled sine or square wave source drives this self-biased input.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
11	QPO	O	Charge Pump Output of the phase detector. This is connected to the external PLL loop filter.	
15	VTUNE	I	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
26	VBG	O	Bandgap Decouple Voltage. Decoupled to ground with a 220nF capacitor.	**N/A**
28	RSSI	O	Buffered Analog RSSI output with a nominal sensitivity of 35mV/dB. In analog test modes, this pin and the AOUT output become test access points controlled by the serial control bus.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
SERIAL BUS SIGNALS				
4	EN	I (CMOS)	Control Bus Enable. Enable pin for the three-wire serial control bus that sets the operating frequency and programmable options. The control registers are loaded on a low-to-high transition of the signal. Serial control bus data is ignored when this signal is high. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
5	DATA	I (CMOS)	Serial Control Bus Data. 16-bit words, which include programming data and the two-bit address of a control, register. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
6	CLK	I (CMOS)	Serial control bus data is clocked in on the rising edge when EN is low. This is a CMOS input; the thresholds are referenced to VDD and VSS.	

FUNCTIONAL DESCRIPTION

The ML2724 is a fully integrated 1.5Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 2.4GHz ISM frequency band. The device has been optimized for digital cordless telephone applications and includes all the frequency generation, receive and transmit functions for a raw data rate of 1.5Mbps. This high data rate allows for data spreading, such as Direct Sequence Spread Spectrum (DSSS) modulation, which improves range. The ML2724 receiver architecture is a dual conversion Low IF, which has all of the sensitivity and selectivity advantages of a traditional super-heterodyne receiver without requiring costly, bulky external filters.

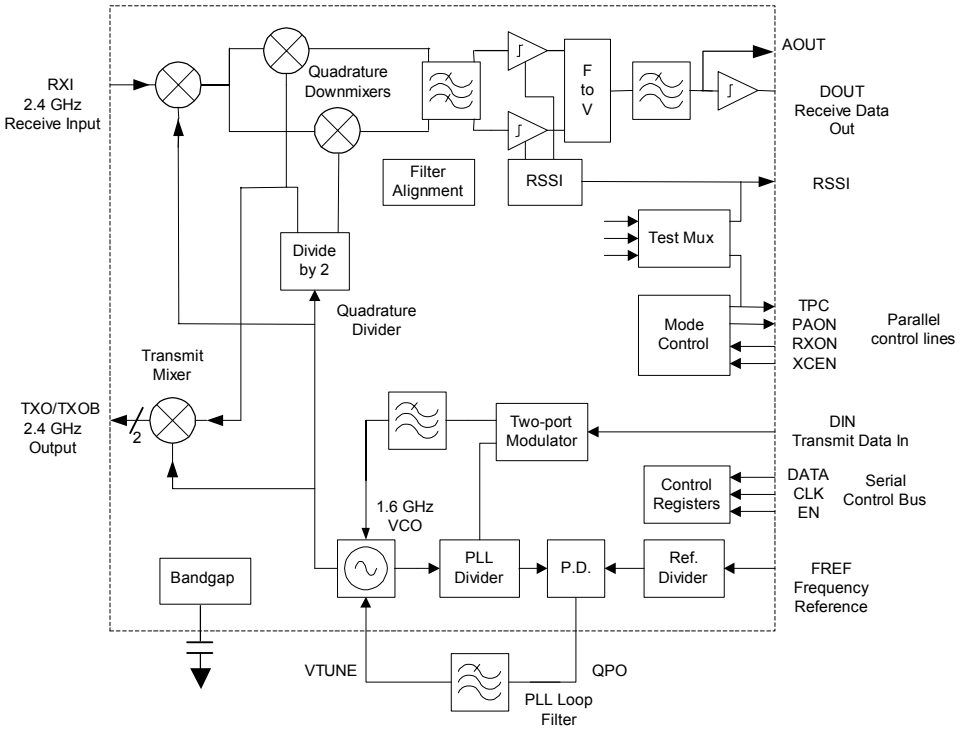


Figure 2: ML2724 Internal Block Diagram

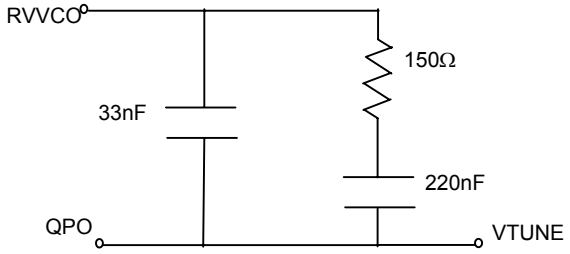
The RF mixer down-converts the 2.4GHz RF input signal to the first intermediate frequency (IF), where it is filtered to remove adjacent channel signals. An active image reject mixer converts this signal down to a Low IF frequency, where the data is limited, filtered, and demodulated. This architecture provides all the benefits of direct conversion to baseband while maintaining the stability and robustness of a traditional super-heterodyne.

A single synthesizer is used for both the receiver and the FSK transmitter. The phase locked loop (PLL) is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator.

In **RECEIVE MODE**, the ML2724 is a dual conversion Low IF receiver. **No external SAW filters are required.** The integrated image reject mixer gives sufficient rejection in this channel. All channel filtering and demodulation is performed using active filters, which are automatically aligned. A matched bit rate filter and a data slicer follow the demodulator. The sliced data is provided at the DOUT pin, and the analog data is available at AOUT.

In **TRANSMIT MODE**, the ML2724 generates a 2.4GHz output using the transmit mixer. An auto-aligned transmit data filter and modulation compensation circuit results in an adjustment-free transmitter. The VCO is modulated by the transmit data, which is put through a sigma-delta fractional-N PLL ensuring modulation accuracy. This modulation occurs while the phase locked loop is closed, thus allowing practically infinite transmit or receive times with excellent frequency accuracy and stability. A 3dBm FSK-modulated differential signal is output at the TXO/TXOB pins at the 2.4GHz carrier frequency.

The integrated PLL frequency synthesizer includes a fully integrated VCO, prescaler, phase detector and charge pump. The reference frequency is generated from the incoming signal at the FREF pin, which can be either 6.144MHz or 12.288MHz. The loop filter is external to allow customers to optimize their loop bandwidth to their system's lock time and in-band phase noise requirements. This frequency-agile synthesizer allows the ML2724 to be used in frequency hopped spread spectrum (FHSS) applications with nominal channel spacing of 2.048MHz. Carrier frequency is programmed via the configuration registers and 3-wire serial interface. The VCO tank circuit (inductor and varactor) is fully integrated.



Example 13KHz Loop Filter

MODES OF OPERATION

There are three key modes of operation:

- **STANDBY:** All circuits powered down, except the control interface (Static CMOS)
- **RECEIVE:** Receiver circuits active
- **TRANSMIT:** Modulated RF output from IC

The two operational modes are RECEIVE and TRANSMIT, controlled by RXON. XCEN is the chip enable/disable control pin, which sets the part in operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is given in **Table 1**.

XCEN	RXON	MODE	FUNCTION
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

Table 1: Modes of Operation

MODE CONTROL

The ML2724 is intended for use in TDD and TDMA radios in battery-powered equipment. To minimize power consumption it is designed to switch rapidly from a low power mode (STANDBY) to an active mode. The ML2724 can also make a quick transition from receive to transmit for TDD operation. Prior to transmitting or receiving, time should be allowed for the PLL to lock and for the filters to align. When the ML2724 is operated in single-carrier TDD mode, the LO is automatically shifted by the second (low) IF frequency when the device is switched between RECEIVE and TRANSMIT modes.

ML2724 carrier frequency can be changed (hopped) at any time, but is usually changed between transmissions. Carrier frequency (channel) is modified in the ML2724 by writing a corresponding new value to the PLL frequency register (Register 1)

RECEIVE

The ML2724 uses a double-conversion super-heterodyne receiver with a nominal second IF of 1.024 MHz. The signal flow in RECEIVE mode is from the RF input, through an RF down-conversion mixer and integrated IF filter, image reject quadrature mixer, integrated Low IF filter, hard limiter, frequency to voltage converter, and data filter to the AOUT pin and data slicer where the digital NRZ data is available at the DOUT pin. A 20dB step AGC extends the dynamic range of the receiver.

The ML2724 receive chain is a Low IF receiver using advanced integrated radio techniques to eliminate external IF filters and minimize external RF filter requirements. The precision filtering and demodulation circuits give improved performance over conventional radio designs using external filters while providing integration comparable to advanced direct conversion radio designs.

Receive Signal Strength Indication (RSSI)

RSSI is an indication of field strength. It can be used to control transmit power to conserve battery life or it may be used to determine if a given channel is occupied. See Figure 3.

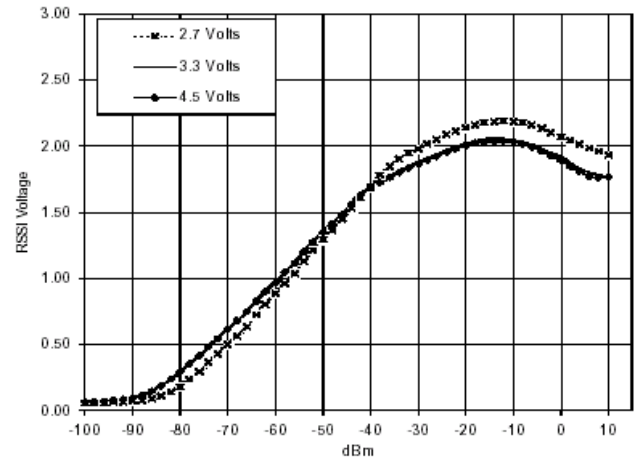


Figure 2. RSSI Output Voltage vs Input Signal Level (Clipped, 25°C, Various Input Voltage Levels)

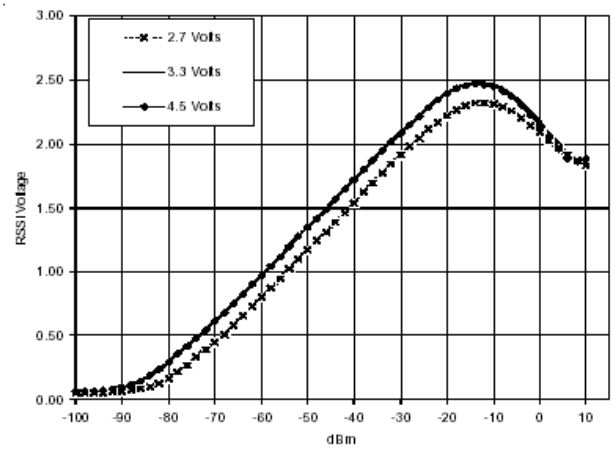


Figure 2a. RSSI Output Voltage vs Input Signal Level (Unclipped, 25°C, Various Input Voltage Levels)

Figure 3: RSSI Voltage vs. Input Signal Level

Automatic Filter Alignment

When the ML2724 is placed in RECEIVE mode, it automatically tunes all the internal filters using the reference frequency from the FREF pin. When the chip is powered up (VDD first applied), the tuning information is reset to mid-range. This self-calibration sets:

- Discriminator center frequency
- IF filter center frequency and bandwidth

- Receiver data low-pass filter bandwidth
- Transmit data low-pass filter bandwidth

TRANSMIT MODE

In TRANSMIT mode, the PLL is closed to eliminate frequency drift. A two-port modulator modulates both the VCO and the fractional-N PLL. The VCO is directly modulated with filtered FSK transmit data. The PLL is driven by a sigma-delta modulator, which ensures that the PLL follows the mean frequency of the modulated VCO.

The transmit modulation filter is automatically tuned during every RECEIVE time, alleviating the need for production alignment. Asserting RXON enables the ML2724. The rising edge of XCEN triggers a complete calibration of all the on-chip filters, which takes up to 256μs, which ensures the modulation filters are aligned to prevent unwanted spurious emissions.

PLL PROGRAMMING & CHANNEL SELECTION

The ML2724 PLL is programmed via control register 2 to the set RF center frequency of operation of the radio. The PLL does not need to be (though it can be) reprogrammed between RECEIVE and TRANSMIT modes. Nominal channel separation is 2.048MHz, allowing for over 40 non-overlapping channels in any given location. With careful planning, channels can be programmed in 1024kHz steps as long as care is exercised to insure that two radio links will not share spectrum at any one time. The equation to determine channel center frequency from the ML2724 control register word is:

$$f_C = CHQ<0:11>*1.024\ MHz$$

STANDBY MODE

In STANDBY mode, the ML2724 transceiver is powered down. The only circuits active are the control interfaces, which are digital CMOS to minimize power consumption. The serial control interface and control registers remain powered up and will accept and retain programming data as long as the digital supply is present. When exiting STANDBY mode, the device may need to be kept in RECEIVE mode for up to 256μs to allow for filter self-calibration.

TEST MODE

The RF to digital functionality of the ML2724 requires special test mode circuitry for IC production test and radio debugging. A test register, accessible via the 3-wire serial interface, controls the test multiplexers. (See **Table 15**).

DATA INTERFACE

There are two control interfaces: CONTROL and SERIAL.

CONTROL INTERFACE

The control interface provides immediate control and monitoring of the ML2724. Input signals include:

- **XCEN:** Transceiver enable. Places the ML2724 in Standby or Active (when asserted) modes.
- **RXON:** Receive On. Places an Active ML2724 in Receive mode when asserted.
- **FREF:** Reference frequency input

Output signals include:

- **RSSI:** Received Signal Strength Indicator: indicates the power of the received signal
- **PAON:** External Power Amplifier Control Pin

SERIAL INTERFACE

A 3-wire serial interface (EN, DATA, CLK) is used for programming the ML2724 configuration registers, which control device mode, pin functions, PLL and reference dividers, internal test modes, and filter alignment. Data words are

entered beginning with the MSB (“big-endian”). The word is divided into a leading 14-bit data field followed by a 2-bit address field. When the address field has been decoded the destination register is loaded on the rising edge of EN. **Providing less than 16 bits of data will result in unpredictable behavior when EN goes high.**

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift register on the rising edge of the CLK pin. This information is loaded into the target control register when EN goes high. This serial interface bus is similar to that commonly found on PLL devices. It can be efficiently programmed by either byte or 16-bit word oriented serial bus hardware. The data latches are implemented in CMOS and use minimal power when the bus is inactive. Refer to Figure 4 and Table 2: 3-Wire Bus Timing Characteristics for timing and register programming illustrations.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
BUS CLOCK (CLK)					
t_r	CLK input rise time			15	Ns
t_f	CLK input fall time			15	Ns
t_{ck}	CLK period	50			Ns
ENABLE (EN)					
t_{ew}	Minimum pulse width	100			Ns
t_l	Delay from last CLK rising edge	15			Ns
t_{se}	Set up time to ignore next rising CLK	15			Ns
BUS DATA (DATA)					
t_s	data to clock set up time	15			Ns
t_h	data to clock hold time	15			Ns

Table 2: 3-Wire Bus Timing Characteristics

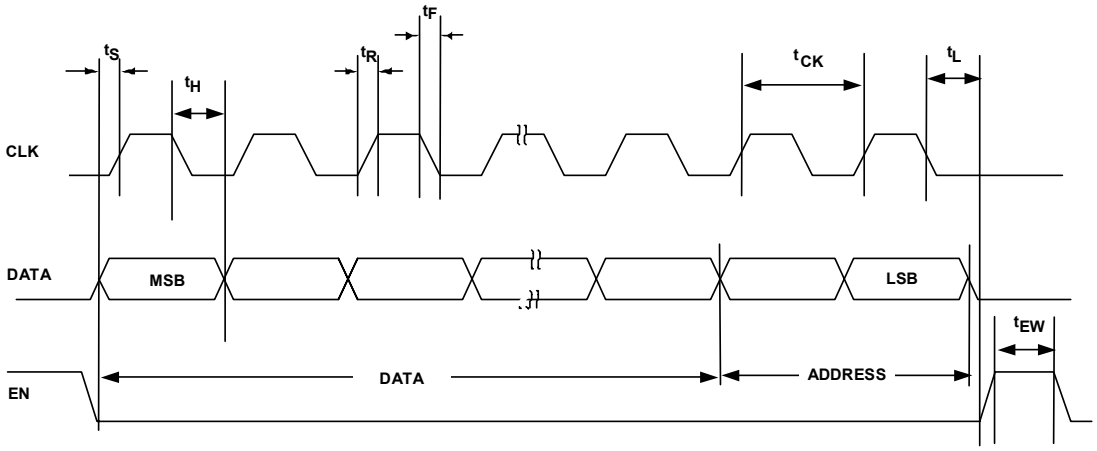


Figure 4: Serial Bus Timing for Address and Data Programming

CONTROL INTERFACES AND REGISTER DESCRIPTIONS

REGISTER INFORMATION

A 3-wire serial data input bus sets the ML2724's transceiver parameters and programs the PLL circuits. Entering 16-bit words into the ML2724 serial interface performs programming. Three 16-bit registers are partitioned such that 14 bits are dedicated for data to program the operation and two bits identify the register address. The contents of these registers cannot be read back via this bus.

The three registers are:

- **Register 0:** PLL Configuration
- **Register 1:** Channel Frequency Data
- **Register 2:** Internal Test Access

Figure 5 shows a register map. Table 3 through Table 5 provide detailed diagrams of the register organization: Table 3 and Table 4 outline the PLL configuration and channel frequency registers, and Table 5 displays the filter tuning and test mode register.

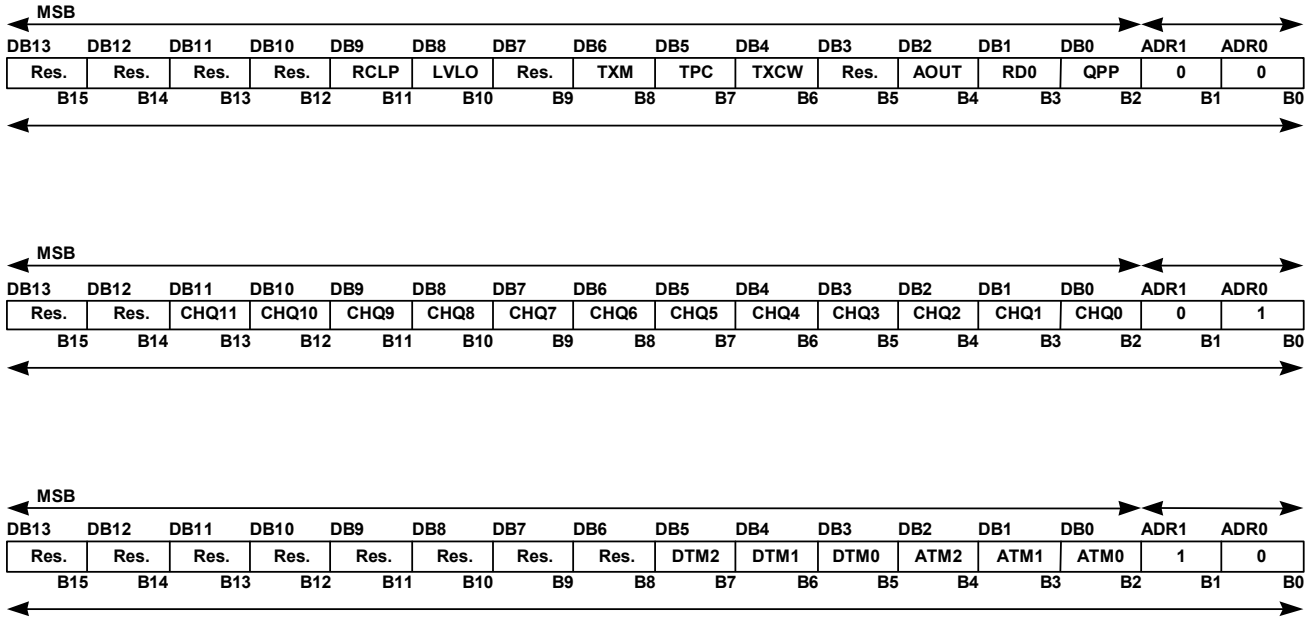


Figure 5: Configuration Register Map

NAME	DESCRIPTION	DEFINITION
Reserved	Reserved	Set all bits to 0 (zero)
Reserved	Reserved	
Reserved	Reserved	
Reserved	Reserved	
RCLP	RSSI Clip Disable	0: RSSI clipped to 1.9V at –15dBm 1: RSSI not clipped
LVLO	Low Voltage Lockout	0: PAON Undisturbed 1: PAON De-asserted for VCCA<2.65V. Reset on RXON high
Reserved	Reserved	Set to 0
TXM	TX RF Output Mode	0: TX RF Output always on in TX mode 1: TX RF Output follows PAON signal
TPC	Transmit Power Control	0: AOUT pin pulled to ground 1: AOUT pin high impedance
TXCW	Transmit Test Mode	0: FSK modulation in Transmit mode 1: CW (no modulation in Transmit mode)
Reserved	Reserved	Set to 0
AOUT	Analog Output	0: AOUT pin is Transmit Power Control 1: AOUT pin is Analog Data Out
RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1: 12.288MHz nominal reference frequency (preferred)
QPP	PLL Charge Pump Polarity	0: For fc < fref, charge pump sources current 1: For fc < fref, charge pump sinks current
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=0

Table 3: Register 0 -- PLL Configuration Register

NAME	DESCRIPTION	DEFINITION
Reserved	Channel Frequency select bits	Set all bits to 0 (zero)
Reserved		
CHQ11		Divide ratio=f_c/1.024
CHQ10		
CHQ9		
CHQ8		
CHQ7		
CHQ6		
CHQ5		
CHQ4		
CHQ3		
CHQ2		
CHQ1		
CHQ0		
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=1

Table 4: Register 1 – Channel Frequency Register

NAME	DESCRIPTION	DEFINITION
Reserved	Reserved	Set all bits to 0 (zero)
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
DTM2	Digital Test Control Bits	See Table 16
DTM1		
DTM0		
ATM2	Analog Test Control Bits	See Table 15
ATM 1		
ATM 0		
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=1

Table 5: Register 2 – Test Mode Register

Power-On State

On Power up, all register bits are cleared to the default value of 0 (zero). Power up is defined as occurring when VDD≥2.0V. The register default values are valid upon power up.

CONTROL REGISTER BIT DESCRIPTIONS

ADR<1:0>, All Registers, Bits 0-1

Address Bits: The ADR<1:0> bits are the least-significant bits of each register. Each register is divided into a data field and an address field. The data field is the leading field, while the last two bits clocked into the register are always the address field. When EN goes high, the address field is decoded and the addressed destination register is loaded. The last 16 bits clocked into the serial bus are loaded into the register. Clocking in less than 16 bits results in a potentially incorrect entry into the register.

RES (Reserved), All Registers

Reserved Bits: These bits are reserved. These bits must be cleared to 0s (zeros) for normal operation. When power is reset, all of the registers' data fields are cleared to 0s (zeros).

QPP - Register 0, Bit 2

Charge Pump Polarity: This bit sets the charge pump polarity to sink or source current. For a majority of applications, this bit is cleared (QPP=0). For applications where an external inverting amplifier is used in the loop filter, this bit is set to change the charge pump polarity (see Table 6).

QPP	PLL CHARGE PUMP POLARITY
0	$f_c > f_{ref}$ =» Charge pump sinks current.
1	$f_c > f_{ref}$ =» Charge pump sources current.

Table 6: PLL Charge Pump Polarity

RD0 - Register 0, Bit 3

Reference Divide: This bit sets the reference divider from the FREF pin to the reference input of the PLL phase/frequency detector to either 9 or 18 (see Table 7).

RD0	REFERENCE DIVISION	FREF XTAL FREQ	PLL REF FREQ
0	9	6.144 MHz	682.67KHz
1	18	12.288 MHz	682.67KHz

Table 7: Reference Frequency Select

AOUT - Register 0, Bit 4

Analog Output Mode: This bit changes the function of the AOUT pin between an analog data output to transmit power control (see Table 8).

AOUT	AOUT PIN FUNCTION
0	Transmit Power Control
1	Data Filter Analog Output

Table 8: AOUT Function Select

TXCW - Register 0, Bit 6

Transmit Continuous Wave: This bit produces a continuous wave (CW) transmitter output for product test when RXON is low (see Table 9).

TXCW	TRANSMIT MODULATION
0	FSK Modulation
1	CW – No Modulation

Table 9: Transmit Modulation Mode

TPC - Register 0, Bit 7

Transmit Power Control: When the AOUT bit is low, this bit controls the state of the open-drain output pin. Although this bit can be changed at any time, the AOUT pin only changes state at the falling edge of RXON (see Table 10).

TPC	TPC PIN STATE
0	High Impedance
1	Pulled to Ground

Table 10: TPC Pin State

TXM - Register 0, Bit 8

Transmit Mode: This bit controls the TX RF buffer state timing mode. It must be reset to 0 for normal operation (see Table 11).

TXM	TXRF BUFFER BEHAVIOR
0	RF Output Always On in TX Mode
1	RF Output Follows PAON

Table 11: TXM Mode

LVLO - Register 0, Bit 10

Low Voltage Lock Out: The LVLO bit enables a transmit low voltage lockout latch, which shuts off the transmitter by de-asserting the PAON output. This latch is set if the supply voltage drops below 2.65V and is reset when the RXON control input goes high (see Table 12).

LVLO	PAON BEHAVIOR
0	PAON Undisturbed
1	PAON de-asserted when VCCA<2.65V, Reset by RXON high.

Table 12: LVLO Operation

RCLP - Register 0, Bit 11

RSSI Clip Enable: The RCLP bit disables the RSSI clipping circuitry. With RCLP low, the RSSI output voltage is clipped to a maximum of about 2.0V at –10dBm. With RCLP high, the RSSI is not clipped. (see Table 13).

RCLP	RSSI BEHAVIOR
0	RSSI output clipped to a maximum of ~1.9V at –15dBm
1	RSSI output not clipped

Table 13: RCLP Operation

CHQ <11:0> - Register 1, Bits 2-13

Channel Frequency Selection: These bits set the RF carrier frequency for the transceiver (see Table 14). With a 6.144MHz or 12.288MHz clock at the FREF pin, the channel frequency value is calculated by multiplying the CHQ value by 1.024. The recommended operating range value of the CHQ is from 2,346 to 2,424. These bits must be programmed to a valid channel frequency before XCEN is asserted.

B15	B14	B13 TO B2	B1	B0
0	0	CHQ - PLL Divide Ratio	0	1

Table 14: Main Divider

The divide ratio is calculated as f_C /1.024 where f_C is the channel frequency in MHz.

$$f_C = 1.024 * CHQ$$

ATM<2:0> - Register 2, Bits 2-4

Analog Test Mode: The test mode selected is described in Table 15. The performance of the ML2724 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power-up) state of these bits is ATM<2:0>=<0,0,0>. When a non-zero value is written to the field, the RSSI and AOUT pins become analog test access ports, giving access to the outputs of key signal processing stages in the transceiver. During normal operation, ATM<2:0> must be set to all zeros.

ATM2	ATM1	ATM0	RSSI	AOUT
0	0	0	RSSI	Set by AOUT bit
0	0	1	No Connect	No Connect
0	1	0	I IF Filter Output	Q IF Filter Output
0	1	1	Q IF Filter – ve Output	Q IF Filter + ve Output
1	0	0	I IF Filter – ve Output	I IF Filter + ve Output
1	0	1	Data Filter + ve Output	Data Filter – ve Output
1	1	0	I IF Limiter Outputs	Q IF Limiter Outputs
1	1	1	1.67V Voltage Reference	VCO Modulation Port Input

Table 15: Analog Test Control Bits

DTM <2:0> - Register 2, Bits 5-7

Digital Test Mode: The DTM<2:0> bit functions are described in Table 16. The performance of the ML2724 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power up) state of these bits is DTM<2:0>=<0,0,0>. When a non-zero value is written to these fields, the DOUT and PAON pins become a digital test access port for key digital signals in the transceiver. During normal operation, DTM<2:0> must be set to all zeros.

DTM2	DTM1	DTM0	PAON	DOUT
0	0	0	PA Control	Data Out
0	0	1	PA Control	AGC Switch State
0	1	0	PA Control	PLL Main Divider Output
0	1	1	PA Control	PLL Reference Divider Output
1	0	0	S – D Modulation LSB	Sigma – Delta Modulation MSB

Table 16: Digital Test Control Bits

DATA INTERFACES

BASEBAND INTERFACE: DIN & DOUT

The DIN and DOUT pins are digital CMOS signals that correspond to FSK modulation of the carrier frequency. The ML2724 is designed to operate as an FSK transceiver in the 2.4GHz ISM band. The frequency deviation and transmit filtering is determined in the transceiver.

Data on the DIN pin is filtered and presented to the transmit two-port modulator. There is no re-timing of the bits, so the transmitted FSK data takes its timing from the input data. In the receive chain, FSK demodulation, data filtering, and data slicing take place in the ML2724, and the digital data is output on the DOUT pin. Bit and word rate timing recovery are performed off chip. The data filter output is available on the AOUT pin for use with an optional external data slicer.

RSSI & FREF

FREF (pin 9) is the master reference frequency for the transceiver. It supplies the frequency reference for the RF channel frequency and the filter tuning. The FREF pin is a CMOS input with internal biasing resistors. It can be AC coupled to sine or square wave source. The FREF input can also be driven by a CMOS logic output. The frequency of the FREF input is limited to one of: 6.144MHz or 12.288MHz.

The Received Signal Strength Indicator (RSSI) pin supplies a voltage proportional to the logarithm of the received power level. It is normally connected to the input of a low speed ADC and is used during channel scanning to detect clear channels on which the radio may transmit. It can also be used to set transmit power to optimize power consumption while maintaining an acceptable bit error rate (BER).

PA CONTROL OUTPUTS (PAON & AOUT)

The PAON (PA control) is a CMOS output that controls an optional off-chip RF PA. It outputs a logic high when the PA should be enabled and a logic low at all other times. This output is inhibited when the PLL fails to lock.

AOUT (pin 7) normally supplies the analog (not data-sliced) data output, but it can also be configured as an open-drain output for transmit power control. This mode is controlled by the TPC bit in Register 0. This bit can be changed at any time, but the AOUT pin will not change mode until the beginning of the next transmit slot, triggered by a falling edge on RXON (see **Figure 6** and Table 17 for details).

In analog test modes the RSSI and AOUT pins become analog test access ports that allow the user to observe internal signals in the ML2724.

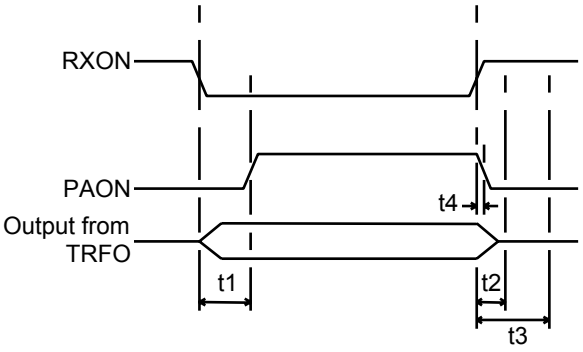


Figure 6: Power Amplifier Interface

SYMBOL	PARAMETER	TIME/µS
T1	RXON falling edge to PAON rising edge	62.5
T2	RXON rising edge to PLL frequency shift	6.5
T3	RXON rising edge to RECEIVE mode	70
T4	RXON rising edge to PAON falling edge	< 0.1

Table 17: Power Amplifier Timing

RF INTERFACE: RXI & TXO/TXOB

The RXI receive input (pin 17) and the TXO/TXOB differential transmit outputs (pins 21 and 22) are the only RF I/O pins. The RXI pin requires a simple impedance matching network for optimum input noise figure. The TXO/TXOB pins require a matching network for maximum power output into the RF power amp. If a single ended output is preferred, the signal from the TXO pin can be matched to the power amp and the TXOB output can be shunted to a power supply through a dummy load. The RF input and output ground (pin 18) must have a direct connection to the RF ground plane, and the RF power supply pins must be decoupled to the same ground plane as close to the device as possible.

PERFORMANCE GRAPHS

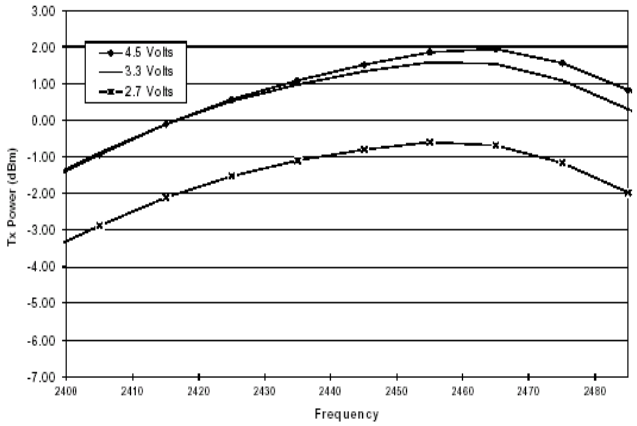


Figure 7: Output Power (Single Ended) vs. Frequency

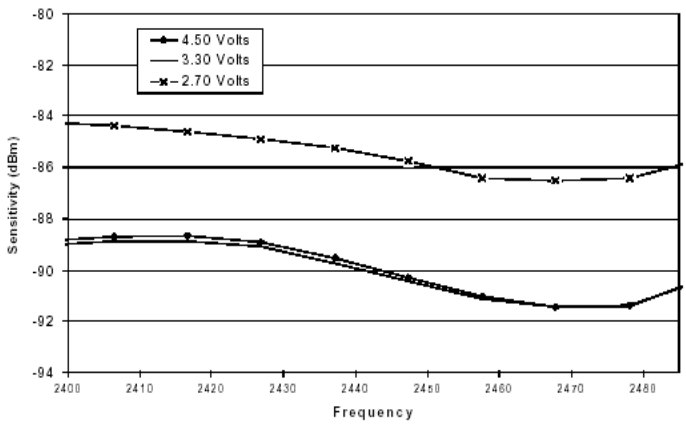


Figure 8: RX Sensitivity (12.5% BER) vs. Frequency

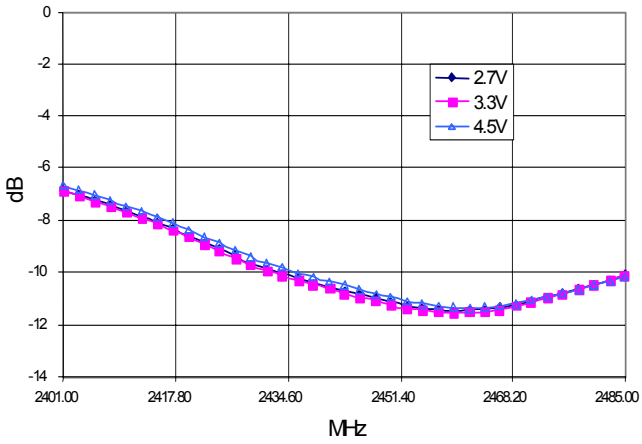


Figure 9: Input Return Loss vs. Frequency and Voltage

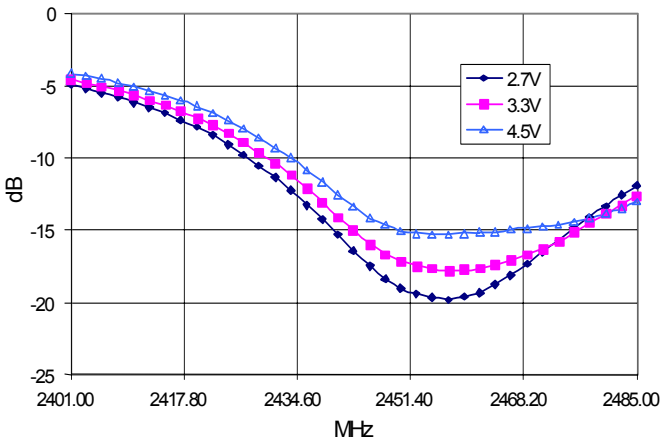


Figure 10: Output Match (SE) vs. Frequency and Voltage

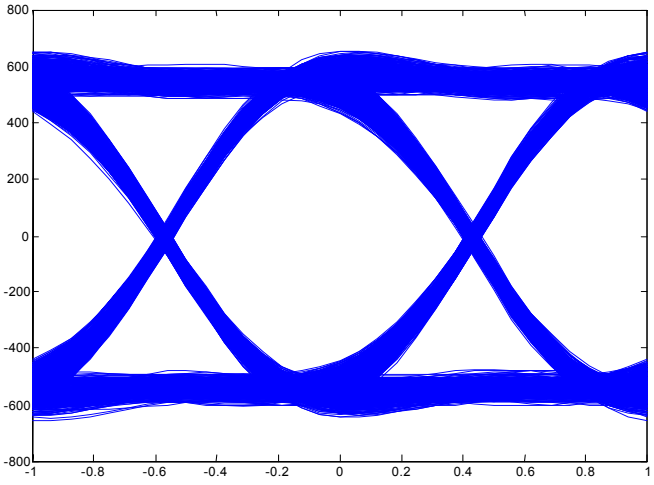


Figure 11: TX Eye Diagram

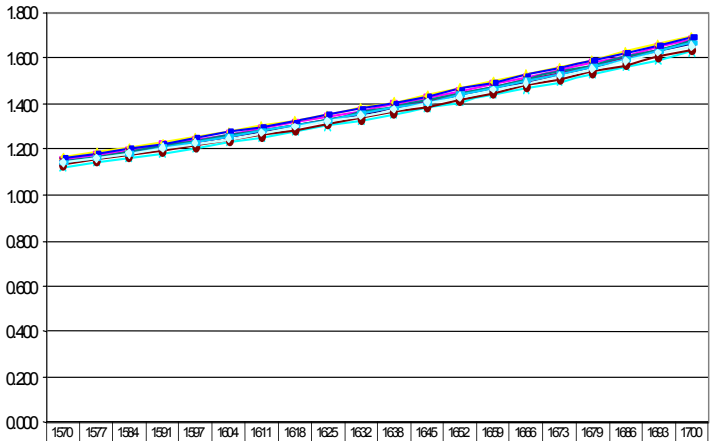
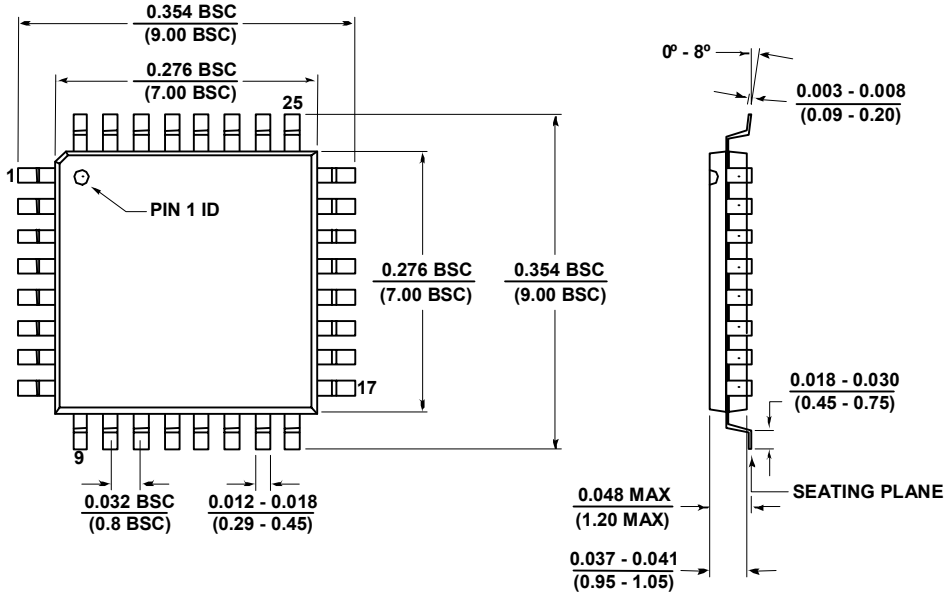


Figure 12: VCO Tuning Voltage vs. Frequency

PHYSICAL DIMENSIONS (*inches/millimeters*)



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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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