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April 1, 2003

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Hitachi Single-Chip Microcomputer H8S Series Technical Q&A

H8S/2655
H8S/2350
H8S/2355
H8S/2357
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H8S/2245
H8S/2148
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H8S/2138
H8S/2134
H8S/2128
H8S/2124

Application Note

ADE-502-059
Rev. 1.0
3/5/03
Hitachi, Ltd
Ougi T

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Preface

The H8S/2000 Series is a new series of Hitachi-original high-performance 16-bit microcomputers designed to offer higher performance and lower power consumption than existing H8 Series models, which are widely used in equipment control, and provide much greater ease of use. These microcomputers include a CPU, RAM, ROM, DMA controller, data transfer controller, bus controller, timers, SCI, A/D converter, and other on-chip supporting modules, making them suitable for use in a wide range of applications from small to large-scale systems. Another major feature of the H8S/2000 Series is upward-compatibility at the CPU object code level with the H8/300H, H8/300, and H8/300L Series within the H8 Series, allowing the use of existing software resources.

This Microcomputer Technical Q&A Application Note covers the H8S/2655 Series, H8S/2350 Series, H8S/2355 Series, H8S/2357, H8S/2345 Series, H8S/2245 Series, H8S/2148 Series, H8S/2144 Series, H8S/2138 Series, H8S/2134 Series, H8S/2128 Series, and H8S/2124 Series.

Using this Application Note

This Application Note is a compilation of responses to queries from Hitachi microcomputer users, presented in Question and Answer format. It should be used in conjunction with the relevant users' manuals.

It may also be helpful to read through this manual before beginning design work on products using H8S Series microcomputers, to gain more in-depth knowledge of the microcomputer products, and as a reminder of items that may present difficulties in the design stage.

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CPU

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MCU Operating Modes

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SCI

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I/O Ports

Clock Pulse Generator

Q&A No.: QAH8S-001

Category: CPU

Subject: Use of General Registers

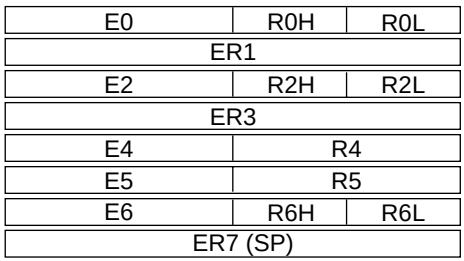
Question

Is it possible to use a mix of 8-bit, 16-bit, and 32-bit general registers?

Answer

Yes. Individual registers can be used in any way desired, as shown below.

Example:



However, note that ER7 is used implicitly as the SP.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-002

Category: CPU

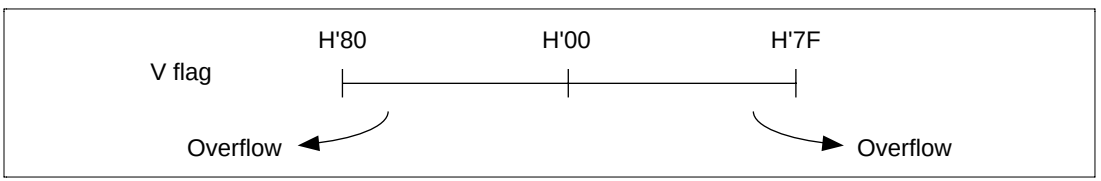
Subject: Difference between V Flag and C Flag in CCR

Question

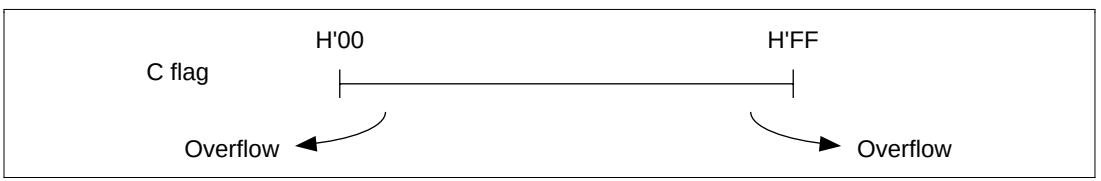
The V flag and C flag in CCR are both set if overflow occurs during an operation. What is the difference between these flags?

Answer

The V flag in CCR is used to identify whether overflow occurs in a signed operation. To take the example of a byte-size operation, this flag is set to 1 if the operation result is smaller than the negative minimum value (H'80) larger than the positive maximum value (H'7F).



The C flag, on the other hand, is used to identify whether overflow occurs in an unsigned operation. To take the example of a byte-size operation, this flag is set to 1 if the operation result is larger than the maximum value (H'FF) or smaller than the minimum value (H'00).



Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-003

Category: CPU

Subject: Relationship between Data Size and Change of V Flag

Question

Do changes of the V flag in the condition code register (CCR) depend on the data size?

Answer

The V flag changes on detection of overflow in the result of a signed arithmetic operation. The change operation is the same regardless of the data size, but the times when the flag changes differ as shown below.

Byte size: In the case of a value larger than H'7F or smaller than H'80
Word size: In the case of a value larger than H'7FFF or smaller than H'8000
Longword size: In the case of a value larger than H'7FFFFFFF or smaller than H'80000000

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-004

Category: CPU

Subject: Area Usable as ROM in Vector Table

Questions

1. Can a free area in the vector table (reserved, or reserved for system use) be used as ROM?
2. Can a free area in the internal I/O register area by used as ROM?

Answers

1. Vector numbers 0 to 6 and 12 to 15 reserved for system use in the vector table cannot be used. Reserved addresses can be used as ROM. Vector addresses for unused interrupts in the vector table can also be used as ROM.
2. Free I/O register areas cannot be used.

Additional Explanation

Areas reserved for system use can be used by development tools.

Addresses of areas reserved for system use, and reserved area addresses, should be checked manually.

In a memory-indirect-addressing branch address area, addresses other than those reserved for system use and the used vector table addresses can be used.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-005

Category: CPU

Subject: H8S/2000 CPU Normal Mode

Question

Are any precautions required when making a transition from H8/300 Series to H8S/2000 Series normal mode?

Answer

In H8S normal mode, address registers are recognized as being 32 bits long. Therefore, the following changes are necessary when using an H8/300 assembler program.

- Register indirect
  Example: MOV.B @R0,R1L → MOV.B @ER0,R1L
  An error is not flagged during assembly.
  Access is possible regardless of the contents of the extended register (E0).
- ADDS/SUBS instruction
  Example: ADDS.W R0 → ADDS.L ER0
  or
  INC.W R0
- SP (stack pointer)
  Example: MOV.W #16,SP → MOV.L #:32,SP
  or
  MOV.W #:16,R7

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-006

Category: CPU

Subject: MAC Register

Question

Why is the MAC register 42 bits long?

Answer

The MAC register is used to store the value obtained by adding together the result of a multiplication and the value in the register itself. The multiplication result is 32 bits (from a 16-bit × 16-bit operation), and if the MAC register value is added as 32 bits, overflow may occur. To prevent overflow, therefore, the 32 bits are increased by 10 bits, giving 42 bits (so that overflow will not occur even if 2^{10} = 1024 multiply-and-accumulate operations are performed).

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-007

Category: CPU

Subject: EXR Register

Question

Why has the EXR registers been added?

Answer

There are two reasons:

- Providing 8 interrupt mask levels using I2 to I0 enables multiple interrupt handling to be speeded up.
- Trace functions are implemented using the T bit. When the T bit is set to 1, trace exception handling is started each time an instruction is executed. For details, see the hardware manual.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-008

Category: Instruction

Subject: SUBX Instruction

Question

Why is the Z flag value unchanged when the result of a SUBX (subtraction with carry) instruction operation is 0?

Answer

This is because the SUBX instruction operation result is ANDed with the Z flag value before execution of the instruction. The logical equation is shown below.

$$Z = Z' \cdot \overline{Rm} \cdot \overline{Rm\text{-}1} \ ... \cdot \overline{R0}$$

When the execution result is 0, $\overline{Rm} \cdot \overline{Rm\text{-}1} \ ... \cdot \overline{R0}$ (abbreviated to $\overline{Rn}$ below) is 1. As the Z flag value for this instruction is the AND of $\overline{Rn}$ and Z', when the execution result is 0, the Z flag value is held.

Notes: m = 31 (longword size), 15 (word-size), or 8 (byte-size)
Ri = Bit I of result
Z' = Z flag value before instruction execution

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-009

Category: Instruction

Subject: BRN Instruction

Question

What kind of instruction is BRN (BF)?

Answer

The BRN instruction is useful as a replacement for a conditional branch instruction during debugging.

The operation of the BRN instruction is similar to that of the NOP instruction, but the instruction size and instruction execution time are different, as shown below.

Instruction		Instruction Size (Bytes)	Instruction Execution Time (States)
BRN	d:8	2	2*
	d:16	4	3*
NOP		2	1*

Note: * When the instruction is fetched from on-chip ROM

Note: Like BRN, the BRA (BT) instruction is useful for debugging, etc.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-010

Category: Instruction

Subject: Difference between BRA Instruction and JMP Instruction

Question

What is the difference between the BRA (BT) instruction and the JMP instruction?

Answer

With the BRA instruction, a branch is made on the basis of the address at which the BRA instruction is located, whereas with the JMP instruction, the branch address is specified indirectly. The differences between these two instructions are summarized below.

- With the BRA instruction, the branching range is limited to +127 bytes to –128 bytes for d:8, and +32767 bytes to –32768 bytes for d:16.
- With the BRA instruction, program relocation is possible if the relative value with respect to the branch destination is changed.
- The instruction length and number of execution states are different. for these two instructions.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-011

Category: Instruction

Subject: BRA and BRN Instructions

Questions

1. What does it mean when the BRA (BT) instruction condition is true?
2. What does it mean when the BRN (BF) instruction condition is false?

Answers

1. Since the BRA instruction always branches (Always), this means that the branch condition is always true.
2. Since the BRN instruction never branches (Never), this means that the branch condition is always false.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-012

Category: Instruction

Subject: Support of DAA (DAS) Instruction Corresponding to INC (DEC) Instruction

Questions

1. The DAA instruction is used for an add instruction (ADD instruction). What operation is performed if a DAA instruction is executed after an INC instruction?
2. The DAS instruction is used for a subtract instruction (SUB instruction). What operation is performed if a DAS instruction is executed after a DEC instruction?

Answers

1. Use of the DAA instruction after execution of an INC instruction is not supported. This is because the operation result is indicated by the C and H flags after an INC instruction is executed. To decrement decimal data, add –1 with an ADD instruction (ADD.B #–1, Rd), then execute a DAA instruction.
2. Use of the DAS instruction after execution of a DEC instruction is not supported. This is because the operation result is indicated by the C and H flags after a DEC instruction is executed. To decrement decimal data, add 1 with an ADD instruction (ADD.B #1, Rd), then invert the C and H flags (XORC #A0, CCR) and execute a DAS instruction.

Note: However, the actual operation is determined by the flag statuses.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-013

Category: Instruction

Subject: Odd Address Value when STC Instruction is Executed

Question

The manual states that when the STC instruction is executed, the CCR value is stored in the (register-indirect) even address. What is the value in the odd address?

Answer

The value is undefined.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-014

Category: Instruction

Subject: Stack Precautions

Question

Are any precautions required concerning the stacking method?

Answer

The CPU always uses word-size or longword-size access to the stack area. Setting the SP (stack pointer) to an odd value may result in misoperation. The PUSH, POP, STM, and LDM instructions should be used for stacking.

The initial value of the stack pointer is undefined, and must be set by the user.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-015

Category: Instruction

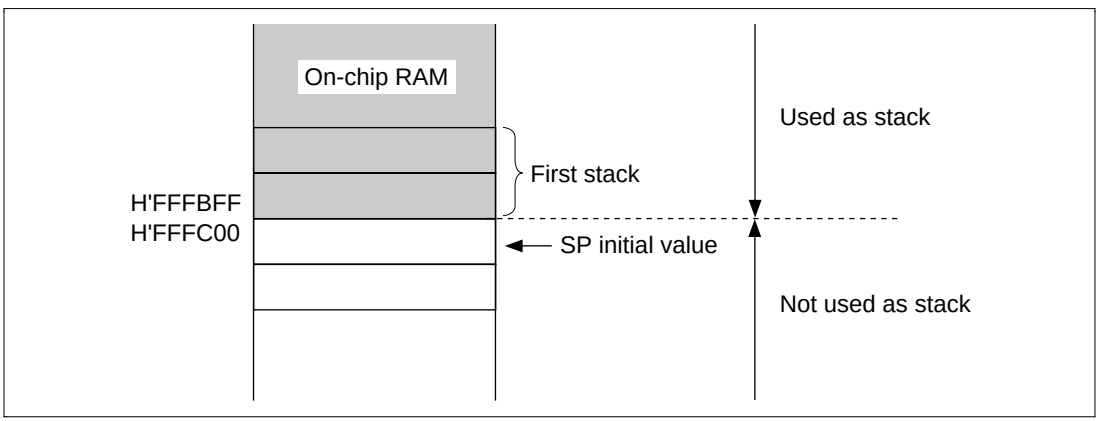
Subject: Stack Pointer

Question

How should the stack pointer (SP: ER7) be initialized?

Answer

To reserve the stack after the end of on-chip RAM, for example, set the initial value of the stack pointer as 1 greater than the last address of on-chip RAM.



Initial Set Value of Stack Pointer (Addresses Are for H8S/2655 Series)

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-016

Category: Instruction

Subject: TAS Instruction

Question

What is the meaning of the test and set instruction (TAS)?

Answer

The TAS instruction test memory contents, then sets the most significant bit (bit 7) to 1. This is a read-modify-write instruction, and the bus cannot be released during these operations.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-017

Category: Instruction

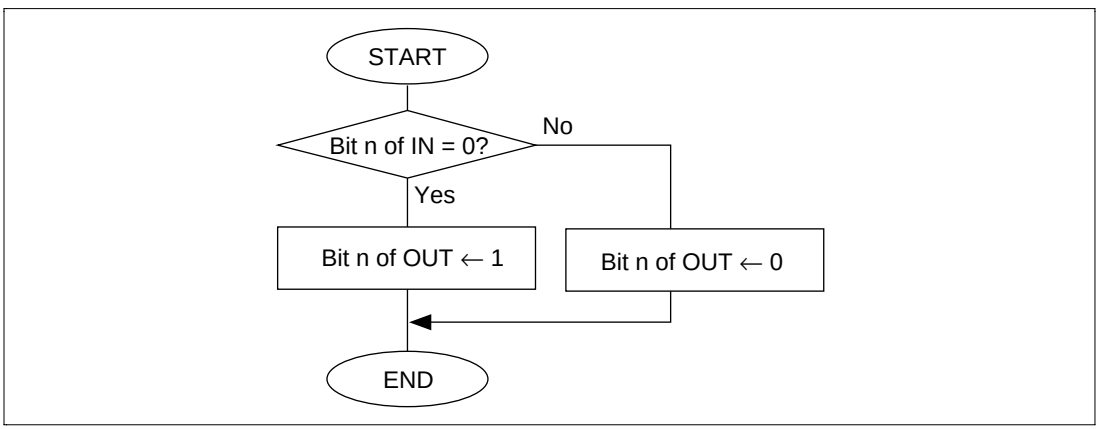
Subject: BLD and BIST Instructions

Question

How are bit-manipulation instructions such as BLD and BIST used?

Answer

These instructions can be used to invert any bit data in memory, and store the value in a bit of another memory address, as shown in the flowchart below.



Using BLD and BIST	Not Using BLD and BIST

`BLD #n,@IN`
`BIST #m,@OUT`
	`BTST #n,@IN`
	`BNE L1`
	`BSET #n,@OUT`
	`BRA L2`
	`L1: BCLR #n,@OUT`
	`L2:`

8 bytes/7 states	16 bytes/11 states

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-018

Category: Instruction

Subject: BOR and BIAND Instructions

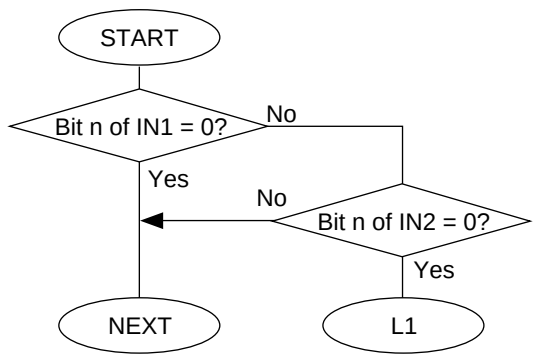
Question

How are bit-manipulation instructions such as BOR and BIAND used?

Answer

These instructions are used to branch after looking at a number of flags. An example of their use is shown below.

Example: To branch to L1 when IN1 flag = 1 and IN2 flag = 0



Using BOR/BIAND	Not Using BOR/BIAND
BLD #n,@IN1	BTST #n,@IN1
BIAND #m,@IN2	BNQ NEXT
BCS L1	BSET #m,@IN2
	BNE NEXT
	BRA L1
	NEXT:
10 bytes/8 states	14 bytes/10 states

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-019

Category: MCU Operating Modes

Subject: Mode Pins

Questions

1. Is it possible to change the MCU operating mode during normal operation?
2. Is there any way of fixing the MCU operating mode (preventing a change of MCU operating mode due to noise, etc.)?

Answers

1. The MCU operating mode cannot be changed during normal operation, as this would cause misoperation.
2. Read the memory control register (MDCR). When MDCR is read, the input levels of the mode pins (MD2 to MD0)[*1] are latched in the corresponding bits. As these latches are cleared by a power-on reset but not by a manual reset[*2], a change of MCU operating mode during operation can be prevented in this way.

Notes: 1. In the H8S/2100 Series, the mode pins are MD1 and MD0.
2. There is no manual reset in the H8S/2100 Series.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-020

Category: MCU Operating Modes

Subject: Use of RAME Bit

Question

How is the RAME bit used?

Answer

The RAME bit is used for on-chip RAM protection, etc. Since CPU operation is halted asynchronously in hardware standby mode, there is a risk of losing the on-chip RAM contents. On-chip RAM contents can be protected by disabling the on-chip RAM with the RAME bit before processing is executed.

Also, the same addresses can be overlapped internally and externally by disabling RAM.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-021

Category: Exception Handling

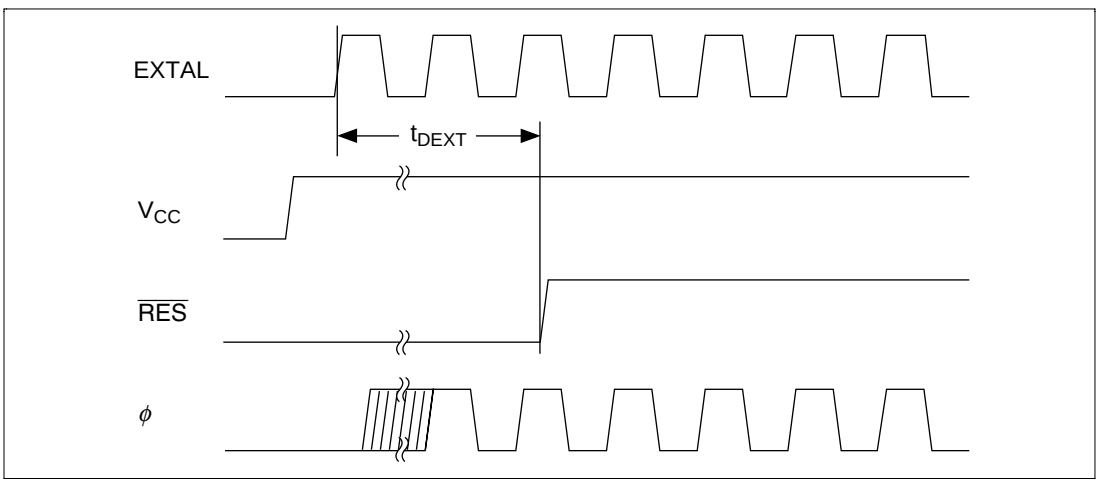
Subject: Reset

Question

A reset time of at least 20 ms is specified. Does this also apply when an external clock is used?

Answer

No, this specification does not apply in the case of an external clock. When an external clock is used, the reset time should be at least 500 µs. A reset of at least the length of the external clock output settling delay time (t_{DEXT} = 500 µs) is necessary to allow the clock output to stabilize (see figure below).



Oscillation Settling Timing

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-022

Category: Interrupts

Subject: Handling of Interrupt Requests when IRQ Interrupts are Disabled

Question

Is an IRQn interrupt request held pending if generated while the IRQnE bit is cleared to 0 in the IRQ enable register (IER)?

Answer

Yes. When the signal specified in the IRQ sense control register (ISCR) is input to the $\overline{\text{IRQn}}$ pin, IRQnF (the IRQn flag) is set to 1 in the IRQ status register (ISR). This does not depend on the status of the IRQnE bit. If the IRQnE bit is set to 1 while IRQnF is set to 1, an interrupt is requested. IRQnF can be cleared to 0 by software.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-023

Category: Interrupts

Subject: Handling of Interrupt Requests when Interrupts are Masked

Question

Is an IRQnF interrupt request held pending if generated when interrupts are masked by the I and UI bits, or bits I2 to I0, in the condition code register (CCR)?

Answer

Yes. IRQnF is independent of the status of the I and UI bits. If interrupt masking is released while the IRQnF and IRQnE bits are set to 1, the interrupt will be accepted.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-024

Category: Interrupts

Subject: Use of IRQ Status Register

Question

The IRQ status register (ISR) can be cleared to 0 by the user. When is this register used?

Answer

The IRQ status register is cleared to 0 automatically. Therefore, the user consciously clears this register in the following cases:

- In level sensing
- If there is a risk of generation of an unwanted interrupt before interrupts are enabled (e.g. during initialization or when pin connections are changed), total clearing can be performed directly before enabling interrupts
- When IRQ status register bits are used as flags, without enabling interrupts
- When multiplication interrupts are generated, to execute only high-priority processing, and not low-priority processing

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-025

Category: Interrupts

Subject: Interrupt Disable Timing (1)

Question

When a supporting module interrupt enable bit is cleared to 0, is the interrupt disabled immediately?

Answer

The interrupt is disabled after execution of the instruction that clears the interrupt enable bit to 0. However, if an interrupt request is generated during execution of the 0-clearing instruction, the interrupt request may be accepted after execution of that instruction.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-026

Category: Interrupts

Subject: Interrupt Disable Timing (2)

Question

When an interrupt enable bit is cleared to 0 in the IRQ enable register (IER), is the interrupt disabled immediately?

Answer

The interrupt is disabled after execution of the instruction that clears the interrupt enable bit to 0. If an interrupt request is generated during execution of the 0-clearing instruction, since the request signal is cleared in the same way as the enable bit, the interrupt request will not be accepted after execution of the instruction. However, since the IRQn flag is held, the interrupt request will be accepted if the corresponding interrupt enable bit is then set to 1.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-027

Category: Interrupts

Subject: Interrupt Immediately after Reset

Question

Is an interrupt ever generated immediately after a reset?

Answer

No, never. Immediately after a reset, all interrupts, including NMI, are disabled. However, NMI is accepted when the first instruction of the program is executed.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-028

Category: Interrupts

Subject: Simultaneous $\overline{\text{IRQ}}$ Interrupts of the Same Priority

Questions

1. With external interrupts, if interrupts within the group with the same priority ($\overline{\text{IRQ4}}$ to $\overline{\text{IRQ7}}$) are generated simultaneously (e.g. $\overline{\text{IRQ4}}$ and $\overline{\text{IRQ7}}$), which has priority?
2. What will happen if an $\overline{\text{IRQ4}}$ interrupt is generated in the $\overline{\text{IRQ7}}$ interrupt handling routine? (Is $\overline{\text{IRQ4}}$ held pending, or is $\overline{\text{IRQ4}}$ handling given priority?)

Answers

1. The priority order within the $\overline{\text{IRQ4}}$ to $\overline{\text{IRQ7}}$ interrupt group is: $\overline{\text{IRQ4}}$ > $\overline{\text{IRQ5}}$ > $\overline{\text{IRQ6}}$ > $\overline{\text{IRQ7}}$.
2. The $\overline{\text{IRQ7}}$ interrupt is accepted first. If interrupts are enabled in the $\overline{\text{IRQ7}}$ handling routine immediately after the $\overline{\text{IRQ7}}$ interrupt is accepted, interrupts $\overline{\text{IRQ4}}$ to $\overline{\text{IRQ7}}$ can then be accepted. If interrupts are not enabled in the $\overline{\text{IRQ7}}$ handling routine, these interrupts can be accepted after returning from the $\overline{\text{IRQ7}}$ handling routine.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-029

Category: Interrupts

Subject: Use of Different Interrupt Modes

Question

There are four interrupt control modes. How are these different modes used?

Answer

Modes 0 and 1 are compatible with the H8/300 Series and/or H8/300H Series. Guidelines for mode selection are given below.

- Mode 0
  Controlled by the I bit; useful when multiple interrupts are not used. If multiple interrupts are not used, the size of the stack, etc., can be limited.
  Compatible with the H8/300 Series and H8/300H Series.

- Mode 1
  Controlled by the I and UI bits. ICR can be handled easily as longword data, enabling ICR settings to be made at the start of an interrupt routine.
  EXR is not used, enabling the stack size to be limited.
  Compatible with the H8/300H Series.

- Mode 2
  Enables 8-level multiple interruption to be controlled at high speed.

Note: Interrupt control modes differ from product to product; see the relevant hardware manual for details.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-030

Category: Interrupts

Subject: Insufficient Number of External Interrupts

Question

Can any substitution method be used if more external interrupts are needed?

Answer

TPU input capture can be used as a substitute.

An unused TPU timer general register (TGR) is set to input capture. When the designated edge is input at the TIOC input, the TGR flag is set and an input capture interrupt is generated. This can be used in the same way as an edge-input IRQ.

16-bit free-running timer (FRT) input capture input can also be used in the same way.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-031

Category: Bus Controller

Subject: $\overline{CS}$ State in On-Chip RAM and Internal I/O Access

Question

Is the chip select signal ($\overline{CS7}$) output when on-chip memory or an internal I/O register (area 7) is accessed in advanced mode?

Answer

No, the chip select signal ($\overline{CS7}$) is not output in internal I/O register access, and a chip select signal is not output in on-chip memory access.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-032

Category: Bus Controller

Subject: ϕ Clock State when Bus is Released

Question

Is the ϕ clock output when the bus is released?

Answer

If the corresponding port data direction register (DDR) bit is set to 1 and the PSTOP bit in the system control register (SYSCR) is cleared to 0, the ϕ clock is output when the bus is released.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-033

Category: Bus Controller

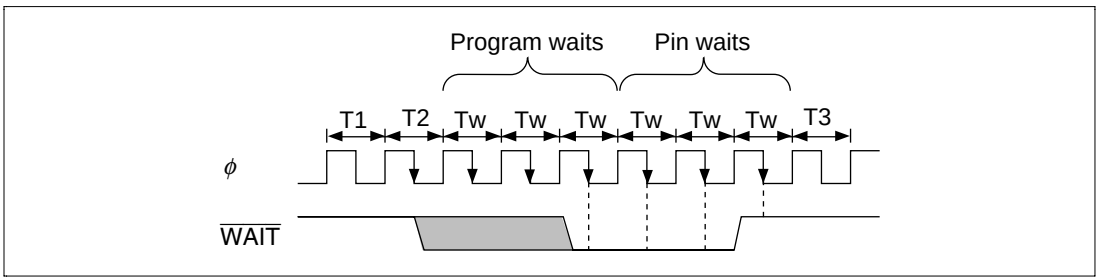
Subject: $\overline{\text{WAIT}}$ (1)

Question

When programmable waits are inserted and the pin wait function is also used, by what point should the $\overline{\text{WAIT}}$ pin level be settled?

Answer

The $\overline{\text{WAIT}}$ pin level should be settled by the fall of ϕ in the last T2 or Tw state.



Wait State Insertion Timing

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-034

Category: Bus Controller

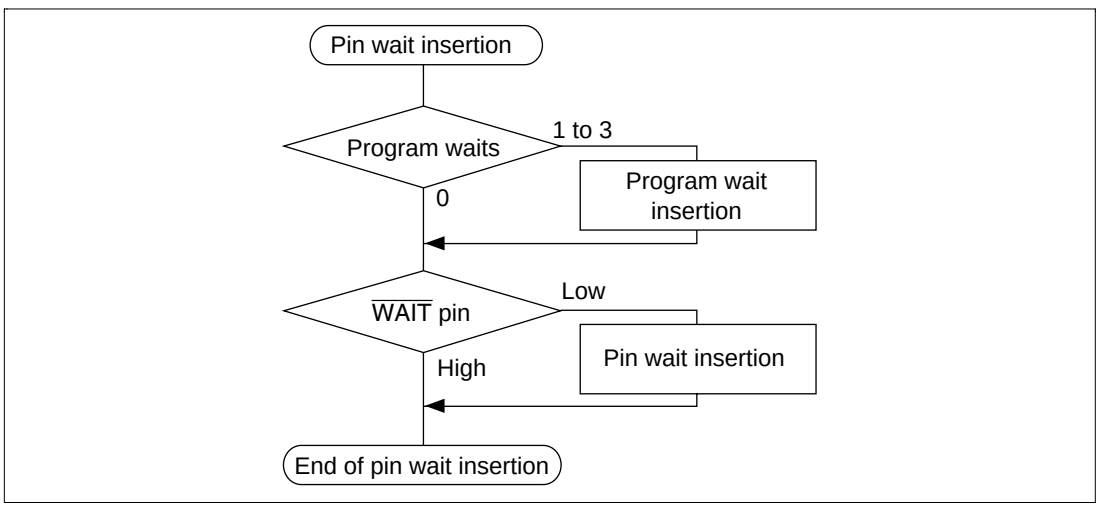
Subject: $\overline{\text{WAIT}}$ (2)

Question

The description of the pin wait function states that “program waits are inserted first.” Are program waits inserted irrespective of the wait control register (WCR) setting?

Answer

As stated in the manual, with pin waits, program waits are inserted in accordance with the WCR setting, followed by pin wait insertion with reference to the $\overline{\text{WAIT}}$ pin. A flowchart of pin wait insertion is shown below.



Pin Wait Insertion Flowchart

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-035

Category: Bus Controller

Subject: Program Wait Switchover Timing

Question

After a power-on reset, 3 program wait states are inserted in an external access cycle, making a 6-state access. When external 3-state access is set, what is the switchover timing?

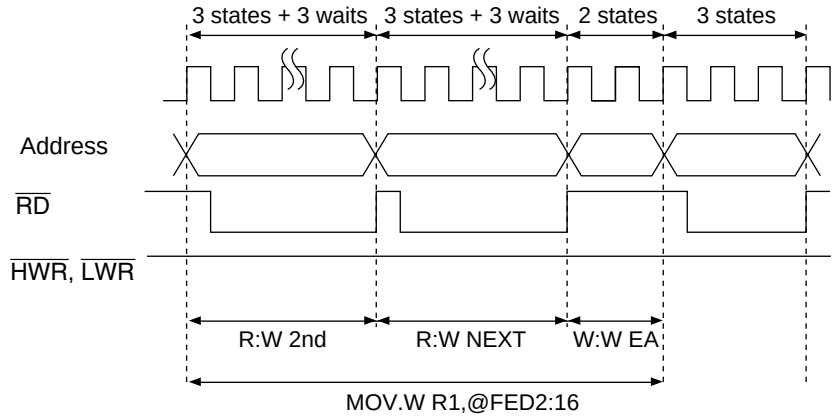
Answer

The switchover is made immediately after the wait control register (WCRH) is set. To set external 3-state access after a power-on reset, clear the Wn0 and Wn1 bits in WCR to 0.

An example of the switchover timing when waits are disabled by clearing all WCR bits to 0 with a MOV instruction is shown below.

Example: MOV.W R1,@H'FED2:16

WCRH (address H'FED2), WCRL (address H'FED3) (assuming 0 is stored in R1)



Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-036

Category: Bus Controller

Subject: $\overline{\text{BREQ}}$ Acceptance in Power-Down Modes

Questions

1. Is $\overline{\text{BREQ}}$ accepted in sleep mode?
2. Is $\overline{\text{BREQ}}$ accepted in hardware standby mode or software standby mode?

Answers

1. Yes. (However, in the H8S/2245 Series, H8S/2345 Series, and H8S/2355 Series, $\overline{\text{BREQ}}$ is not accepted in sleep mode when all modules are stopped.)
2. No, $\overline{\text{BREQ}}$ is not accepted in hardware standby mode or software standby mode.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-037

Category: Bus Controller

Subject: External Connection of RAM to 8-Bit-Access Space

Question

When RAM is connected externally to 8-bit-access space, is the $\overline{\text{HWR}}$ signal or the $\overline{\text{LWR}}$ signal used for access?

Answer

The $\overline{\text{HWR}}$ signal is used.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-038

Category: Bus Controller

Subject: Bus Controller Settings for Area 7

Question

Area 7 includes a mix of on-chip RAM and internal I/O registers. For which areas are the bus width and number of access states set in the bus controller valid?

Answer

In area 7, the bus width and number of access states set in the bus controller are valid for areas other than on-chip RAM and internal I/O registers*. The bus width and number of access states for on-chip RAM and on-chip supporting modules are fixed as shown in the table below.

Note: * Depends on the product; see the relevant hardware manual for details.

CPU bus Interface (Example of H8S/2655)

	On-Chip Modules		On-Chip Memory	
On-Chip Supporting Modules	**Bus Width**	**Access**	**Bus Width**	**Access**
A/D, TPU, 8-bit timers, WDT	16 bits	2 states	16 bits	1 state
Others	8 bits			

When the RAME bit is cleared to 0 in the system control register (SYSCR), on-chip RAM is disabled, and the area 7 settings are followed. In this case, the $\overline{CS7}$ signal goes low for the area 7 RAM area.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-039

Category: Bus Controller

Subject: External Bus states during CPU Operation

Questions

1. What is the state of the external buses during CPU internal processing?
2. What is the state of the external buses after $\overline{\text{DREQ}}$ acceptance?
3. What is the state of the external buses after $\overline{\text{BREQ}}$ acceptance?

Answer

The states in cases 1 to 3 are summarized in the table below.

Bus States during CPU Operation

No.	Bus State	Address Bus	Data Bus
1	During CPU internal processing	Held	High impedance
2	After $\overline{\text{DREQ}}$ acceptance	DMA address	DMA data
3	After $\overline{\text{BREQ}}$ acceptance	High impedance	High impedance

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-040

Category: Bus Controller

Subject: Internal I/O Register Access when Bus is Released

Question

When the H8S/2000 CPU releases the bus to an external device, can the external device (bus master) access H8S Series internal registers?

Answer

No, internal I/O registers cannot be accessed by an external device.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-041

Category: Bus Controller

Subject: $\overline{CS}$ Signals after Power-On Reset

Question

What is the state of the $\overline{CS}$ signals after a power-on reset?

Answer

After a power-on resets, all the $\overline{CS}$ signals except $\overline{CS0}$ are in the input state (in modes 1, 4, and 5). In expanded modes with on-chip ROM disabled, vectors and starts of programs should be located in area 0.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-042

Category: Bus Controller

Subject: Bus Release Wait Time after $\overline{\text{BREQ}}$ Input

Question

In what circumstances is there a long wait time from $\overline{\text{BREQ}}$ input to $\overline{\text{BACK}}$ output?

Answer

A $\overline{\text{BREQ}}$ request is held pending in the following cases:

- In DMAC data transfer in burst mode or block transfer mode
- In DTC data transfer
- When a wait is inserted in an external address access

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-043

Category: Bus Controller

Subject: External Bus Right Release and Refresh Control

Question

Are refresh requests held pending while the bus is released?

Answer

If a refresh request is generated while the external bus right is released, refresh control is deferred until the external bus master cancels the bus request. Only one refresh request is held.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-044

Category: Bus Controller

Subject: 2-CAS DRAM Interface

Question

Please explain the use of the LCASS bit with the 2-CAS DRAM interface.

Answer

The LCASS bit in bus control register L (BCRL) selects whether the $\overline{\text{LWR}}$ pin or the $\overline{\text{LCAS}}$ pin is used for the $\overline{\text{LCAS}}$ signal on the 2-CAS DRAM interface.

LCASS	Description
0	The $\overline{\text{LCAS}}$ pin is used for the 2-CAS DRAM interface $\overline{\text{LCAS}}$ signal. • More pins are needed for bus control. ($\overline{\text{BREQO}}$ output and $\overline{\text{WAIT}}$ input cannot be used.) • RAS down mode can be used, and DRAM fast page mode can be used effectively. • CBR refreshing can be performed in parallel with ordinary space access, limiting the drop in performance due to refreshing. • An idle cycle is not necessary in CBR refreshing after DRAM access. • Compatible with H8S/2350 Series
1	The $\overline{\text{LWR}}$ pin is used for the 2-CAS DRAM interface $\overline{\text{LCAS}}$ signal. (Initial value) • Fewer pins are needed for bus control. ($\overline{\text{BREQO}}$ output and $\overline{\text{WAIT}}$ input can be used.) • RAS down mode cannot be used. • Another ordinary space access cannot be performed during the CBR refresh period. • An idle cycle is inserted in CBR refreshing after DRAM access. • Not compatible with H8S/2350 Series

Clearing the LCASS bit to 0 and using the $\overline{\text{LCAS}}$ pin for the $\overline{\text{LCAS}}$ signal enables DRAM to be accessed efficiently.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-045

Category: Power-Down State

Subject: Medium-Speed Mode

Question

Why is it that, in medium-speed mode, a divided clock is supplied to the bus masters (CPU, DTC, DMAC), while the original system clock is supplied to the other on-chip supporting modules?

Answer

The internal clock supplied to the on-chip supporting modules is always fixed. Therefore, if medium-speed mode is set during SCI transmission/reception, for example, SCI operation will continue normally even though the bus master clock is changed. Medium-speed mode can thus be set at any time without regard to the operation of the on-chip supporting modules.

Also, non-operating modules can be stopped individually by means of the module stop function.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-046

Category: Power-Down State

Subject: Oscillation Settling Wait Time after Software Standby Mode

Question

What are the pin states during the oscillation settling wait period after exiting software standby mode?

Answer

The pin states during the oscillation settling wait period in this case are the same as for software standby mode. For details, see the appendix “Port States in Each Processing State” in the relevant hardware manual.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-047

Category: Power-Down State

Subject: On-Chip Supporting Modules in Software Standby Mode

Question

What is the state of the on-chip supporting modules in software standby mode?

Answer

In the H8S Series, on-chip supporting module register contents are generally held in software standby mode, and the contents of these registers do not have to be set again when software standby mode is exited. However, some on-chip supporting modules are reset in software standby mode. See the relevant hardware manual for details.

Example: In the H8S/2655 Series, the SCI is reset but the states of the other on-chip supporting modules are held. (See table 21.1, Operating States, in section 21, Power-Down State, in the hardware manual.)

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-048

Category: Power-Down State

Subject: Mode Pins (MD2 to MD0) in Hardware Standby Mode

Question

How does the microcomputer operate if the state of the mode pins (MD2 to MD0) is changed in hardware standby mode?

Answer

Normal hardware standby mode operation will not be performed. In hardware standby mode, as in normal operation, the mode pins (MD2 to MD0) must not be changed.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-049

Category: Power-Down State

Subject: Hardware Standby Mode at Power-On

Question

How can hardware standby mode be entered at power-on?

Answer

Drive the $\overline{\text{STBY}}$ pin low at power-on.

Note: The mode pins (MD2 to MD0) must be set to the prescribed input state at this time. (In the H8S/2655 Series, at least one of pins MD2 to MD0 should be driven high, and one of modes 1 to 7 must be selected as the MCU operating mode.)

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-050

Category: Power-Down State

Subject: Module Stop Mode

Question

When a write is performed on an 8-bit timer register, the value is not written. Why is this?

Answer

Immediately after a reset, an H8S Series chip enters module stop mode to hold down current dissipation, and the internal I/O registers of the relevant modules cannot be read or written to. Module stop mode should be cleared in advance for on-chip supporting modules that are to be used.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-051

Category: Power-Down State

Subject: Timer Output in Module Stop Mode

Question

If module stop mode is set during output compare match output (TIOC output) by the TPU, what happens to this output?

Answer

In module stop mode, the TPU stops, and the register contents and TIOC output state are held.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-052

Category: Electrical Characteristics

Subject: Current Dissipation Value

Question

In the current dissipation entry in the H8S/2245 Series Electrical Characteristics section, there is an item for which three modes—sleep, all-module-stop, and medium-speed mode (ϕ/32)—are combined into one. What is this?

Answer

This indicates a state combining all software-controllable power-down states. When these three modes are combined, the current dissipation can be minimized.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-053

Category: Electrical Characteristics

Subject: $\overline{RD}$ Signal Timing

Question

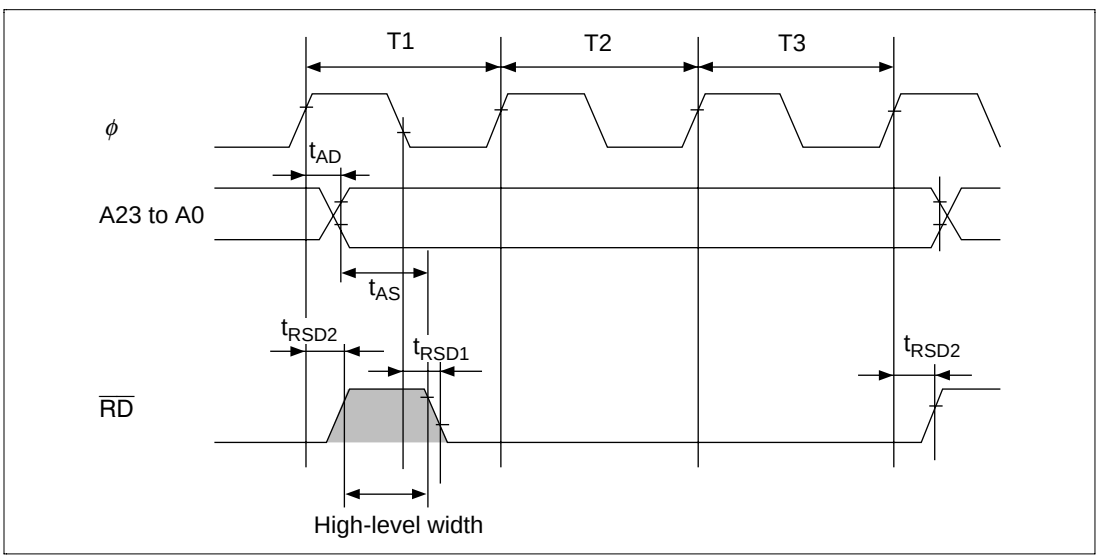
With successive read cycles, does the $\overline{RD}$ signal go high momentarily when the bus cycle changes, or does it remain low?

Answer

The $\overline{RD}$ signal goes high momentarily. The $\overline{RD}$ signal rise delay time t_{RSD2} and fall delay time t_{RSD1} are virtually the same ($t_{RSD1} \approx t_{RSD2}$). Therefore, the high-level width of the $\overline{RD}$ signal is as follows:

Since $t_{RSD1} \approx t_{RSD2}$,

$$\overline{RD} \text{ signal high-level width} = (t_{cyc}/2) + t_{RSD1} - t_{RSD2} \approx (t_{cyc}/2)$$



$\overline{RD}$ Signal Timing

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-054

Category: Pins

Subject: Handling of Unused Pins

Question

How should unused pins be handled?

Answer

For I/O ports and input ports, clear the DDR (data direction register) bits to 0 to set the input state, and pull each pin up or down individually with a resistance of approximately 10 kΩ.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-055

Category: Pins

Subject: $\overline{\text{RES}}$ Pin, $\overline{\text{STBY}}$ Pin, and NMI Pin Input Circuits

Question

What kind of circuits are the $\overline{\text{RES}}$ pin, $\overline{\text{STBY}}$ pin, and NMI pin input circuits?

Answer

The $\overline{\text{RES}}$ pin, $\overline{\text{STBY}}$ pin, and NMI pin are Schmitt-trigger inputs. The signals are transferred internally via a noise canceler.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-056

Category: Pins

Subject: Address Pin States in On-Chip Memory Access

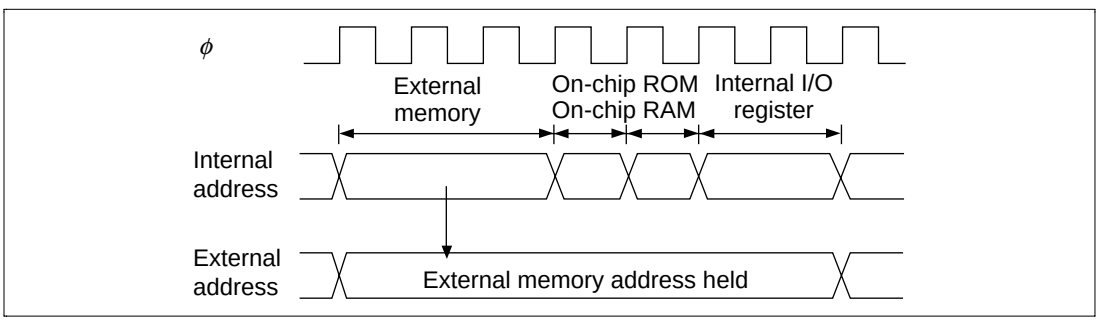
Question

When on-chip ROM or on-chip RAM is accessed, is the on-chip ROM or on-chip RAM address output off-chip?

Answer

When on-chip ROM, on-chip RAM, or an internal I/O register is accessed, the address bus retains its previous address value, and the on-chip ROM or on-chip RAM address value is not output off-chip (see figure below).

This is effective in reducing current dissipation and noise.



Address Bus in On-Chip ROM, On-Chip RAM, and Internal I/O Register Access

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-057

Category: Pins

Subject: Built-In MOS Pull-Ups in Reset

Question

Can built-in MOS pull-ups be turned on in the reset state?

Answer

In a manual reset, I/O port states are held, and therefore built-in MOS pull-ups can be turned on. In a power-on reset, I/O ports are initialized, and therefore built-in MOS pull-up settings are cleared.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-058

Category: Pins

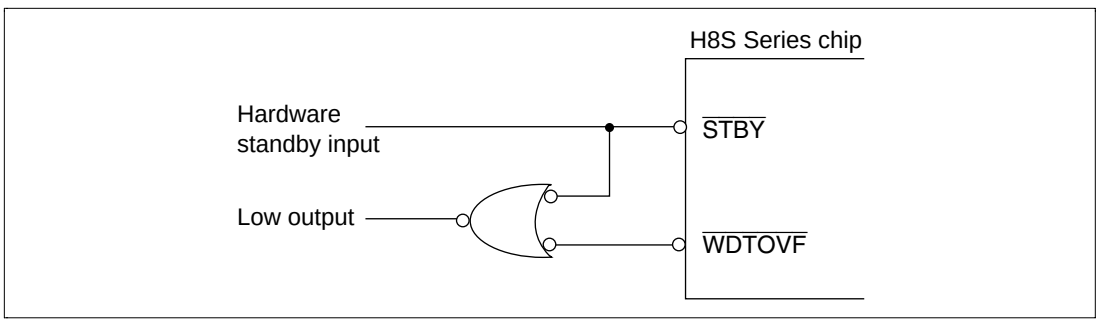
Subject: $\overline{\text{WDTOVF}}$ Pin

Questions

1. What is the state of the $\overline{\text{WDTOVF}}$ pin in hardware standby mode?
2. The $\overline{\text{WDTOVF}}$ pin is high during the hardware standby period. Please give an example of a circuit that drives this signal low.
3. What is the $\overline{\text{WDTOVF}}$ pin output specification?

Answers

1. In hardware standby mode, the $\overline{\text{WDTOVF}}$ pin is high.
2. An example of a circuit that drives the $\overline{\text{WDTOVF}}$ signal low during the hardware standby period is shown below.



Sample $\overline{\text{WDTOVF}}$ Signal Low-Level Output Circuit

3. The $\overline{\text{WDTOVF}}$ pin is a CMOS output pin.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-201

Category: DMAC

Subject: Number of States between Transfers

Question

A minimum of two states are necessary between the first DMAC transfer and the next. Why is this?

Answer

When the DMAC is activated, the bus request signal is sent to the bus controller at the rise of the first clock, and enabling is accepted at the fall. At the rise of the next clock, a read/write request is sent to the bus controller. This operation requires two cycles = two states for the bus cycle.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-202

Category: DMAC

Subject: Maximum Transfer Rate

Question

What is the maximum transfer rate for single address transfer?

Answer

Two states are required for the DMAC activation wait, and two states for a two-word data transfer. Thus, at 20 MHz operation, the maximum transfer rate is 16 bits / ($2t_{cyc}$ + $2t_{cyc}$)× 50 ns = 10 Mbytes/s.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-203

Category: DMAC

Subject: Difference between DMAC and DTC

Question

What is the difference between the DMAC and the DTC?

Answer

The DMAC has data transfer information registers within the module, and performs data transfer on up to four channels. The DMAC achieves a high transfer speed of 0.1 µs (min.) per channel.

The DTC places transfer data information in on-chip RAM, and can perform transfer on up to 85 channels. The transfer speed is 0.65 µs per channel. The DTC can perform chain transfer in which multiple data transfers are initiated by a single activation source.

Item	DMAC	DTC	Notes
Minimum transfer time	0.1 µs	0.65 µs	At 20 MHz operation
Transfer information	Dedicated registers	On-chip RAM	
Activation sources	13	28	H8S/2655
Transfer channels	4	85	
Chain transfer	No	Yes	

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-204

Category: DMAC

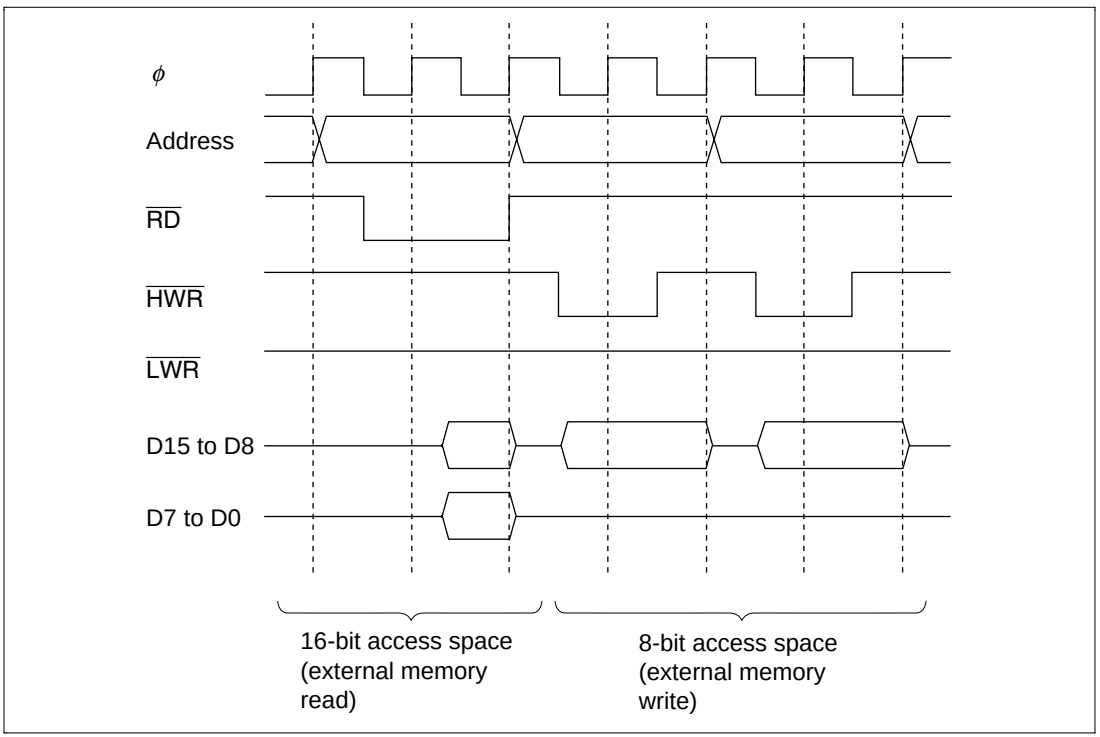
Subject: Alternate 8-Bit/16-Bit Space Accesses

Question

Can data transfer be performed between 8-bit space and 16-bit space using the DMAC or DTC?

Answer

Yes. As the input/output bus width is managed by the bus controller, as long as the bus width is set by the bus controller, the user can use the DMAC or DTC without having to be aware of the bus width.



Timing of Data Transfer from 16-Bit Access Space to 8-Bit Access Space

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-205

Category: DMAC

Subject: TEND Signal Output Conditions when Using Write Buffer Function

Question

What are the TEND signal output conditions when the write buffer function is used?

Answer

The TEND output signal goes low in an external bus cycle if either a DMAC read cycle or write cycle is an external access.

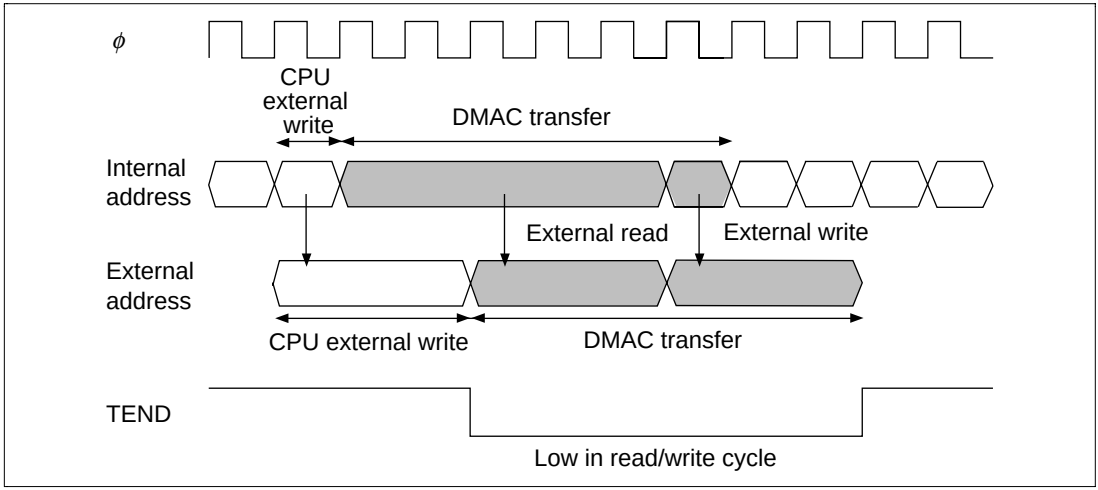
If a DMAC data transfer involves internal addresses, on the other hand, the TEND signal is not output while the external bus is used (during external bus release, an external write using the write buffer function, the DRAM refresh period, etc.). The TEND signal is output when the external bus is not in use.

DMAC TEND signal output is shown in the table below.

DMAC TEND Signal Output

DMAC Access Area	Read	Write
External address → external address	O	O
Internal address → external address	Δ	O
External address → internal address	O	O
Internal address → internal address	Δ	Δ

Note: Δ : Output when external bus is not being used
O : Always output



Example of External Address → External Address Transfer

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-206

Category: DMAC

Subject: Interrupt Acceptance After End of Transfer

Question

After the transfer count register value reaches H'0000 and an end interrupt is generated while the DMAC is being used, when is the next transfer request accepted?

Answer

The next transfer request is accepted when a bit is set to 1 by software in the data transfer control register (DTCR). When the transfer count register value reaches H'0000 and a transfer end interrupt is generated, the DTE bit is cleared and data transfer is disabled. To perform transfer again, make the transfer count register setting in the transfer end interrupt routine, then set the DTE bit to 1.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-207

Category: DMAC

Subject: Handling of Transfer Request before Start of Transfer

Question

If a transfer request is generated before the DMAC starts transfer, is the request ignored?

Answer

- If the activation source is an internal interrupt
  If the DTE bit is 0, a CPU interrupt is requested. When the DTE bit is set to 1 while that interrupt is masked by the CPU, an activation request is sent to the DMAC.
- If the activation source is an external request
  When edge-sensing is selected, the first activation after enabling is performed on detection of a low level, and therefore the request will not be ignored if the low level is held.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-208

Category: DMAC

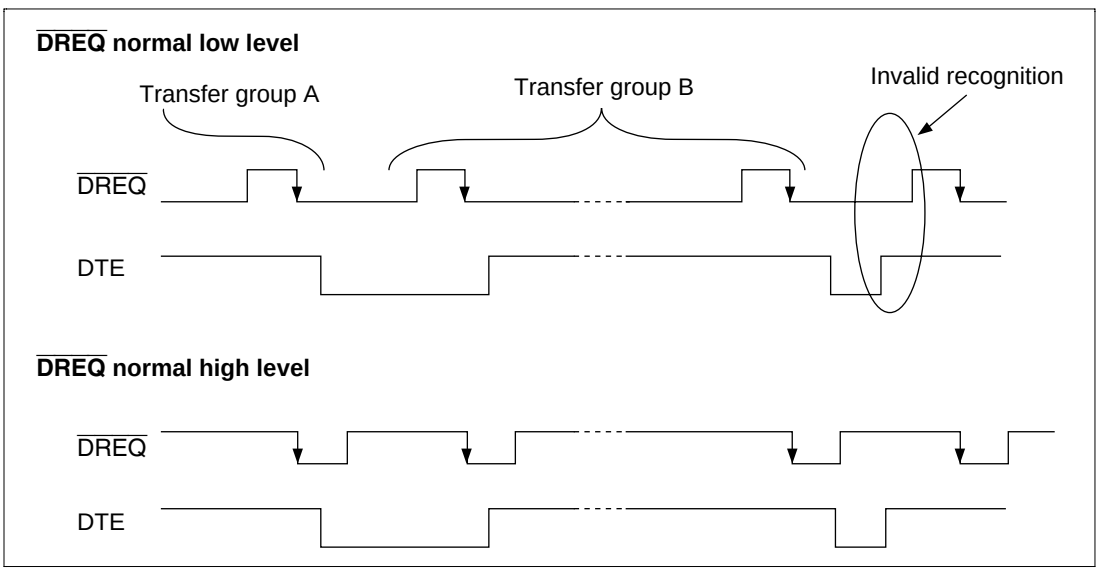
Subject: Activation Request Signal Detection

Question

When the $\overline{\text{DREQ}}$ pin is designated falling-edge input, why is the first transfer request performed at the low level?

Answer

If a falling edge at the $\overline{\text{DREQ}}$ pin were used for the first activation, it would not be possible to recognize a request at first when transfer is enabled (DTE = 1) after the $\overline{\text{DREQ}}$ signal falling edge. For this reason, the first activation after transfer is enabled is by low level detection.



$\overline{\text{DREQ}}$ and DTE Timing Chart

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-209

Category: DMAC

Subject: Short Address Mode and Full Address Mode

Question

What is the difference between the DMAC’s short address mode and full address mode?

Answer

The DMAC requires specification of the source address and destination address in order to perform data transfer. In full address mode, both of these addresses are specified as 24-bit addresses, whereas in short address mode, one is specified as a 24-bit address and the other as a 16-bit address. H'FF is written in the upper 8 bits of the 16-bit address. In short address mode, whether the 16-bit specification is to be used for the source or the destination address can be selected with a register setting.

If transfer is to be performed by means of internal interrupts in full address mode, setting a block size of 1 in block transfer mode results in the same operation as for sequential mode in short address mode.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-210

Category: DMAC

Subject: Bus Right in Standby State

Question

In the DMAC full address mode and external request mode, a standby state may be entered after a DMAC write. What happens to the bus right during this period?

Answer

The DMAC releases the bus right in the standby state, and so the bus is transferred to the CPU, refresh controller, etc.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-211

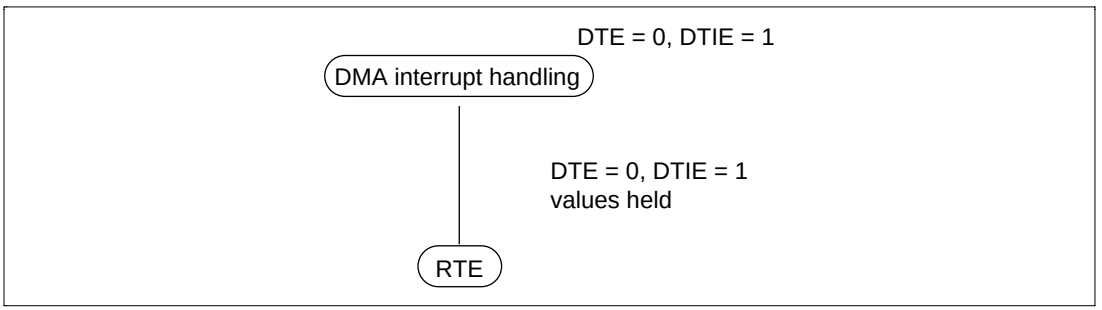
Category: DMAC

Subject: Handling of Transfer End Interrupt

Questions

The manual states that if DTE is cleared to 0 when DTIE = 1, an interrupt request is sent to the CPU.

1. In the case shown in the figure, will DMA transfer end interrupts be generated continually?
2. How can interrupt generation be prevented?



Answers

1. In the case in the figure, interrupts will be generated continually.
2. An interrupt will always be generated if DTIE is set to 1 (enabling interrupts) when DTE = 0. Therefore, either set the DTE bit to 1 (the BSET instruction can be used) or clear the DTIE bit to 0 (the BCLR instruction can be used).

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-212

Category: DMAC

Subject: $\overline{\text{DREQ}}$ Signal Input

Question

When the $\overline{\text{DREQ}}$ pin is used in level-sensing mode, must it be held low until the data transfer ends?

Answer

The $\overline{\text{DREQ}}$ signal is latched at the rise of ϕ, and once latched the activation source is held. The activation source will therefore be held if the $\overline{\text{DREQ}}$ pin remains low for at least two states.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
	H8S/2355	Yes	H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-213

Category: DTC

Subject: Nature of DTC

Question

Is the DTC special hardware, or is the DTC function executed by a CPU microprogram, etc.?

Answer

The DTC consists of special hardware. This enables it to perform high-speed data transfer without imposing any load on the CPU.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245	Yes	H8S/2148		H8S/2144
Yes	H8S/2138		H8S/2134	Yes	H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-214

Category: DTC

Subject: Maximum Number of Channels

Question

What is the maximum number of DTC channels?

Answer

DTC register information is located in a 1-kbyte area in on-chip RAM. The amount of RAM required for one DTC transfer is 12 bytes, enabling a maximum of 85 channels to be set.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245	Yes	H8S/2148		H8S/2144
Yes	H8S/2138		H8S/2134	Yes	H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-215

Category: DTC

Subject: Setting Register Information

Question

Are any precautions necessary when setting DTC register information?

Answer

Place DTC register information in the 1-kbyte area from H'FFF800 to H'FFFBFF* in on-chip RAM, and set the RAME bit to 1 in the system control register (SYSCR).

Note: * H'FFEC00 to H'FFEFFF in the H8S/2100 Series

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245	Yes	H8S/2148		H8S/2144
Yes	H8S/2138		H8S/2134	Yes	H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-216

Category: DTC

Subject: Order of Setting Register Information

Question

Is there a particular order for setting DTC register information?

Answer

There is no particular order, but the following point should be noted.

If the DTC mode registers (MRA/MRB) are set first, followed by the DTC source address register (SAR) and DTC destination address register (DAR):

Since SAR and DAR are 24-bit registers, when SAR and DAR are set with a longword instruction (MOV.L), the previously set MRA and MRB information will be corrupted. This can be avoided by making the SAR and DAR settings by longword access first, followed by the MRA and MRB settings.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245	Yes	H8S/2148		H8S/2144
Yes	H8S/2138		H8S/2134	Yes	H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-217

Category: DTC

Subject: Use of DTC Interrupt Select Bit (DISEL)

Question

How is the DISEL bit in DTC mode register B (MRB) used?

Answer

The use of the DISEL bit is shown below.

DISEL	Description
0	The CPU executes interrupt handling (end processing or activation processing) after completion of the specified number of data transfers. Suitable when performing data transfer only.
1	The CPU executes interrupt handling at the end of (end processing or activation processing) at the end of each DTC data transfer. If interrupt handling by the CPU is necessary each time, high-speed execution is possible by having the DTC replace the data transfer section.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245	Yes	H8S/2148		H8S/2144
Yes	H8S/2138		H8S/2134	Yes	H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-218

Category: TPU

Subject: Non-Timer Use of Port

Question

How can the TIOC I/O port be used for a purpose other than TPU input/output?

Answer

Set B'0000 in bits 7 to 4 or bits 3 to 0 of the timer I/O control register (TIOR) (disabling output).

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-219

Category: TPU

Subject: Cascaded Connection

Question

Can cascaded connection be used with the TPU?

Answer

Yes. The two timer register combinations shown below can be used. The upper and lower registers operate in synchronization with the clock.

1. TCNT1 + TCNT2
2. TCNT4 + TCNT5

With combination 2, the following points must be noted.

- Longword access cannot be used on the TCNT4/TCNT5 (TCNT, TGR) register pair, so two word accesses must be used. Consequently, there will be a lag between the read/write timings of the upper and lower registers.
- Compare matches occur separately for the upper and lower registers. In the case of an upper register compare match, in particular, care is required if the lower counter overflows or underflows.

Note: TCTN4 and TCNT5 are not provided in the H8S/2245 Series.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-220

Category: TPU

Subject: Dual Use of PWM Mode 1 and Input Capture

Question

When TPU channels 0 and 3 are set to PWM mode 1 and only timer general registers TGRnA and TGRnB are used, can the remaining timer general registers (TGRnC and TGRnD) be used for input capture?

Answer

No. There is one operating mode per channel. TGRnC and TGRnD can be used as output compare registers by disabling output.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-221

Category: TPU

Subject: Setting PWM Mode 2 Cycle

Question

Which register is used to set the cycle in PWM mode 2?

Answer

The cycle is determined by the register selected by CCLRn (counter clear) in the timer control register (TCR). In this case, output is automatically disabled for the output pins corresponding to the register used as the counter clear source.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-222

Category: TPU

Subject: Synchronous Operation of Two Sets

Question

Is synchronous operation of two sets possible?

Answer

No. The timer synchro register (TSYR) does not permit a synchronous operation setting for two or more sets.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-223

Category: TPU

Subject: Two-Phase PWM Output

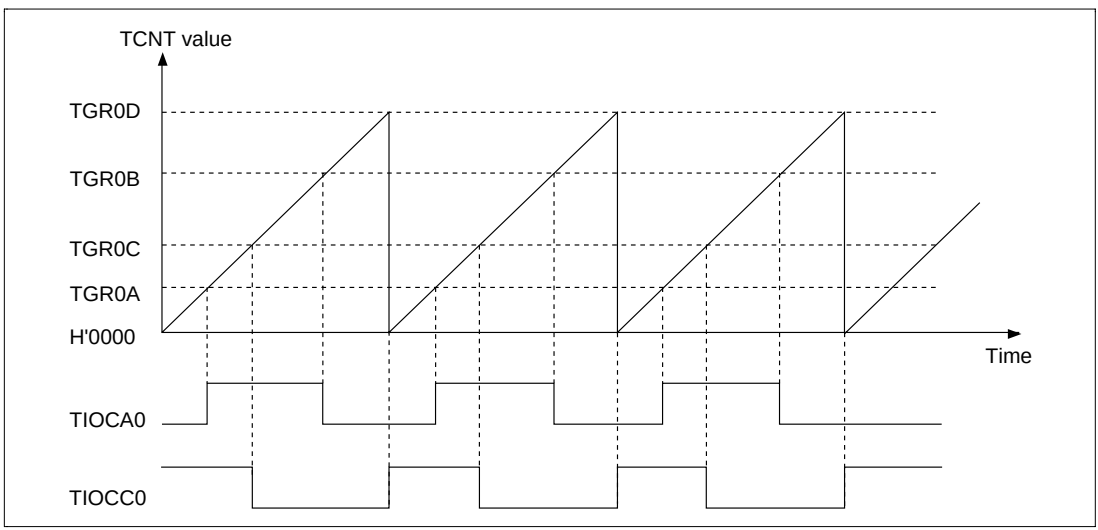
Question

Is it possible to obtain two-phase PWM output with a common cycle but different duty cycles and a phase difference?

Answer

This is possible in PWM mode 1, using channels 0 and 3 (or synchronous operation of two channels). The setting method for channel 0 is described below.

1. Set channel 0 to PWM mode.
2. Set TGRA and TGRB, and TGRC and TGRD, to different output with the timer I/O control register (TIOR).
3. Set a common cycle in TGRD, and set counter clearing by a TGRD compare match.
4. Set the phase difference in TGRA. Also, set the TIOC output duty cycle in TGRC so that TGRB – TGRA is the TIOCA output duty cycle.



Two-Phase PWM Output

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-224

Category: WDT

Subject: Interval Timer with Arbitrary Time Interval

Question

When the WDT is used as an interval timer, is it possible generate interrupts at fixed intervals?

Answer

Yes. However, since the WDT generates only overflow interrupts*, the initial value should be written in TCNT. Note that TCNT is always in the reset state when TME = 0.

Note: * An NMI interrupt setting can also be made in the H8S/2100 Series.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-225

Category: SCI

Subject: SCI Initialization

Question

In SCI initialization, why is there a minimum 1-bit wait before the TE bit or RE bit is set in the serial control register (SCR)?

Answer

This 1-bit interval is the minimum time necessary for internal processing to fix the data. If transmission is performed without this 1-bit wait, indefinite data will be transmitted. A wait of at least 1-bit duration is therefore essential before performing transmission.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-226

Category: SCI

Subject: Difference between TDRE Flag and TEND Flag

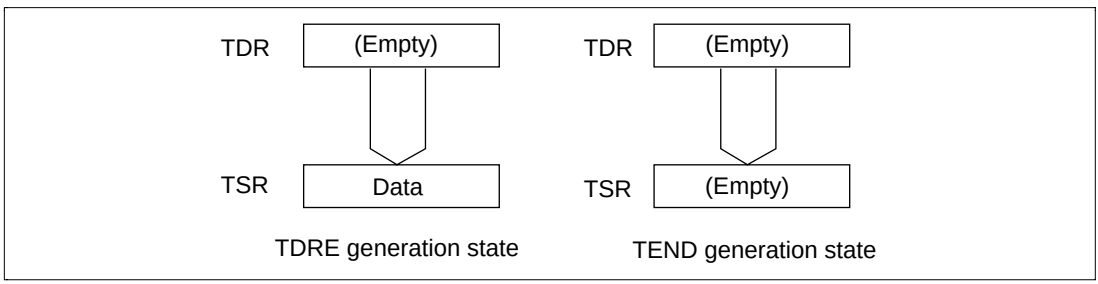
Question

What is the difference between the TDRE flag and TEND flag in the serial status register (SSR)?

Answer

The TDRE flag indicates that the transmit data register (TDR) is in the write-enabled state, without regard to the internal state of the transmit shift register (TSR).

The TEND flag indicates that TSR is empty, and TDR is in the write-enabled state. The status of the TEND flag should be checked to confirm whether all data has been transmitted.



TDRE and TEND Generation States

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-227

Category: SCI

Subject: Initial State of TxD Pin

Question

What happens to the initial value of the TxD pin when the TE bit is set to 1 in the serial control register (SCR) in serial transmission?

Answer

When the TE bit is set to 1, the TxD pin goes high automatically in both asynchronous mode and synchronous mode.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-228

Category: SCI

Subject: Maximum External Clock Input Value (Asynchronous Mode)

Question

What is the maximum possible external clock input frequency in asynchronous mode?

Answer

The cycle of the external clock input to the SCI must be at least $4 \times t_{cyc}$ (min.). With a 20 MHz operating frequency, the maximum value for external clock input is 5 MHz (max.).

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-229

Category: SCI

Subject: Transmit/Receive Operation in Synchronous Mode

Question

Can reception alone be performed in transmit/receive operation (TE = RE = 1) in synchronous mode?

Answer

As the same clock is used for transmission and reception in synchronous mode, transmission and reception are performed simultaneously in transmit/receive operation (TE = RE = 1). Consequently, transmit/receive operation cannot be performed until transmission is started (TDRE is cleared to 0).

When the H8S Series chip performs clock output, when TDRE is cleared to 0 the clock is output and transmission and reception are performed simultaneously.

When the H8S Series chip uses clock input, TDRE should be cleared to 0 before inputting the clock. The clock will be ignored if input before TDRE is cleared to 0.

To perform reception only, write dummy data to TDR to clear TDRE to 0.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-230

Category: SCI

Subject: SCI Transmission Using DTC

Question

Is it possible to performs SCI transmission by activating the DTC at successive timer compare matches?

Answer

No. The reason is that, in DTC data transfer, TDRE is cleared to 0 in the serial data register (SSR) only when the DTC activation source is the SCI transmission-completed interrupt.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-231

Category: SCI

Subject: Permissible Bit Rate Error in Asynchronous Mode

Question

What is the permissible bit rate error in asynchronous mode?

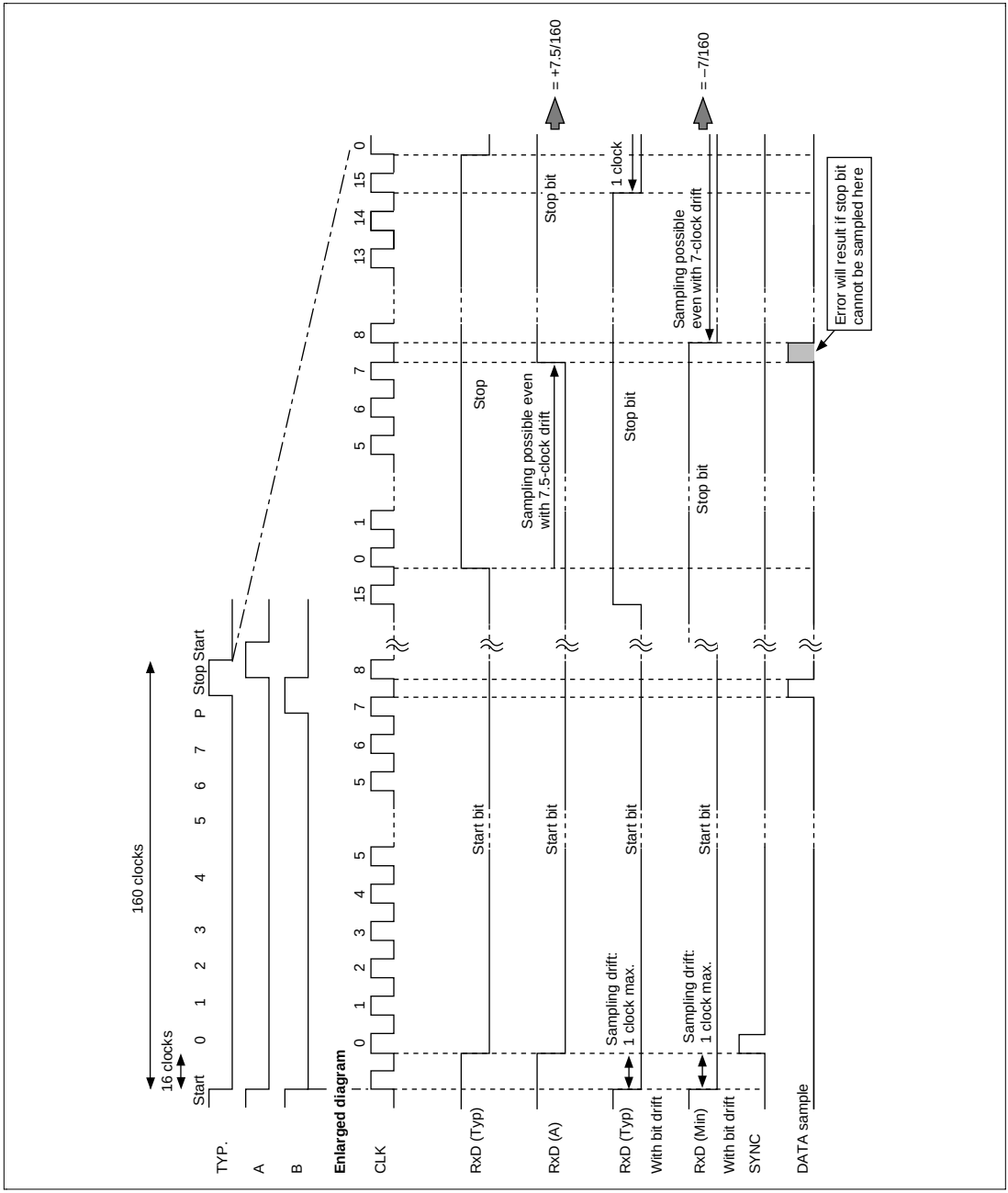
Answer

When the H8S Series chip is receiving, the permissible error within one frame is as shown below. This shows the worst case for the sampling timing of the last bit (stop bit) of the frame. With 8-bit data and no parity, one frame consists of 160 internal basic clocks. Assuming no per-bit distortion, the conditions under which the stop bit can be sampled are as follows:

- When transmitting side is slow: 7.5/160 = 0.046
- When transmitting side is fast: –7/160 = –0.043

From the above two points, the permissible error can be calculated to be approximately 4.3%

This is a theoretical value. A margin should be allowed on the system side in actual system designs.



Receive Margins in Asynchronous Mode

However, if the transmitting side is fast, the next frame will begin before completion of the receive operation, and it may not be possible to receive this next frame. Two-stop mode should therefore be used when receiving, since the second stop bit is ignored in this mode.

Note: See “Receive Data Sampling Timing in Asynchronous Mode and Receive Margin” in the hardware manual.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-232

Category: SCI

Subject: Operation of RDRF Flag

Question

An operation to clear the RDRF flag to 0 in the serial status register (SSR) is necessary in SCI reception. What will happen if this flag is cleared to 0 directly without first reading 1?

Answer

It will not be cleared. However, if the BCLR instruction is used, after a byte-unit read of SSR, the RDRF flag is cleared to 0, and a byte-unit write is performed. Therefore, the RDRF flag can be cleared to 0 with a BCLR instruction when the flag is set to 1 (in the RXI interrupt handling routine).

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-233

Category: SCI

Subject: RDRF Flag Set Timing

Questions

When data reception ends, the RDRF flag is set to 1 in the serial status register (SSR).

1. What is the timing for RDRF flag setting in asynchronous mode?
2. What is the timing for RDRF flag setting in synchronous mode?

Answers

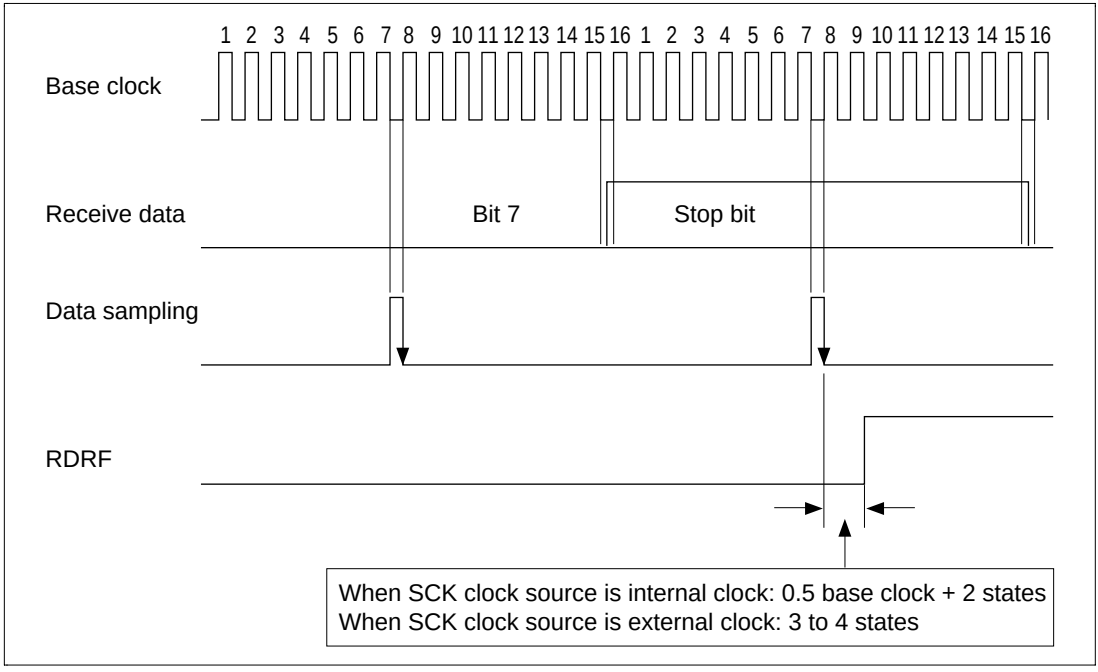
See the next page.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

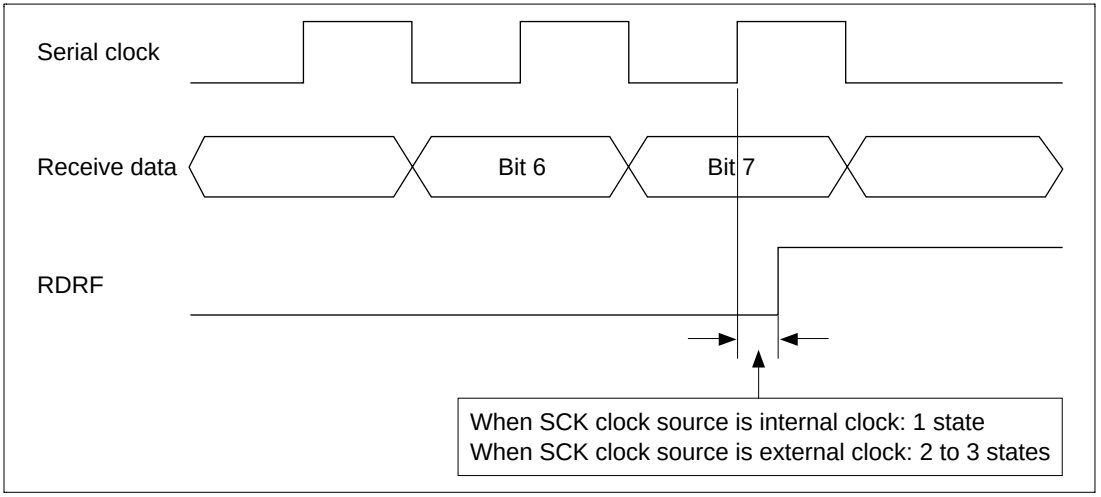
Answers

1. The RDRF flag is set following the fall of the data sampling clock after the stop bit data is received (see figure below).



With 8-Bit Data and 1 Stop Bit

2. The RDRF flag is set following the fall of the serial clock after the MSB data is received (see figure below).



In Synchronous Mode

Q&A No.: QAH8S-234

Category: SCI

Subject: Interrupt Source Flag Clearing

Question

If a receive-error interrupt is generated, and the receive error flags (ORER, FER, PER) in the serial status register (SSR) are not cleared in the interrupt handling routine before returning to the main routine, will another receive-error interrupt be generated?

Answer

Yes. As the receive error flags are not cleared to 0 automatically, another receive-error interrupt will be generated on return to the main routine (on execution of the RTE instruction).

Note: The interrupt will be generated as soon as interrupt masking is released.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-235

Category: SCI

Subject: Continuous Transmission/Reception in Synchronous Mode Using External Clock

Questions

In synchronous mode operation using an external clock:

1. If, after transmission of one data byte is completed, the external clock is input to the SCK pin before the CPU has written the next transmit data to the transmit data register (TDR), will the SCI start the next transmit operation?
2. What happens after completion of reception?
3. What will happen if the TDRE bit is cleared to 0 in the serial status register (SSR) without writing transmit data to TDR?

Answers

1. No, transmission will not be started. The next transmission is not performed until the TDRE bit is cleared to 0 in the serial status register (SSR).
2. Reception is started. However, if the RDRF bit is not cleared to 0 in SSR before reception of the next data is completed, an overrun error will occur.
3. The first time, H'FF (the initial value of TDR) will be transmitted. From the second time onward, the previous TDR value will be transmitted.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-236

Category: SCI

Subject: Use of RDR and TDR when SCI is Not Used

Questions

Can the following registers be used as data registers when the SCI is not used?

1. Receive data register (RDR)
2. Transmit data register (TDR)

Answers

1. No: as the receive data register (RDR) is a read-only register, it cannot be used as a data register.
2. Yes, the transmit data register (TDR) can be used as a data register.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-237

Category: SCI

Subject: SCI Clock Pin Input/Output Setting

Question

When the SCI is used, is the input/output specification for the SCK pin made in the data direction register (DDR) for the port corresponding to that pin?

Answer

No. When the SCI is used, the SCK pin input/output specification is made with the C/$\overline{A}$ bit (communication mode bit) in the serial mode register (SMR) and bits CKE1 and CKE0 (clock enable) in the serial control register (SCR). A setting is not required in the DDR for the corresponding port.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-238

Category: SCI

Subject: Serial Internal I/O Pin States

Question

After the TxD, RxD, and SCK pins—which are multiplexed as I/O ports—were used as SCI pins, SCI operation was disabled with the serial control register (SCR) and serial mode register (SMR), and these pins were set as I/O ports.

In this case, what is the data direction register (DDR) value for each of these pins?

Answer

SCI operation does not affect the contents of I/O port data direction registers. Therefore, when the pins are used as described above, DDR will retain the values it held before the pins were set as SCI pins. The data register (DR) values are similarly retained.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-239

Category: SCI

Subject: Setting Asynchronous Mode

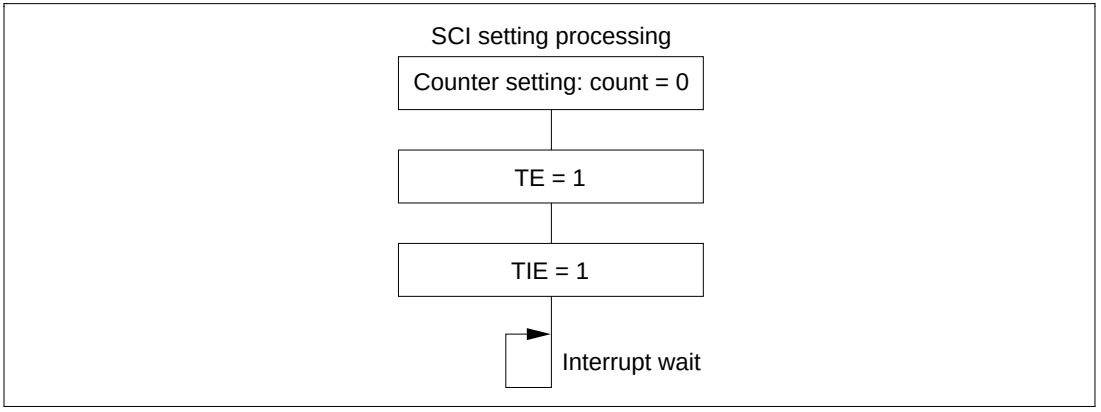
Question

When performing asynchronous mode transfer with the SCI, what is the setting procedure for performing transfer by software, without using the DMAC or DTC?

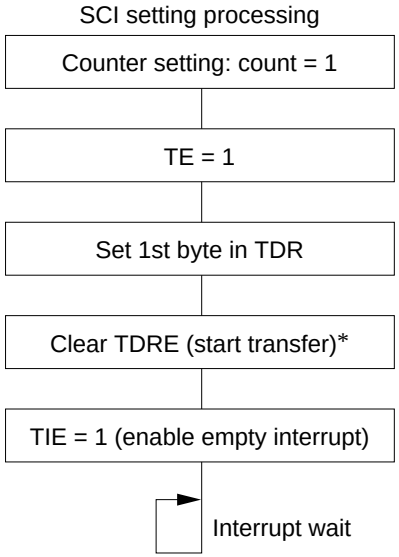
Answer

When TDRE = 1, a data-empty interrupt is always generated when TIE is set to 1. There are thus two methods, as follows.

1. Performing first byte setting in the TXI interrupt handling routine



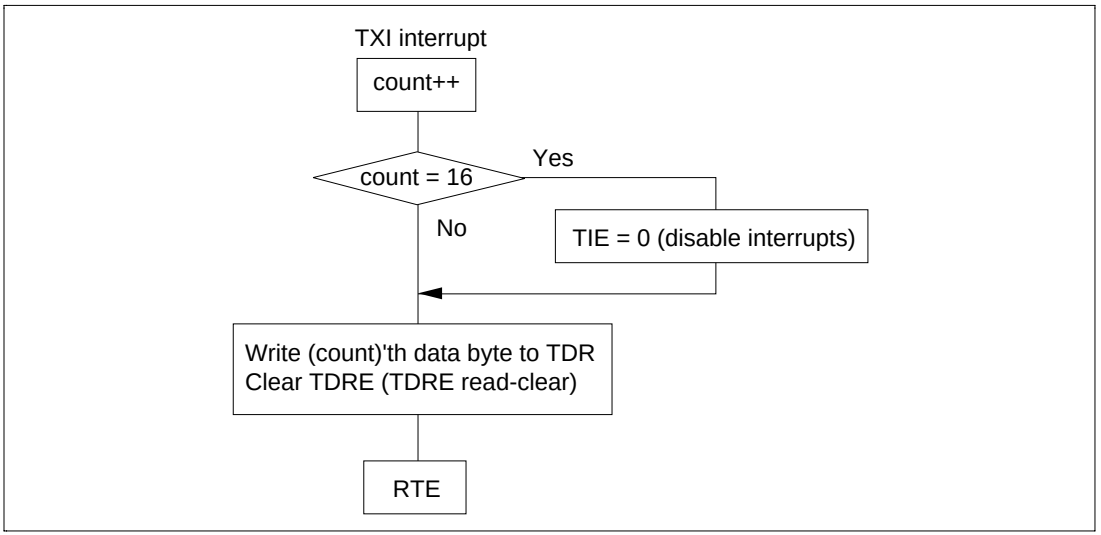
2. Performing first byte setting at the same time as SCI setting



As 1st data byte is stored in TDR by software, counter is set to 1.

Note: * After the data is transferred from TDR to TSR, TDRE is set to 1.

In both of the above cases, the TXI interrupt handling routine flowchart is as shown below.



Applicable Products

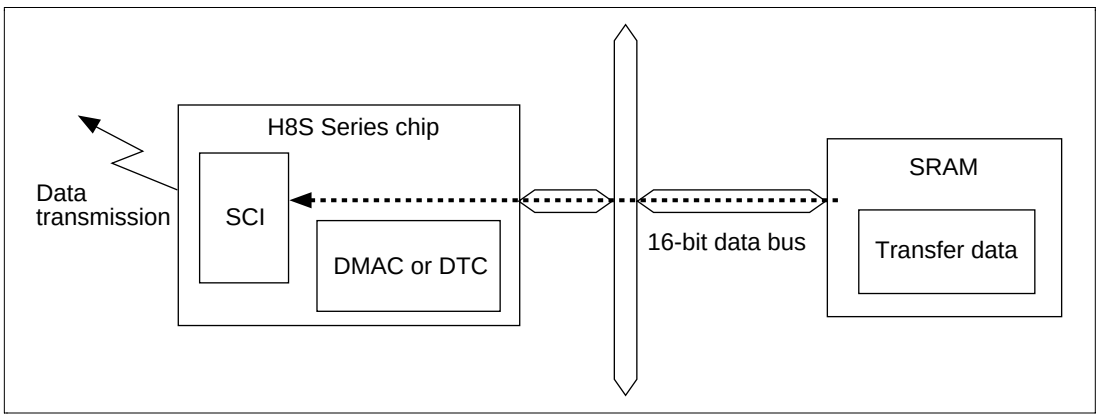
Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-240

Category: SCI

Subject: Data Transfer to TDR

Questions



To transfer data in 16-bit-access space* to the SCI transmit data register (TDR: 8 bits long), as shown above:

1. Is there any way of performing the transfer by software?
2. Is there any way of performing the transfer with the DMAC?

Note: * The H8S/2138, H8S/2134, H8S/2128, and H8S/2124 Series have only 8-bit-access space.

Answers

1. Transfer by software

   Byte access can also be used in 16-bit-access space. Read the transfer data in SRAM one byte at a time, and transfer it to the SCI's TDR (using the MOV.B instruction).
2. Transfer using DMAC or DTC

   Designate the TXI interrupt as the DMAC or DTC activation source, set the data size as byte, and transfer the transfer data in SRAM to the SCI's TDR one byte at a time. (Word-size transfer is not possible, since the DMAC or DTC is activated each time one byte is transmitted.)

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-241

Category: SCI

Subject: TDRE Flag Set Timing

Questions

When data transmission ends, the TDRE flag is set to 1 in the serial status register (SSR).

1. What is the timing for TDRE flag setting in asynchronous mode?
2. What is the timing for TDRE flag setting in synchronous mode?

Answers

See the next page.

Applicable Products

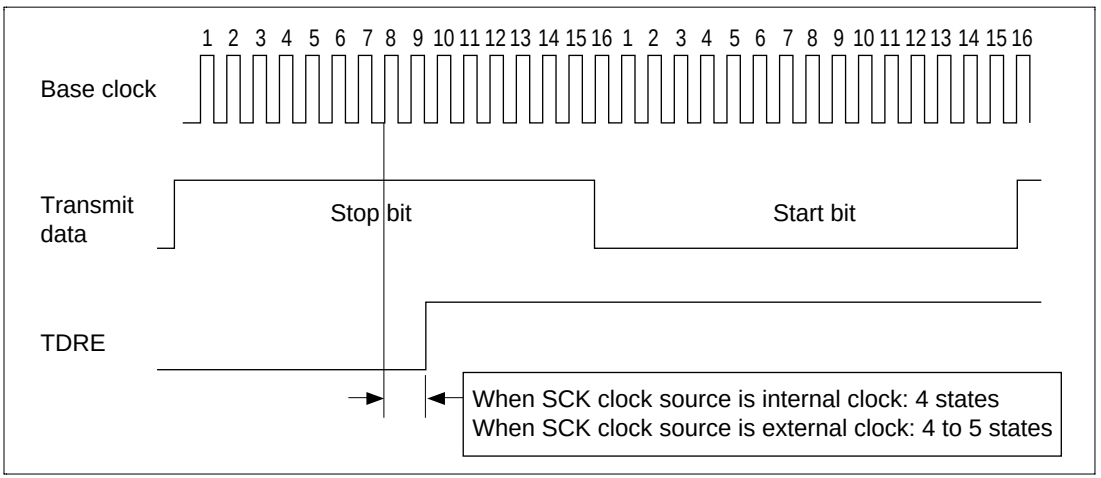
Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Answers

The TDRE set timing differs depending on whether or not the transmit shift register (TSR) contains transmit data.

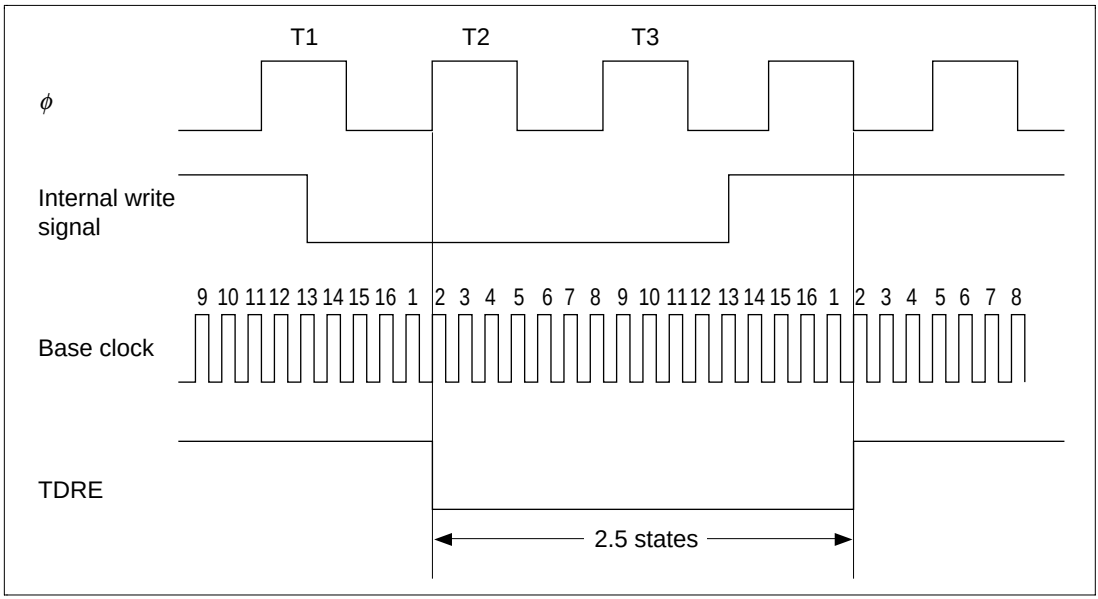
1. Asynchronous mode

   a. When TSR contains transmit data (see figure below)



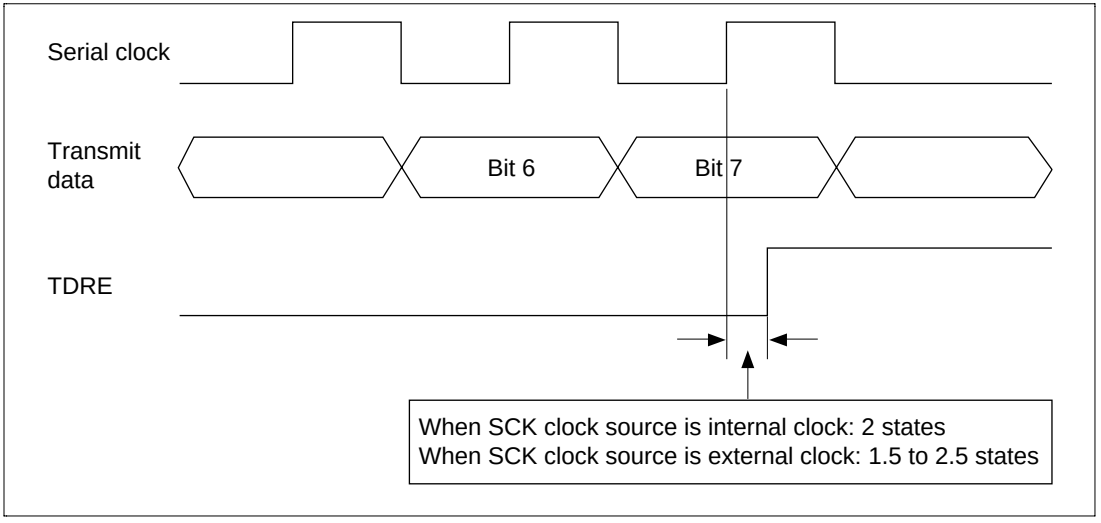
This timing also applies when transmission is started by setting the TE (transmit enable) bit.

b. When TSR does not contain transmit data (see figure below)

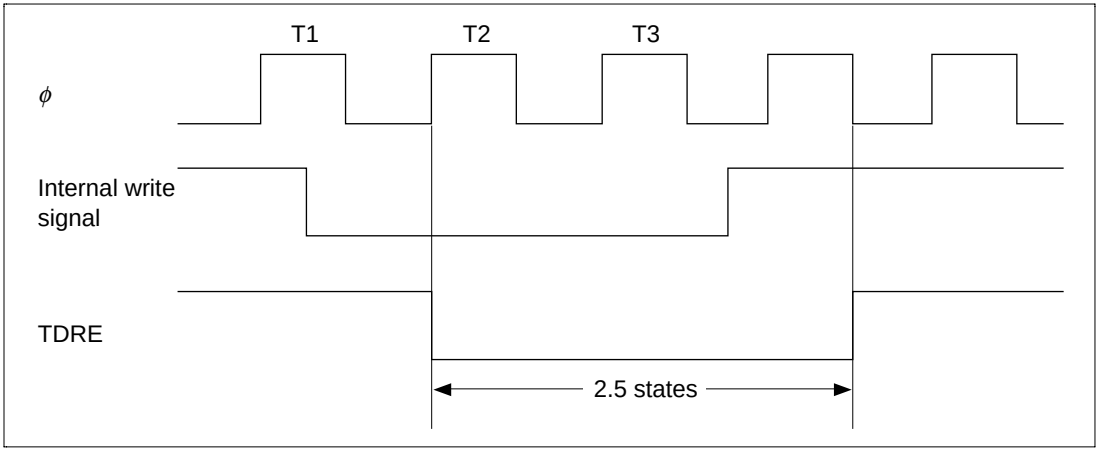


2. Synchronous mode

a. When TSR contains transmit data (see figure below)



b. When TSR does not contain transmit data (see figure below)



Q&A No.: QAH8S-242

Category: SCI

Subject: Phases of System Clock and SCK

Question

Is SCK (the serial clock transfer clock) output in synchronization with the rise or fall of ϕ (the system clock)?

Answer

The SCK signal is output in synchronization with the fall of ϕ.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-243

Category: A/D Converter

Subject: Idea Behind External C and R

Question

What is the idea behind the connection of a signal source impedance (tap resistance, etc.) and low-pass filter to the A/D converter input pins?

Answer

The ideas behind these connections are as follows.

- Permissible signal source impedance

  The analog inputs of H8S Series chips are designed so that conversion accuracy is guaranteed for an input signal with a permissible signal source impedance, R_{out}, of 5 kΩ or less (when ϕ > 12 MHz).

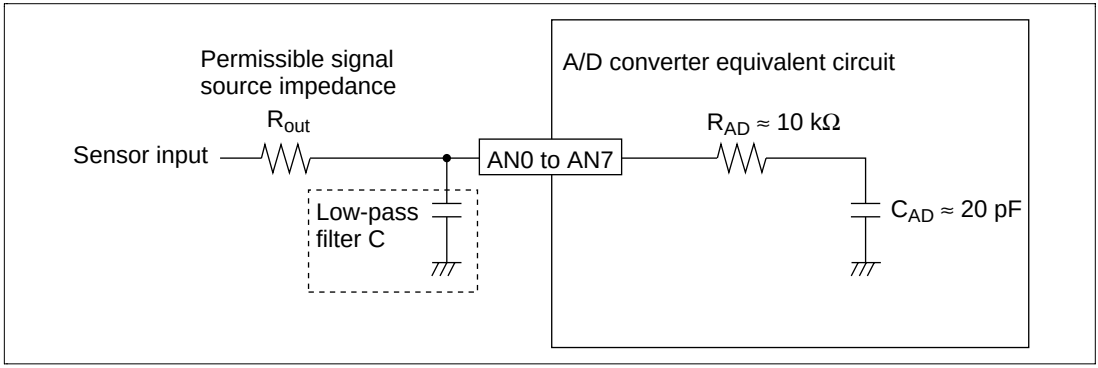
  The figure below shows an equivalent circuit of the analog input circuit. In order for A/D converter to be performed correctly, internal capacitance C_{AD} must be charged within the sampling period, t_{SPL}.

  Charge time constant τ is expressed as $\tau = C_{AD} \times (R_{out} + R_{AD})$, so that, for a permissible conversion error of ±4 LSB, for example, the calculation is as follows:

  $$V_{CC} \times 1020/1024 > V_{CC} \times (1\text{-}\exp(-t_{SPL}/\tau))$$
  $$\therefore\ t_{SPL} > 5.6 \times \tau = 5.6 \times C_{AD} \times (R_{out} + R_{AD})$$

  If t_{SPL} = 2 µs (ϕ = 16 MHz, CKS = 1), C_{AD} = 20 pF and R_{AD} = 10 kΩ; thus:

  $$\tau < 360 \text{ ns}$$
  $$\therefore\ R_{out} < 8 \text{ k}\Omega$$



Example of Analog Input Circuit

- Low-pass filter

  Adding a large capacitance (up to 0.1 µF or so) to the input pins makes sensor output impedance R_{out} essentially negligible in single-mode conversion.

  When scan mode is used, however, the internal capacitance must be charged in a short time, and so error may arise.

  Therefore, if permissible signal source impedance R_{out} exceeds 5 kΩ and a low-pass filter is added, use of single mode is recommended, with the following times set for conversion cycle T_{int}.

  T_{int} > 2 ms (100 kΩ ≥ R_{out} > 5 kΩ)

  T_{int} > 4 ms (200 kΩ ≥ R_{out} > 100 kΩ)

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-244

Category: A/D Converter

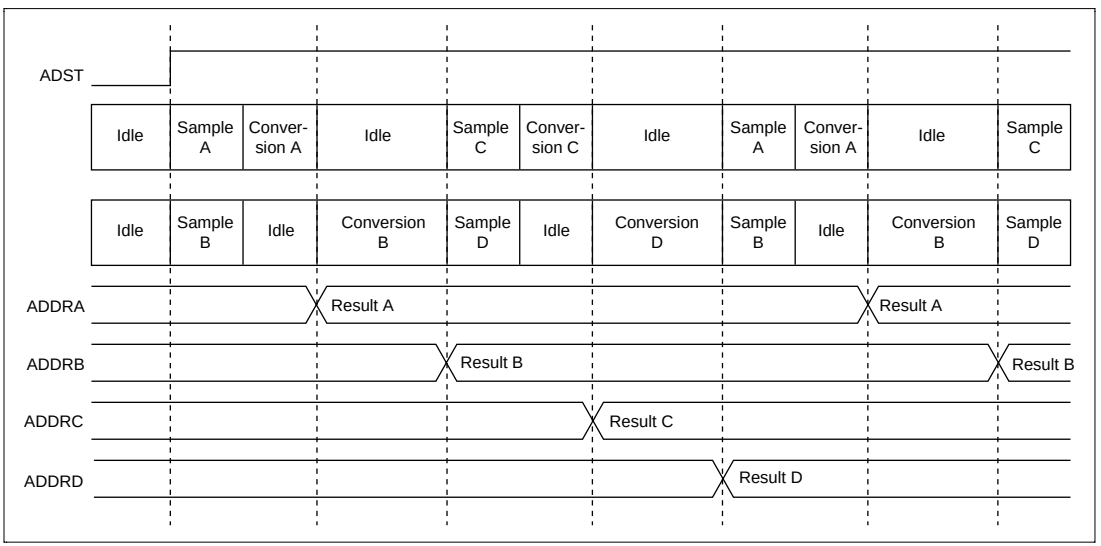
Subject: A/D Conversion in Simultaneous Sampling Operation

Question

How does A/D conversion operate with group scan mode simultaneous sampling?

Answer

An example of A/D conversion operation with group scan mode simultaneous sampling is shown below.



Example of Group Scan Mode Simultaneous Sampling Operation

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-245

Category: A/D Converter

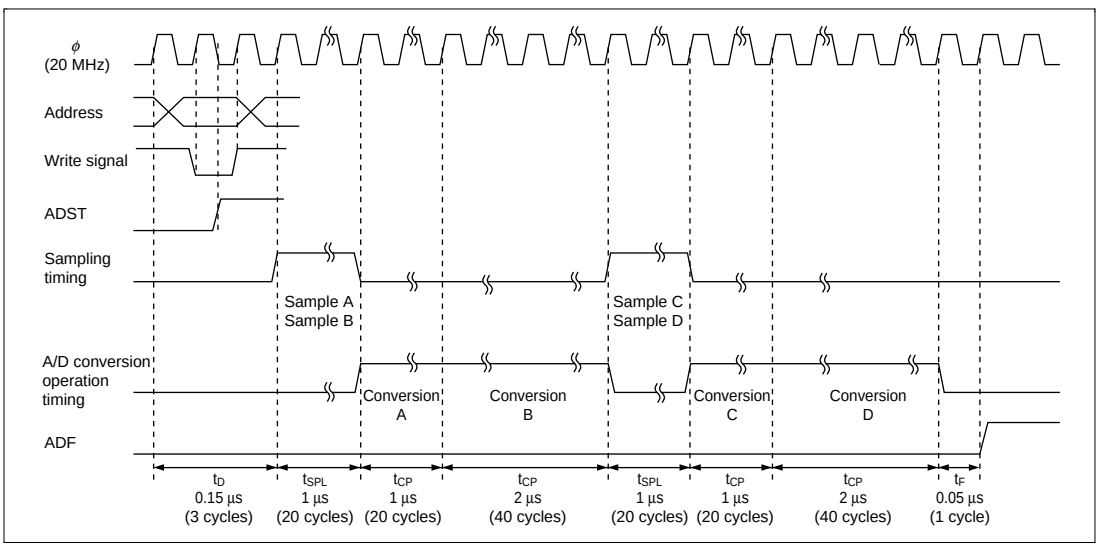
Subject: A/D Conversion Time in Simultaneous Sampling Operation

Question

What is the A/D conversion time in simultaneous sampling operation?

Answer

The conversion time is normally 1 µs, but with simultaneous sampling, as shown in the figure below, the conversion time for even-numbered conversions (B and D) is twice that for odd-numbered conversions (A and C). The conversion time is thus 1 µs for even-numbered conversions and 2 µs for odd-numbered conversions.



A/D Conversion Times in Simultaneous Sampling Operation

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-246

Category: I/O Ports

Subject: I/O Port Manipulation

Question

When a particular bit of an I/O port is specified as an output port, can a bit-manipulation instruction be executed on that port?

Answer

Yes. The port data registers (DRs) can be read or written to at any time, and can be manipulated with bit-manipulation instructions.

The data direction registers (DDRs) are write-only registers, and so cannot be manipulated with bit-manipulation instructions.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-247

Category: I/O Ports

Subject: Reserved Bits

Question

Write data rules are sometimes given for reserved bits in internal I/O registers. Is there any problem with writing data other than that prescribed to these reserved bits?

Answer

Only the data prescribed in the manual should be written, otherwise correct operation is not guaranteed. For example, the ICE and the production chip may operate differently.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-248

Category: I/O Ports

Subject: Disabling ϕ Output

Question

Is there any way of fixing ϕ output high in normal operation?

Answer

Yes. To fix ϕ output high, set the PSTOP bit to 1 in the system clock control register (SCKCR) (see table below). Also, ϕ output can be disabled by clearing the corresponding port data direction register (DDR) bit to 0, designating input port operation.

Disabling or fixing ϕ output is effective in reducing peripheral noise, current dissipation, etc.

ϕ Pin States in Each Processing State

DDR	0	1	
PSTOP	**—**	**0**	**1**
Hardware standby mode	High impedance	High impedance	High impedance
Software standby mode	High impedance	Fixed high	Fixed high
Sleep mode	High impedance	ϕ output	Fixed high
Normal operating state	High impedance	ϕ output	Fixed high

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-249

Category: I/O Ports

Subject: Port 3 Open-Drain Output

Question

Port 3 pins are multiplexed as SCI0 and SCI1 input/output pins. Can port 3 pins be used as open-drain outputs only when the I/O port function is used, or also when the SCI output pin function is used?

Answer

Open-drain output is also possible when port 3 pins are used as SCI output pins.

In both I/O port operation and SCI output pin operation, open-drain output can be selected by setting port 3 open-drain control register (P3ODR) bits to 1. After making the P3ODR setting, set the relevant pins to output mode.

Note: When open-drain output is used, it is still necessary to ensure that the relevant pin levels do not exceed the input voltage range values specified in the Electrical Characteristics section.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series	Yes	H8S/2655	Yes	H8S/2350
Yes	H8S/2355	Yes	H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-250

Category: I/O Ports

Subject: Multiplexing as $\overline{\text{IRQ3}}$ and $\overline{\text{LWR}}$

Question

The PF3 pin is also multiplexed as $\overline{\text{LWR}}$ and $\overline{\text{IRQ3}}$. Can $\overline{\text{IRQ3}}$ input be used in modes 1, 2, 4, 5, and 6?

Answer

No. The PF3/$\overline{\text{LWR}}$/$\overline{\text{IRQ3}}$ pin becomes the $\overline{\text{LWR}}$ output automatically in modes 1, 2, 4, 5, and 6, and so cannot be used as the $\overline{\text{IRQ3}}$ input.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357	Yes	H8S/2345
Yes	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

Q&A No.: QAH8S-251

Category: Clock Pulse Generator

Subject: Crystal Resonator Capacitance Value

Question

Crystal resonator capacitance value C0 is given as 7 pF in the hardware manual. Can a larger capacitance be used?

Answer

The C0 value given in the hardware manual is a reference value. The C0 value will depend on the user's system, and therefore oscillation should be confirmed in with the chip in actual use.

Applicable Products

Applicability	Series	Applicability	Series	Applicability	Series
Yes	Entire H8S Series		H8S/2655		H8S/2350
	H8S/2355		H8S/2357		H8S/2345
	H8S/2245		H8S/2148		H8S/2144
	H8S/2138		H8S/2134		H8S/2128
	H8S/2124	—	—	—	—

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