YAMAHA LSI

YGV604

VSG (Video Screen Generator)

■ Outline

High level display functionality and a high speed drawing function makes VSG the ideal VDP to control consumer television display screens. A variety of graphic systems can be easily constructed, for example; video titling, OSD, education equipment, and many others.

■ Features

Display functions

• Display mode	bitmap graphics
• Display resolution	NTSC : 384 × 240 (480) 768 × 240 (480) PAL : 384 × 290 (580) 768 × 290 (580) Figure inside ( ) are for interlace display mode.
• Number of display colors	Simultaneous display of 16 colors out of 32768 by using the built-in color pallet Simultaneous 256-color display Simultaneous 32768-color display
• Scrolling function	Smooth scrolling in any direction. Image space setting by free page construction is possible. Scrolling display range setting inside image space is possible. Range setting can be anysize. Display window setting is possible.
• Cursor function	Size 32 × 32 dots 16 colors can be selected from 32768 colors for each dot unit.
• Others	Fade IN/OUT display is possible by using the color volume function Superimpose function Linear RGB output by built-in DAC

YAMAHA CORPORATION

YGV604 CATALOG
CATALOG No.: LSI-4GV6042
1993. 2

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Graphic Drawing functions

• Types of commands	Block transfer (XY coordinate specification, Linear address specification)
	Font color development
	Linear
	Boundary color coordinate detection
• Graphic Drawing attributes	Bit mask
	Logical operation (NOT, AND, OR, EOR, etc.)
	Transparent color detection
• Drawing speed	105nsec/dot Max.

Others

• Usable VRAM	Dual port DRAM (120ns)is used.
	Capacity 128kbyte (Four 64k × 4 are used.)
	256kbyte (Two 128k × 8 are used.)
	512kbyte (Four 256k × 4 are used.)
	1Mbyte (Eight 256k × 4 are used.)
• CPU interface	8-bit parallel bus
• Package	CMOS, 100-pin QFP, 5V single-power supply

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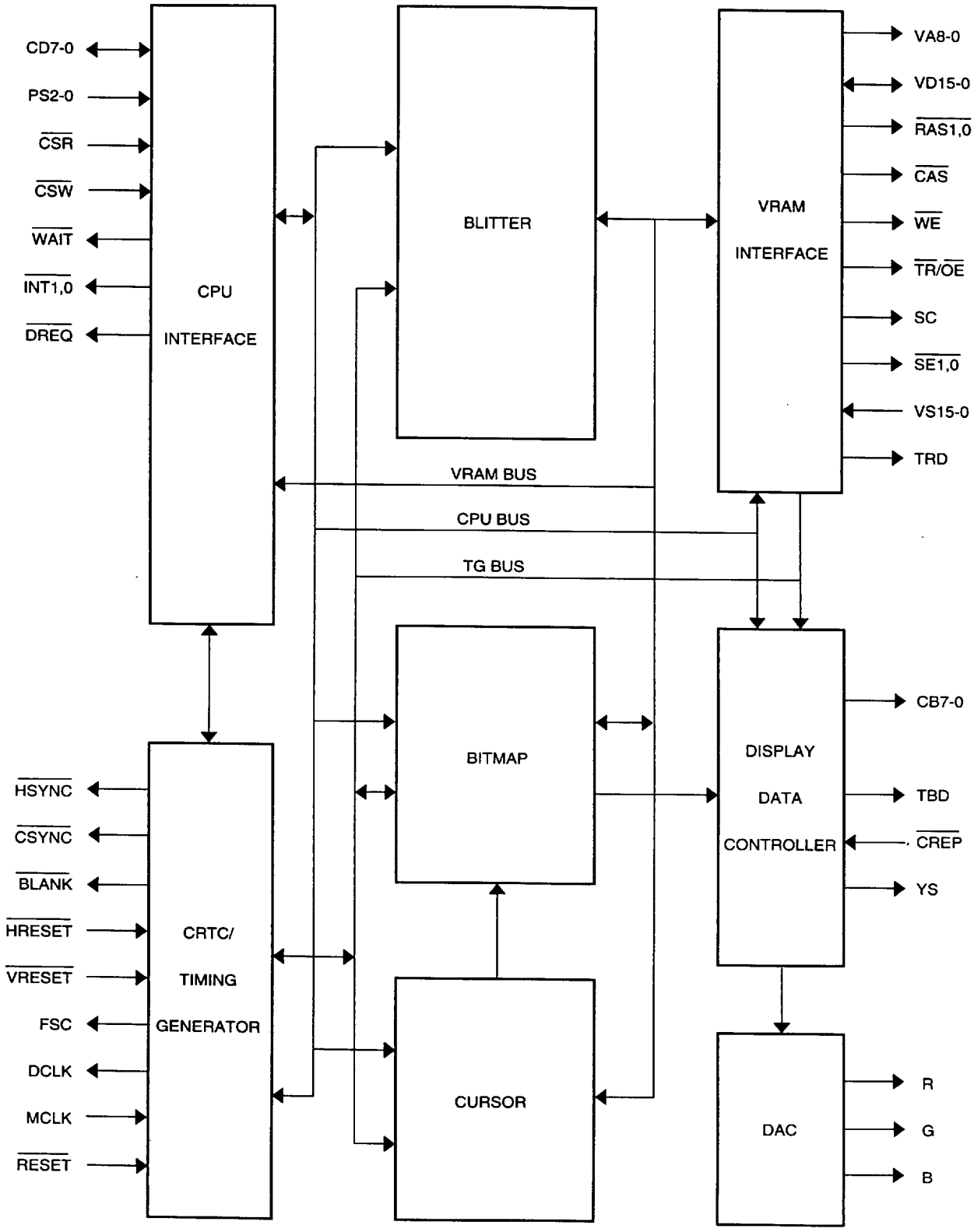
■ INTERNAL BLOCK DIAGRAM



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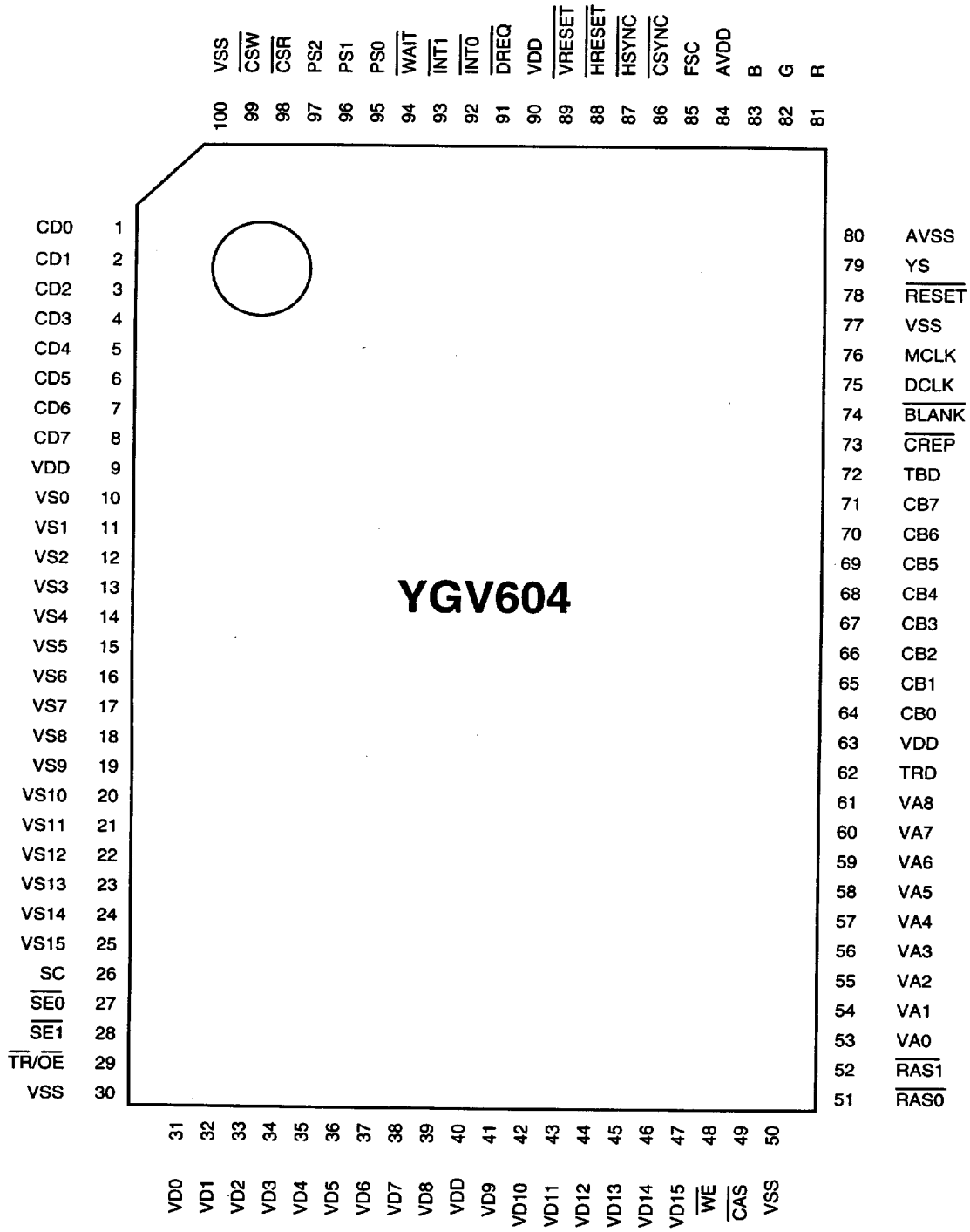
■ PIN ASSIGNMENT



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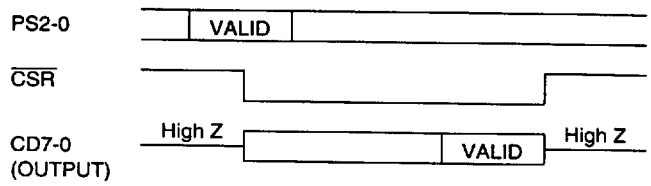
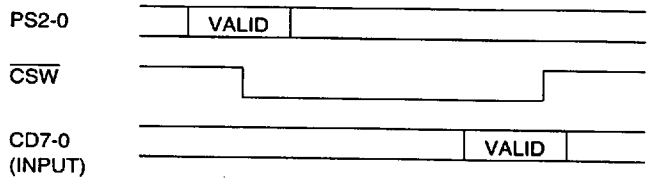
■ DESCRIPTION OF TERMINAL FUNCTIONS

1) CPU interface

- CD7-0 (I/O)
  8-bit bi-directional data bus of CPU
- PS2-0 (I)
  Input of I/O port No. address. VSG P#7~P#0 are selected.
- $\overline{CSR}$ (I)
  Input of strobing signal for data read from VSG to CPU.
- $\overline{CSW}$ (I)
  Input of strobing signal for data write from CPU to VSG.



CPU-VSG READ CYCLE



CPU-VSG WRITE CYCLE

- $\overline{WAIT}$ (O:Open drain output)
  WAIT signal output to CPU. It becomes low level until read data is prepared during $\overline{CSR}$ input, and while VSG is BUSY during $\overline{CSW}$ input.
- INT1 and $\overline{INT0}$ (O: Open drain output)
  Interruption request signal output to CPU. $\overline{INT1}$ is output at the specified display position by the internal register. $\overline{INT0}$ is output when vertical display period is completed, or when graphic drawing command is completed.
- $\overline{DREQ}$ (O: Open drain output)
  Data request signal output to CPU during graphic drawing command execution.

2) VRAM interface

- VA8-0 (O)
  VRAM row/column address output
- VD15-0 (I/O)
  Bi-directional data bus for RAM port of VRAM
- VS15-0 (I)
  VRAM data bus for serial port
- $\overline{RAS1}$, $\overline{RAS0}$ (O)
  VRAM row address strobing signal. Only $\overline{RAS0}$ is used when the VRAM capacity is within 512Kbyte and $\overline{RAS1}$ is used for VRAM with the latter 512Kbyte when the VRAM capacity is extended to 1Mbyte.
- $\overline{CAS}$ (O)
  VRAM column address strobing signal.
- $\overline{WE}$ (O)
  VRAM write strobing signal.

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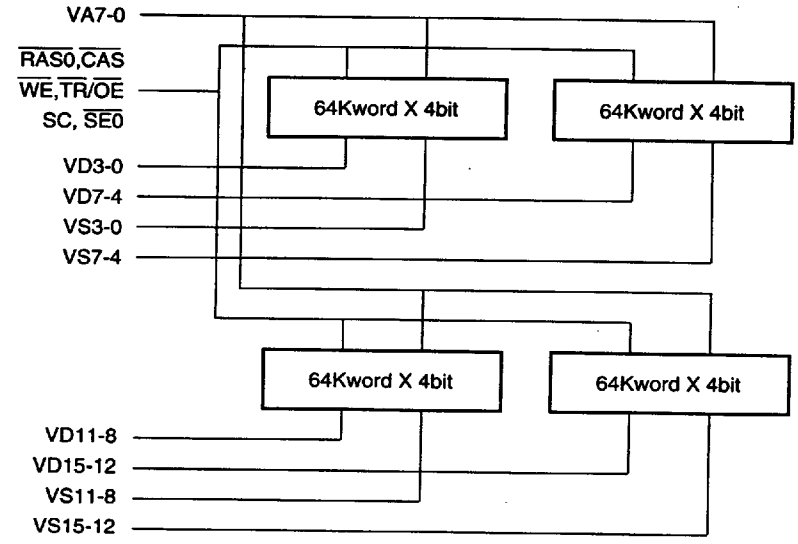
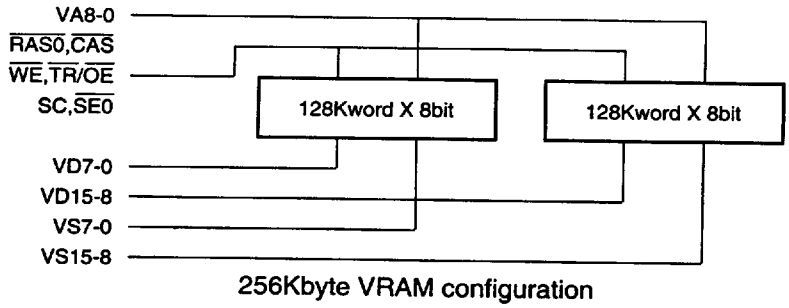
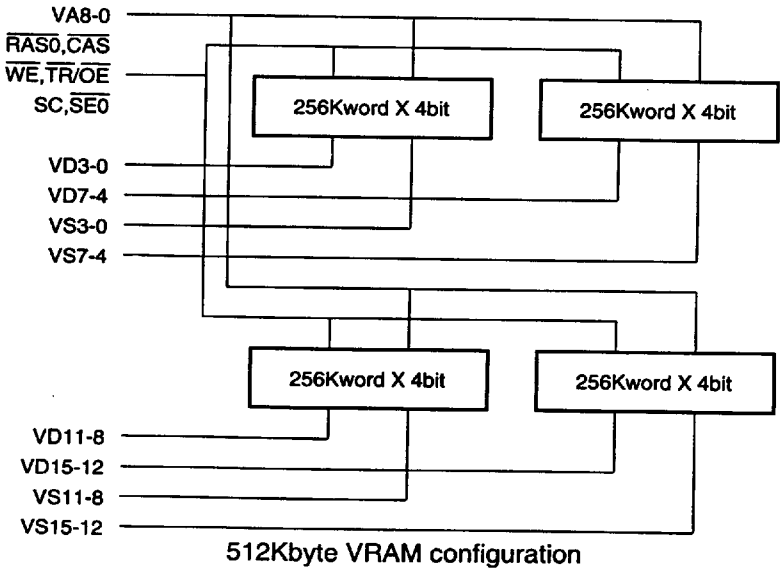
- $\overline{TR/OE}$ (O)
  VRAM data transfer control signal or the data output enable signal of RAM port.
- SC (O)
  VRAM serial clock signal.
- $\overline{SE1}$, $\overline{SE0}$ (O)
  VRAM serial port data enable signal. This is used when the VRAM capacity is extended to 1Mbyte. $\overline{SE0}$ is used for the first half 512Kbyte and $\overline{SE1}$ is used for the second half 512Kbyte.
- TRD (O)
  VRAM read transfer timing for reading bitmap screen display data



128Kbyte VRAM configuration



256Kbyte VRAM configuration



512Kbyte VRAM configuration

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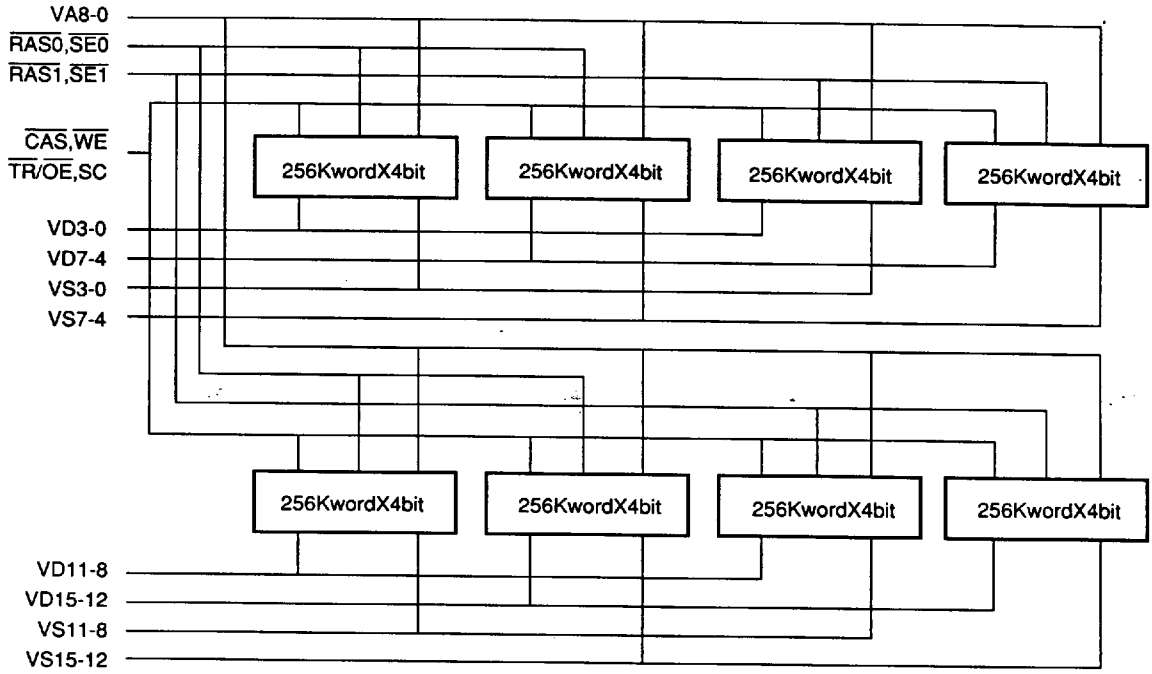
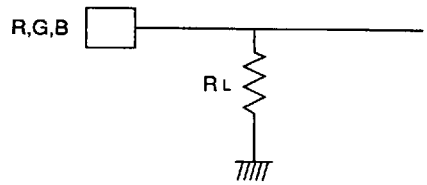


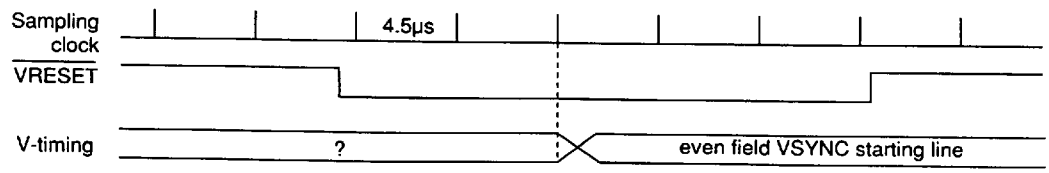
1Mbyte VRAM configuration

3) CRT interface

- R, G, B (O: analog output)
  Linear RGB output.



- YS (O)
  Superimpose timing signal. It becomes high level during VSG data display timing.
- $\overline{\text{HSYNC}}$ (O)
  Horizontal synchronous signal. Equalizing pulse is not inserted.
- $\overline{\text{CSYNC}}$ (O)
  Compound synchronous signal
- $\overline{\text{BLANK}}$ (O)
  It becomes low level during retrace line blanking interval.
- $\overline{\text{HRESET}}$ (I)
  VSG horizontal timing is set to horizontal synchronous position when this signal is falling, and L mode dot clock phase is locked.
- $\overline{\text{VRESET}}$ (I)
  VSG vertical timing is set to the vertical synchronous starting position of the even number field, when this signal is sampled by the cycle clock at approx. 4.5µsec, and when it becomes low level three times in succession.



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- FSC (O)

  Sub-carrier clock signal of NTSC. 1/4 of the clock frequency input to terminal MCLK is output.

4) Others

- CB7-0 (O)

  Color bus signal. It is output synchronizing with the clock of terminal DCLK. It is output in the same timing with RGB output. The data contents are shown below:

When 4bit/dot

	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	sampling timing
BITMAP timing	AT3	AT2	AT1	AT0	CC3	CC2	CC1	CC0	DCLK ↑
CURSOR timing	AT3	AT2	AT1	AT0	CS3	CS2	CS1	CS0	DCLK ↑
BACKDROP timing	AT3	AT2	AT1	AT0	BC3	BC2	BC1	BC0	DCLK ↑

When 8bit/dot

	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	sampling timing
BITMAP timing	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	DCLK ↑
CURSOR timing	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	DCLK ↑
BACKDROP timing	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	DCLK ↑

When 16bit/dot

	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	sampling timing
BITMAP timing	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	DCLK ↑
	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	DCLK ↓
CURSOR timing (Palette:CS3-0)	R2	R1	R0	B4	B3	B2	B1	B0	DCLK ↑
	AT0	G4	G3	G2	G1	G0	R4	R3	DCLK ↓
BACKDROP timing (Palette:BC3-0)	R2	R1	R0	B4	B3	B2	B1	B0	DCLK ↑
	AT0	G4	G3	G2	G1	G0	R4	R3	DCLK ↓

CC15-0: BITMAP color code CS3-0: CURSOR color code CS7-4: CURSOR COLOR REGISTER
BC7-0: BACKDROP COLOR REGISTER G4-0, R4-0, B4-0, AT3-0: COLOR PALETTE data

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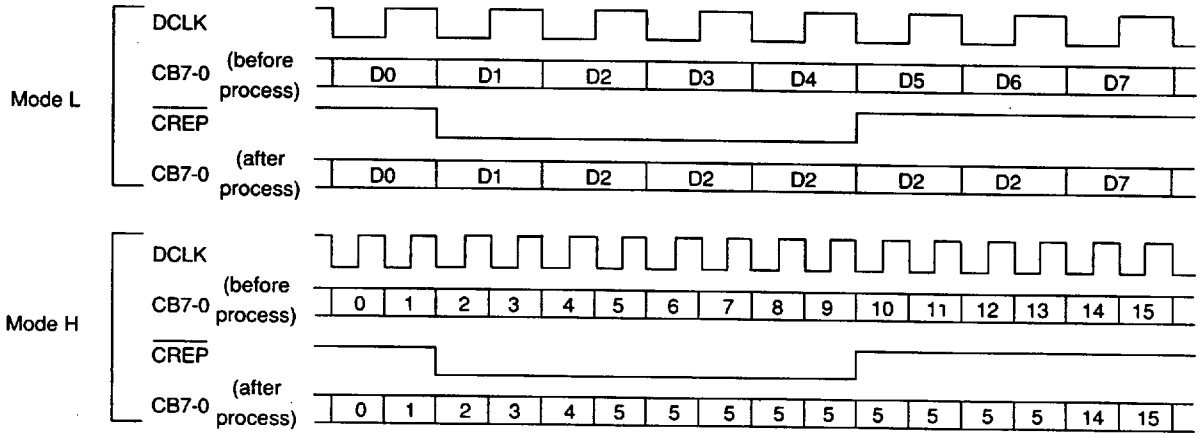
- $\overline{\text{CREP}}$ (I)

  Color repeat timing signal which controls the display data of the bitmap screen. When it is low level, the previous dot data is displayed repeatedly. This is input before 2 dots (4 dots for mode H) at the color bus signal clock rate, synchronizing with the clock of terminal DCLK.



- TBD (O)

  Back drop display timing signal. This is output synchronizing with the clock of terminal DCLK.

- DCLK (O)

  Dot clock signal. The 1/2 frequency clock of the terminal MCLK is output during mode L, and the clock with the same frequency as that of terminal MCLK is output during mode H.

- MCLK (I)

  VSG main clock input

- $\overline{\text{RESET}}$ (I)

  Power on reset input. VSG is initialized during low level.

- AVDD, AVSS (I)

  Analog power supply for RGB.

- VDD, VSS (I)

  Digital power supply

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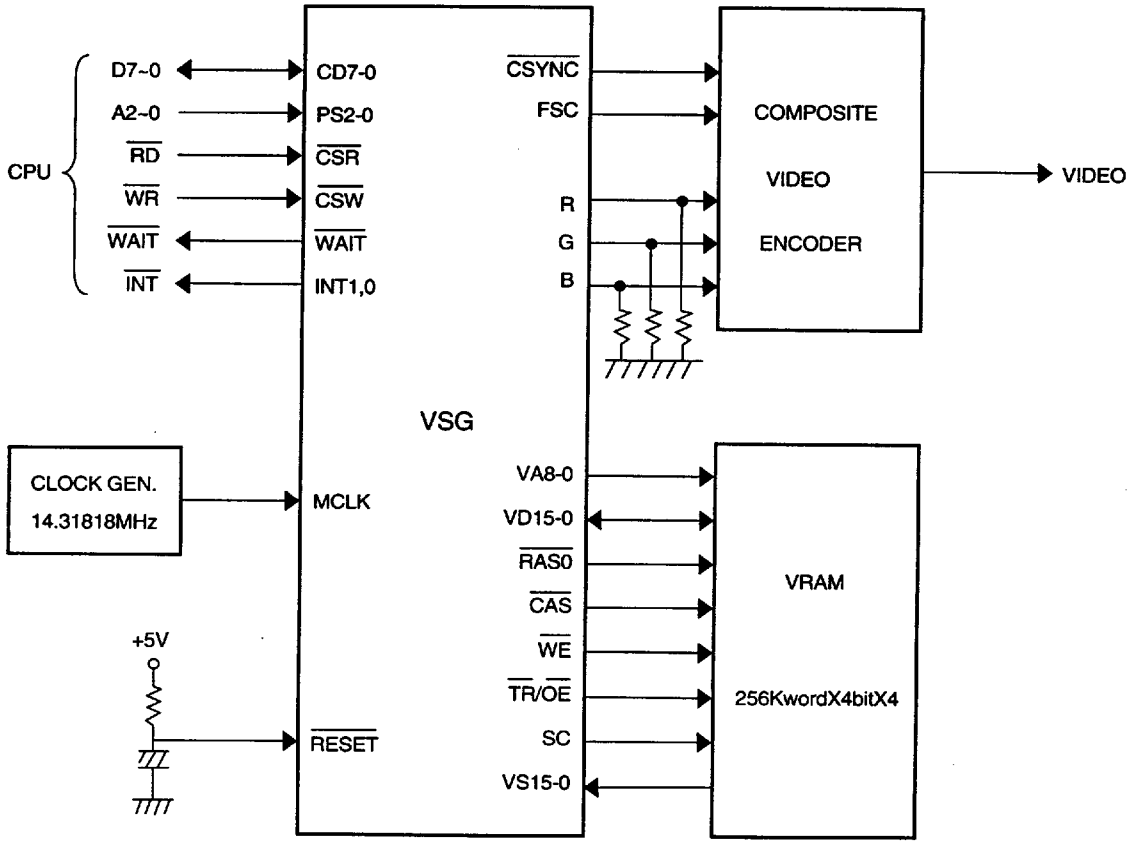
■ EXAMPLE OF SYSTEM CONFIGURATION



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■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	− 0.5 ~ + 7.0	V
Input terminal voltage	V_I	− 0.5 ~ V_{DD} + 0.5	V
Output terminal voltage	V_O	− 0.5 ~ V_{DD} + 0.5	V
Output terminal current	I_O	− 20 ~ + 20	mA
Storage temperature	T_{STG}	− 50 ~ + 125	°C

● Recommended Operating Conditions

Symbol	Item	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	4.75	5.00	5.25	V
V_{SS}	Supply voltage		0		V
V_{IL}	Low-level input voltage	− 0.3		0.8	V
V_{IH}	High-level input voltage	2.0		V_{DD}	V
T_{OP}	Operating temperature	0		70	°C

● Electrical Characteristics under the Recommended Operating Conditions

- DC characteristics

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	High-level output voltage (OPEN DRAIN terminal is excluded.)	I_{OH} = −1.0mA	3.0			V
I_{LI}	Input leak current				10	µA
I_{LO}	Output leak current				25	µA
I_{DD}	Power consumption			70		mA

- Terminal capacity

Symbol	Item	Min.	Typ.	Max.	Unit
C_I	Input terminal capacity			8	pF
C_O	Output terminal capacity			10	
C_{IO}	Input/Output terminal capacity			12	

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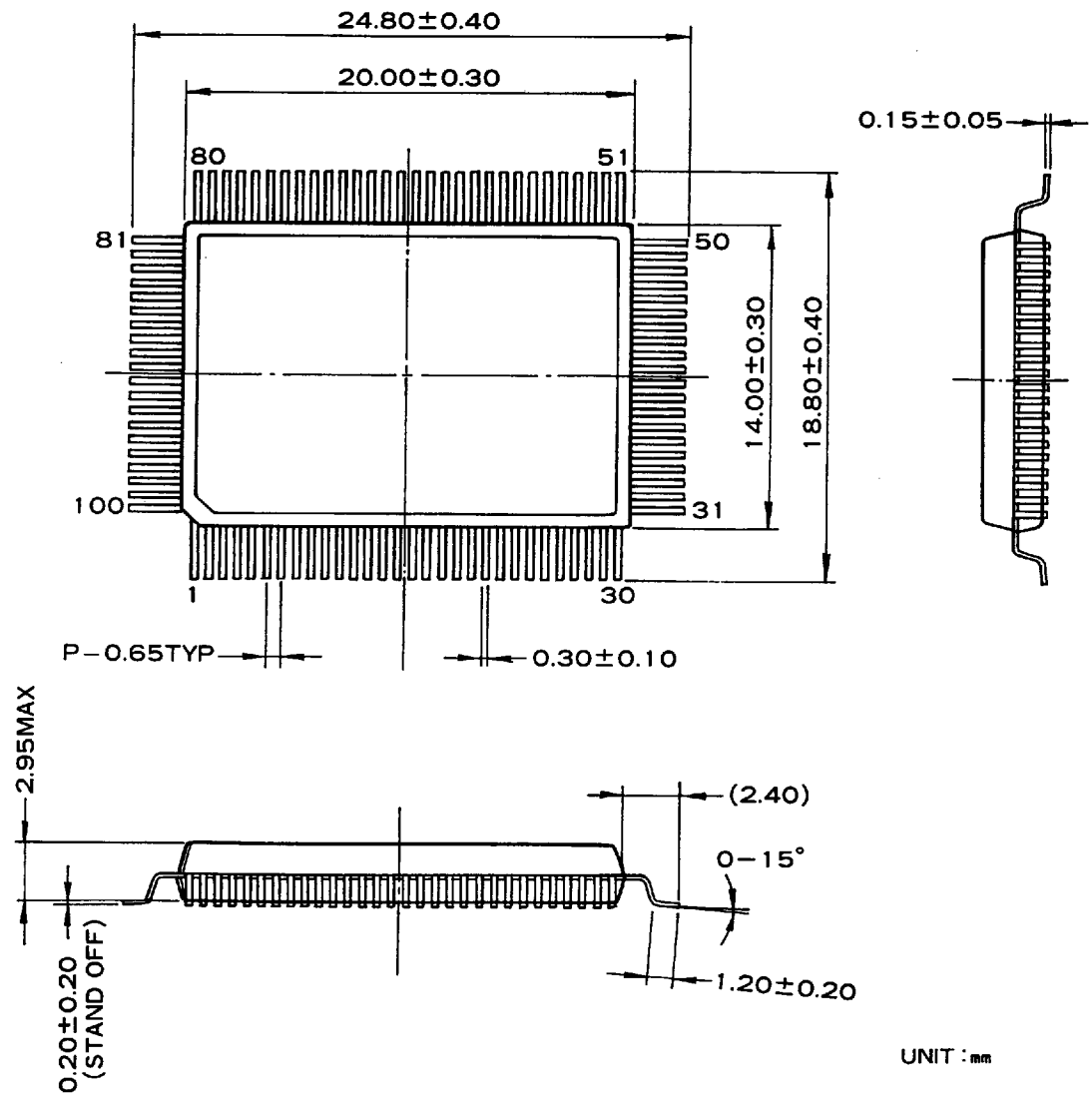
■ EXTERNAL DIAGRAM OF THE PACKAGE



The specifications of this product are subject to improvement changes without prior notice.

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