Fast CMOS Buffer/Clock Driver

Product Features:

- Extremely low output skew: –0.7ns.
- Monitor output pin
- Clock busing with 3-state control
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive, I_{OL} = 64 mA
- Extremely low static power (1 mW, typ.)
- Hysteresis on all inputs
- Packaged in 20-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

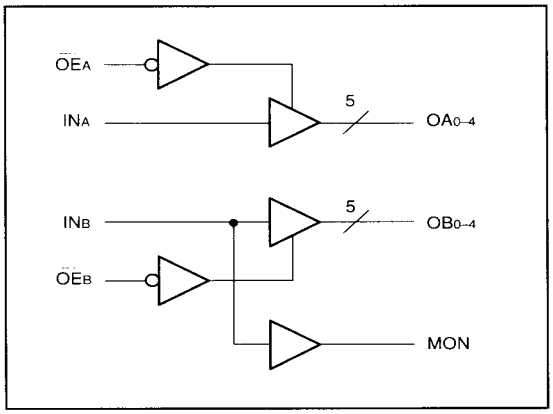
Product Description:

Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

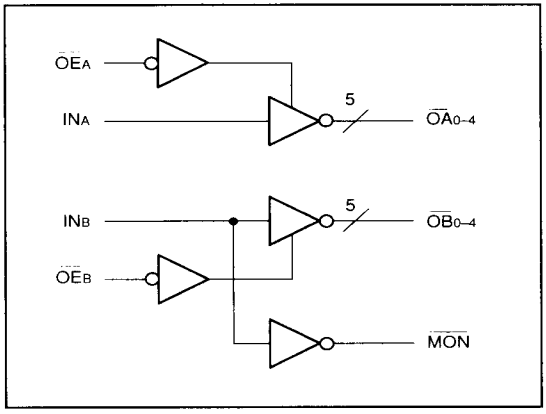
The PI49FCT805T is a non-inverting clock driver and the PI49FCT806T is an inverting clock driver designed with two independent groups of buffers. These buffers have 3-state Output Enable inputs (active LOW) with a 1-in, 5-out configuration per group. Each clock driver consists of two banks of drivers, driving five outputs each from a standard TTL compatible CMOS input.

These products are available in three package types: 20-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

PI49FCT805T Logic Block Diagram



PI49FCT806T Logic Block Diagram



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Product Pin Description

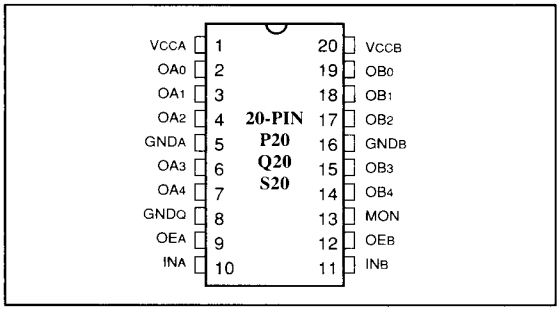
Pin Name	Description
OE_A, $\overline{OE_B}$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_N, OB_N	Clock Outputs
MON	Monitor Output
GND	Ground
V_{CC}	Power

PI49FCT805T Truth Table[1]

Inputs		Outputs	
OE_A, OE_B	IN_A, IN_B	OA_N, OB_N	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE: 1. H = High Voltage Level, L = Low Voltage Level, Z = High Impedance

PI49FCT805T Product Pin Configuration

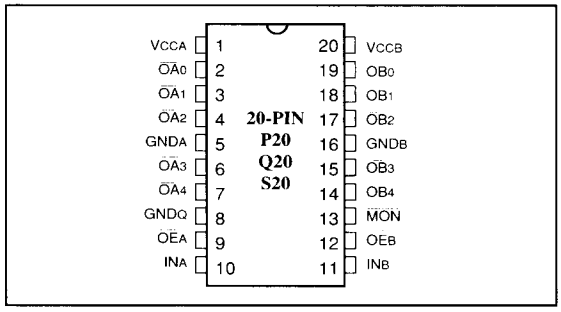


PI49FCT806T Truth Table[1]

Inputs		Outputs	
OE_A, $\overline{OE_B}$	IN_A, IN_B	$\overline{OA_N}$, $\overline{OB_N}$	$\overline{MON}$
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

NOTE: 1. H = High Voltage Level, L = Low Voltage Level, Z = High Impedance

PI49FCT806T Product Pin Configuration



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.3	0.55	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–5	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = V_{CC}			+10	µA
I_{OZL}	Output Current		V_{OUT} = GND			–10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120	–225	mA
V_H	Input Hysteresis	V_{CC} = 5 V			200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

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Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.2	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4 V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10 MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Five Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND		7.7	14.0[5]	mA
			V_{IN} = 3.4 V V_{IN} = GND		8.0	15.0[5]	
		V_{CC} = Max., Outputs Open f_i = 2.5 MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND		4.3	8.4[5]	
			V_{IN} = 3.4 V V_{IN} = GND		4.8	10.4[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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PI49FCT805/806T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	805T/806T Com. Min	805T/806T Com. Max	805AT/806AT Com. Min	805AT/806AT Com. Max	805BT/806BT Com. Min	805BT/806BT Com. Max	805CT/806CT Com. Min	805CT/806CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_N, IN_B to OB_N	$Z_O = 50\Omega$ with Thevenin	1.5	6.5	1.5	5.8	1.5	5.2	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE_A}$ to OA_N, $\overline{OE_B}$ to OB_N	termination (See Figure c)	1.5	8.0	1.5	8.0	1.5	8.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE_A}$ to OA_N, $\overline{OE_B}$ to OB_N	$t \leq 100MHz$ Outputs	1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	ns
$t_{SKEW(O)}$[3]	Skew between two outputs of same package (same transition)	gauged in groups of two	—	0.7	—	0.7	—	0.7	—	0.5	ns
$t_{SKEW(t)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of the same output		—	1.0	—	0.7	—	0.7	—	0.5	ns
$t_{SKEW(p)}$[3]	Skew between two outputs of different package at same temperature (same transition)		—	1.5	—	1.0	—	1.0	—	0.7	ns

Parameters	Description	Conditions[1]	805T/806T Com. Min	805T/806T Com. Max	805AT/806AT Com. Min	805AT/806AT Com. Max	805BT/806BT Com. Min	805BT/806BT Com. Max	805CT/806CT Com. Min	805CT/806CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_N, IN_B to OB_N	$C_L = 30$ pF $t \leq 67MHz$	1.5	6.5	1.5	5.8	1.5	5.2	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE_A}$ to OA_N, $\overline{OE_B}$ to OB_N	(See Figure b)	1.5	8.0	1.5	8.0	1.5	6.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE_A}$ to OA_N, $\overline{OE_B}$ to OB_N		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	ns
$t_{SKEW(O)}$[3]	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	—	0.7	—	0.5	ns
$t_{SKEW(t)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of the same output		—	1.0	—	0.7	—	0.7	—	0.5	ns
$t_{SKEW(p)}$[3]	Skew between two outputs of different package at same temperature (same transition)		—	1.5	—	1.0	—	1.0	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measuresd at worse cast temperature (max. temp).

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PI49FCT805/806T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	805T/806T Com.		805AT/806AT Com.		805BT/806BT Com.		805CT/806CT Com.		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_N, IN_B to OB_N	$Z_O = 50\Omega$ with Thevenin	1.5	6.5	1.5	5.8	1.5	5.2	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE_A}$ to OA_N, $\overline{OE_B}$ to OB_N	termination (See Figure c)	1.5	8.0	1.5	8.0	1.5	8.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE_A}$ to OA_N, $\overline{OE_B}$ to OB_N	$t \leq 100MHz$ Outputs	1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	ns
$t_{SKEW(O)}$[3]	Skew between two outputs of same package (same transition)	gauged in groups of two	—	0.7	—	0.7	—	0.7	—	0.5	ns
$t_{SKEW(t)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of the same output		—	1.0	—	0.7	—	0.7	—	0.5	ns
$t_{SKEW(p)}$[3]	Skew between two outputs of different package at same temperature (same transition)		—	1.5	—	1.0	—	1.0	—	0.7	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measuresd at worse cast temperature (max. temp).

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Tests Circuits and Waveforms

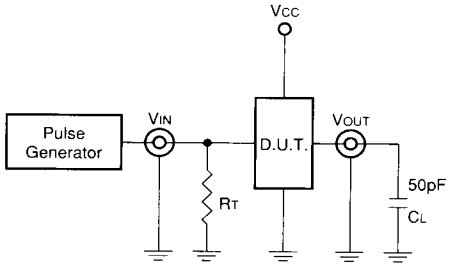

Figure a

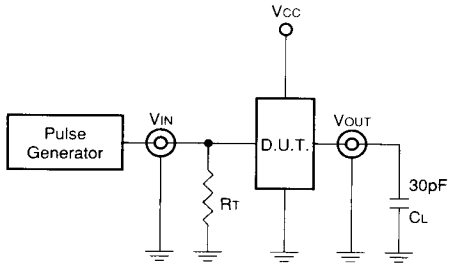

Figure b

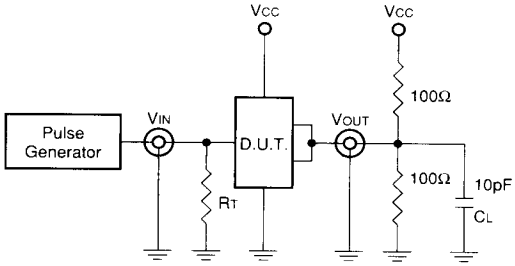

Figure c

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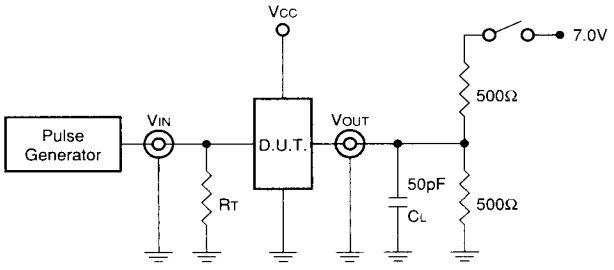
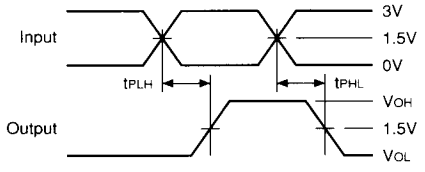
Tests Circuits and Waveforms (Continued)

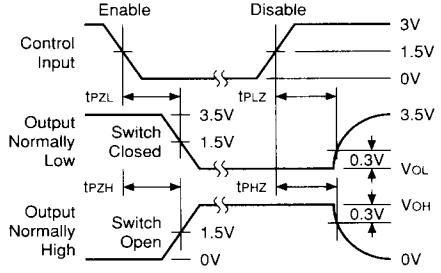
Tests Circuits For All Outputs(1)



Propagation Delay



Enable and Disable Times(2)

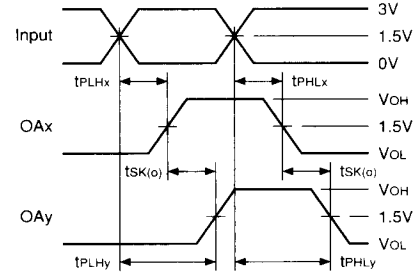


Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

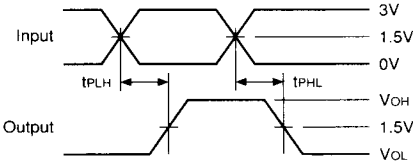
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

Output Skew – tSK(o)



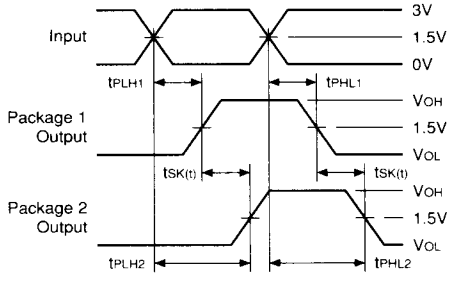
$$t_{SK(o)} = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

Pulse Skew – tSK(p)



$$t_{SK(p)} = |t_{PHL} - t_{PLH}|$$

Package Skew – tSK(t)



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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