Freescale Semiconductor
Data Sheet: Product Preview

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MPC5744P Data Sheet

32-bit Qorivva MCU suitable for ISO26262 ASIL-D chassis and safety applications

The MPC5744P Qorivva microcontroller is based on the Power Architecture® developed by Freescale. It targets chassis and safety applications and other applications requiring a high Automotive Safety Integrity Level (ASIL). The MPC5744P is a SafeAssure solution.

This document provides electrical specifications, pin assignments, and package diagram information for the MPC5744P series of microcontroller units (MCUs). All information is preliminary and subject to change without notice. For functional characteristics and the programming model, see the *MPC5744P Microcontroller Reference Manual*.

Table of Contents

1 Introduction

1.1 Feature list

Table 1 summarizes major features of the MPC5744P device. The feature column represents a combination of module names and capabilities of certain modules.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution Speed	0 MHz to TBD (design target: 180 MHz or greater) (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory	
Code/data flash memory	**2.5 MB**, ECC, RWW
Data flash memory	Supported with RWW
SRAM	**384 KB**, ECC
Modules	
Interrupt controller	32 interrupt priority levels, 16 software programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel

Table 1. MPC5744P feature summary (continued)

Feature	Details
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules
Clockout	Yes
Fault Collection and Control Unit (FCCU)	Yes
Cross Triggering Unit (CTU)	2 modules
eTimer	3 modules with 6 channels
FlexPWM	2 modules with 4 x (2+1) channels
Analog-to-digital converter (ADC)	4 modules with 12 bit ADC, (25 external channels including shared channels plus internal channels)
Sine-wave generator (SWG)	32 point
DSPI	4 modules As many as 8 chip selects
CRC Unit	Yes
SENT	2 modules with 2 channels
Interprocessor serial link interface (SIPI)	Yes
Junction temperature sensor	Yes Replicated module
Digital I/Os	>= 16
Peripheral register protection	Yes
Supply	
Device Power Supply	3.3 V with external ballast transistor or 3.3 V with external 1.25 V low drop-out (LDO) regulator
ADC Analog Reference voltage	3.15 V to 3.6 V and 4.5 V to 5.5 V
Clocking	
Phase Lock Loop (PLL)	1 x PLL and 1 coupled FMPLL
Internal RC Oscillator	16 MHz
External Crystal Oscillator	8 MHz to 40 MHz
Low power modes	
HALT and STOP	Yes
Debug	
Nexus	Level 3+, MDO and Aurora interface
Package	
LQFP	144 pins
LQFP exposed pads (EP)	176 pins

Table 1. MPC5744P feature summary (continued)

Feature	Details
MAPBGA	257 MAPBGA
Temperature	
Temperature range (junction)	-40°C to +150°C, option for 165°C
Ambient temperature range (LQFP)	-40°C to +125°C, TBD option (with 165°C junction option)
Ambient temperature range (BGA)	-40°C to +125°C, TBD option (with 165°C junction option)

1.2 Block diagram

Figure 1 shows the top-level block diagram of the MPC5744P device.

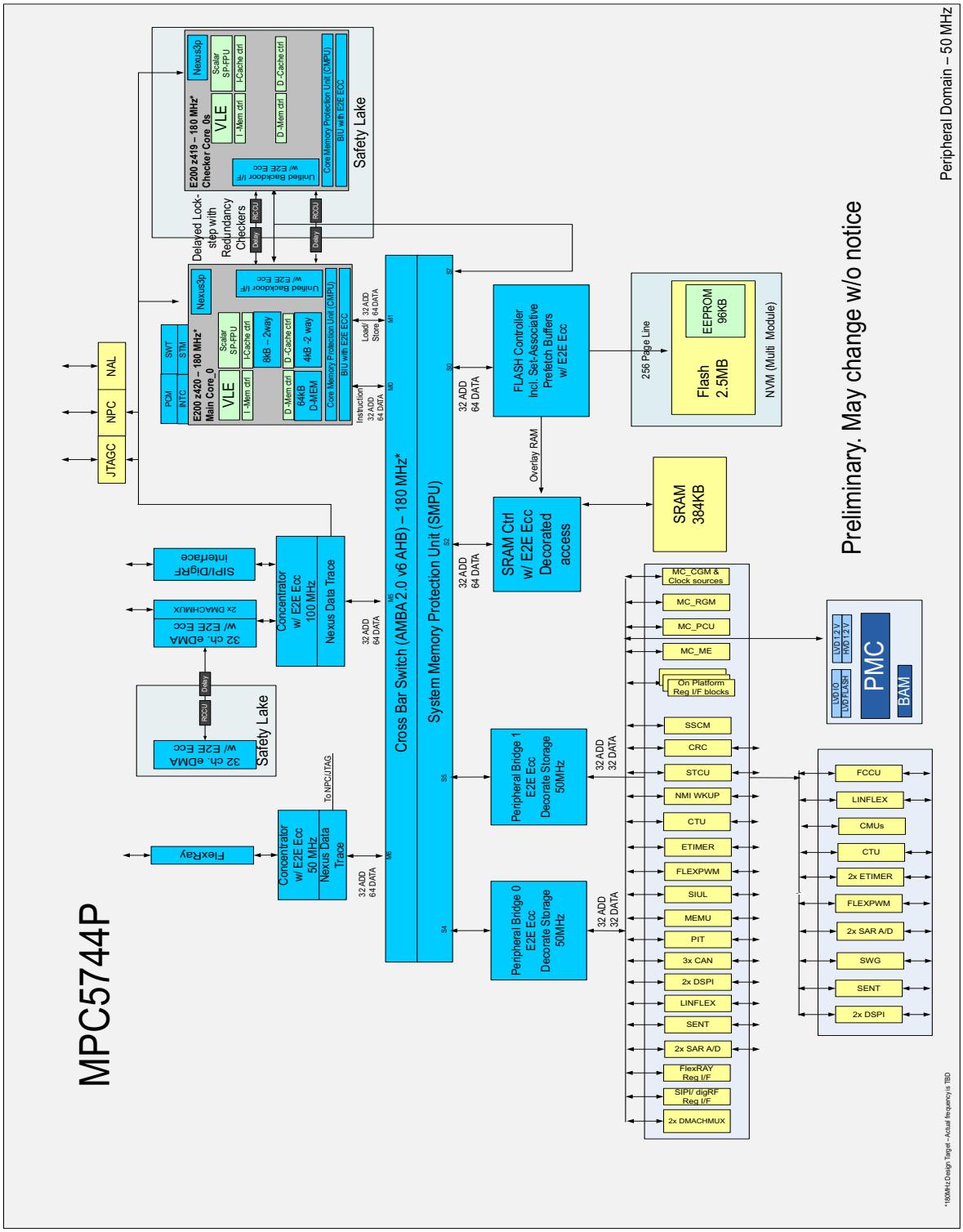


Figure 1. System Block Diagram

2 Pinouts

2.1 Package pinouts and ballouts

The following figures show the LQFP pinouts and the BGA ballmap.

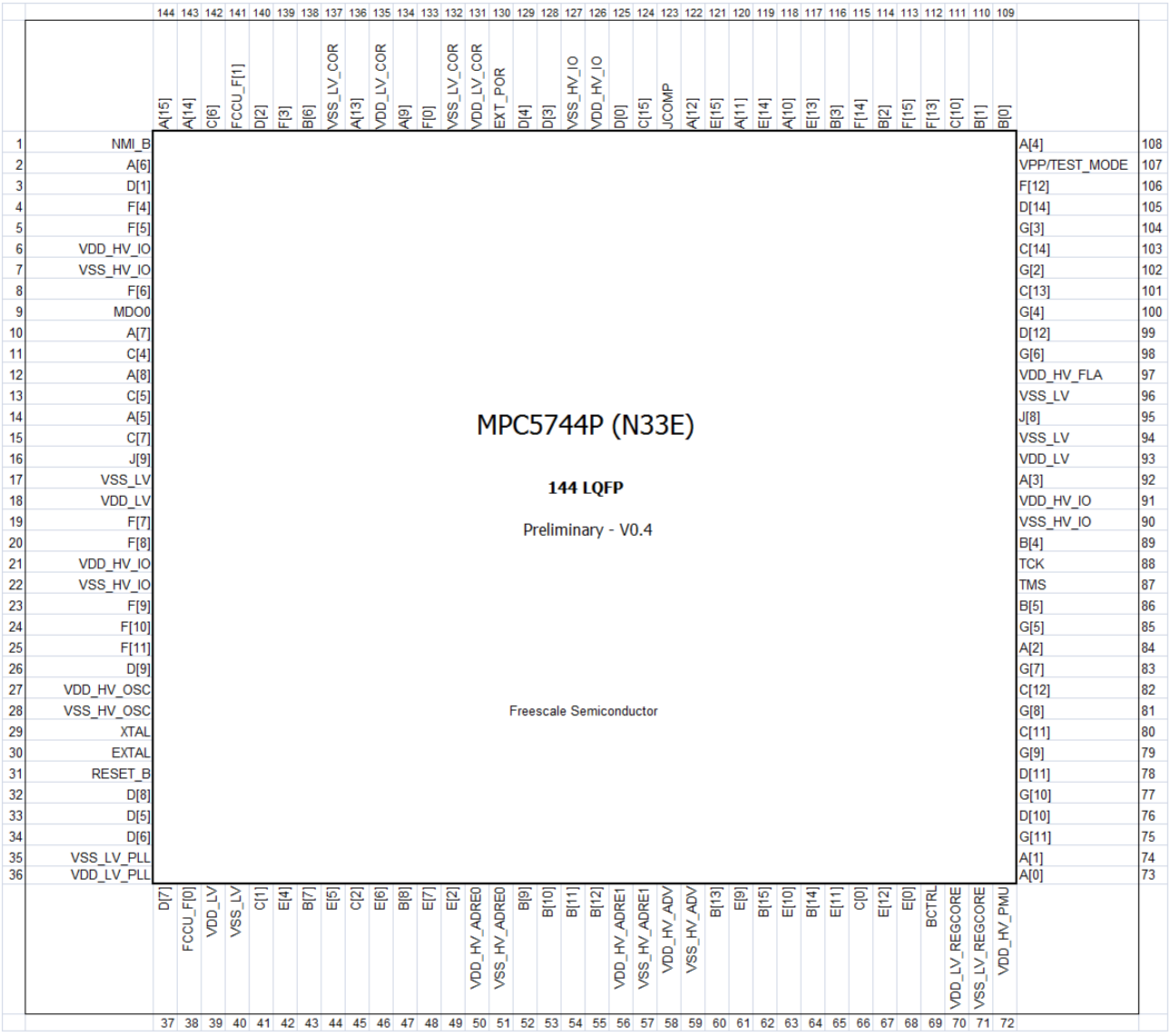


Figure 2. 144LQFP pinout

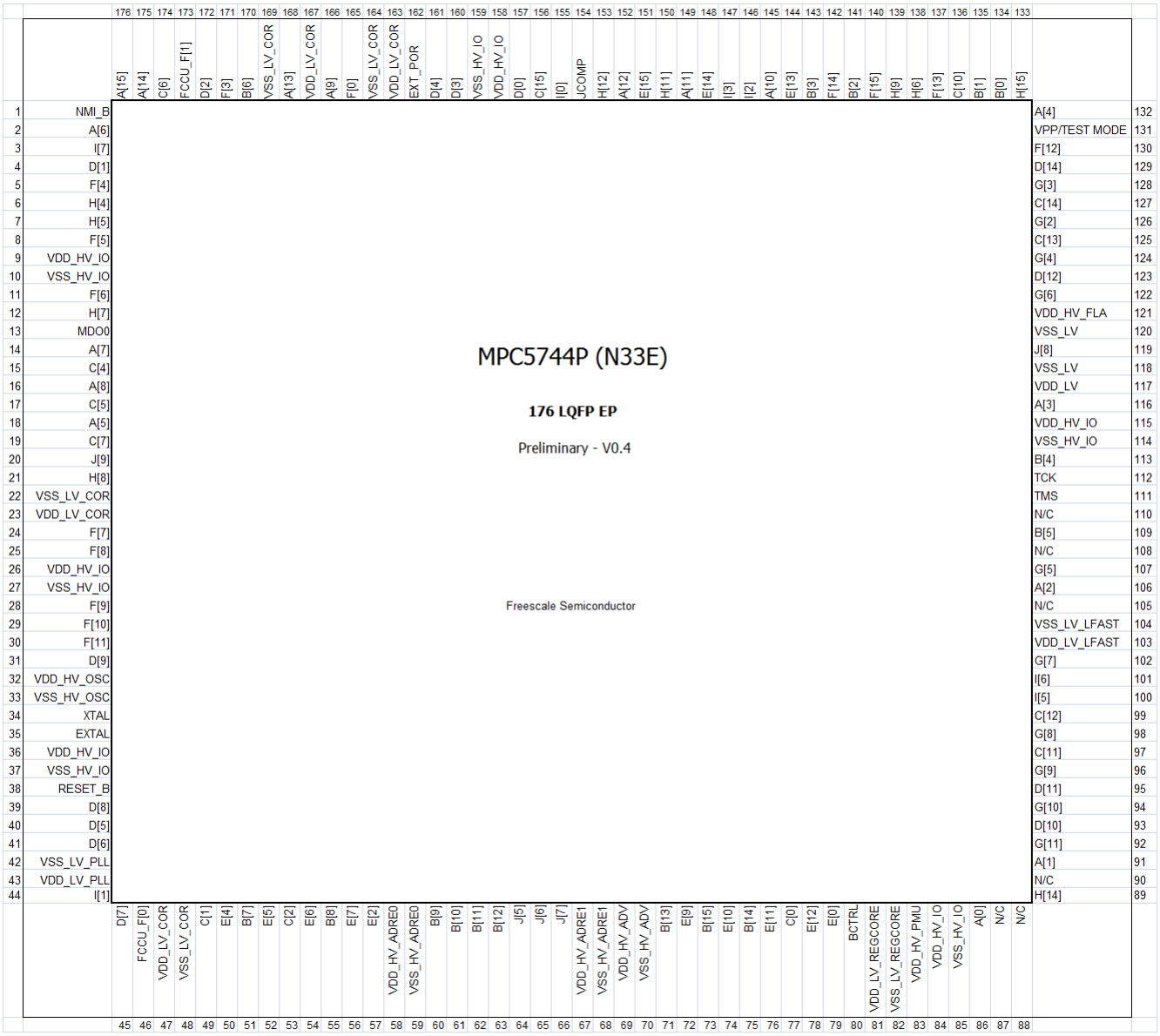
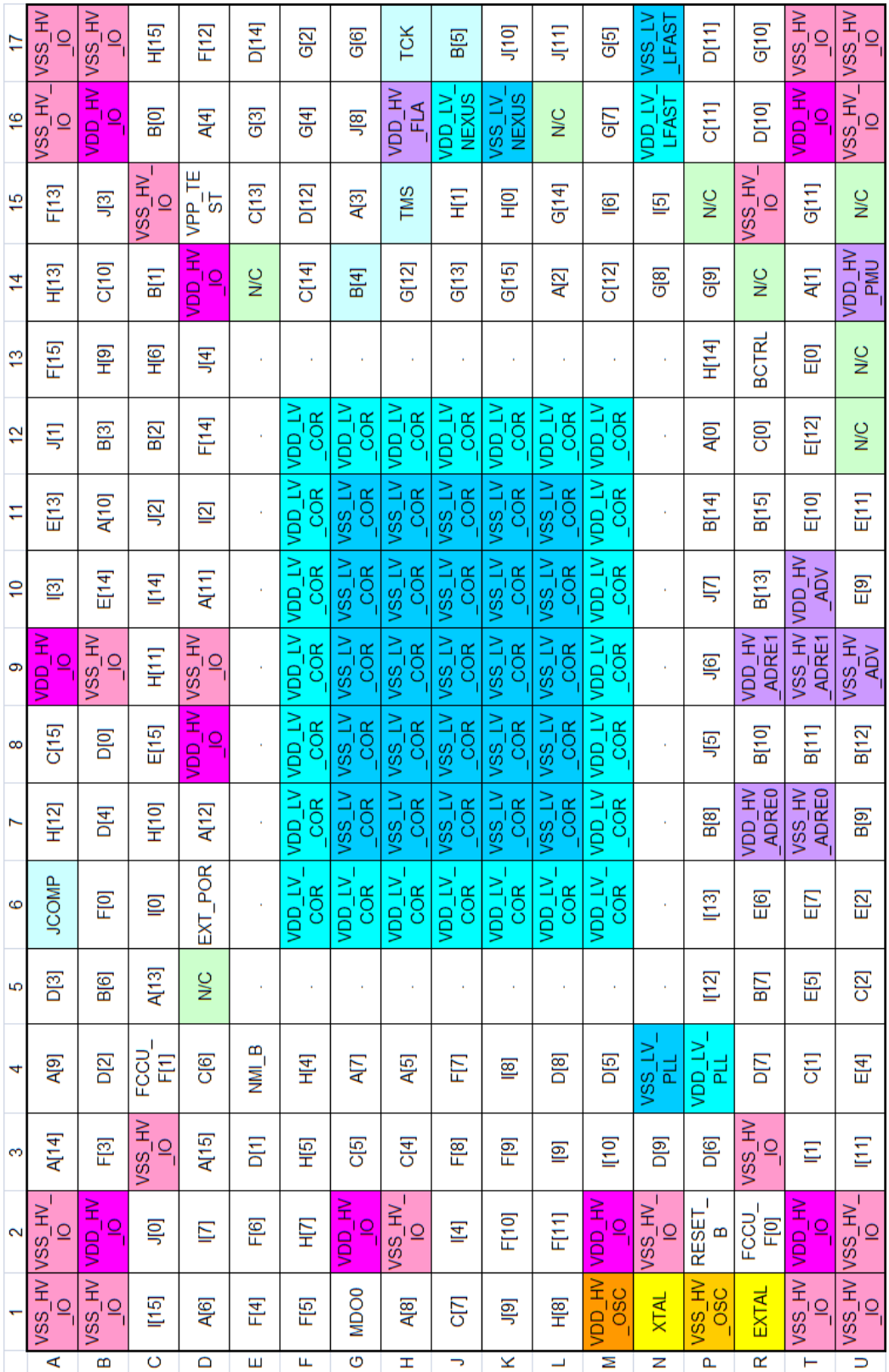


Figure 3. 176LQFP pinout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS_HV_IO	VSS_HV_IO	A[14]	A[9]	D[3]	JCOMP	H[12]	C[15]	VDD_HV_IO	I[3]	E[13]	J[1]	F[15]	H[13]	F[13]	VSS_HV_IO	VSS_HV_IO
B	VSS_HV_IO	VDD_HV_IO	F[3]	D[2]	B[6]	F[0]	D[4]	D[0]	VSS_HV_IO	E[14]	A[10]	B[3]	H[9]	C[10]	J[3]	VDD_HV_IO	VSS_HV_IO
C	I[15]	J[0]	VSS_HV_IO	FCCU_F[1]	A[13]	I[0]	H[10]	E[15]	H[11]	I[14]	J[2]	B[2]	H[6]	B[1]	VSS_HV_IO	B[0]	H[15]
D	A[6]	I[7]	A[15]	C[6]	N/C	EXT_POR	A[12]	VDD_HV_IO	VSS_HV_IO	A[11]	I[2]	F[14]	J[4]	VDD_HV_IO	VPP_TEST	A[4]	F[12]
E	F[4]	F[6]	D[1]	NMI_B	.	.	.	.	.	.	.	.	.	N/C	C[13]	G[3]	D[14]
F	F[5]	H[7]	H[5]	H[4]	.	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	.	C[14]	D[12]	G[4]	G[2]
G	MDO0	VDD_HV_IO	C[5]	A[7]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	B[4]	A[3]	J[8]	G[6]
H	A[8]	VSS_HV_IO	C[4]	A[5]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	G[12]	TMS	VDD_HV_FLA	TCK
J	C[7]	I[4]	F[8]	F[7]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	G[13]	H[1]	VDD_LV_NEXUS	B[5]
K	J[9]	F[10]	F[9]	I[8]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	G[15]	H[0]	VSS_LV_NEXUS	J[10]
L	H[8]	F[11]	I[9]	D[8]	.	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	.	A[2]	G[14]	N/C	J[11]
M	VDD_HV_OSC	VDD_HV_IO	I[10]	D[5]	.	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	.	C[12]	I[6]	G[7]	G[5]
N	XTAL	VSS_HV_IO	D[9]	VSS_LV_PLL	.	.	.	.	.	.	.	.	.	G[8]	I[5]	VDD_LV_LFAST	VSS_LV_LFAST
P	VSS_HV_OSC	RESET_B	D[6]	VDD_LV_PLL	I[12]	I[13]	B[8]	J[5]	J[6]	J[7]	B[14]	A[0]	H[14]	G[9]	N/C	C[11]	D[11]
R	EXTAL	FCCU_F[0]	VSS_HV_IO	D[7]	B[7]	E[6]	VDD_HV_ADRE0	B[10]	VDD_HV_ADRE1	B[13]	B[15]	C[0]	BCTRL	N/C	VSS_HV_IO	D[10]	G[10]
T	VSS_HV_IO	VDD_HV_IO	I[1]	C[1]	E[5]	E[7]	VSS_HV_ADRE0	B[11]	VSS_HV_ADRE1	VDD_HV_ADV	E[10]	E[12]	E[0]	A[1]	G[11]	VDD_HV_IO	VSS_HV_IO
U	VSS_HV_IO	VSS_HV_IO	I[11]	E[4]	C[2]	E[2]	B[9]	B[12]	VSS_HV_ADV	E[9]	E[11]	N/C	N/C	VDD_HV_PMU	N/C	VSS_HV_IO	VSS_HV_IO

Figure 4. 257MAPBGA ballmap

2.2 Pin/ball descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5744P devices. Note that this section is under development.

2.2.1 Pin/ball startup and reset states

This table provides startup state and reset state information for device pins/balls.

Table 2. Pin/ball startup and reset states

Pin	Startup state[1]	State during reset	State after reset	144 LQFP	176 LQFP	257MAPBGA
GPIOs	hi-z	hi-z	hi-z	[2]	[2]	[2]
Analog inputs[3]	hi-z	hi-z	hi-z	[2]	[2]	[2]
JCOMP (TRST)	hi-z	input, weak pull-down	input, weak pull-down	[4]	[4]	[4]
TDI	hi-z	input, weak pull-up	input, weak pull-up	[4]	[4]	[4]
TDO	hi-z	weak pull-up	hi-z	[4]	[4]	[4]
TMS	hi-z	input, weak pull-down	input, weak pull-down	[4]	[4]	[4]
TCK	hi-z	input, weak pull-down	input, weak pull-down	[4]	[4]	[4]
XTAL/EXTAL	hi-z	hi-z	hi-z	[4]	[4]	[4]
FCCU_F[0]	hi-z	input, hi-z	output/input, hi-z	38	46	R2
FCCU_F[1]	hi-z	input, hi-z	output/input, hi-z	141	173	C4
EXT_POR	hi-z	input, weak pull-down	input, weak pull-down	[4]	[4]	[4]
RESET_B	hi-z	input, weak pull-down	input, weak pull-down	[4]	[4]	[4]

NOTES:
1. Startup state is exited when the core and high-voltage supplies reach minimum levels as defined in the Power Management chapter.
2. See Section 2.2.5, Generic pins/balls.
3. Not all non-supply or reference pins on the device that are explicitly defined in this table.
4. See Section 2.2.3, System pins/balls.

2.2.2 Power supply and reference voltage pins/balls

Table 3. Power supply and reference voltage pins/balls

Supply			QFP		PBGA
Symbol	**Type**	**Description**	**144LQFP**	**176LQFP**	**257MAPBGA**
V_{DD_LV}	Power	Low voltage power Supply	18 39 70 93 131 135	23 47 81 117 163 167	F6 F7 F8 F9 F10 F11 F12 G6 G12 H6 H12 J6 J12 K6 K12 L6 L12 M6 M7 M8 M9 M10 M11 M12

Table 3. Power supply and reference voltage pins/balls

Supply			QFP		PBGA
Symbol	**Type**	**Description**	**144LQFP**	**176LQFP**	**257MAPBGA**
V_{SS_LV}	Ground	Low voltage ground. PLL Ground is also connected to low voltage ground for core logic on 144 LQFP (pin 35)..	17 35 40 71 94 96 132 137	22 42 48 82 118 120 164 169	G7 G8 G9 G10 G11 H7 H8 H9 H10 H11 J7 J8 J9 J10 J11 K7 K8 K9 K10 K11 L7 L8 L9 L10 L11
$V_{DD\_LV\_PLL}$	Power	PLL low voltage Supply	36	43	P4
$V_{SS\_LV\_PLL}$	Ground	PLL low voltage Ground	35	42	N4
$V_{DD\_HV\_IO}$	Power	High voltage Power Supply for I/O.	6 21 91 126	9 26 36 84 115 158	A9 B2 B16 D8 D14 G2 M2 T2 T16

Table 3. Power supply and reference voltage pins/balls

Supply			QFP		PBGA
Symbol	**Type**	**Description**	**144LQFP**	**176LQFP**	**257MAPBGA**
$V_{SS\_HV\_IO}$	Ground	High voltage Ground Supply for I/O	7 22 90 127	10 27 37 85 114 159	A1 A2 A16 A17 B1 B9 B17 C3 C15 D9 H2 N2 R3 R15 T1 T17 U1 U2 U16 U17
$V_{DD\_HV\_PMU}$ $V_{DD\_HV\_PMU\_AUX}$	Power	PMU high voltage Supply	72	83	U14
$V_{DD\_HV\_OSC0}$	Power	Power Supply for the oscillator	27	32	M1
$V_{SS\_HV\_OSC0}$	Ground	Ground Supply for the oscillator	28	33	P1
$V_{DD\_HV\_FLA0}$	Power	Decoupling supply pin for Flash	97	121	H16
$V_{DD\_HV\_ADV0/1}$	Power	High voltage Supply for ADC, SWG(3.3V)	58	69	T10
$V_{SS\_HV\_ADV0/1}$	Ground	High voltage Ground for ADC	59	70	U9
$V_{DD\_HV\_AD0\_VDDE}$[1] $V_{DD\_HV\_ADRE0}$ $V_{DD\_HV\_ADSW0}$	Supply	High voltage Supply for digital portion of ADC pads Voltage reference of ADC/TSENS High voltage Supply for ADC and ADC pad switches	50	58	R7
$V_{SS\_HV\_AD0\_VSSE}$ $V_{SS\_HV\_ADRE0}$ $V_{SS\_HV\_ADSW0}$	Ground	High voltage Ground for digital portion of ADC pads Voltage reference Ground of ADC/TSENS High voltage Ground for ADC and ADC pad switches	51	59	T7
$V_{DD\_HV\_AD1\_VDDE}$[2] $V_{DD\_HV\_ADRE1}$ $V_{DD\_HV\_ADSW1}$	Supply	High voltage Supply for digital portion of ADC pads Voltage reference of ADC/TSENS High voltage Supply for ADC and ADC pad switches	56	67	R9

Table 3. Power supply and reference voltage pins/balls

Supply			QFP		PBGA
Symbol	**Type**	**Description**	**144LQFP**	**176LQFP**	**257MAPBGA**
$V_{SS\_HV\_AD1\_VSSE}$ $V_{SS\_HV\_ADRE1}$ $V_{SS\_HV\_ADSW1}$	Ground	High voltage Ground for digital portion of ADC pads Voltage reference Ground of ADC/TSENS High voltage Ground for ADC and ADC pad switches	57	68	T9
$V_{DD\_LV\_LFAST}$	Supply	LFAST PLL low voltage Supply	-	99	N16
$V_{SS\_LV\_LFAST}$	Ground	LFAST PLL low voltage Ground	-	100	N17
$V_{DD\_LV\_NEXUS}$	Supply	Aurora LVDS Supply	-	-	J16
$V_{SS\_LV\_NEXUS}$	Ground	Aurora LVDS Ground	-	-	K16

NOTES:
1 Connected to ADC0/2. Can be 3.3V or 5V.
2 Connected to ADC1/3. Can be 3.3V or 5V.

2.2.3 System pins/balls

The following table contains information on system pin functions for the devices.

Table 4. System Pins/Balls

Symbol	Type	Description	QFP		PBGA
			144LQFP	176LQFP	257MAPBGA
NMI_B	Input	Non maskable Interrupt	1	1	E4
XTAL	Input	Crystal Oscillator/External Clock Input	29	34	N1
EXTAL	Input	Input of the oscillator amplifier circuit	30	35	R1
RESET_B	Input	Functional Reset	31	38	P2
EXT_POR	Input	External Power On Reset	130	162	D6
VPP_TEST[1]	Input	SoC Test Mode	107	131	D15
JCOMP	Input	JTAGC, JTAG Compliance Enable	123	154	A6
TCK	Input	JTAGC, Test Clock Input	88	112	H17
TMS	Input	JTAGC, Test Mode Select	87	111	H15
TDO	Output	JTAGC, Test Data Out	89	113	G14
TDI	Input	JTAGC, Test Data Input	86	109	J17
MDO[0]	Output	NEXUS, Message data out pins; reflects the state of the internal power on reset signal until RESET is negated	9	13	G1
MDO[3:1]	Output	NEXUS, Message data out pins	4,5,8	5,8,11	E1,F1,E2
EVTO	Output	NEXUS, Event Out Pin	24	29	K2
EVTI	Input	NEXUS, Event In Pin	25	30	L2
MCKO	Output	NEXUS, Message clock out pin	19	24	J4
MSEO	Output	NEXUS, Message Start/End out pin	20	25	J3
RDY_B	Output	NEXUS, Read/Write Transfer completed	-	-	J2
BCTRL	Output	Base control signal of external npn ballast	69	80	R13
J[11],J[10]	--	Freescale Factory Test[2]	-	-	L17,K17

NOTES:
1 VPP_TEST must be connected to ground.
2 Do not connect on the board.

2.2.4 LVDS pins/balls

The following table contains information on LVDS pin functions for the devices.

Table 5. SIPI LFAST LVDS pin descriptions

Functional block	Port pin	Signal	Signal description	Direction	176LQFP	257MAPBGA
SIPI LFAST[1]	I[5]	SIPI_TXN	Interprocessor Bus LFAST, LVDS Transmit Negative Terminal	O	102	N15
	C[12][2]	SIPI_TXP	Interprocessor Bus LFAST, LVDS Transmit Positive Terminal	O	101	M14
	I[6]	SIPI_RXN	Interprocessor Bus LFAST, LVDS Receive Negative Terminal	I	103	M15
	G[7][2]	SIPI_RXP	Interprocessor Bus LFAST, LVDS Receive Positive Terminal	I	104	M16

NOTES:
1 DRCLK and TCK/DRCLK usage for SIPI LFAST and Debug LFAST are described in the MPC5744P reference manual's SIPI LFAST and Debug LFAST chapters..
2 G[7] and C[12] are available in the 144LQFP, but there is no SIPI LFAST functionality available.

SIPI LFAST pins are muxed with GPIOs. Do not use GPIO and SIPI LFAST functionality in parallel.

Table 6. Aurora LVDS pin descriptions

Functional Block	PAD	Signal	Signal Description	Direction	MAPBGA 257[1]
Nexus Aurora High Speed Trace	G[12]	TX0P	Nexus Aurora High Speed Trace Lane 0, LVDS Positive Terminal	O	H14
	G[13]	TX0N	Nexus Aurora High Speed Trace Lane 0, LVDS Negative Terminal	O	J14
	G[14]	TX1P	Nexus Aurora High Speed Trace Lane 1, LVDS Positive Terminal	O	L15
	G[15]	TX1N	Nexus Aurora High Speed Trace Lane 1, LVDS Negative Terminal	O	K14
	H[0]	CLKP	Nexus Aurora High Speed Trace Clock, LVDS Positive Terminal	I	K15
	H[1]	CLKN	Nexus Aurora High Speed Trace Clock, LVDS Negative Terminal	I	J15

NOTES:
1 Nexus Aurora High Speed Trace is only available on the 257 Pin MAPBGA

2.2.5 Generic pins/balls

The I/O signal descriptions for the device are in the following table. It contains the port definition, multiplexing, direction, pad type, and package pin/ball numbers for each I/O pin on the device. See the device Reference Manual for the MSCR register address map.

Table 7. Pin Muxing

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
A[0]	MSCR[0]	0000 (Default)[1]	GPIO[0]	SIUL2-GPIO[0]	General Purpose IO A[0]	I/O	73	86	P12
		0001	ETC0	eTimer_0	eTimer_0 Input/Output Data Channel 0	I/O			
		0010	SCK	DSPI2	DSPI 2 Serial Clock (output)	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[59]	0010 (Default)	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I/O			
	IMCR[173]	0001	REQ0	SIUL2	SIUL2 External Interrupt 0	I			
A[1]	MSCR[1]	0000 (Default)	GPIO[1]	SIUL2-GPIO[1]	General Purpose IO A[1]	I/O	74	91	T14
		0001	ETC1	eTimer_0	eTimer_0 Input/Output Data Channel 1	I/O			
		0010	SOUT	DSPI2	DSPI 2 Serial Data Out	O			
		0011-1111	-	Reserved	-	-			
	IMCR[60]	0010	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I/O			
	IMCR[174]	0001	REQ1	SIUL2	SIUL2 External Interrupt Source 1	I			
A[2]	MSCR[2]	0000 (Default)	GPIO[2]	SIUL2-GPIO[2]	General Purpose IO A[2]	I/O	84	106	L14
		0001	ETC2	eTimer_0	eTimer_0 Input/Output Data Channel 2	I/O			
		0010	-	Reserved	-	-			
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input 3	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[169]	0000 (Default)	ABS1	MC_RGM	RGM external boot mode 1	I			
	IMCR[47]	0010	SIN	DSPI2	DSPI 2 Serial Data Input	I			
	IMCR[61]	0010	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I			
	IMCR[175]	0001	REQ2	SIUL2	SIUL2 External Interrupt Source 2	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
A[3]	MSCR[3]	0000 (Default)	GPIO[3]	SIUL2-GPIO[3]	General Purpose IO A[3]	I/O	92	116	G15
		0001	ETC3	eTimer_0	eTimer_0 Input/Output Data Channel 3	I/O			
		0010	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O			
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[171]	0000	ABS2	MC_RGM	RGM external boot mode 2	I			
	IMCR[62]	0010	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I/O			
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I			
A[4]	MSCR[4]	0000 (Default)	GPIO[4]	SIUL2-GPIO[4]	General Purpose IO A[4]	I/O	108	132	D16
		0001	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O			
		0010	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O			
		0011	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O			
		0100	A2	FlexPWM_1	FlexPWM_1 Channel A Input/Output 2	I/O			
		0101-1111	-	Reserved	-	-			
	IMCR[112]	0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I/O			
	IMCR[177]	0001	REQ4	SIUL2	SIUL2 External Interrupt Source 4	I			
	IMCR[172]	0000	FAB	MC_RGM	RGM Force Alternate Boot Mode	I			
	IMCR[63]	0011	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I/O			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
A[5]	MSCR[5]	0000 (Default)	GPIO[5]	SIUL2-GPIO[5]	General Purpose IO A[5]	I/O	14	18	H4
		0001	CS0	DSPI1	DSPI 1 Peripheral Chip Select 0	I/O			
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O			
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O			
		0100-1111	-	Reserved	-	-			
	IMCR[178]	0001	REQ5	SIUL2	SIUL2 External Interrupt Source 5	I			
A[6]	MSCR[6]	0000 (Default)	GPIO[6]	SIUL2-GPIO[6]	General Purpose IO A[6]	I/O	2	2	D1
		0001	SCK	DSPI1	DSPI 1 Serial Clock (output)	I/O			
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[179]	0001	REQ6	SIUL2	SIUL2 External Interrupt Source 6	I			
A[7]	MSCR[7]	0000 (Default)	GPIO[7]	SIUL2-GPIO[7]	General Purpose IO A[7]	I/O	10	14	G4
		0001	SOUT	DSPI1	DSPI 1 Serial Data Out	O			
		0010	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[180]	0001	REQ7	SIUL2	SIUL2 External Interrupt Source 7	I			
A[8]	MSCR[8]	0000 (Default)	GPIO[8]	SIUL2-GPIO[8]	General Purpose IO A[8]	I/O	12	16	H1
		0001	-	Reserved	-	-			
		0010	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[44]	0001	SIN	DSPI1	DSPI 1 Serial Data Input	I			
	IMCR[181]	0001	REQ8	SIUL2	SIUL2 External Interrupt Source 8	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
A[9]	MSCR[9]	0000 (Default)	GPIO[9]	SIUL2-GPIO[9]	General Purpose IO A[9]	I/O	134	166	A4
		0001	CS1	DSPI2	DSPI 2 Peripheral Chip Select 1	O			
		0010	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O			
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[183]	0001	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I/O			
A[10]	MSCR[10]	0000 (Default)	GPIO[10]	SIUL2-GPIO[10]	General Purpose IO A[10]	I/O	118	145	B11
		0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O			
		0010	B0	FlexPWM_0	FlexPWM_0 Channel B Input/Output 0	I/O			
		0011	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 2	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[182]	0001	REQ9	SIUL2	SIUL2 External Interrupt Source 9	I			
A[11]	MSCR[11]	0000 (Default)	GPIO[11]	SIUL2-GPIO[11]	General Purpose IO A[11]	I/O	120	149	D10
		0001	SCK	DSPI2	DSPI 2 Serial Clock (output)	I/O			
		0010	A0	FlexPWM_0	FlexPWM_0 Channel A Input/Output 0	I/O			
		0011	A2	FlexPWM_0	FlexPWM_0 Channel A Input/Output 2	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[183]	0001	REQ10	SIUL2	SIUL2 External Interrupt Source 10	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
A[12]	MSCR[12]	0000 (Default)	GPIO[12]	SIUL2-GPIO[12]	General Purpose IO A[12]	I/O	122	152	D7
		0001	SOUT	DSPI2	DSPI 2 Serial Data Out	O			
		0010	A2	FlexPWM_0	FlexPWM_0 Channel A Input/Output 2	I/O			
		0011	B2	FlexPWM_0	FlexPWM_0 Channel B Input/Output 2	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[184]	0001	REQ11	SIUL2	SIUL2 External Interrupt Source 11	I			
A[13]	MSCR[13]	0000 (Default)	GPIO[13]	SIUL2-GPIO[13]	General Purpose IO A[13]	I/O	136	168	C5
		0001	-	Reserved	-	-			
		0010	B2	FlexPWM_0	FlexPWM_0 Channel B Input/Output 2	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[83]	0010	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I			
	IMCR[47]	0001	SIN	DSPI2	DSPI 2 Serial Data Input	I			
	IMCR[185]	0001	REQ12	SIUL2	SIUL2 External Interrupt Source 12	I			
A[14]	MSCR[14]	0000 (Default)	GPIO[14]	SIUL2-GPIO[14]	General Purpose IO A[14]	I/O	143	175	A3
		0001	TXD	CAN1	CAN 1 Transmit Pin	O			
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[186]	0001	REQ13	SIUL2	SIUL2 External Interrupt Source 13	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
A[15]	MSCR[15]	0000 (Default)	GPIO[15]	SIUL2-GPIO[15]	General Purpose IO A[15]	I/O	144	176	D3
		0001	-	Reserved	-	-			
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O			
		0011-1111	-	Reserved	-	-			
	IMCR[32]	0001	RXD	CAN0	CAN 0 Receive Pin	I			
	IMCR[33]	0001	RXD	CAN1	CAN 1 Receive Pin	I			
	IMCR[187]	0001	REQ14	SIUL2	SIUL2 External Interrupt Source 14	I			
B[0]	MSCR[16]	0000 (Default)	GPIO[16]	SIUL2-GPIO[16]	General Purpose IO B[0]	I/O	109	134	C16
		0001	TXD	CAN0	CAN 0 Transmit Pin	O			
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O			
		0011	DEBUG0	SSCM	SSCM Debug Output 0	O			
		0100-1111	-	Reserved	-	-			
	IMCR[188]	0001	REQ15	SIUL2	SIUL2 External Interrupt Source 15	I			
B[1]	MSCR[17]	0000 (Default)	GPIO[17]	SIUL2-GPIO[17]	General Purpose IO B[1]	I/O	110	135	C14
		0001	-	Reserved	-	-			
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O			
		0011	DEBUG1	SSCM	SSCM Debug Output 1	O			
		0100-1111	-	Reserved	-	-			
	IMCR[32]	0010	RXD	CAN0	CAN 0 Receive Pin	I			
	IMCR[33]	0010	RXD	CAN1	CAN 1 Receive Pin	I			
	IMCR[189]	0001	REQ16	SIUL2	SIUL2 External Interrupt Source 16	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
B[2]	MSCR[18]	0000 (Default)	GPIO[18]	SIUL2-GPIO[18]	General Purpose IO B[2]	I/O	114	141	C12
		0001	TXD	LIN0	LINFlexD 0 Transmit Pin	O			
		0010	-	Reserved	-	-			
		0011	DEBUG2	SSCM	SSCM Debug Output 2	O			
		0100-1111	-	Reserved	-	-			
	IMCR[190]	0001	REQ17	SIUL2	SIUL2 External Interrupt Source 17	I			
B[3]	MSCR[19]	0000 (Default)	GPIO[19]	SIUL2-GPIO[19]	General Purpose IO B[3]	I/O	116	143	B12
		0001	-	Reserved	-	-			
		0010	-	Reserved	-	-			
		0011	DEBUG3	SSCM	SSCM Debug Output 3	O			
		0100-1111	-	Reserved	-	-			
	IMCR[165]	0001	RXD	LIN0	LIN 0 Receive Pin	I			
B[4]	MSCR[20]	0000	GPIO[20]	SIUL2-GPIO[20]	General Purpose IO B[4]	I/O	89	113	G14
		0001 (Default)	TDO	TDO_MUX	JTAGC Test Data Out (TDO)	O			
		0010-1111	-	Reserved	-	-			
B[5]	MSCR[21]	0000 (Default)	GPIO[21]	SIUL2-GPIO[21]	JTAGC Test Data In (TDI)[2] General Purpose IO B[5]	I/O	86	109	J17
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
B[6]	MSCR[22]	0000 (Default)	GPIO[22]	SIUL2-GPIO[22]	General Purpose IO B[6]	I/O	138	170	B5
		0001	CLK_OUT	MC_RGM	CGM Clock out for off-chip use and observation	O			
		0010	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O			
		0011-1111	-	Reserved	-	-			
	IMCR[191]	0001	REQ18	SIUL2	SIUL2 External Interrupt Source 18	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
B[7]	MSCR[23]	0000 (Default)	GPI[23][3] ADC0_AN[0]	SIUL2-GPI[23]	General Purpose Input B[7]	I	43	51	R5
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[165]	0010	RXD	LIN0	LIN 0 Receive Pin	I			
B[8]	MSCR[24]	0000	GPI[24][3] ADC0_AN[1]	SIUL2-GPI[24]	General Purpose Input B[8]	I	47	55	P7
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[64]	0001	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I			
B[9]	MSCR[25]	0000 (Default)	GPI[25][3] ADC0_AN[2]	SIUL2-GPI[25]	General Purpose Input B[9]	I	52	60	U7
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
B[10]	MSCR[26]	0000 (Default)	GPI[26][3] ADC0_ADC1_AN[12]	SIUL2-GPI[26]	General Purpose Input B[10]	I	53	61	R8
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
B[11]	MSCR[27]	0000 (Default)	GPI[27][3] ADC0_ADC1_AN[13]	SIUL2-GPI[27]	General Purpose Input B[11]	I	54	62	T8
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
B[12]	MSCR[28]	0000 (Default)	GPI[28][3] ADC0_ADC1_AN[14]	SIUL2-GPI[28]	General Purpose Input B[12]	I	55	63	U8
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
B[13]	MSCR[29]	0000 (Default)	GPI[29][3] ADC1_AN[0]	SIUL2-GPI[29]	General Purpose Input B[13]	I	60	71	R10
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[166]	0001	RXD	LIN1	LIN 1 Receive Pin	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
B[14]	MSCR[30]	0000 (Default)	GPI[30][3] ADC1_AN[1]	SIUL2-GPI[30]	General Purpose Input B[14]	I	64	75	P11
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved		-			
	IMCR[63]	0001	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I			
	IMCR[192]	0001	REQ19	SIUL2	SIUL2 External Interrupt Source 19	I			
B[15]	MSCR[31]	0000 (Default)	GPI[31][3] ADC1_AN[2]	SIUL2-GPI[31]	General Purpose Input B[15]	I	62	73	R11
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[193]	0001	REQ20	SIUL2	SIUL2 External Interrupt Source 20	I			
C[0]	MSCR[32]	0000 (Default)	GPI[32][3] ADC1_AN[3]	SIUL2-GPI[32]	General Purpose Input C[0]	I	66	77	R12
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
C[1]	MSCR[33]	0000 (Default)	GPI[33][3] ADC0_AN[2]	SIUL2-GPI[33]	General Purpose Input C[1]	I	41	49	T4
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
C[2]	MSCR[34]	0000 (Default)	GPI[34][3] ADC0_AN[3]	SIUL2-GPI[34]	General Purpose Input C[2]	I	45	53	U5
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
C[4]	MSCR[36]	0000 (Default)	GPIO[36]	SIUL2-GPIO[36]	General Purpose IO C[4]	I/O	11	15	H3
		0001	CS0	DSPI0	DSPI 0 Peripheral Chip Select 0	I/O			
		0010	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 1	I/O			
		0011	DEBUG4	SSCM	SSCM Debug Output 4	O			
		0100-1111	-	Reserved	-	-			
	IMCR[195]	0001	REQ22	SIUL2	SIUL2 External Interrupt Source 22	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
C[5]	MSCR[37]	0000 (Default)	GPIO[37]	SIUL2-GPIO[37]	General Purpose IO C[5]	I/O	13	17	G3
		0001	SCK	DSPI0	DSPI 0 Serial Clock (output)	I/O			
		0010	-	Reserved	-	-			
		0011	DEBUG5	SSCM	SSCM Debug Output 5	O			
		0100-1111	-	Reserved	-	-			
	IMCR[86]	0001	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I			
	IMCR[196]	0001	REQ23	SIUL2	SIUL2 External Interrupt Source 23	I			
C[6]	MSCR[38]	0000 (Default)	GPIO[38]	SIUL2-GPIO[38]	General Purpose IO C[6]	I/O	142	174	D4
		0001	SOUT	DSPI0	DSPI 0 Serial Data Out	O			
		0010	B1	FlexPWM_0	FlexPWM_0 Channel B Input/Output 1	I/O			
		0011	DEBUG6	SSCM	SSCM Debug Output 6	O			
		0100-1111	-	Reserved	-	-			
	IMCR[197]	0001	REQ24	SIUL2	SIUL2 External Interrupt Source 24	I			
C[7]	MSCR[39]	0000 (Default)	GPIO[39]	SIUL2-GPIO[39]	General Purpose IO C[7]	I/O	15	19	J1
		0001	-	Reserved	-	-			
		0010	A1	FlexPWM_0	FlexPWM_0 Channel A Input/Output 1	I/O			
		0011	DEBUG7	SSCM	SSCM Debug Output 7	O			
		0100-1111	-	Reserved	-	-			
	IMCR[41]	0001	SIN	DSPI0	DSPI 0 Serial Data Input	I			
C[10]	MSCR[42]	0000 (Default)	GPIO[42]	SIUL2-GPIO[42]	General Purpose IO C[10]	I/O	111	136	B14
		0001	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O			
		0010	-	Reserved	-	-			
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[84]	0001	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
C[11]	MSCR[43]	0000 (Default)	GPIO[43]	SIUL2-GPIO[43]	General Purpose IO C[11]	I/O	80	97	P16
		0001	ETC4	eTimer_0	eTimer_0 Input/Output Data Channel 4	I/O			
		0010	CS2	DSPI2	DSPI 2 Peripheral Chip Select 2	O			
		0011-1111	-	Reserved	-	-			
	IMCR[63]	0100	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I			
C[12]	MSCR[44]	0000 (Default)	GPIO[44]	SIUL2-GPIO[44]	General Purpose IO C[12]	I/O	82	101	M14
		0001	ETC5	eTimer_0	eTimer_0 Input/Output Data Channel 5[4]	I/O			
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O			
		0011	-	Reserved	-	O			
		0100-1111	-	Reserved	-	-			
	IMCR[64]	0011	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I			
C[13]	MSCR[45]	0000 (Default)	GPIO[45]	SIUL2-GPIO[45]	General Purpose IO C[13]	I/O	101	125	E15
		0001	ETC1	eTimer_1	eTimer_1 Input/Output Data Channel 1	I/O			
		0010-0011	-	Reserved	-	-			
		0100	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I/O			
		0101-1111	-	Reserved	-	-			
	IMCR[38]	0001 (Default)	EXT_IN	CTU_0	CTU 0 External Trigger Input	I			
	IMCR[87]	0001	EXT_SYNC	FlexPWM_0	FlexPWM_0 External Trigger Input	I			
	IMCR[105]	0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
C[14]	MSCR[46]	0000 (Default)	GPIO[46]	SIUL2-GPIO[46]	General Purpose IO C[14]	I/O	103	127	F14
		0001	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O			
		0010	EXT_TGR	CTU_0	CTU0 External Trigger Output	O			
		0011	CS7	DSPI1	DSPI 1 Peripheral Chip Select 7	O			
		0100	B0	FlexPWM_1	FlexPWM_1 Channel B Input/Output 0	I/O			
		0101-1111	-	Reserved	-	-			
	IMCR[106]	0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I			
C[15]	MSCR[47]	0000 (Default)	GPIO[47]	SIUL2-GPIO[47]	General Purpose IO C[15]	I/O	124	156	A8
		0001	FR_A_TXEN	FLEXRAY	FlexRay Transmit Enable Channel A	O			
		0010	ETC0	eTimer_1	eTimer_1 Input/Output Data Channel 0	I/O			
		0011	A1	FlexPWM_0	FlexPWM_0 Channel A Input/Output 1	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[38]	0010	EXT_IN	CTU_0	CTU 0 External Trigger Input	I			
	IMCR[87]	0010	EXT_SYNC	FlexPWM_0	FlexPWM_0 External Sync Input	I			
D[0]	MSCR[48]	0000 (Default)	GPIO[48]	SIUL2-GPIO[48]	General Purpose IO D[0]	I/O	125	157	B8
		0001	FR_A_TX	FLEXRAY	FlexRay Transmit Data Channel A	O			
		0010	ETC1	eTimer_1	eTimer_1 Input/Output Data Channel 1	I/O			
		0011	B1	FlexPWM_0	FlexPWM_0 Channel B Input/Output 1	I/O			
		0100-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
D[1]	MSCR[49]	0000 (Default)	GPIO[49]	SIUL2-GPIO[49]	General Purpose IO D[1]	I/O	3	4	E3
		0001	-	Reserved	-	-			
		0010	ETC2	eTimer_1	eTimer_1 Input/Output Data Channel 2	I/O			
		0011	EXT_TGR	CTU_0	CTU 0 External Trigger Output	O			
		0100-1111	-	Reserved	-	-			
	IMCR[136]	0001	FR_A_RX	FLEXRAY	FlexRay Channel A Receive Pin	I			
D[2]	MSCR[50]	0000 (Default)	GPIO[50]	SIUL2-GPIO[50]	General Purpose IO D[2]	I/O	140	172	B4
		0001	-	Reserved	-	-			
		0010	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O			
		0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[137]	0001	FR_B_RX	FLEXRAY	FlexRay Channel B Receive Pin	I			
D[3]	MSCR[51]	0000 (Default)	GPIO[51]	SIUL2-GPIO[51]	General Purpose IO D[3]	I/O	128	160	A5
		0001	FR_B_TX	FLEXRAY	FlexRay Transmit Data Channel B	O			
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O			
		0011	A3	FlexPWM_0	FlexPWM_0 Channel A Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			
D[4]	MSCR[52]	0000 (Default)	GPIO[52]	SIUL2-GPIO[52]	General Purpose IO D[4]	I/O	129	161	B7
		0001	FR_B_TXEN	FLEXRAY	FlexRay Transmit Enable Channel B	O			
		0010	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O			
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
D[5]	MSCR[53]	0000 (Default)	GPIO[53]	SIUL2-GPIO[53]	General Purpose IO D[5]	I/O	33	40	M4
		0001	CS3	DSPI0	DSPI 0 Peripheral Chip Select 3	O			
		0010-1111	-	Reserved	-	-			
	IMCR[85]	0001	FAULT2	FlexPWM_0	FlexPWM_0 Fault Input 2	I			
	IMCR[205]	0001	SENT_RX[0]	SENT0	SENT 0 Receiver channel 0	I			
D[6]	MSCR[54]	0000 (Default)	GPIO[54]	SIUL2-GPIO[54]	General Purpose IO D[6]	I/O	34	41	P3
		0001	CS2	DSPI0	DSPI 0 Peripheral Chip Select 2	O			
		0010	-	Reserved	-	-			
		0011	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 3	I/O			
		0100-1111	-	Reserved	-	-			
	IMCR[84]	0010	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I			
D[7]	MSCR[55]	0000 (Default)	GPIO[55] SWG OUT[5]	SIUL2-GPIO[55]	General Purpose IO D[7]	I/O	37	45	R4
		0001	CS3	DSPI1	DSPI 1 Peripheral Chip Select 3	O			
		0010	-	Reserved	-	-			
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O			
		0100-1111	-	Reserved	-	-			
	IMCR[213]	0001	SENT_RX[0]	SENT1	SENT 1 Receiver channel 0	I			
D[8]	MSCR[56]	0000 (Default)	GPIO[56]	SIUL2-GPIO[56]	General Purpose IO D[8]	I/O	32	39	L4
		0001	CS2	DSPI1	DSPI 1 Peripheral Chip Select 2	O			
		0010	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O			
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O			
		0100-1111	-	Reserved	-	-			
	IMCR[86]	0010	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
D[9]	MSCR[57]	0000 (Default)	GPIO[57]	SIUL2-GPIO[57]	General Purpose IO D[9]	I/O	26	31	N3
		0001	X0	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 0	I/O			
		0010	TXD	LIN1	LINFlexD 1 Transmit Pin	O			
		0011-1111	-	Reserved	-	-			
D[10]	MSCR[58]	0000 (Default)	GPIO[58]	SIUL2-GPIO[58]	General Purpose IO D[10]	I/O	76	93	R16
		0001	A0	FlexPWM_0	FlexPWM_0 Channel A Input/Output 0	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[59]	0001	ETC0	eTimer_0	eTimer_0 Input Data Channel 0	I			
D[11]	MSCR[59]	0000 (Default)	GPIO[59]	SIUL2-GPIO[59]	General Purpose IO D[11]	I/O	78	95	P17
		0001	B0	FlexPWM_0	FlexPWM_0 Channel B Input/Output 0	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[60]	0001	ETC1	eTimer_0	eTimer_0 Input Data Channel 1	I			
D[12]	MSCR[60]	0000 (Default)	GPIO[60]	SIUL2-GPIO[60]	General Purpose IO D[12]	I/O	99	123	F15
		0001	X1	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 1	I/O			
		0010	CS6	DSPI1	DSPI 1 Peripheral Chip Select 6	O			
		0011-1111	-	Reserved	-	-			
	IMCR[166]	0010	RXD	LIN1	LIN 1 Receive Pin	I			
D[14]	MSCR[62]	0000 (Default)	GPIO[62]	SIUL2-GPIO[62]	General Purpose IO D[14]	I/O	105	129	E17
		0001	B1	FlexPWM_0	FlexPWM_0 Channel B Input/Output 1	I/O			
		0010-1111	-	Reserved		-			
	IMCR[62]	0001	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
E[0]	MSCR[64]	0000 (Default)	GPI[64][3] ADC1_ADC3_AN[5]	SIUL2-GPI[64]	General Purpose Input E[0]	I	68	79	T13
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[2]	MSCR[66]	0000 (Default)	GPI[66][3] ADC0_AN[5]	SIUL2-GPI[66]	General Purpose Input E[2]	I	49	57	U6
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[4]	MSCR[68]	0000 (Default)	GPI[68][3] ADC0_AN[7]	SIUL2-GPI[68]	General Purpose Input E[4]	I	42	50	U4
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[5]	MSCR[69]	0000 (Default)	GPI[69][3] ADC0_AN[8]	SIUL2-GPI[69]	General Purpose Input E[5]	I	44	52	T5
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[6]	MSCR[70]	0000 (Default)	GPI[70][3] ADC0_AN[4]	SIUL2-GPI[70]	General Purpose Input E[6]	I	46	54	R6
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[7]	MSCR[71]	0000 (Default)	GPI[71][3] ADC0_AN[6]	SIUL2-GPI[71]	General Purpose Input E[7]	I	48	56	T6
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[9]	MSCR[73]	0000	GPI[73][3] ADC1_ADC3_AN[7]	SIUL2-GPI[73]	General Purpose Input E[9]	I	61	72	U10
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[10]	MSCR[74]	0000 (Default)	GPI[74][3] ADC1_ADC3_AN[8]	SIUL2-GPI[74]	General Purpose Input E[10]	I	63	74	T11
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
E[11]	MSCR[75]	0000 (Default)	GPI[75][3] ADC1_ADC3_AN[5]	SIUL2-GPI[75]	General Purpose Input E[11]	I	65	76	U11
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[12]	MSCR[76]	0000 (Default)	GPI[76][3] ADC1_ADC3_AN6]	SIUL2-GPI[76]	General Purpose Input E[12]	I	67	78	T12
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
E[13]	MSCR[77]	0000 (Default)	GPIO[77]	SIUL2-GPIO[77]	General Purpose IO E[13]	I/O	117	144	A11
		0001	ETC5	eTimer_0	eTimer_0 Input/Output Data Channel 5	I/O			
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O			
		0011	CS4	DSPI1	DSPI 1 Peripheral Chip Select 4	O			
		0100-1111	-	Reserved	-	-			
	IMCR[198]	0001	REQ25	SIUL2	SIUL2 External Interrupt Source 25	I			
	IMCR[64]	0100	ETC5	eTimer_0	eTimer_0 Input Data Channel	I			
E[14]	MSCR[78]	0000 (Default)	GPIO[78]	SIUL2-GPIO[78]	General Purpose IO E[14]	I/O	119	148	B10
		0001	ETC5	eTimer_1	eTimer_1 Input/Output Data Channel 5	I/O			
		0010	-	Reserved	-	-			
		0011	CS5	DSPI1	DSPI 1 Peripheral Chip Select 5	O			
		0100	B2	FlexPWM_1	FlexPWM_1 Channel B Input/Output 2	I/O			
		0101-1111	-	Reserved	-	-			
	IMCR[113]	0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I			
	IMCR[199]	0001	REQ26	SIUL2	SIUL2 External Interrupt Source 26	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
E[15]	MSCR[79]	0000 (Default)	GPIO[79]	SIUL2-GPIO[79]	General Purpose IO E[15]	I/O	121	151	C8
		0001	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O			
		0010-1111	-	Reserved	-	-			
	IMCR[200]	0001	REQ27	SIUL2	SIUL2 External Interrupt Source 27	I			
F[0]	MSCR[80]	0000 (Default)	GPIO[80]	SIUL2-GPIO[80]	General Purpose IO F[0]	I/O	133	165	B6
		0001	A1	FlexPWM_0	FlexPWM_0 Channel A Input/Output 1	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[61]	0001	ETC2	eTimer_0	eTimer_0 Input Data Channel 2	I			
	IMCR[201]	0001	REQ28	SIUL2	SIUL2 External Interrupt Source 28	I			
F[3]	MSCR[83]	0000 (Default)	GPIO[83]	SIUL2-GPIO[83]	General Purpose IO F[3]	I/O	139	171	B3
		0001	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O			
		0010-1111	-	Reserved	-	-			
F[4]	MSCR[84]	0000 (Default)	GPIO[84]	SIUL2-GPIO[84]	General Purpose IO F[4]	I/O	4	5	E1
		0001	-	Reserved	-	I/O			
		0010	MDO[3]	NPC_WRAPPER	Nexus - Message Data Out Pin 3	O			
		0011-1111	-	Reserved	-	-			
F[5]	MSCR[85]	0000 (Default)	GPIO[85]	SIUL2-GPIO[85]	General Purpose IO F[5]	I/O	5	8	F1
		0001	-	Reserved	-	I/O			
		0010	MDO[2]	NPC_WRAPPER	Nexus Message Data Out Pin 2	O			
		0011-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
F[6]	MSCR[86]	0000 (Default)	GPIO[86]	SIUL2-GPIO[86]	General Purpose IO F[6]	I/O	8	11	E2
		0001	-	Reserved	-	I/O			
		0010	MDO[1]	NPC_WRAPPER	Nexus Message Data Out Pin 1	O			
		0011-1111	-	Reserved	-	-			
F[7]	MSCR[87]	0000 (Default)	GPIO[87]	SIUL2-GPIO[87]	General Purpose IO F[7]	I/O	19	24	J4
		0001	-	Reserved	-	I/O			
		0010	MCKO	NPC_WRAPPER	Nexus Message Clock Out for development tools	O			
		0011-1111	-	Reserved	-	-			
F[8]	MSCR[88]	0000 (Default)	GPIO[88]	SIUL2-GPIO[88]	General Purpose IO F[8]	I/O	20	25	J3
		0001	-	Reserved	-	I/O			
		0010	MSEO_B[1]	NPC_WRAPPER	Nexus Message Start/End Out Pin 1	O			
		0011-1111	-	Reserved	-	-			
F[9]	MSCR[89]	0000 (Default)	GPIO[89]	SIUL2-GPIO[89]	General Purpose IO F[9]	I/O	23	28	K3
		0001	-	Reserved	-	I/O			
		0010	MSEO_B[0]	NPC_WRAPPER	Nexus Message Start/End Out Pin 0	O			
		0011-1111	-	Reserved	-	-			
F[10]	MSCR[90]	0000 (Default)	GPIO[90]	SIUL2-GPIO[90]	General Purpose IO F[10]	I/O	24	29	K2
		0001	-	Reserved	-	-			
		0010	EVTO_B	NPC_WRAPPER	Nexus Event Out Pin	O			
		0011-1111	-	Reserved	-	-			
F[11]	MSCR[91]	0000 (Default)	GPIO[91]	SIUL2-GPIO[91]	General Purpose IO F[11]	I/O	25	30	L2
		0001	-	Reserved	-	-			
		0010	EVTI_IN	NPC_WRAPPER	Nexus Event In Pin	I			
		0011-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
F[12]	MSCR[92]	0000 (Default)	GPIO[92]	SIUL2-GPIO[92]	General Purpose IO F[12]	I/O	106	130	D17
		0001	ETC3	eTimer_1	eTimer_1 Input/Output Data Channel 3	I/O			
		0010-0011	-	Reserved	-	-			
		0100	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I/O			
		0101-1111	-	Reserved	-	-			
	IMCR[109]	0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I			
	IMCR[203]	0001	REQ30	SIUL2	SIUL2 External Interrupt Source 30	I			
F[13]	MSCR[93]	0000 (Default)	GPIO[93]	SIUL2-GPIO[93]	General Purpose IO F[13]	I/O	112	137	A15
		0001	ETC4	eTimer_1	eTimer_1 Input/Output Data Channel 4	I/O			
		0010-0011	-	Reserved	-	-			
		0100	B1	FlexPWM_1	FlexPWM_1 Channel B Input/Output 1	I/O			
		0101-1111	-	Reserved	-	-			
	IMCR[110]	0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I			
	IMCR[204]	0001	REQ31	SIUL2	SIUL2 External Interrupt Source 31	I			
F[14]	MSCR[94]	0000 (Default)	GPIO[94]	SIUL2-GPIO[94]	General Purpose IO F[14]	I/O	115	142	D12
		0001	TXD	LIN1	LINFlexD 1 Transmit Pin	O			
		0010	TXD	CAN2	CAN 2 Transmit Pin	O			
		0011-1111	-	Reserved	-	-			
F[15]	MSCR[95]	0000 (Default)	GPIO[95]	SIUL2-GPIO[95]	General Purpose IO F[15]	I/O	113	140	A13
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[166]	0011	RXD	LIN1	LIN1 RXD	I			
	IMCR[34]	0001	RXD	CAN2	CAN2 RXD	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
G[2]	MSCR[98]	0000 (Default)	GPIO[98]	SIUL2-GPIO[98]	General Purpose IO G[2]	I/O	102	126	F17
		0001	X2	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 1	I/O			
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O			
		0011-1111	-	Reserved	-	-			
G[3]	MSCR[99]	0000 (Default)	GPIO[99]	SIUL2-GPIO[99]	General Purpose IO G[3]	I/O	104	128	E16
		0001	A2	FlexPWM_0	FlexPWM_0 Channel A Input/Output 2	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[63]	0010	ETC4	eTimer_0	eTimer_0 Input Data Channel 4	I			
G[4]	MSCR[100]	0000 (Default)	GPIO[100]	SIUL2-GPIO[100]	General Purpose IO G[4]	I/O	100	124	F16
		0001	B2	FlexPWM_0	FlexPWM_0 Channel B Input/Output 2	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[64]	0010	ETC5	eTimer_0	eTimer_0 Input Data Channel 5	I			
G[5]	MSCR[101]	0000 (Default)	GPIO[101]	SIUL2-GPIO[101]	General Purpose IO G[5]	I/O	85	107	M17
		0001	X3	FlexPWM_0	FlexPWM_0 Auxiliary Input/Output 3	I/O			
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O			
		0011-1111	-	Reserved	-	-			
G[6]	MSCR[102]	0000 (Default)	GPIO[102]	SIUL2-GPIO[102]	General Purpose IO G[6]	I/O	98	122	G17
		0001	A3	FlexPWM_0	FlexPWM_0 Channel A Input/Output 3	I/O			
		0010-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
G[7]	MSCR[103]	0000 (Default)	GPIO[103]	SIUL2-GPIO[103]	General Purpose IO G[7][6]	I/O	83	104	M16
		0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input/Output 3	I/O			
		0010	-	Reserved	-	-			
		0011	-	Reserved	-	-			
		0100-1111	-	Reserved	-	-			
G[8]	MSCR[104]	0000 (Default)	GPIO[104]	SIUL2-GPIO[104]	General Purpose IO G[8]	I/O	81	98	N14
		0001	FR_DBG[0]	FLEXRAY	FlexRay Debug Strobe Signal 0	O			
		0010	CS1	DSPI0	DSPI 0 Peripheral Chip Select 1	O			
		0011-1111	-	Reserved	-	-			
	IMCR[194]	0001	REQ21	SIUL2	SIUL2 External Interrupt Source 21	I			
	IMCR[83]	0011	FAULT0	FlexPWM_0	FlexPWM_0 Fault Input 0	I			
G[9]	MSCR[105]	0000 (Default)	GPIO[105]	SIUL2-GPIO[105]	General Purpose IO G[9]	I/O	79	96	P14
		0001	FR_DBG[1]	FLEXRAY	FlexRay Debug Strobe Signal 1	O			
		0010	CS1	DSPI1	DSPI 1 Peripheral Chip Select 1	O			
		0011-1111	-	Reserved	-	-			
	IMCR[202]	0001	REQ29	SIUL2	SIUL2 External Interrupt Source 29	I			
	IMCR[84]	0011	FAULT1	FlexPWM_0	FlexPWM_0 Fault Input 1	I			
G[10]	MSCR[106]	0000 (Default)	GPIO[106]	SIUL2-GPIO[106]	General Purpose IO G[10]	I/O	77	94	R17
		0001	FR_DBG[2]	FLEXRAY	FlexRay Debug Strobe Signal 2	O			
		0010	CS3	DSPI2	DSPI 2 Peripheral Chip Select 3	O			
		0011-1111	-	Reserved	-	-			
	IMCR[85]	0010	FAULT2	FlexPWM_0	FlexPWM_0 Fault Input 2	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
G[11]	MSCR[107]	0000 (Default)	GPIO[107]	SIUL2-GPIO[107]	General Purpose IO G[11]	I/O	75	92	T15
		0001	FR_DBG[3]	FLEXRAY	FlexRay Debug Strobe Signal 3	O			
		0010-1111	-	Reserved	-	-			
	IMCR[86]	0011	FAULT3	FlexPWM_0	FlexPWM_0 Fault Input 3	I			
H[4]	MSCR[116]	0000 (Default)	GPIO[116]	SIUL2-GPIO[116]	General Purpose IO H[4]	I/O		6	F4
		0001	X0	FlexPWM_1	FlexPWM_1 Auxiliary Input/Output 0	I/O			
		0010	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O			
		0011-1111	-	Reserved	-	-			
H[5]	MSCR[117]	0000 (Default)	GPIO[117]	SIUL2-GPIO[117]	General Purpose IO H[5]	I/O		7	F3
		0001	A0	FlexPWM_1	FlexPWM_1 Channel A Input/Output 0	I/O			
		0010	-	Reserved	-	-			
		0011	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O			
		0100-1111	-	Reserved	-	-			
	IMCR[105]	0010	A0	FlexPWM_1	FlexPWM_1 Channel A Input 0	I			
H[6]	MSCR[118]	0000 (Default)	GPIO[118]	SIUL2-GPIO[118]	General Purpose IO H[6]	I/O		138	C13
		0001	B0	FlexPWM_1	FlexPWM_1 Channel B Input/Output 0	I/O			
		0010	-	Reserved	-	-			
		0011	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O			
		0100-1111	-	Reserved	-	-			
	IMCR[106]	0010	B0	FlexPWM_1	FlexPWM_1 Channel B Input 0	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
H[7]	MSCR[119]	0000 (Default)	GPIO[119]	SIUL2-GPIO[119]	General Purpose IO H[7]	I/O		12	F2
		0001	X1	FlexPWM_1	FlexPWM_1 Auxiliary Input/Output 1	I/O			
		0010	ETC1	eTimer_2	eTimer_2 Input/Output Data Channel 1	I/O			
		0011-1111	-	Reserved	-	-			
H[8]	MSCR[120]	0000 (Default)	GPIO[120]	SIUL2-GPIO[120]	General Purpose IO H[8]	I/O		21	L1
		0001	A1	FlexPWM_1	FlexPWM_1 Channel A Input/Output 1	I/O			
		0010	-	Reserved	-	-			
		0011	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O			
		0100-1111	-	Reserved	-	-			
	IMCR[109]	0010	A1	FlexPWM_1	FlexPWM_1 Channel A Input 1	I			
H[9]	MSCR[121]	0000 (Default)	GPIO[121]	SIUL2-GPIO[121]	General Purpose IO H[9]	I/O		139	B13
		0001	B1	FlexPWM_1	FlexPWM_1 Channel B Input/Output 1	I/O			
		0010	-	Reserved	-	-			
		0011	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O			
		0100-1111	-	Reserved	-	-			
	IMCR[110]	0010	B1	FlexPWM_1	FlexPWM_1 Channel B Input 1	I			
H[10]	MSCR[122]	0000 (Default)	GPIO[122]	SIUL2-GPIO[122]	General Purpose IO H[10]	I/O			C7
		0001	X2	FlexPWM_1	FlexPWM_1 Auxiliary Input/Output 2	I/O			
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O			
		0011-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
H[11]	MSCR[123]	0000 (Default)	GPIO[123]	SIUL2-GPIO[123]	General Purpose IO H[11]	I/O		150	C9
		0001	A2	FlexPWM_1	FlexPWM_1 Channel A Input/Output 2	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[112]	0010	A2	FlexPWM_1	FlexPWM_1 Channel A Input 2	I			
H[12]	MSCR[124]	0000 (Default)	GPIO[124]	SIUL2-GPIO[124]	General Purpose IO H[12]	I/O		153	A7
		0001	B2	FlexPWM_1	FlexPWM_1 Channel B Input/Output 2	I/O			
		0010-1111	-	Reserved	-	-			
	IMCR[113]	0010	B2	FlexPWM_1	FlexPWM_1 Channel B Input 2	I			
H[13]	MSCR[125]	0000 (Default)	GPIO[125]	SIUL2-GPIO[125]	General Purpose IO H[13]	I/O			A14
		0001	X3	FlexPWM_1	FlexPWM_1 Auxiliary Input/Output 3	I/O			
		0010	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O			
		0011-1111	-	Reserved	-	-			
H[14]	MSCR[126]	0000 (Default)	GPIO[126]	SIUL2-GPIO[126]	General Purpose IO H[14]	I/O		89	P13
		0001	A3	FlexPWM_1	FlexPWM_1 Channel A Input/Output 3	I/O			
		0010	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O			
		0011-1111	-	Reserved	-	-			
H[15]	MSCR[127]	0000 (Default)	GPIO[127]	SIUL2-GPIO[127]	General Purpose IO H[15]	I/O		133	C17
		0001	B3	FlexPWM_1	FlexPWM_1 Channel B Input/Output 3	I/O			
		0010	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O			
		0011-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
I[0]	MSCR[128]	0000 (Default)	GPIO[128]	SIUL2-GPIO[128]	General Purpose IO I[0]	I/O		155	C6
		0001	ETC0	eTimer_2	eTimer_2 Input/Output Data Channel 0	I/O			
		0010	CS4	DSPI0	DSPI 0 Peripheral Chip Select 4	O			
		0011-1111	-	Reserved	-	-			
	IMCR[100]	0001	FAULT0	FlexPWM_1	FlexPWM_1 Fault Input 0	I			
I[1]	MSCR[129]	0000 (Default)	GPIO[129]	SIUL2-GPIO[129]	General Purpose IO I[1]	I/O		44	T3
		0001	ETC1	eTimer_2	eTimer_2 Input/Output Data Channel 1	I/O			
		0010	CS5	DSPI0	DSPI 0 Peripheral Chip Select 5	O			
		0011-1111	-	Reserved	-	-			
	IMCR[101]	0001	FAULT1	FlexPWM_1	FlexPWM_1 Fault Input 1	I			
I[2]	MSCR[130]	0000 (Default)	GPIO[130]	SIUL2-GPIO[130]	General Purpose IO I[2]	I/O		146	D11
		0001	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	I/O			
		0010	CS6	DSPI0	DSPI 0 Peripheral Chip Select 6	O			
		0011-1111	-	Reserved	-	-			
	IMCR[102]	0001	FAULT2	FlexPWM_1	FlexPWM_1 Fault Input 2	I			
I[3]	MSCR[131]	0000 (Default)	GPIO[131]	SIUL2-GPIO[131]	General Purpose IO I[3]	I/O		147	A10
		0001	ETC3	eTimer_2	eTimer_2 Input/Output Data Channel 3	I/O			
		0010	CS7	DSPI0	DSPI 0 Peripheral Chip Select 7	O			
		0011	EXT_TGR	CTU_0	CTU0 External Trigger Output	O			
		0100-1111	-	Reserved	-	-			
	IMCR[103]	0001	FAULT3	FlexPWM_1	FlexPWM_1 Fault Input 3	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
RDY_B /I[4]	MSCR[132]	0000 (Default)	GPIO[132]	SIUL2-GPIO[132]	General Purpose IO I[4]	I/O			J2
		0001	-	Reserved	-	-			
		0010	NEX_RDY_B	NPC_WRAPPER	Nexus data ready for transfer (RDY_B)	O			
		0011-1111	-	Reserved	-	-			
I[5]	MSCR[133]	0000 (Default)	GPIO[133]	SIUL2-GPIO[133]	General Purpose IO I[5][7]	I/O		102	N15
		0001	TXD	CAN2	CAN 2 Transmit Pin	O			
		0010	-	Reserved	-	-			
		0011	-	Reserved	-	O			
		0100-1111	-	Reserved	-	-			
I[6]	MSCR[134]	0000 (Default)	GPIO[134]	SIUL2-GPIO[134]	General Purpose IO I[6][8]	I/O		103	M15
		0001	-	Reserved	-	-			
		0010	-	Reserved	-	-			
		0011	-	Reserved	-	I			
		0100-1111	-	Reserved	-	-			
	IMCR[34]	0010	RXD	CAN2	CAN 2 Receive Pin	I			
I[7]	MSCR[135]	0000 (Default)	GPIO[135]	SIUL2-GPIO[135]	General Purpose IO I[7]	I/O		3	D2
		0001	LFAST_REF_CLK	MC_CGM	SIPI LFAST reference clock	-			
		0010-1111	-	Reserved	-	-			
	IMCR[717	0010	SENT_RX[0]	SENT0	SENT 0 Receiver channel 0	I			
I[8]	MSCR[136]	0000 (Default)	GPIO[136]	SIUL2-GPIO[136]	General Purpose IO I[8]	I/O			K4
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[213]	0010	SENT_RX[0]	SENT1	SENT 1 Receiver channel 0	I			
I[9]	MSCR[137]	0000 (Default)	GPIO[137]	SIUL2-GPIO[137]	General Purpose IO I[9]	I/O			L3
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O			
		0010-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
I[10]	MSCR[138]	0000 (Default)	GPIO[138]	SIUL2-GPIO[138]	General Purpose IO I[10]	I/O			M3
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O			
		0010-1111	-	Reserved	-	-			
I[11]	MSCR[139]	0000 (Default)	GPIO[139]	SIUL2-GPIO[139]	General Purpose IO I[11]	I/O			U3
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[206]	0001	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I			
I[12]	MSCR[140]	0000 (Default)	GPIO[140]	SIUL2-GPIO[140]	General Purpose IO I[12]	I/O			P5
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[214]	0001	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I			
I[13]	MSCR[141]	0000	GPIO[141]	SIUL2-GPIO[141]	General Purpose IO I[13]	I/O			P6
		0001	EXT_TGR	CTU_1	CTU1 External Trigger Output	I/O			
		0010-1111	-	Reserved	-	-			
I[14]	MSCR[142]	0000 (Default)	GPIO[142]	SIUL2-GPIO[142]	General Purpose IO I[14]	I/O			C10
		0001	CS0	DSPI3	DSPI 3 Peripheral Chip Select 0	O			
		0010-1111	-	Reserved	-	-			
I[15]	MSCR[143]	0000 (Default)	GPIO[143]	SIUL2-GPIO[143]	General Purpose IO I[15]	I/O			C1
		0001	SCK	DSPI3	DSPI 3 Serial Clock (output)	I/O			
		0010-1111	-	Reserved	-	-			
J[0]	MSCR[144]	0000 (Default)	GPIO[144]	SIUL2-GPIO[144]	General Purpose IO J[0]	I/O			C2
		0001	SOUT	DSPI3	DSPI 3 Serial Data Out	O			
		0010-1111	-	Reserved	-	-			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
J[1]	MSCR[145]	0000 (Default)	GPIO[145]	SIUL2-GPIO[145]	General Purpose IO J[1]	I/O			A12
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[50]	0001	SIN	DSPI3	DSPI 3 Serial Data Input	I			
J[2]	MSCR[146]	0000 (Default)	GPIO[146]	SIUL2-GPIO[146]	General Purpose IO J[2]	I/O			C11
		0001	CS1	DSPI3	DSPI 3 Peripheral Chip Select 1	O			
		0010-1111	-	Reserved	-	-			
J[3]	MSCR[147]	0000 (Default)	GPIO[147]	SIUL2-GPIO[147]	General Purpose IO J[3]	I/O			B15
		0001	CS2	DSPI3	DSPI 3 Peripheral Chip Select 2	O			
		0010-1111	-	Reserved	-	-			
J[4]	MSCR[148]	0000 (Default)	GPIO[148]	SIUL2-GPIO[148]	General Purpose IO J[4]	I/O			D13
		0001	CS3	DSPI3	DSPI 3 Peripheral Chip Select 3	O			
		0010-1111	-	Reserved	-	-			
	IMCR[39]	0001	EXT_IN	CTU_1	CTU 1 External Trigger Input	I			
J[5]	MSCR[149]	0000 (Default)	GPI[149][3] ADC2_ADC3_AN[0]	SIUL2-GPI[149]	General Purpose Input J[5]	I		64	P8
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[206]	0010	SENT_RX[1]	SENT0	SENT 0 Receiver channel 1	I			
J[6]	MSCR[150]	0000 (Default)	GPI[150][3] ADC2_ADC3_AN[1]	SIUL2-GPI[150]	General Purpose Input J[6]	I		65	P9
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
	IMCR[214]	0010	SENT_RX[1]	SENT1	SENT 1 Receiver channel 1	I			

Table 7. Pin Muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value	Signal	Module	Short Signal Description	Dir	LQFP144	LQFP176	BGA257
J[7]	MSCR[151]	0000 (Default)	GPI[151][3] ADC2_ADC3_AN[2]	SIUL2-GPI[151]	General Purpose Input J[7]	I		66	P10
		0001	-	Reserved	-	-			
		0010-1111	-	Reserved	-	-			
J[8]	MSCR[152]	0000 (Default)	GPIO[152]	SIUL2-GPIO[152]	General Purpose IO J[8]	I/O	95	119	G16
		0001	ETC4	eTimer_2	eTimer_2 Input/Output Data Channel 4	I/O			
		0010	ETC2	eTimer_2	eTimer_2 Input/Output Data Channel 2	-			
		0011-1111	-	Reserved	-	-			
	IMCR[34]	0011	RXD	CAN2	CAN 2 Receive Pin	I			
J[9]	MSCR[153]	0000 (Default)	GPIO[153]	SIUL2-GPIO[153]	General Purpose IO J[9]	I/O	16	20	K1
		0001	ETC5	eTimer_2	eTimer_2 Input/Output Data Channel 5	I/O			
		0010	NEX_RDY_B	NPC	Nexus data ready for transfer (RDY_B)	O			
		0011-1111	-	Reserved	-	-			
	IMCR[39]	0010	EXT_IN	CTU_1	CTU_1 External Trigger Input	I			

NOTES:

1. **(Default) = ALT mode configuration after reset.**
2. Changing B[5] configuration during debug might impact availability of TDI.
3. ADC analog input. Program corresponding MSCR APC bit and enable ADC to switch-on analog input path. See Table 13 for details.
4. Shared with SIPI LFAST transmit pad SIPI_TXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
5. Sine Wave Generator (SWG) output if SWG is enabled. See Table 13 for details.
6. Shared with SIPI LFAST receive pad SIPI_RXP. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
7. Shared with SIPI LFAST transmit pad SIPI_TXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.
8. Shared with SIPI LFAST receive pad SIPI_RXN. Alternative modes and GPIO must be disabled (OBE=0, IBE=0) if port is used for SIPI LFAST.

Table 8 list ports that are not implemented. The corresponding control and data registers are not implemented.

Table 8. Ports - Not Implemented

Port Name	Port Index
C	3,8,9
D	15,13
E	1,3,8
F	1,2
G	0,1
J	[15:12]
H	2,3

Any attempt to access unimplemented MSCRs generates a bus error. The read value from unimplemented ports must be masked in case of parallel port accesses.

2.2.6 Peripheral pin muxing

The following table describes the peripheral muxing capabilities of the MPC5744P. See the device Reference Manual for MSCR register addresses.

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherals	Source Functions
FlexCAN_0	RXD	IMCR[32]	0000_0000 (Default)[1]	-	Disable
			0000_0001	I/O-Pad	A[15]
			0000_0010	I/O-Pad	B[1]
			0000_0011-1 111_1111	-	Reserved
FlexCAN_1	RXD	IMCR[33]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[15]
			0000_0010	I/O-Pad	B[1]
			0000_0011-1 111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
FlexCAN_2	RXD	IMCR[34]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[15]
			0000_0010	I/O-Pad	I[6]
			0000_0011	I/O-Pad	J[8]
			0000_0100-1111_1111	-	Reserved
CTU_0	EXT_IN	IMCR[38]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[13]
			0000_0010	I/O-Pad	C[15]
			0000_0011-1111_1111	-	Reserved
CTU_1	EXT_IN	IMCR[39]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	J[4]
			0000_0010	I/O-Pad	J[9]
			0000_0011-1111_1111	-	Reserved
DSPI_0	SIN	IMCR[41]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[7]
			0000_0010-1111_1111	-	Reserved
DSPI_1	SIN	IMCR[44]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[8]
			0000_0010-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
DSPI_2	SIN	IMCR[47]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[13]
			0000_0010	I/O-Pad	A[2]
			0000_0011-1111_1111	-	Reserved
DSPI_3	SIN	IMCR[50]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	J[1]
			0000_0010-1111_1111	-	Reserved
eTimer_0	ETC0	IMCR[59]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[10]
			0000_0010	I/O-Pad	A[0]
			0000_0011-1111_1111	-	Reserved
eTimer_0	ETC1	IMCR[60]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[11]
			0000_0010	I/O-Pad	A[1]
			0000_0011-1111_1111	-	Reserved
eTimer_0	ETC2	IMCR[61]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[0]
			0000_0010	I/O-Pad	A[2]
			0000_0011-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
eTimer_0	ETC3	IMCR[62]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[14]
			0000_0010	I/O-Pad	A[3]
			0000_0011-1111_1111	-	Reserved
eTimer_0	ETC4	IMCR[63]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[14]
			0000_0010	I/O-Pad	G[3]
			0000_0011	I/O-Pad	A[4]
			0000_0100	I/O-Pad	C[11]
			0000_0101-1111_1111	-	Reserved
eTimer_0	ETC5	IMCR[64]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[8]
			0000_0010	I/O-Pad	G[4]
			0000_0011	I/O-Pad	C[12]
			0000_0100	I/O-Pad	E[13]
			0000_0101-1111_1111	-	Reserved
flexPWM_0	FAULT0	IMCR[83]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[9]
			0000_0010	I/O-Pad	A[13]
			0000_0011	I/O-Pad	G[8]
			0000_0100-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
flexPWM_0	FAULT1	IMCR[84]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[10]
			0000_0010	I/O-Pad	D[6]
			0000_0011	I/O-Pad	G[9]
			0000_0100-1 111_1111	-	Reserved
flexPWM_0	FAULT2	IMCR[85]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[5]
			0000_0010	I/O-Pad	G[10]
			0000_0011-1 111_1111	-	Reserved
flexPWM_0	FAULT3	IMCR[86]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[5]
			0000_0010	I/O-Pad	D[8]
			0000_0011	I/O-Pad	G[11]
			0000_0100-1 111_1111	-	Reserved
flexPWM_0	EXT_SYNC	IMCR[87]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[13]
			0000_0010	I/O-Pad	C[15]
			0000_0011-1 111_1111	-	Reserved
flexPWM_1	FAULT0	IMCR[100]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	I[0]
			0000_0010-1 111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
flexPWM_1	FAULT1	IMCR[101]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	I[1]
			0000_0010-1 111_1111	-	Reserved
flexPWM_1	FAULT2	IMCR[102]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	I[2]
			0000_0010-1 111_1111	-	Reserved
flexPWM_1	FAULT3	IMCR[103]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	I[3]
			0000_0010-1 111_1111	-	Reserved
flexPWM_1	A0	IMCR[105]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[13]
			0000_0010	I/O-Pad	H[5]
			0000_0011-1 111_1111	-	Reserved
flexPWM_1	B0	IMCR[106]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[14]
			0000_0010	I/O-Pad	H[6]
			0000_0011-1 111_1111	-	Reserved
flexPWM_1	A1	IMCR[109]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[12]
			0000_0010	I/O-Pad	H[8]
			0000_0011-1 111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
flexPWM_1	B1	IMCR[110]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[13]
			0000_0010	I/O-Pad	H[9]
			0000_0011-1111_1111	-	Reserved
flexPWM_1	A2	IMCR[112]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[4]
			0000_0010	I/O-Pad	H[11]
			0000_0011-1111_1111	-	Reserved
flexPWM_1	B2	IMCR[113]	0000_0000	-	Disable
			0000_0001	I/O-Pad	E[14]
			0000_0010	I/O-Pad	H[12]
			0000_0011-1111_1111	-	Reserved
flexRay	FR_A_RX	IMCR[136]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[1]
			0000_0010-1111_1111	-	Reserved
flexRay	FR_B_RX	IMCR[137]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[2]
			0000_0010-1111_1111	-	Reserved
LIN_0	RXD	IMCR[165]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[3]
			0000_0010	I/O-Pad	B[7]
			0000_0011-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
LIN_1	RXD	IMCR[166]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[13]
			0000_0010	I/O-Pad	D[12]
			0000_0011	I/O-Pad	F[15]
			0000_0100-1111_1111	-	Reserved
MC_RGM	ABS1	IMCR[169]	0000_0000 (Default)	I/O-Pad	A[2]
			0000_0001	-	Disable
			0000_0010-1111_1111	-	Reserved
MC_RGM	ABS2	IMCR[171]	0000_0000 (Default)	I/O-Pad	A[3]
			0000_0001	-	Disable
			0000_0010-1111_1111	-	Reserved
MC_RGM	FAB	IMCR[172]	0000_0000 (Default)	I/O-Pad	A[4]
			0000_0001	-	Disable
			0000_0010-1111_1111	-	Reserved
SIUL	REQ0	IMCR[173]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[0]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ1	IMCR[174]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[1]
			0000_0010-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherals	Source Functions
SIUL	REQ2	IMCR[175]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[2]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ3	IMCR[176]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[3]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ4	IMCR[177]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[4]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ5	IMCR[178]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[5]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ6	IMCR[179]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[6]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ7	IMCR[180]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[7]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ8	IMCR[181]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[8]
			0000_0010-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
SIUL	REQ9	IMCR[182]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[10]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ10	IMCR[183]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[11]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ11	IMCR[184]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[12]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ12	IMCR[185]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[13]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ13	IMCR[186]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[14]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ14	IMCR[187]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	A[15]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ15	IMCR[188]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[0]
			0000_0010-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherals	Source Functions
SIUL	REQ16	IMCR[189]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[1]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ17	IMCR[190]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[2]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ18	IMCR[191]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[6]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ19	IMCR[192]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[14]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ20	IMCR[193]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	B[15]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ21	IMCR[194]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	G[8]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ22	IMCR[195]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[4]
			0000_0010-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
SIUL	REQ23	IMCR[196]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[5]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ24	IMCR[197]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	C[6]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ25	IMCR[198]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	E[13]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ26	IMCR[199]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	E[14]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ27	IMCR[200]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	E[15]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ28	IMCR[201]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[0]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ29	IMCR[202]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	G[9]
			0000_0010-1111_1111	-	Reserved

Table 9. Peripheral Muxing

Destination Peripherals	Destination Functions	IMCR Register	IMCR:SSS Field Value	Source Peripherials	Source Functions
SIUL	REQ30	IMCR[203]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[12]
			0000_0010-1111_1111	-	Reserved
SIUL	REQ31	IMCR[204]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	F[13]
			0000_0010-1111_1111	-	Reserved
SENT_0	SENT_RX[0]	IMCR[205]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[5]
			0000_0010	I/O-Pad	I[7]
			0000_0011-1111_1111	-	Reserved
SENT_0	SENT_RX[1]	IMCR[206]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	I[11]
			0000_0010	I/O-Pad	J[5]
			0000_0011-1111_1111	-	Reserved
SENT_1	SENT_RX[0]	IMCR[213]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	D[7]
			0000_0010	I/O-Pad	I[8]
			0000_0011-1111_1111	-	Reserved
SENT_1	SENT_RX[1]	IMCR[214]	0000_0000 (Default)	-	Disable
			0000_0001	I/O-Pad	I[12]
			0000_0010	I/O-Pad	J[6]
			0000_0011-1111_1111	-	Reserved

[1] (Default) = configuration after reset.

Peripheral Muxing Example:
SSS field in IMCR register 214: 0x1
I/O-Pad I[12] is connected to SENT_1 Receive input SENT_RX[1]
SSS field in IMCR register 214: 0x2
I/O-Pad J[6] is connected to SENT_1 Receive input SENT_RX[1]

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at TBD (design target: 180 MHz or greater). The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

NOTE

The specification classifications in the “Symbol” column of the tables are preliminary and may change in future releases of this document.

3.2 Absolute maximum ratings

Table 10. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{DD\_HV\_PMU}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	4.0[3, 4]	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	3.63[3, 4]	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	3.63[3, 4]	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.0[3, 4]	V

Table 10. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADRE0}$[5] $V_{DD\_HV\_ADRE1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADRE0}$ $V_{SS\_HV\_ADRE1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.0[3, 4]	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Supply ramp rate	—	0.5	3.0×10^6 (3.0 V / s)	V/µs
V_{INA}	SR	Voltage on analog pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	–0.3	6.0	V
V_{IN}	SR	Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IOx}$)	Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3[6]	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	165	°C

NOTES:
1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. 5.3 V for 10 hours cumulative over lifetime of device, 3.3 V +10% for time remaining.
4. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
5. $V_{DD\_HV\_ADRE0}$ and $V_{DD\_HV\_ADRE1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.
6. Only when $V_{DD\_HV\_IOx} < 3.63$ V.

3.3 Recommended operating conditions

Table 11. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD\_HV\_PMU}$	SR	3.3 V voltage regulator supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V

Table 11. Recommended operating conditions ($V_{DD\_HV\_xx}$ = 3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD\_HV\_ADRE0}$[2] $V_{DD\_HV\_ADRE1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	3.0 to 5.5		V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	3.15	3.6	V
$V_{SS\_HV\_ADRE0}$[2] $V_{SS\_HV\_ADRE1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_COR}$	SR	Core supply, 1.25 V +/-5%	—	1.19	1.32	V
$V_{DD\_LV\_CORx}$	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$	SR	Internal PLL supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_PLL}$[3]	SR	Internal PLL reference voltage	—	0	0	V
$V_{DD\_LV\_NEXUS}$	SR	Aurora LVDS supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_NEXUS}$	SR	Aurora LVDS supply ground	—	0	0	V
$V_{DD\_LV\_LFAST}$	SR	LFAST supply voltage	—	1.19	1.32	V
$V_{SS\_LV\_LFAST}$	SR	LFAST supply ground	—	0	0	V
T_A	SR	Ambient temperature under bias	$f_{CPU} \le$ TBD[3]	–40	TBD	°C
T_J	SR	Junction temperature under bias	—	–40	165	°C

NOTES:
1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. $V_{DD\_HV\_ADRE0}$ and $V_{DD\_HV\_ADRE1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.
3. Maximum frequency is TBD (design target: 180 MHz or greater).

3.4 Thermal characteristics

Table 12. Thermal characteristics for 144 LQFP package[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[2]	Single layer board – 1s	42	°C/W
				Four layer board – 2s2p	34	
$R_{\theta JMA}$	CC	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	34	°C/W
				Four layer board – 2s2p	28	
$R_{\theta JB}$	CC	D	Thermal resistance junction-to-board[3]	—	22	°C/W
$R_{\theta JC}$	CC	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	CC	D	Junction-to-package-top natural convection[5]	—	3	°C/W

NOTES:
1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 13. Thermal characteristics for 176 LQFP-EP package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection[2]	Single layer board – 1s	43	°C/W
			Four layer board – 2s2p	24	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	34	°C/W
			Four layer board – 2s2p	18	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	12	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case top[4]	—	10	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	3	°C/W

NOTES:
1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 14. Thermal characteristics for 257 MAPBGA package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	26	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	37	°C/W
			Four layer board – 2s2p	22	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	13	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	2	°C/W

NOTES:
1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.4.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.5 Electromagnetic Interference (EMI) characteristics

The Electromagnetic Interference (EMI) target characteristics are shown in Table 16:

- Device configuration, test conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in Table 16 is explained in Table 15.

Table 15. EMI configuration summary

Configuration name	Description
Configuration A	• High emission = all pads have max slew rate, LVDS pads running at 40 MHz • Oscillator frequency = 40 MHz • System bus frequency = 80 MHz • No PLL frequency modulation • IEC level I (≤ 36 dBµV)
Configuration B	• Reference emission = pads use min, mid and max slew rates, LVDS pads disabled • Oscillator frequency = 40 MHz • System bus frequency = 80 MHz • 2% PLL frequency modulation • IEC level K(≤ 30 dBµV)

Table 16. EMI emission testing specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{EME}	CC	Radiated emissions	Configuration A; frequency range 150 kHz–50 MHz	—	16	—	dBµV
			Configuration A; frequency range 50–150 MHz	—	16	—	
			Configuration A; frequency range 150–500 MHz	—	32	—	
			Configuration A; frequency range 500–1000 MHz	—	25	—	
			Configuration B; frequency range 50–150 MHz	—	15	—	
			Configuration B; frequency range 50–150 MHz	—	21	—	
			Configuration B; frequency range 150–500 MHz	—	30	—	
			Configuration B; frequency range 500–1000 MHz	—	24	—	

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 17. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

NOTES:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.7 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_MAIN_4) for 3.3 V ADC supply (V_{DDADC})
- Low voltage detector (LVD_MAIN_5) for 3.3 V OSC supply (V_{DDOSC})
- Low voltage detector (LVD_CORE) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_CORE_BK) for the self-test of LVD_CORE
- High voltage detector (HVD_CORE) for 1.2 V digital core supply (HPV_{DD})
- High voltage detector (HVD_CORE_BK) for the self-test of HVD_CORE.
- Power on Reset (POR)

The following bipolar transistors are supported:

- BCP68 from ON Semiconductor
- NJD2873
- NSS20501Uw3

Table 18. Voltage regulator electrical specifications

Symbol		C	Parameter	Conditions	Min	Typ	Max	Unit
C_{ld}	SR	—	External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	10	—		µF
	SR	—	Combined ESR of external capacitor	—	0.03	—	0.15	Ω
t_{SU}	CC		Start-up time after main supply stabilization	C_{ld} = 10 µF	—	—	2.5	ms
L_{bw}	SR	—	Bonding inductance				13	nH
R_{bw}	SR	—	Bonding wire and pad resistance				0.5	Ω
R_{sd}	SR	—	Series resistance of on-chip power grid				0.1	Ω
C_{sd}	SR	—	On-chip power grid to ground capacitance				tbd	nF
C_{pd}	SR	—	Parallel decoupling capacitor	per pin, no more than 300 nF total	47			nF
R_{sn}	SR	—	Snubber resistor for stability	dep. on transistor			tbd	Ω
C_{sn}	SR	—	Snubber capacitor for stability	dep. on transistor			tbd	nF
—	SR	—	Power Supply Rejection (C_{ld}=10uF)	@DC no load @200 kHz no load @DC 400 mA @200 kHz 400 mA			-23 -23 -23 -23	dB dB dB dB
—	SR	—	Load current transient	I_{load} from 20% to 80% C_{ld} = 10 µF			1.0	µs
—	CC	D	Supply ramp rate VDD12_CORE	—	0.01	—	1	V/ms
—	CC	D	Supply Ramp Rate VDD33_REG	—	25	—	1000	V/ms
—	CC	T	POR VDD12_CORE		0.98	1.02	1.08	V
	CC	T	POR VDD33_REG		2.4	2.59	2.76	V
	CC	P	LVD_CORE, LVD_CORE_BK	calibrated (trimmed)	1.12	1.15	1.18	V
	CC	P	HVD_CORE, HVD_CORE_BK	calibrated (trimmed)	1.32	1.36	1.40	V
	CC	P	LVD_REG	calibrated (trimmed)	2.93	3.05	3.13	V
	CC	P	LVD_IO	calibrated (trimmed)	2.93	3.05	3.13	V

Table 18. Voltage regulator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Min	Typ	Max	Unit
	CC	P	LVD_FLS	calibrated (trimmed)	2.93	3.05	3.13	V
	CC	P	LVD_ADC	calibrated (trimmed)	2.93	3.05	3.13	V
	CC	P	LVD_OSC	calibrated (trimmed)	2.93	3.05	3.13	V
	CC	T	Hysteresis LVD_CORE			20		mV
	CC	T	Hysteresis HVD_CORE			20		mV
	CC	T	Hysteresis LVD_xxx			20		mV
	CC	T	LVD/HVD trimming	16 steps		5		mV
T_j	CC	T	Junction Temperature		-40	—	165	°C

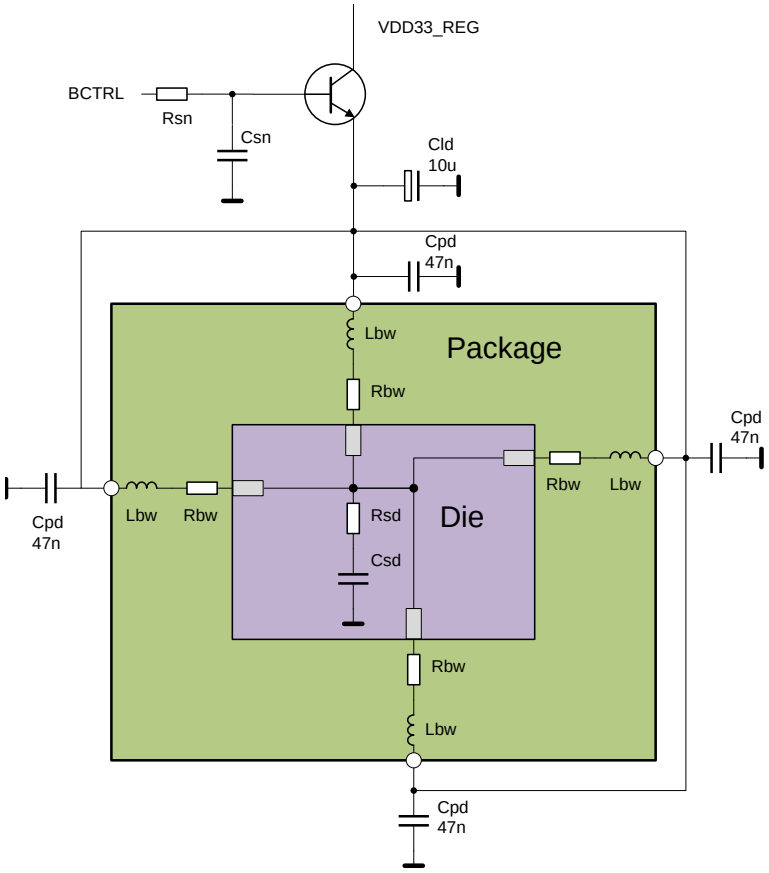


Figure 19. Core supply decoupling and parasitics

3.8 DC electrical characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 20 provides output driver characteristics FlexRay I/Os (SYM).
- Table 21 provides output driver characteristics for LFAST I/Os.

Table 20. FlexRay (SYM) configuration output buffer electrical characteristics[1]

Symbol		C	Parameter	Conditions[2]	Value[3]			Unit
					Min	Typ	Max	
R_{OH_Y}	CC	P	PMOS output impedance SYM configuration	Push Pull, I_{OH} = 2 mA, $V_{OH} = V_{DD\_HV\_IOx}$ - (0.28...0.52 V)	35	50	65	Ω
R_{OL_Y}	CC	P	PMOS output impedance SYM configuration	Push Pull, I_{OL} = 2 mA, V_{OL} = 0.28...0.52 V	35	50	65	Ω
F_{max_Y}	CC	T	Output frequency SYM configuration	C_L= 20pF(3), $V_{DD\_HV\_IOx}$ = 3.3 V –5%, +10%	—	—	50	MHz
T_{tr_Y}	CC	T	Transition time output pin SYM configuration	C_L = 20 pF(3), $V_{DD\_HV\_IOx}$ = 3.3 V –5%, +10%	1	—	6	ns
$\lvert T_{skew\_Y} \rvert$	CC	T	Difference between rise and fall time	—	0	—	1	ns

NOTES:
1 Please refer to FlexRay section for parameter dedicated to this interface.
2 $V_{DD\_HV\_IOx}$ = 3.3 V (–5%, +10%), T_J = –40 / 165 °C, unless otherwise specified
3 All values need to be confirmed during device validation.

Table 21. LFAST output buffer electrical characteristics[1]

Symbol		C	Parameter	Conditions[2]	Value[3]			Unit
					Min	Typ	Max	
$\lvert \Delta_{VO\_L} \rvert$	CC	T	Absolute value for differential output voltage swing (terminated)	—	100	200	285	mV
V_{ICOM_L}	CC	T	Common mode voltage	—	1.08	1.2	1.32	V
T_{tr_L}	CC	T	Transition time output pin LVDS configuration	—	0.2	—	1.5	ns

NOTES:
1 Please refer to LFAST section for parameter dedicated to this interface.
2 $V_{DD\_HV\_IOx}$ = 3.3 V (–5%, +10%), T_J = –40 / 165 °C, unless otherwise specified
3 All values need to be confirmed during device validation.

NOTE

Fast IOs must be specified only as fast (and not as high current). See Table 22.

Table 22. DC Electrical Specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Vdd[1]	CC	D	LV (core) Supply Voltage	—	1.18	—	1.32	V
Vdde[1]	SR	—	I/O Supply Voltage	—	3.15	—	3.6	V
Vih	CC	D	CMOS Input Buffer High Voltage (with hysteresis disabled)	—	0.55 * Vdde	—	Vdde + 0.3	V
Vil	CC	D	CMOS Input Buffer Low Voltage (with hysteresis disabled)	—	Vss - 0.3	—	0.40 * Vdde	V
Vhys	CC	D	CMOS Input Buffer Hysteresis	—	0.1 * Vdde	—		V
Pull_Ioh	CC	D	Weak Pullup Current[2]	—	15	—	50	uA
Pull_Iol	CC	D	Weak Pulldown Current[3]	—	15	—	50	uA
Iinact_d	CC	D	Digital Pad Input Leakage Current (weak pull inactive)	—	-2.5	—	2.5	uA
Voh	CC	D	Output High Voltage[4]	—	0.8 * Vdde	—	-	V
Vol	CC	D	Output Low Voltage[5]	—	-	—	0.2 * Vdde	V
Ioh_f	CC	D	Full drive Ioh[6] (ipp_sre[1:0] = 11)	—	18	—	70	mA
Iol_f	CC	D	Full drive Iol[6] (ipp_sre[1:0] = 11)	—	21	—	120	mA
Ioh_h	CC	D	Half drive Ioh[6] (ipp_sre[1:0] = 10)	—	9	—	35	mA
Iol_h	CC	D	Half drive Iol[6] (ipp_sre[1:0] = 10)	—	10.5	—	60	mA

Note:

1. Max power supply ramp rate is 100 V / ms
2. Measured when pad = 0 V
3. Measured when pad = VDDE
4. Measured when pad is sourcing 2 mA.
5. Measured when pad is sinking 2 mA.
6. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

3.9 Supply current characteristics

Current consumption data is given in Table 23. These specifications are design targets and are subject to change per device characterization.

Table 23. Current consumption characteristics

Symbol		C	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_LV\_TYP}$[2] + $I_{DD\_LV\_PLL}$	CC	P	Operating current	1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	400 mA	TBD	mA
	CC	C		1.2 V supplies T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	480 mA	—	
$I_{DD\_LV\_FULL}$[3] + $I_{DD\_LV\_PLL}$	CC	C	Operating current	1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	570 mA	mA
	CC			1.2 V supplies T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	660 mA	
$I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$	CC	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	mA
	CC	T		1.2 V supplies T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
	CC	T		1.2 V supplies T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
$I_{DD\_LV\_STOP}$	CC	T	Operating current in V_{DD} STOP mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	mA
	CC	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
	CC	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
	CC	T		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
$I_{DD\_LV\_HALT}$	CC	T	Operating current in V_{DD} HALT mode	T_A = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	mA
	CC	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
	CC	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	
	CC	T		T_J = 165 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	TBD	

Table 23. Current consumption characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_HV\_ADV}$[4,5]	CC	T	Operating current	T_J = 150 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	—	TBD	mA
	CC	T		T_J = 165 °C 4 ADCs operating at 80 MHz $V_{DD\_HV\_ADV}$ = 3.6 V	—	—	TBD	
$I_{DD\_HV\_ADRE}$[5]	CC	T	Operating current	T_J = 150 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	—	TBD	mA
				T_J = 150 °C TBD frequency[6] ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	—	TBD	
				T_J = 165 °C ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 3.6 V	—	—	TBD	
				T_J = 165 °C TBD frequency[6] ADC operating at 80 MHz $V_{DD\_HV\_ADRE}$ = 5.5 V	—	—	TBD	
$I_{DD\_HV\_OSC}$	CC	T	Operating current	T_J = 150 °C 3.3 V supplies TBD frequency[6]	—	—	TBD	µA
				T_J = 165 °C 3.3 V supplies TBD frequency[6]	—	—	TBD	
$I_{DD\_HV\_FLASH}$	CC	T	Operating current	T_J = 150 °C 3.3 V supplies TBD frequency[6]	—	—	TBD	mA
				T_J = 165 °C 3.3 V supplies TBD frequency[6]	—	—	TBD	

NOTES:
1. The content of the Conditions column identifies the components that draw the specific current.
2. Enabled Modules in 'Typical mode': two FlexCANs, ADC0/1, CTU, FlexPWM, three eTimers, three DSPIs, SWG, DMA, STM, SWT, PIT (list subject to change). At maximum frequency. I/O supply current excluded.
3. Enabled Modules in 'Full mode': TBD. At maximum frequency. I/O supply current excluded.
4. Internal structures hold the input voltage less than VDD_HV_ADV + 1.0 V on all pads powered by VDDA supplies, if the maximum injection current specification is met (3 mA for all pins) and VDDA is within the operating voltage specifications.
5. This value is the total current for four ADCs.
6. Maximum frequency is TBD (design target: 180 MHz or greater).

3.10 Temperature Sensor

The following table describes the temperature sensor electrical characteristics.

Table 24. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Temperature monitoring range	—	-40	—	165	°C
—	CC	C	Sensitivity	—	—	5.18	—	mV/°C
—	CC	T	Accuracy	T_J = -40 to 165 °C	TBD	—	TBD	°C
—	CC	C	Operating Current	T_J = -40 to 165 °C	—	—	600	µA

3.11 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver. Figure 5 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

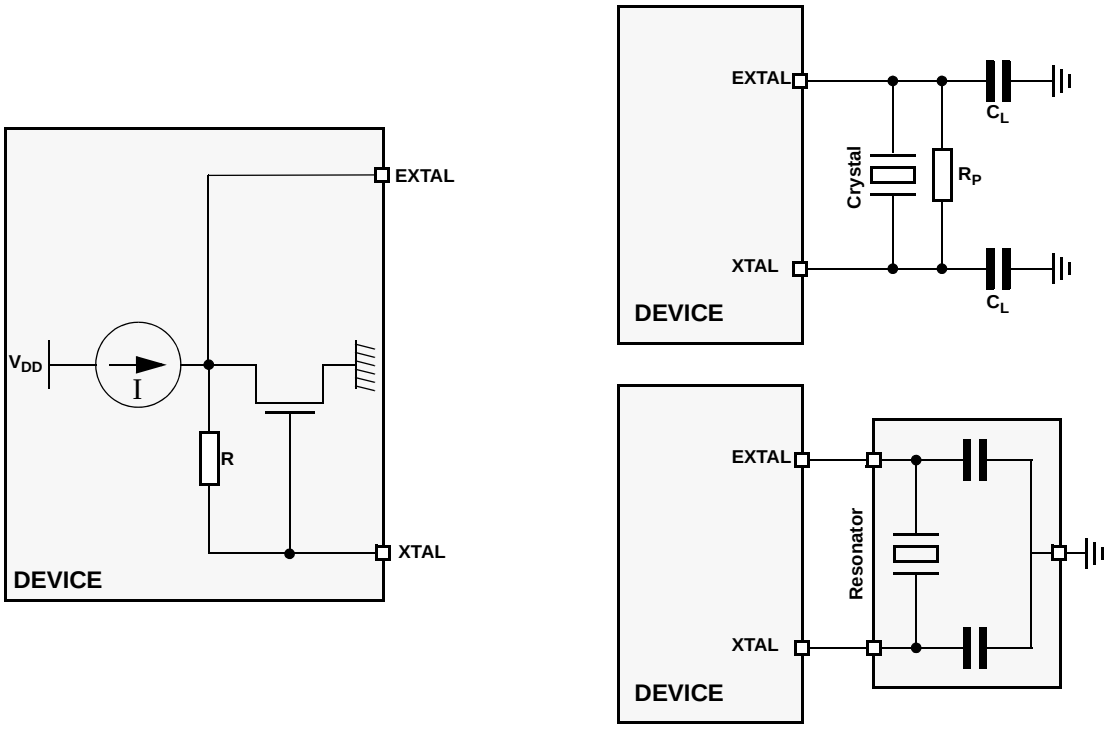


Figure 5. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

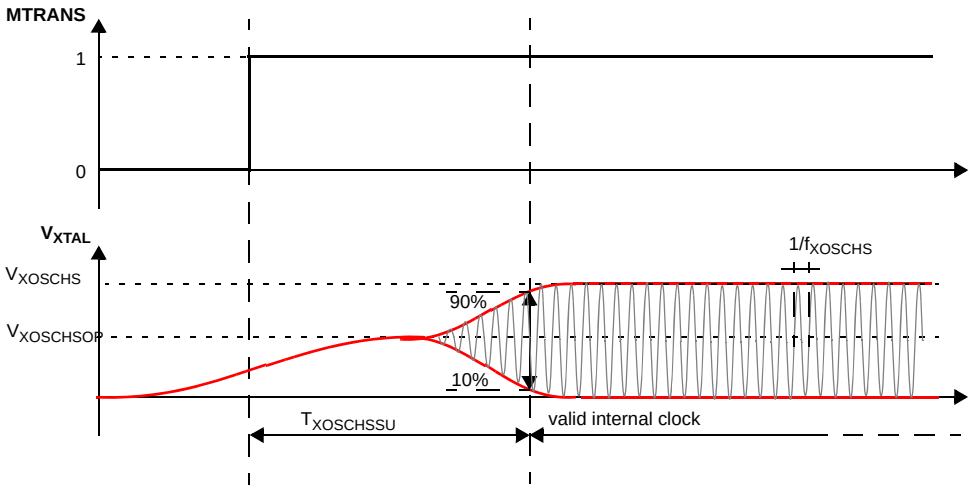


Figure 6. Main oscillator electrical characteristics

Table 25. Main oscillator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{XOSCHS}	SR	—	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	CC	P	Oscillator transconductance	$V_{DD\_HV\_OSC}$ = 3.3 V –5%, +10%	TBD	TBD	TBD	mA/V
V_{XOSCHS}	CC	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz		TBD		V
				f_{OSC} = 40 MHz		TBD		
$V_{XOSCHSOP}$	CC	D	Oscillation operating point	—		TBD		V
I_{XOSCHS}	CC	D	Oscillator consumption	—		TBD		mA
$T_{XOSCHSSU}$	CC	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz[2]		TBD		ms
				f_{OSC} = 16, 40 MHz[2]		TBD		
V_{IH}	SR	—	Input high level CMOS Schmitt Trigger	Oscillator bypass mode		TBD		V
V_{IL}	SR	—	Input low level CMOS Schmitt Trigger	Oscillator bypass mode		TBD		V

NOTES:
1 $V_{DD\_HV\_OSC}$ = 3.3 V -5%,+±10%, T_J = –40 to +165 °C, unless otherwise specified.
2 The recommended configuration for maximizing the oscillator margin are:
XOSC_MARGIN = 0 for 4 MHz quartz
XOSC_MARGIN = 1 for 8/16/40 MHz quartz

3.12 FMPLL electrical characteristics

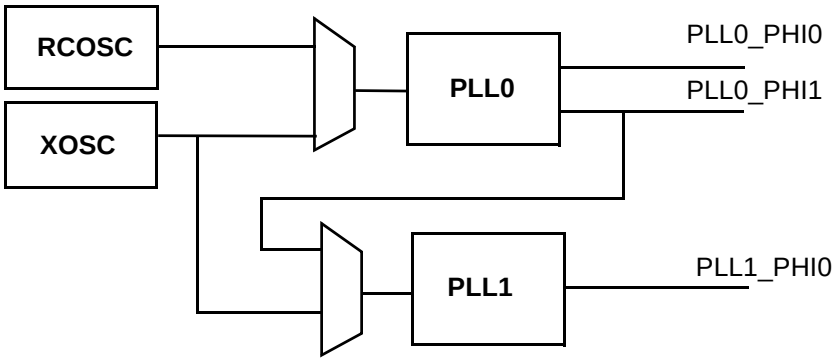


Figure 7. PLL integration

Table 26. PLL0 electrical characteristics

Symbol			Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock[2]	—	14	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	CC	D	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output clock PHI0	—	4.76	—	625	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	156	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL0LTJ}\rvert$	CC	T	PLL0 long term jitter f_{PLL0IN} = 8 MHz (resonator),	$f_{PLL0PHI0}$ = 40 MHz, 1 µs	—	—	0.1	%
				$f_{PLL0PHI0}$ = 40 MHz, 13 µs	—	—	TBD	%
I_{PLL0}	CC	C	PLL0 consumption	FINE LOCK state	—	—	5	mA

NOTES:
1 V_{DD_LV} =1.25 V ± 5%, T_J = -40 / 165 °C unless otherwise specified.
2 PLL0IN clock retrieved directly from either internal RCOSC or external XOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.

Table 27. FMPLL1 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLL1IN}	SR	—	PLL1 input clock[2]	—	38	—	78	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle[2]	—	35	—	65	%
$f_{PLL1VCO}$	CC	D	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	CC	D	PLL1 output clock PHI0	—	4.76	—	625	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	CC	T	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
				Down spread	0.5	—	4	%
I_{PLL1}	CC	C	PLL1 consumption	FINE LOCK state	—	—	6	mA

NOTES:
1 V_{DD_LV} =1.25 V ± 5%, T_J = -40 / 165 °C unless otherwise specified.
2 PLL1IN clock retrieved directly from either internal PLL0 or external FXOSC clock. Input characteristics are granted when using internal PPL0 or external oscillator is used in functional mode.

3.13 Internal 16 MHz RC oscillator electrical characteristics

Table 28. Internal RC Oscillator electrical specifications

($V_{DD\_HV\_PMU}$ = 3.15 V to 3.6 V, V_{SS} = 0 V, V_{DD_LV} = 1.18 V to 1.32 V, V_{SS} = 0 V, T_J = –40 / 165 °C)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
$F_{Untrimmed}$	CC	D	IRC frequency (Untrimmed)	—	9.6	—	24	MHz
δF_{var_noT}	CC	P	IRC frequency variation without temperature compensation[1]	T_J < 150 °C	–8	—	+8	%
				T_J < 165 °C	–10	—	+10	
$T_{startup}$	CC	T	Startup time without temperature compensation[1]		—	—	5	µs
I_{VDD3}	CC	T	Current consumption on 3.3V power supply	After $T_{startup}$	—	—	55	µA
I_{VDD12}	CC	T	Current consumption on 1.2V power supply	After $T_{startup}$	—	—	270	µA

NOTES:
1 Pending silicon characterization

3.14 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

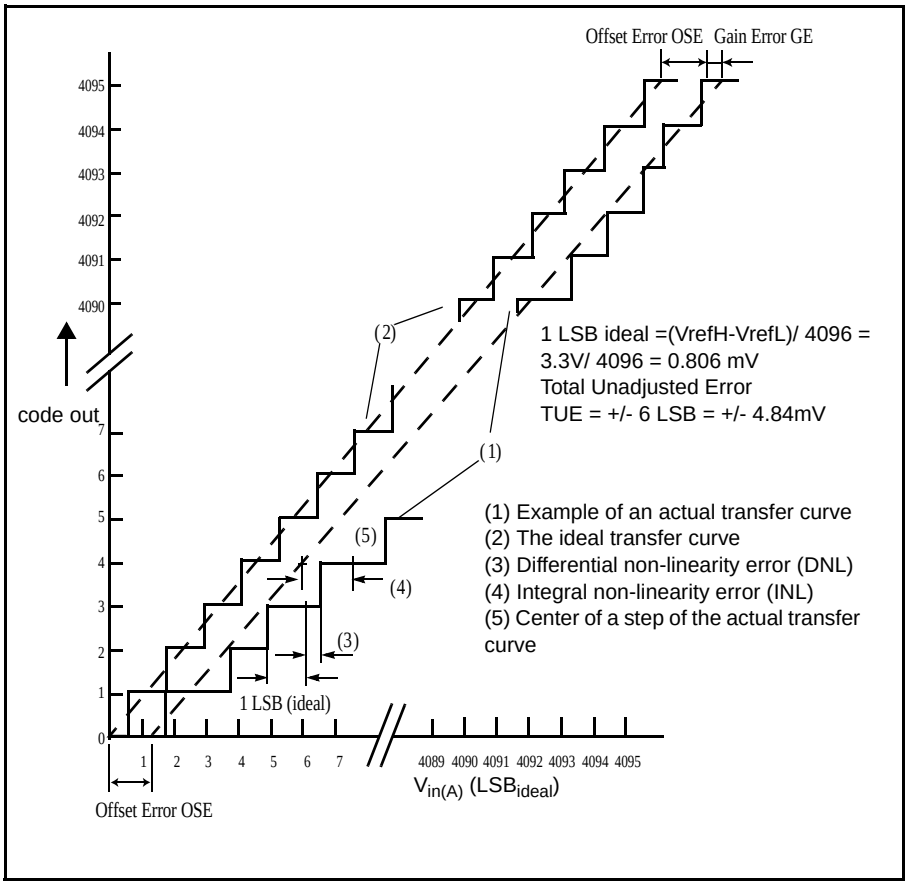


Figure 8. ADC characteristics and error definitions

3.14.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz,

with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_C \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 9:

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 9}$$

Equation 9 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

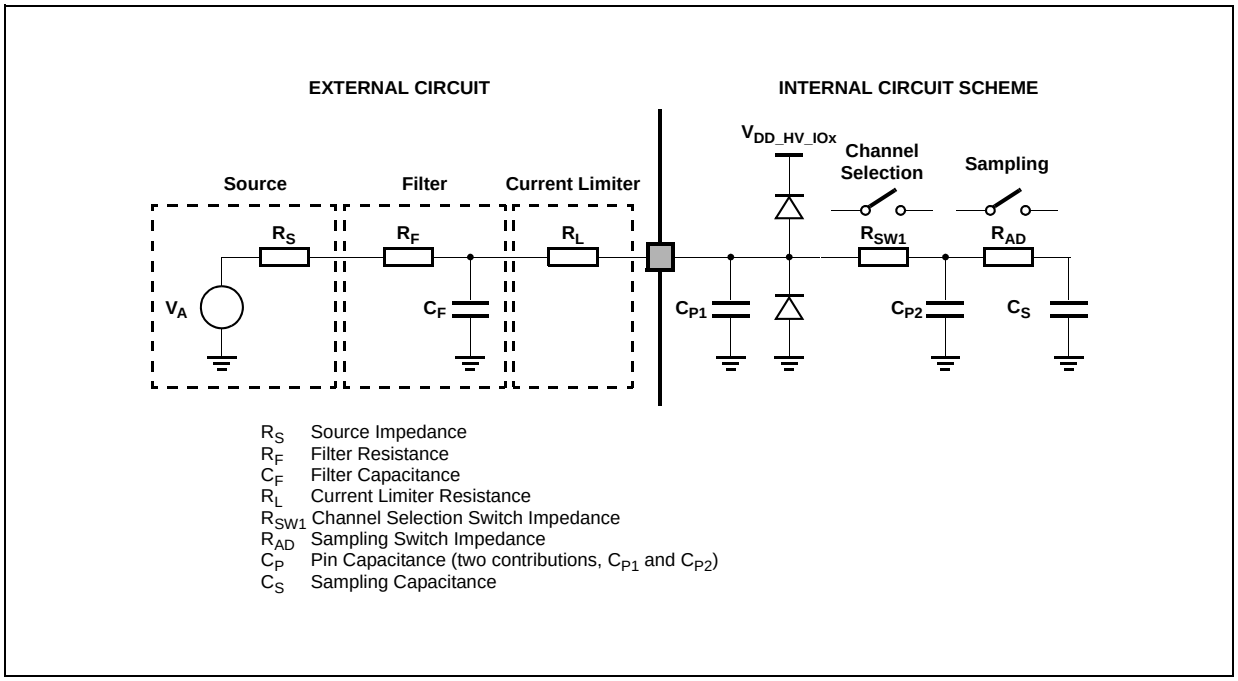


Figure 29. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 29): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

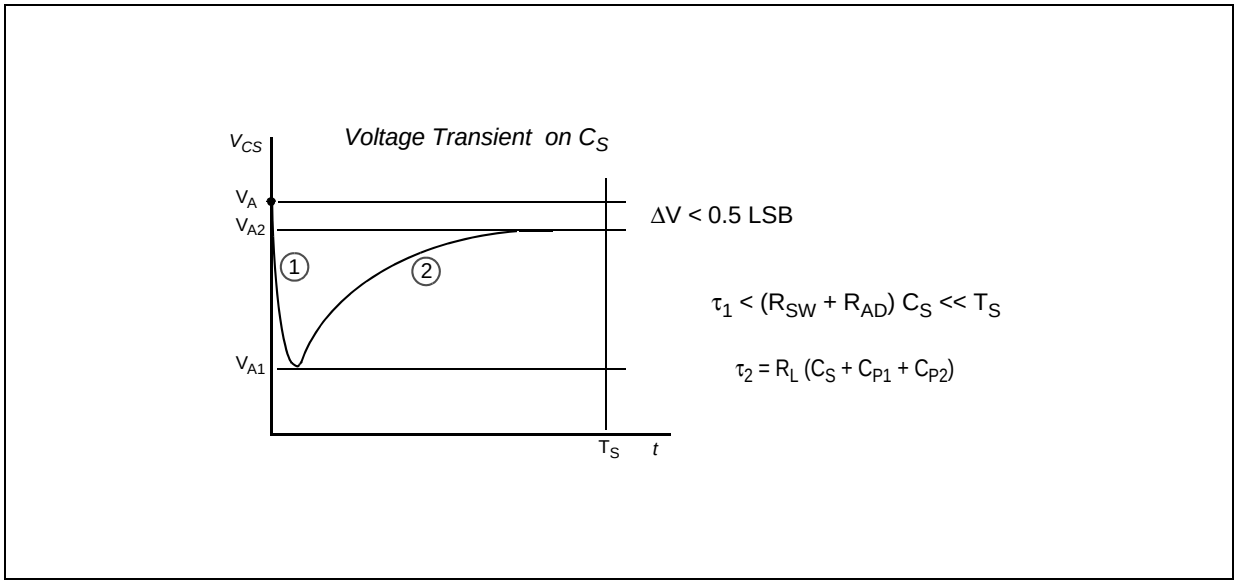


Figure 30. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 10}$$

  Equation 10 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S \qquad \textit{Eqn. 11}$$

  The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 12:

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2}) \qquad \textit{Eqn. 12}$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2}) \qquad \textit{Eqn. 13}$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S \qquad \textbf{Eqn. 14}$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 15 must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S) \qquad \textbf{Eqn. 15}$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

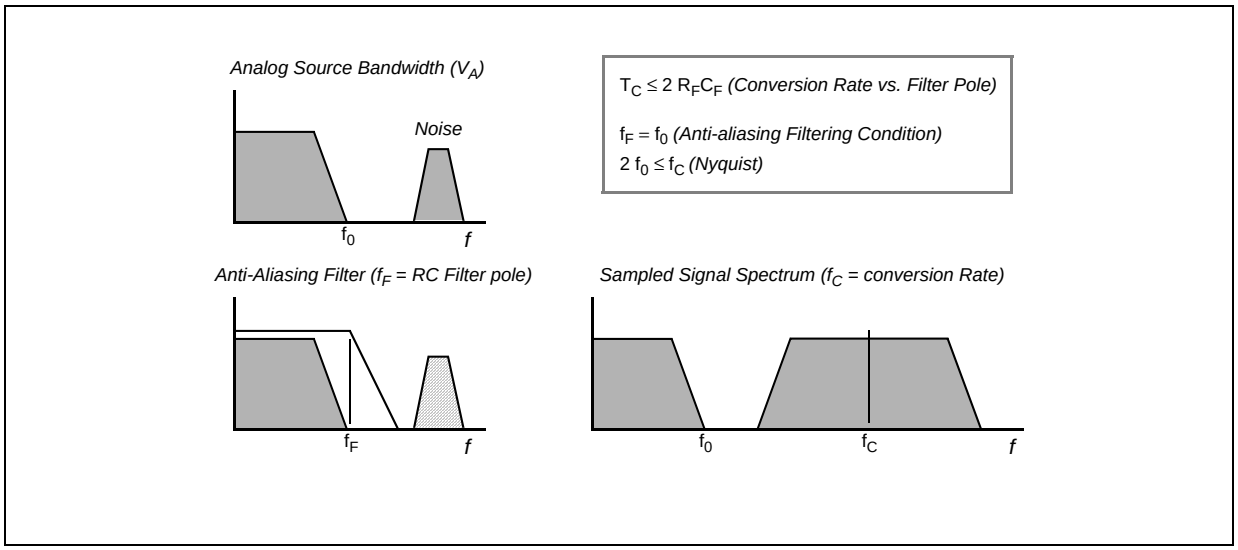


Figure 31. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 16 between the ideal and real sampled voltage on C_S:

Eqn. 16

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 17

$$C_F > 2048 \bullet C_S$$

Table 32. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	SR	—	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	20	—	80	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	CC	D	Sample time[3]	80 MHz@200 Ohm source impedance	275	—	—	ns
t_{conv}	CC	D	Conversion time[4]	80 MHz	650	—	—	ns
C_S[5]	CC	D	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	CC	D	ADC input pin capacitance 1 - TBD not in ADC spec	—	—	—	5(6)	pF
C_{P2}[5]	CC	D	ADC input pin capacitance 2 - TBD not in ADC spec	—	—	—	0.8	pF
R_{SW1}[5]	CC	D	Internal resistance of analog source - TBD not in ADC spec	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
	CC			V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[5]	CC	D	Internal resistance of analog source - TBD not in ADC spec	—	—	—	825	Ω
INL	CC	D	Integral non linearity	—	–2	—	2	LSB
DNL	CC	D	Differential non linearity[7]	—	–1	—	1	LSB
OFS	CC	T	Offset error	—	–4	—	4	LSB
GNE	CC	T	Gain error	—	–4	—	4	LSB
Input (single ADC channel)	CC	D	Max leakage	150C	—	—	250	nA
	CC	D	Max positive/negative injection		–3	—	3	mA

Table 32. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Min	Typ	Max	Unit
Input (double ADC channel)	CC	D	Max leakage	150C	—	—	300	nA
	CC	D	Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150 mV	–3.6	—	3.6	mA
SNR	CC	T	Signal-to-noise ratio	V_{REF} = 3.3 V, Fin < 125 kHz	67	—	—	dB
SNR	CC	T	Signal-to-noise ratio	V_{REF} = 5.0 V, Fin < 125 kHz	69	—	—	dB
THD	CC	T	Total harmonic distortion	@ 125 kHz	TBD	—	—	dB
SINAD	CC	T	Signal-to-noise and distortion	Fin < 125 kHz	65	—	—	dB
ENOB	CC	T	Effective number of bits	Fin < 125 kHz	10.5	—	—	bits
$TUE_{IS1WINJ}$	CC	D	Total unadjusted error for IS1WINJ	Without current injection	–6	—	6	LSB
$TUE_{IS1WWINJ}$	CC	D	Total unadjusted error for IS1WWINJ	Without current injection	–6	—	6	LSB

NOTES:
1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 to +165 °C, unless otherwise specified, and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 29.
6. For the 144-pin package
7. No missing codes

3.15 Flash memory electrical characteristics

Table 33. Flash memory program and erase specifications

Symbol	Characteristic	Typ[1,2]	Initial Max 25C[3]	Initial Max All Temps[4]	Lifetime Max[5]	Unit
$t_{dwprogram}$	Double Word (64 bits) Program Time[6]	25	100	—	500	µs
$t_{pprogram}$	Page (256 bits) Program Time[7]	53	200	—	500	µs
$t_{qprogram}$	Quad-Page (1024 bits) Program Time[8]	203	800	1,200	2,000	µs
$t_{16kpperase}$	16 KB Block Pre-program and Erase Time	225	1,000	1,500	5,000	ms
$t_{32kpperase}$	32 KB Block Pre-program and Erase Time	250	1,000	1,500	5,000	ms
$t_{64kpperase}$	64 KB Block Pre-program and Erase Time	325	1,000	1,500	5,000	ms
$t_{256kpperase}$	256 KB Block Pre-program and Erase Time	695	2,000	3,000	15,000	ms
$t_{factory256kpperase}$	256 KB Block Factory pre-program and Erase Time	510	1,500	2,250	n/a	ms

NOTES:
1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25C. These values are characterized, but not tested.
2. For memory sizes greater than 1MB, and for blocks with less than or equal to 100 program/erase cycles, the user can apply a 90% typical + 10% Init Max (25C or All Temps depending on temperature) for each unit (page or block) to calculate the total program or erase time.
3. Initial Max 25C program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, 20C < Tj < 30C junction temperature, and nominal (+/- 2%) supply voltages. These values are verified at production test.
4. Initial Max All Temps program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, -40C < Tj < 150C junction temperature, and nominal (+/- 2%) supply voltages. These values are verified at production test.
5. Lifetime Max program and erase times apply across the voltage, temperature and cycling range of product life. This maximum value is characterized but not tested.
6. Program times are actual hardware programming times and do not include software overhead.
7. Program times are actual hardware programming times and do not include software overhead.
8. Program times are actual hardware programming times and do not include software overhead.

Table 34. Flash memory environmental ratings

Symbol	Characteristic	Min	Typical	Max	Units
T_A	Operating Ambient Temperature: - Automotive - Automotive with reduced functionality (slower read performance (15% slower), higher currents, slower erase when done at spec value (2x), and no program, erase or margin reads allowed at greater than 150C). - Consumer	 -40 -40 -20	—	 +125 +140 +70	C
T_J	Operating Junction Temperature: - Automotive - Automotive with reduced functionality (slower read performance (15% slower), higher currents, slower erase when done at spec value (2x), and no program, erase or margin reads allowed at greater than 150C). - Consumer	 -40 -40 -20	—	 +150 +165 +95	C
T_S	Storage Ambient Temperature - Automotive - Automotive with reduced functionality	 -40 -40	—	 +150 +165	C
T_{MAX}	Absolute maximum ambient temperature exposure, 30 seconds or less.	—	—	+250	C
T_{UV}	Allowed time of exposure to UV light	—	—	0	µs

Table 35. Flash memory module life general use specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E Cycles	Number of program/erase cycles per block for 16KB, 32KB and 64KB blocks.[1]	-	100,000	—	P/E Cycles
	Number of program/erase cycles per block for 256KB blocks.[2]	-	1,000	100,000	P/E Cycles
Data Retention	Minimum data retention.	Blocks with 0-1,000 P/E cycles.	20	—	Years
		Blocks with 1,001 to 10,000 P/E cycles.	10	—	Years
		Blocks with 10,001 to 100,000 P/E cycles.	5	—	Years

NOTES:
1 Program and Erase supported across standard temperature specs. See table Table 34.
2 Program and Erase supported across standard temperature specs. See table Table 34.

3.16 SWG electrical characteristics

Table 36. SWG electrical characteristics

Symbol		C	Parameter	Min	Max	Unit
SINAD	CC	C	Signal-to-noise ratio plus distortion	50	—	dB
FREQ	CC	T	Frequency Range of the sine wave	1	50	kHz
FRP	CC	T	Frequency precision of the sine wave	-5	5	%
APP	CC	T	Sine wave amplitude (peak to peak)	0.426	2.063	V
Load	CC	D	Load capacitance	25	100	pF
Current	CC	D	Output current	-	100	µA
T_J	CC	D	Junction Temperature	-40	165	°C

3.17 AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +165°C and for the full operating range of the VDD_IO supply defined in Section 3.8, “DC electrical characteristics.”

Table 37. Functional Pad AC Specifications

Symbol		C	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	ipp_sre[1:0]
			Min	Max	Min	Max		MSB,LSB
I/O (output)	CC	T	2.5/2.5	7.5/7.5	0.9.0.9	3/3	50	11
						12/12	200	
				8/8		3.5/3.5	25	10
				11.5/11.5		6.5/6.5	50	
						30/30	200	
				45/45		25/25	50	01[2]
				65/65		30/30	200	
				75/75		40/40	50	00[2]
				110/110		50/50	200	
I/O (input)	SR	—		1.5/1.5		0.5/0.5	0.5	NA

1.As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes.

Note: Data based on characterization results, not tested in production.

3.17.1 Reset pad ($\overline{\text{EXT\_POR}}$, $\overline{\text{RESET}}$) electrical characteristics

The device implements a dedicated bidirectional RESET pin.

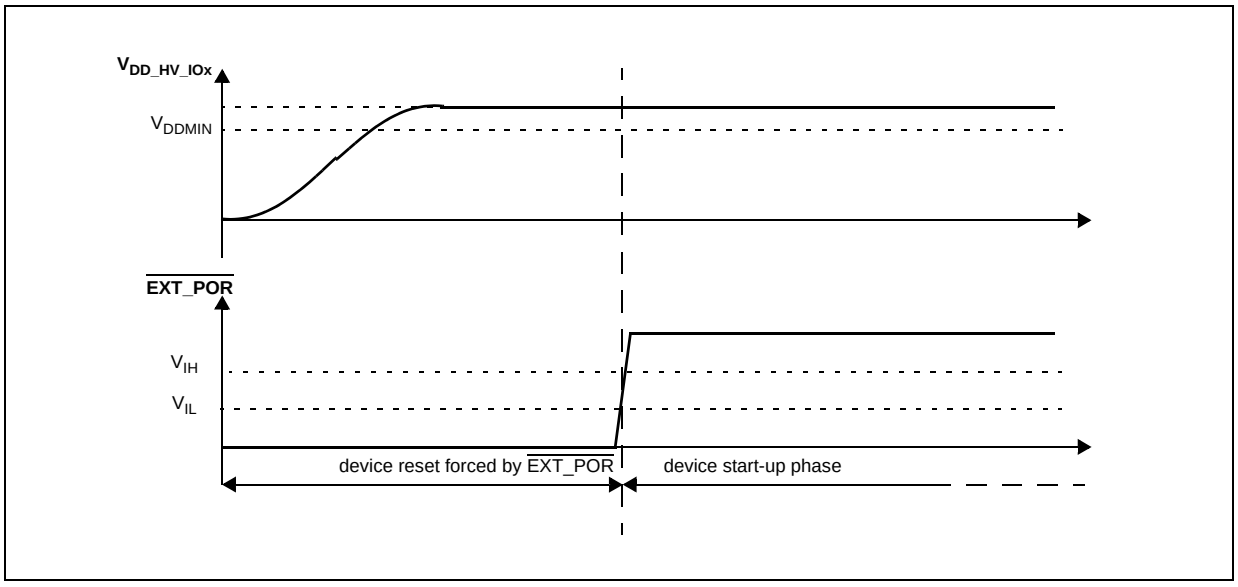


Figure 18. Start-up reset requirements

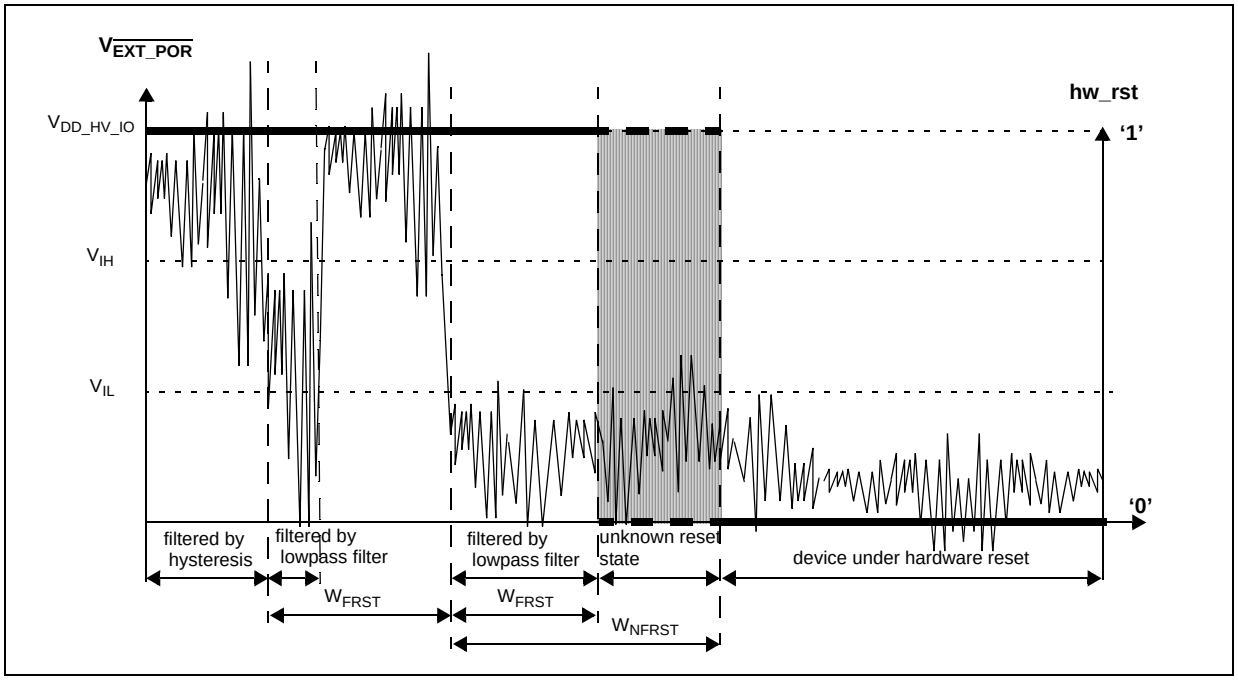


Figure 19. Noise filtering on reset signal

Table 38. Reset ($\overline{\text{EXT\_POR}}$, $\overline{\text{RESET}}$) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	—	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_IOx}$ + 0.4	V
V_{IL}	SR	—	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}[3]	CC	C	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	CC	P	Strong pull-down current	Device under power-on reset $V_{DD\_HV\_IO}$ = 1.0 V, V_{OL} = 0.35*$V_{DD\_HV\_IO}$	0.2	—	—	mA
				Device under power-on reset $V_{DD\_HV\_IO}$ = 3.0 V, V_{OL} = 0.35*$V_{DD\_HV\_IO}$	15	—	—	mA
W_{FRST}	SR	P	($\overline{\text{EXT\_POR}}$, $\overline{\text{RESET}}$)-input filtered pulse	—	—	—	10	ns
W_{NFRST}	SR	P	($\overline{\text{EXT\_POR}}$, $\overline{\text{RESET}}$)-input not filtered pulse	—	100	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	RESET_B pin V_{IN} = 0 V	30	—	80	µA
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	EXT_POR pin V_{IN} = $V_{DD\_HV\_IOx}$	30	—	80	µA

NOTES:
1 $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 165 °C, unless otherwise specified
2 All values need to be confirmed during device validation.
3 Data based on characterization results, not tested in production

3.17.2 WKUP/NMI timing

Table 39. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	20	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	400	—	—	ns

3.17.3 Debug/JTAG/Nexus/Aurora timing

3.17.3.1 JTAG interface timing

Table 40. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time[2]	36	—	ns
2	t_{JDC}	CC	T	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	15[3]	ns
7	t_{TDOI}	CC	C	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	600[4]	ns
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

NOTES:
1 These specifications apply to JTAG boundary scan only.

2 This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency

3 Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

4 Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

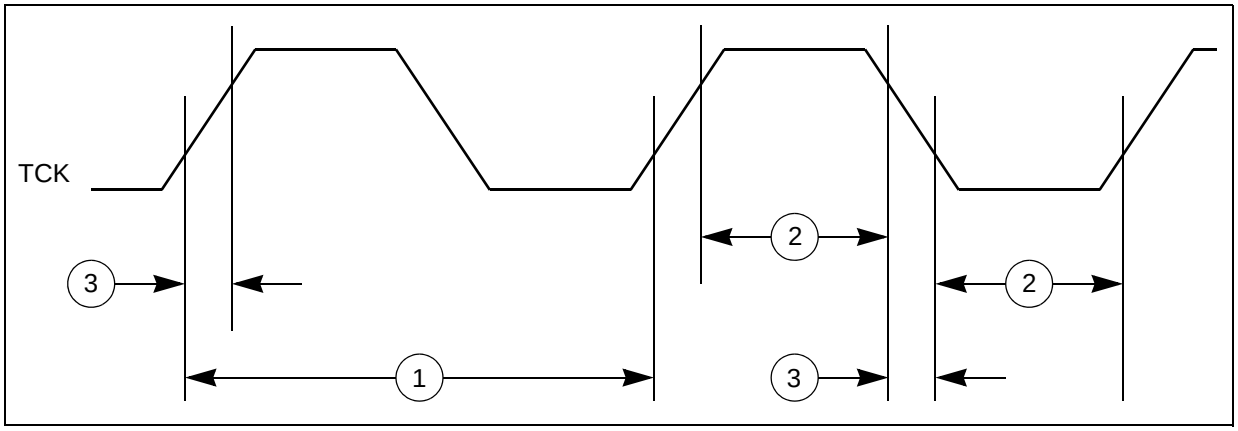


Figure 20. JTAG test clock input timing

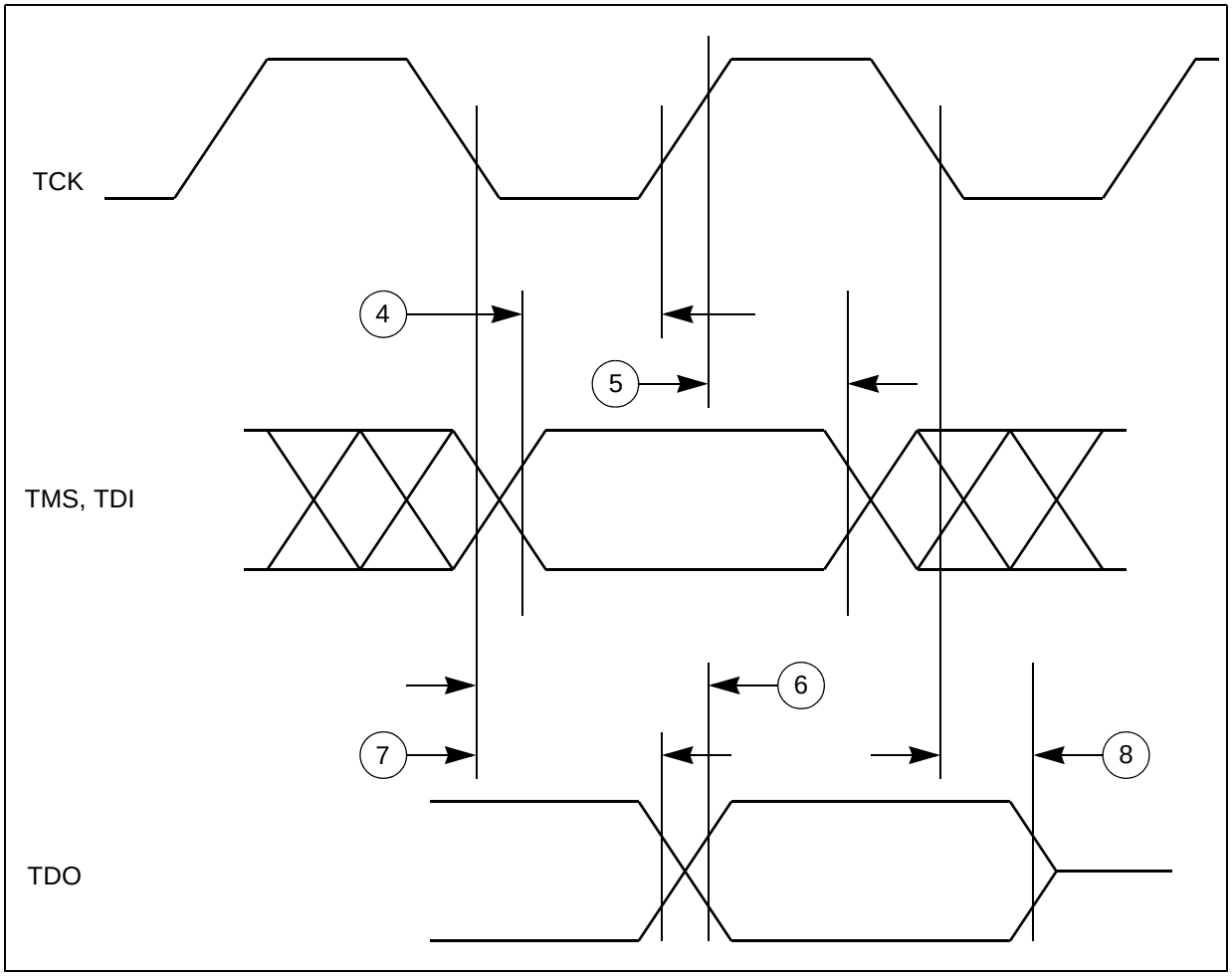


Figure 21. JTAG test access port timing

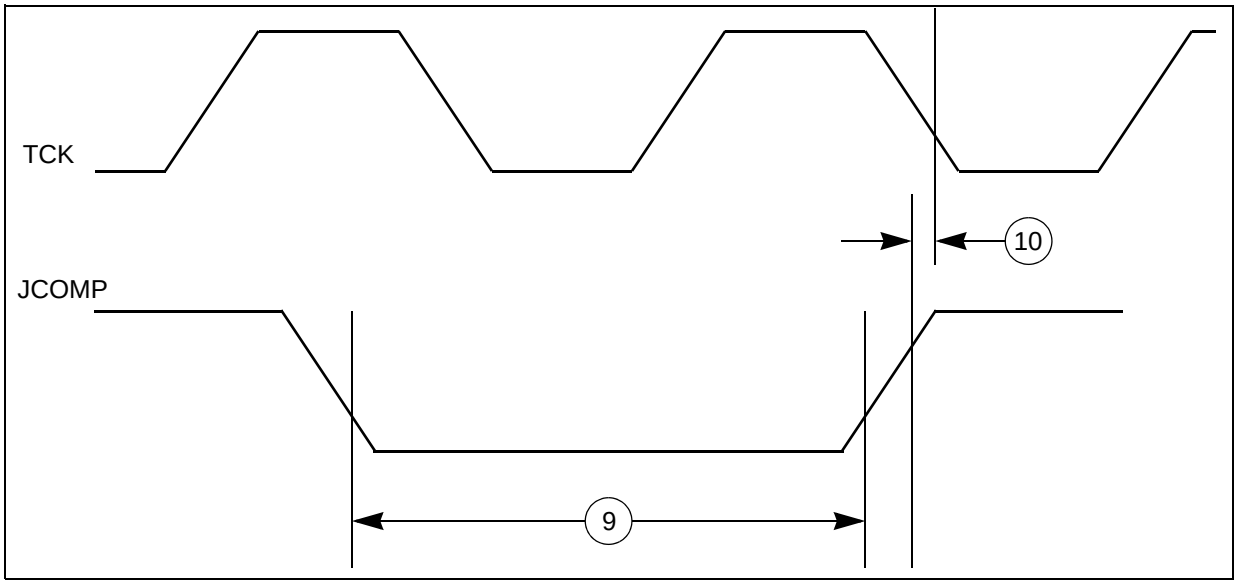


Figure 22. JTAG JCOMP timing

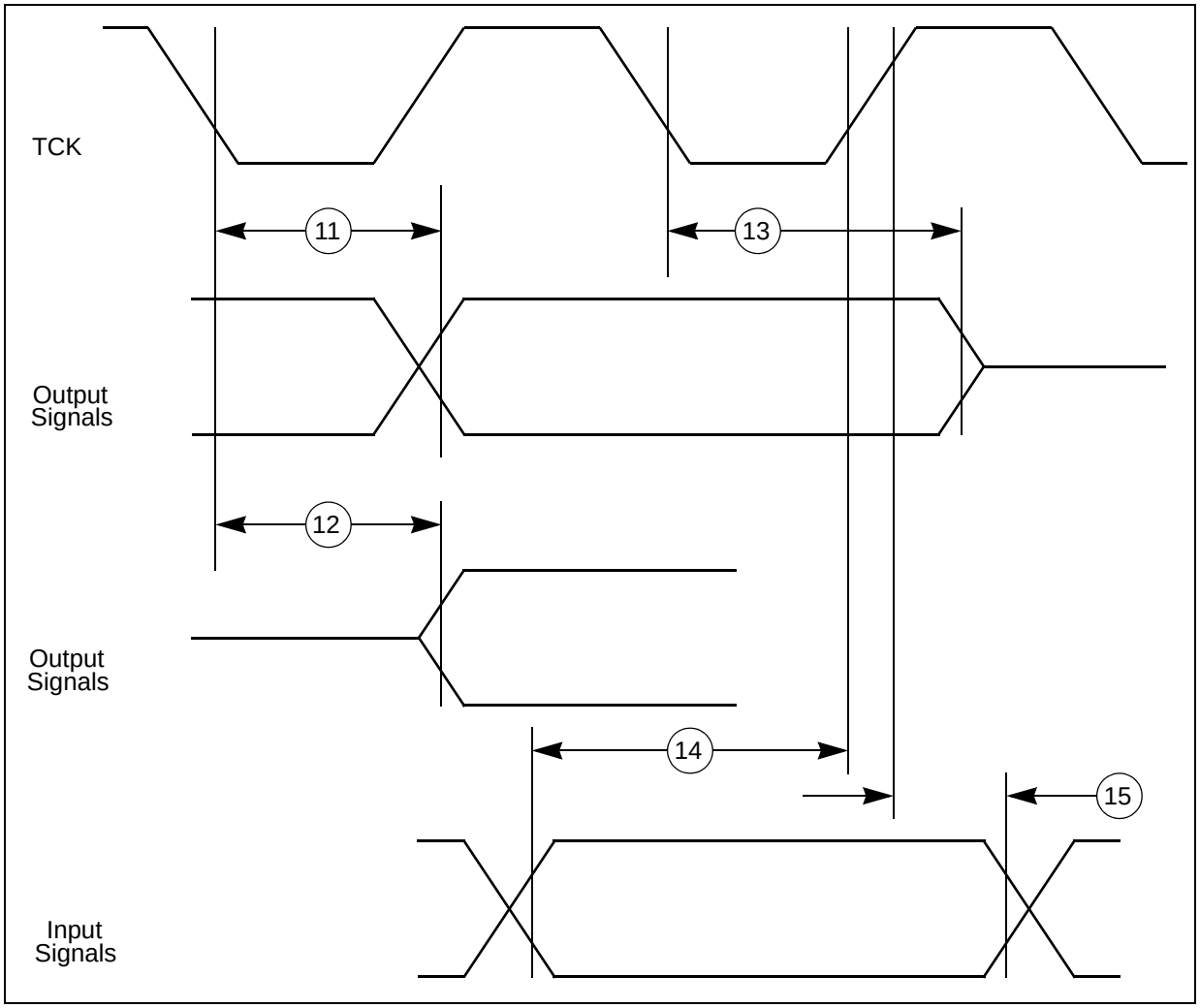


Figure 23. JTAG boundary scan timing

3.17.3.2 Nexus timing

Table 41. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	CC	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	CC	D	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	CC	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	CC	D	TDI, TMS Data Setup Time	—	8	—	ns

Table 41. Nexus debug port timing[1] (continued)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	CC	D	TDI, TMS Data Hold Time		5	—	ns
10	t_{JOV}	CC	D	TCK Low to TDO/RDY Data Valid		0	25	ns

NOTES:
1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2 For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3 The system clock frequency needs to be four times faster than the TCK frequency.

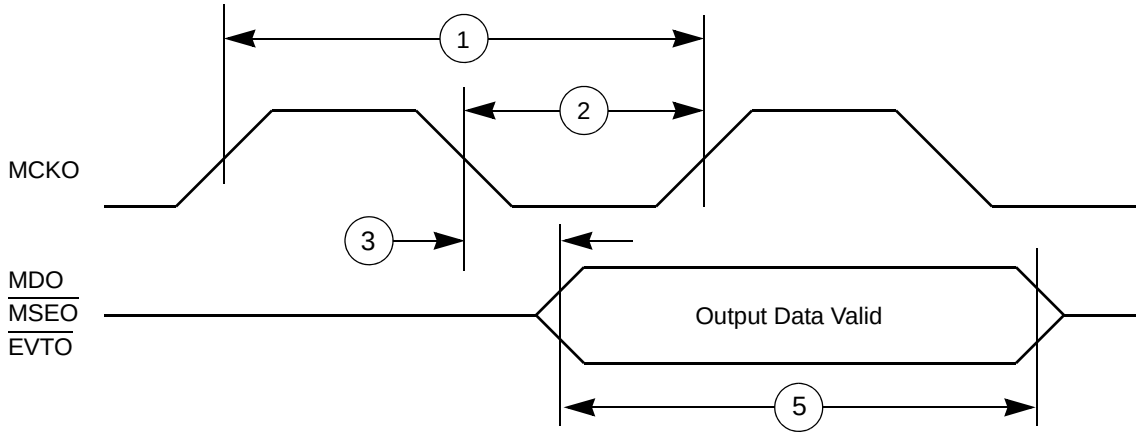


Figure 24. Nexus output timing

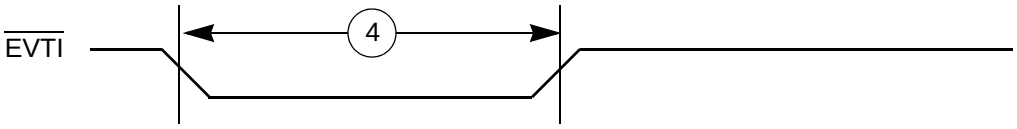


Figure 25. Nexus EVTI Input Pulse Width

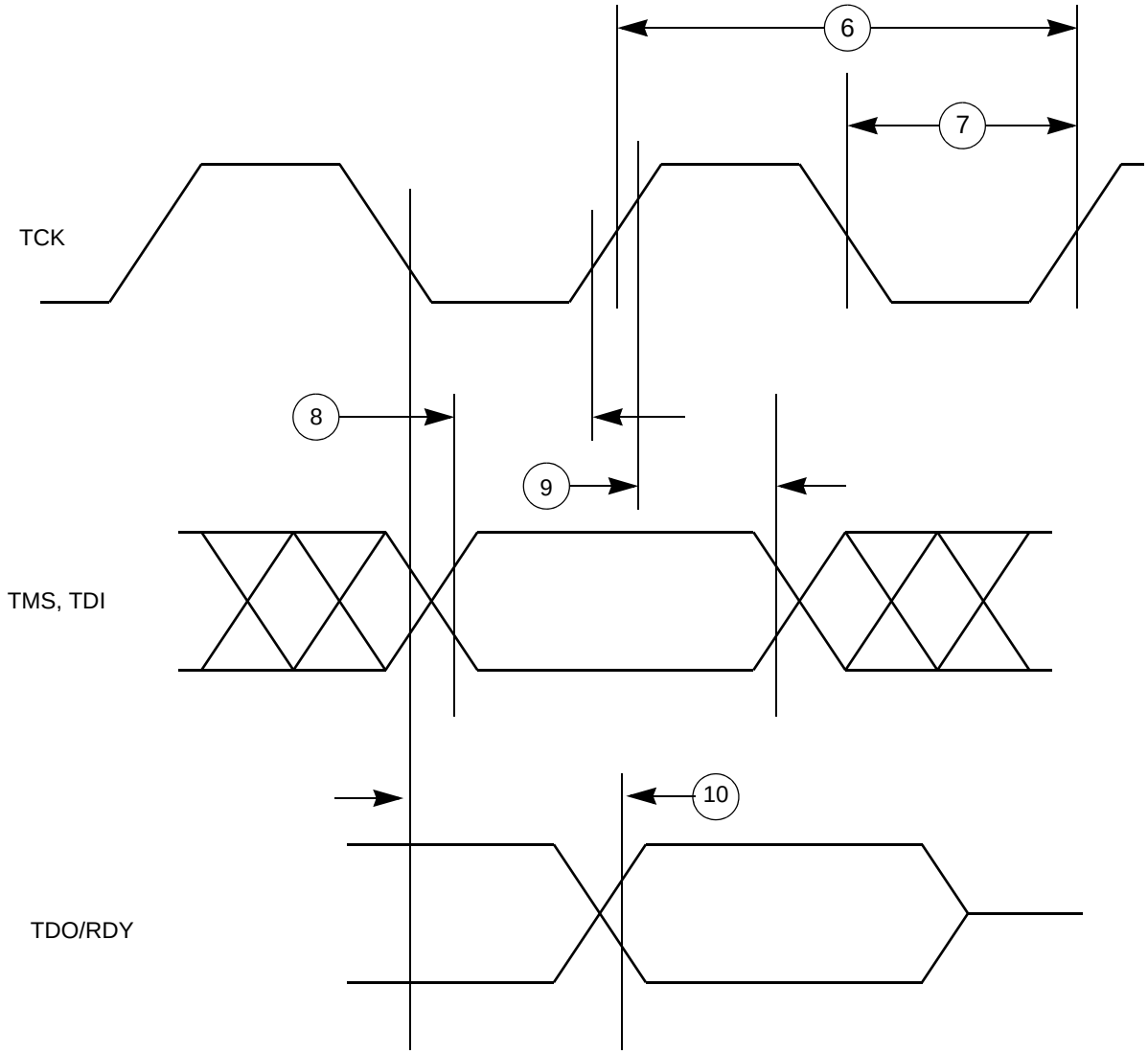


Figure 26. Nexus TDI, TMS, TDO timing

3.17.3.3 Aurora LVDS driver electrical characteristics

Table 42. Aurora LVDS driver specifications

Symbol	C		Parameter[1]	Value[2]			Unit
				Min	Typ	Max	
Data Rate							
DATARATE	SR	—	Data rate	—	1250	Typ+0.1%	Mbps
STARTUP							
T_{STRT_BIAS}	CC	T	Bias startup time[3]	—	—	5	µs
T_{STRT_TX}	CC	T	Transmitter startup time[4]	—	—	5	µs

Table 42. Aurora LVDS driver specifications (continued)

Symbol		C	Parameter[1]	Value[2]			Unit
				Min	Typ	Max	
T_{STRT_RX}	CC	T	Receiver startup time[5]	—	—	4	µs

NOTES:
1 Conditions for these values are $V_{DD\_HV\_IOx}$ = 3.3 V (–5%, +10%), T_J = –40 / 150 °C
2 All values need to be confirmed during device characterization.
3 Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
4 Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.
5 Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.17.3.4 Nexus Aurora debug port timing

Table 43. Nexus Aurora debug port timing

#	Symbol		C	Characteristic	Min	Max	Unit
1	t_{REFCLK}	CC	T	Reference clock frequency	625	1250	MHz
1a	t_{MCYC}	CC	T	Reference Clock rise/fall time	—	400	ps
2	t_{RCDC}	CC	D	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	CC	D	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	CC	D	Reference Clock Stability	50	—	PPM
5	BER	CC	D	Bit Error Rate	—	10^{-12}	—
6	J_D	CC	D	Transmit lane Deterministic Jitter	—	0.17	OUI
7	J_T	CC	D	Transmit lane Total Jitter	—	0.35	OUI
8	S_O	CC	T	Differential output skew	—	20	ps
9	S_{MO}	CC	T	Lane to lane output skew	—	1000	ps
10	OUI	CC	D	Aurora lane Unit Interval[1]	400	400	ps

NOTES:
1 ± 100 PPM

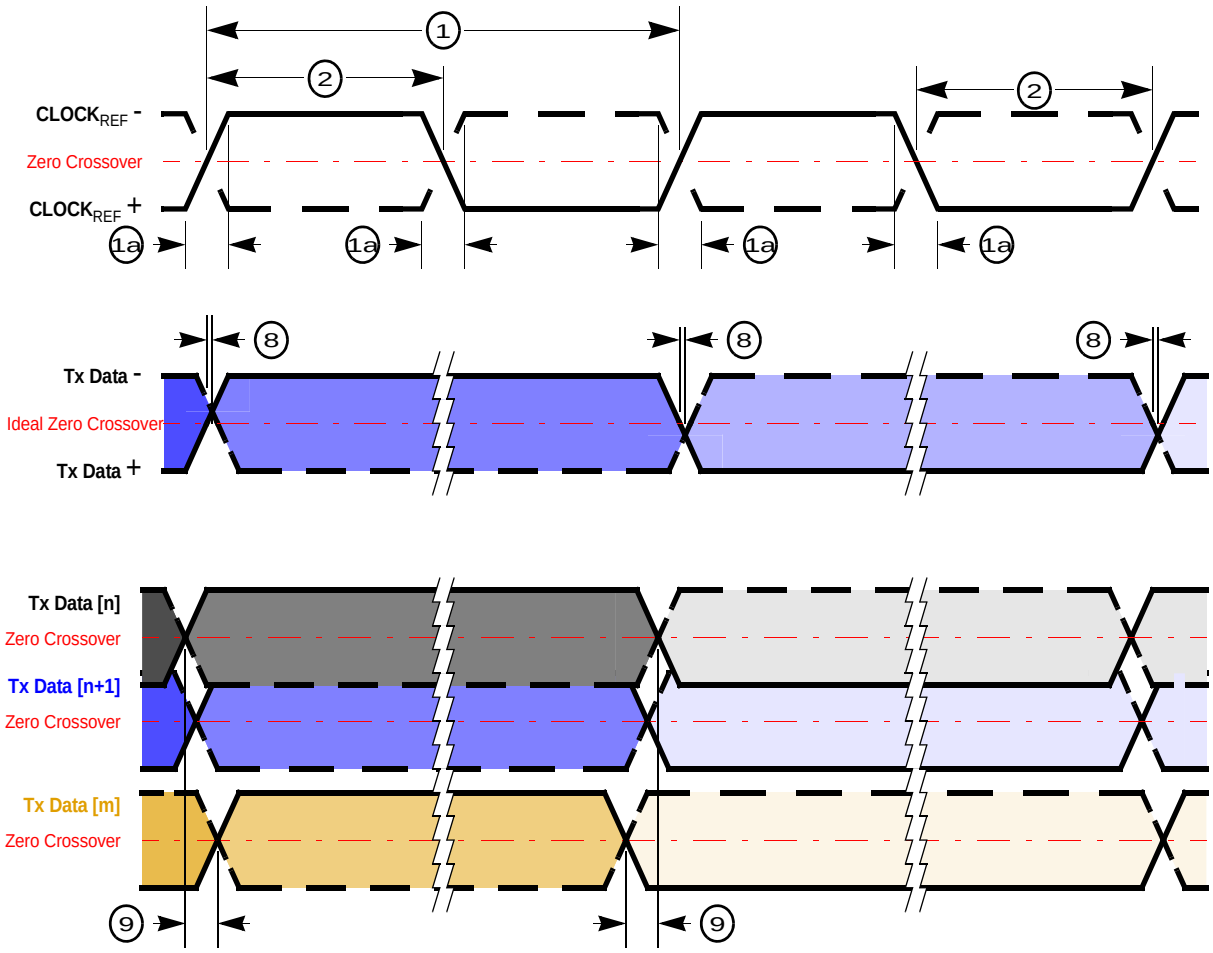


Figure 27. Nexus Aurora timings

3.17.4 External interrupt timing (IRQ pin)

Table 44. External interrupt timing

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	CC	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time[1]	—	6	—	t_{CYC}

NOTES:
1 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

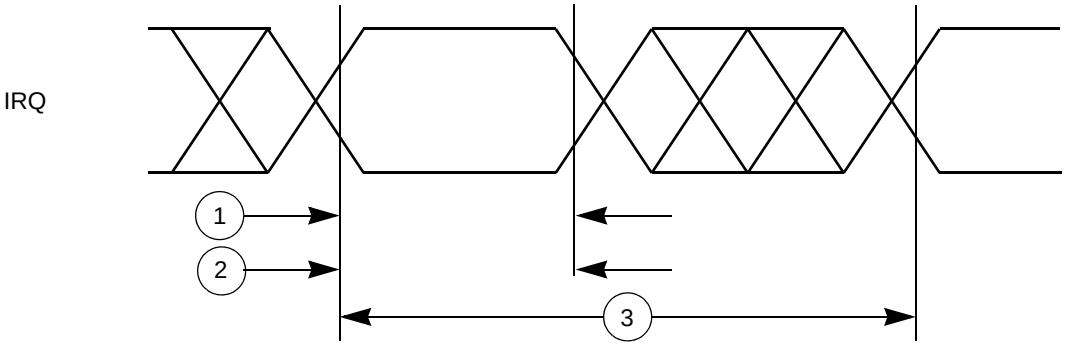


Figure 28. External interrupt timing

3.17.5 DSPI timing

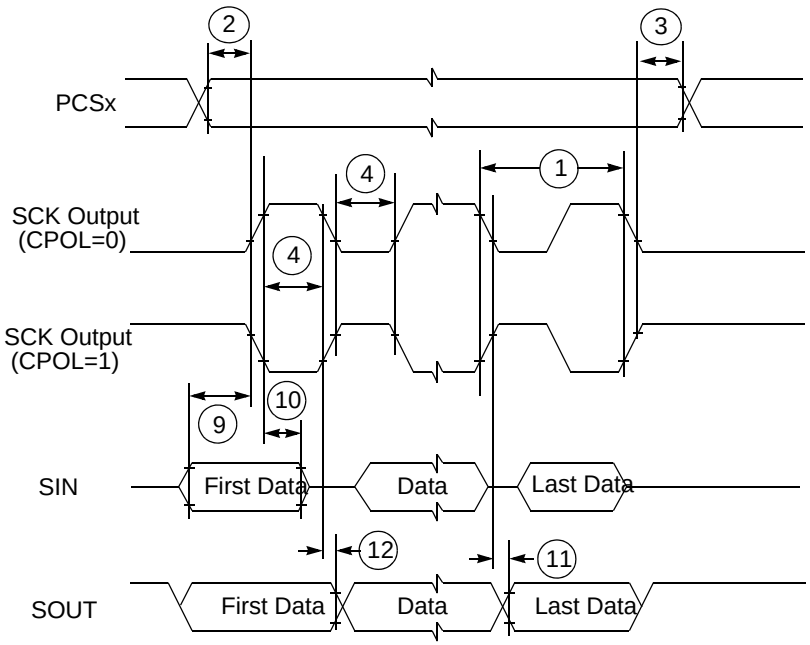
Table 45. DSPI timing

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		CC	D		Slave (MTFE = 0)	62	—	
		CC	D		Slave Receive Only Mode[1]	16	—	
2	t_{CSC}	CC	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	16	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
					Slave	2	—	
					Master (MTFE = 1, CPHA = 0)	5	—	
					Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
					Slave	—	23	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	4	

Table 45. DSPI timing (continued)

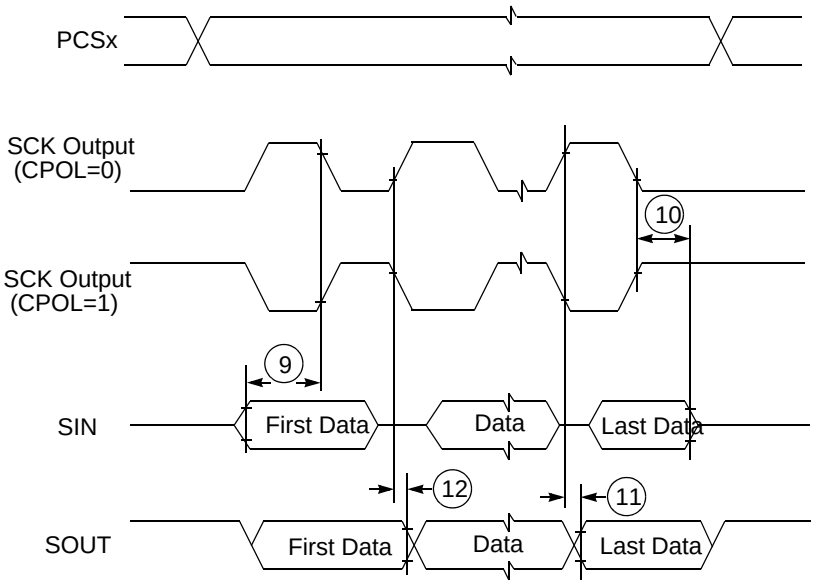
No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

NOTES:
1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.



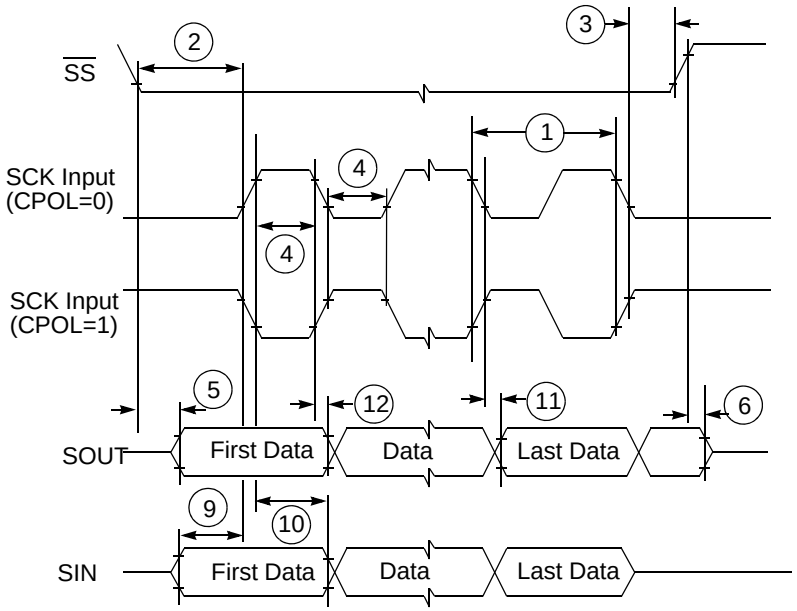
Note: The numbers shown are referenced in Table 45.

Figure 29. DSPI classic SPI timing — master, CPHA = 0



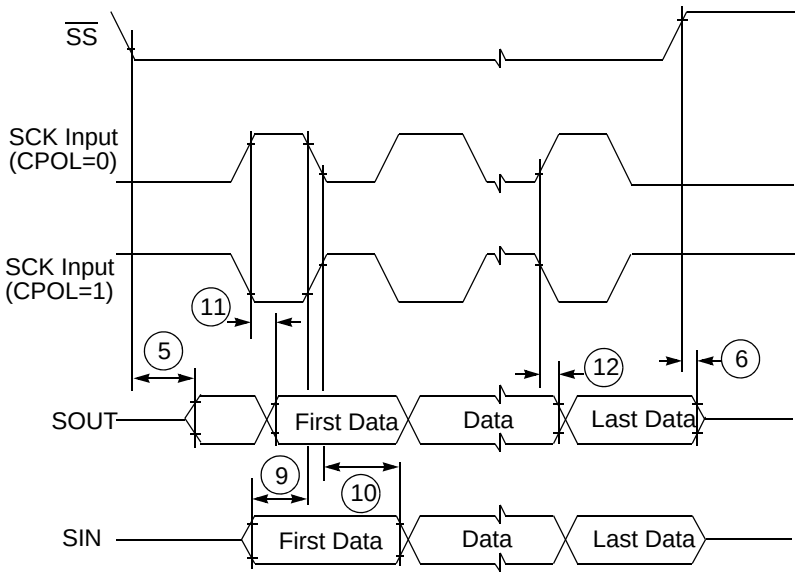
Note: The numbers shown are referenced in Table 45.

Figure 30. DSPI classic SPI timing — master, CPHA = 1



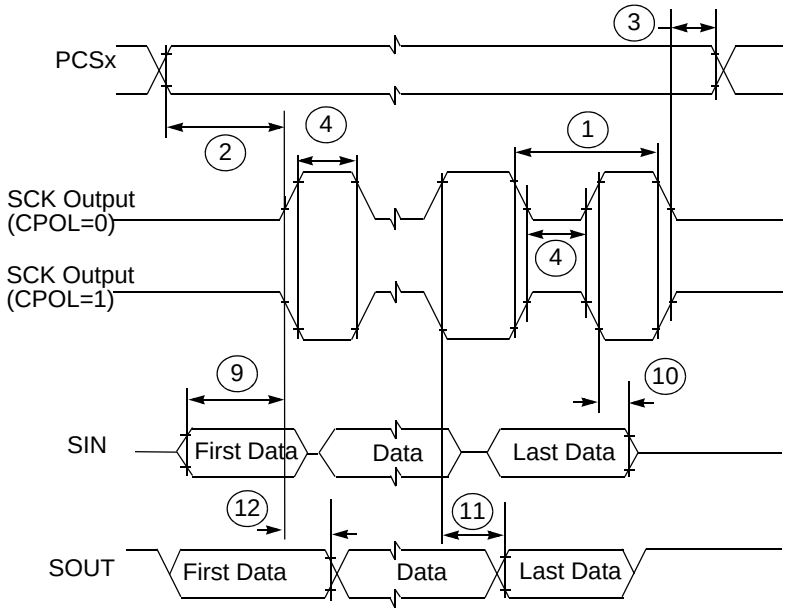
Note: The numbers shown are referenced in Table 45.

Figure 31. DSPI classic SPI timing — slave, CPHA = 0



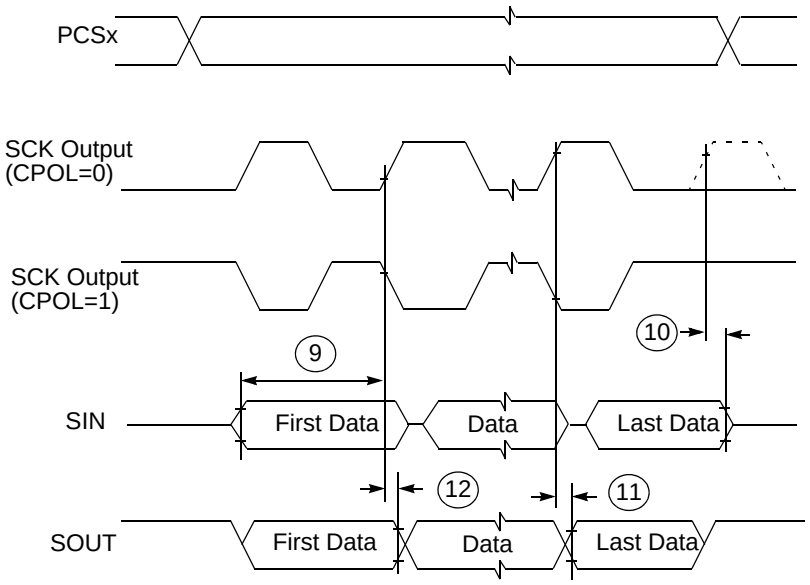
Note: The numbers shown are referenced in Table 45.

Figure 32. DSPI classic SPI timing — slave, CPHA = 1



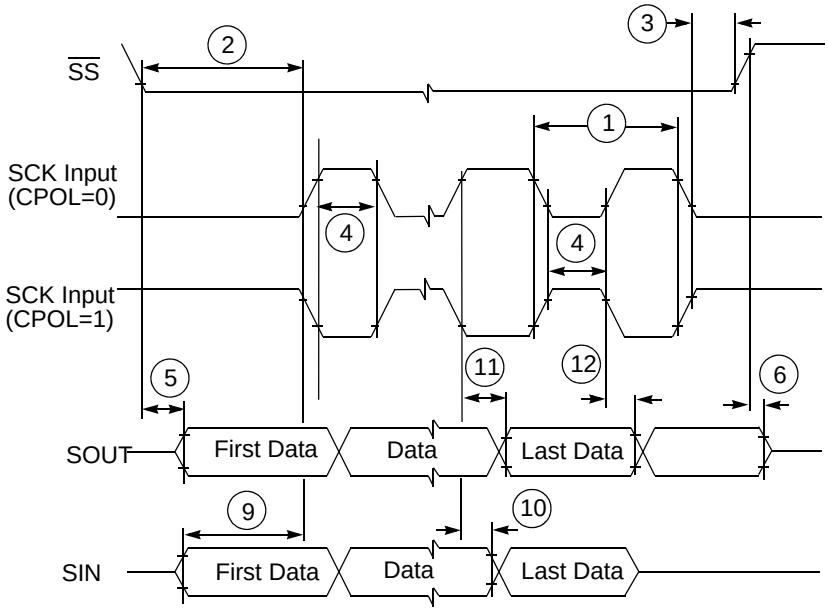
Note: The numbers shown are referenced in Table 45.

Figure 33. DSPI modified transfer format timing — master, CPHA = 0



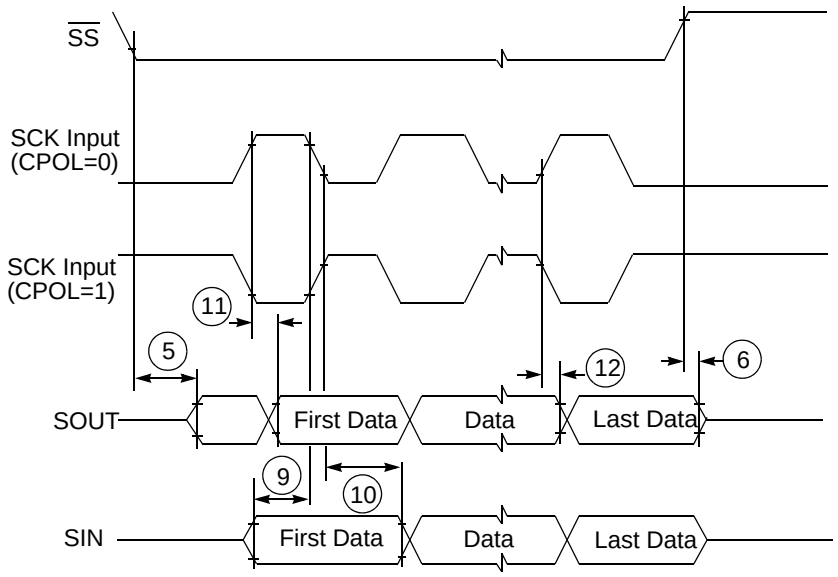
Note: The numbers shown are referenced in Table 45.

Figure 34. DSPI modified transfer format timing — master, CPHA = 1



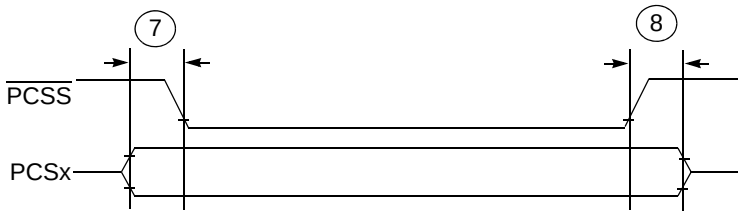
Note: The numbers shown are referenced in Table 45.

Figure 35. DSPI modified transfer format timing – slave, CPHA = 0



Note: The numbers shown are referenced in Table 45.

Figure 36. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in Table 45.

Figure 37. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.17.6 LVDS Fast Asynchronous Transmission (LFAST) electrical characteristics

3.17.6.1 LFAST interface timing diagrams

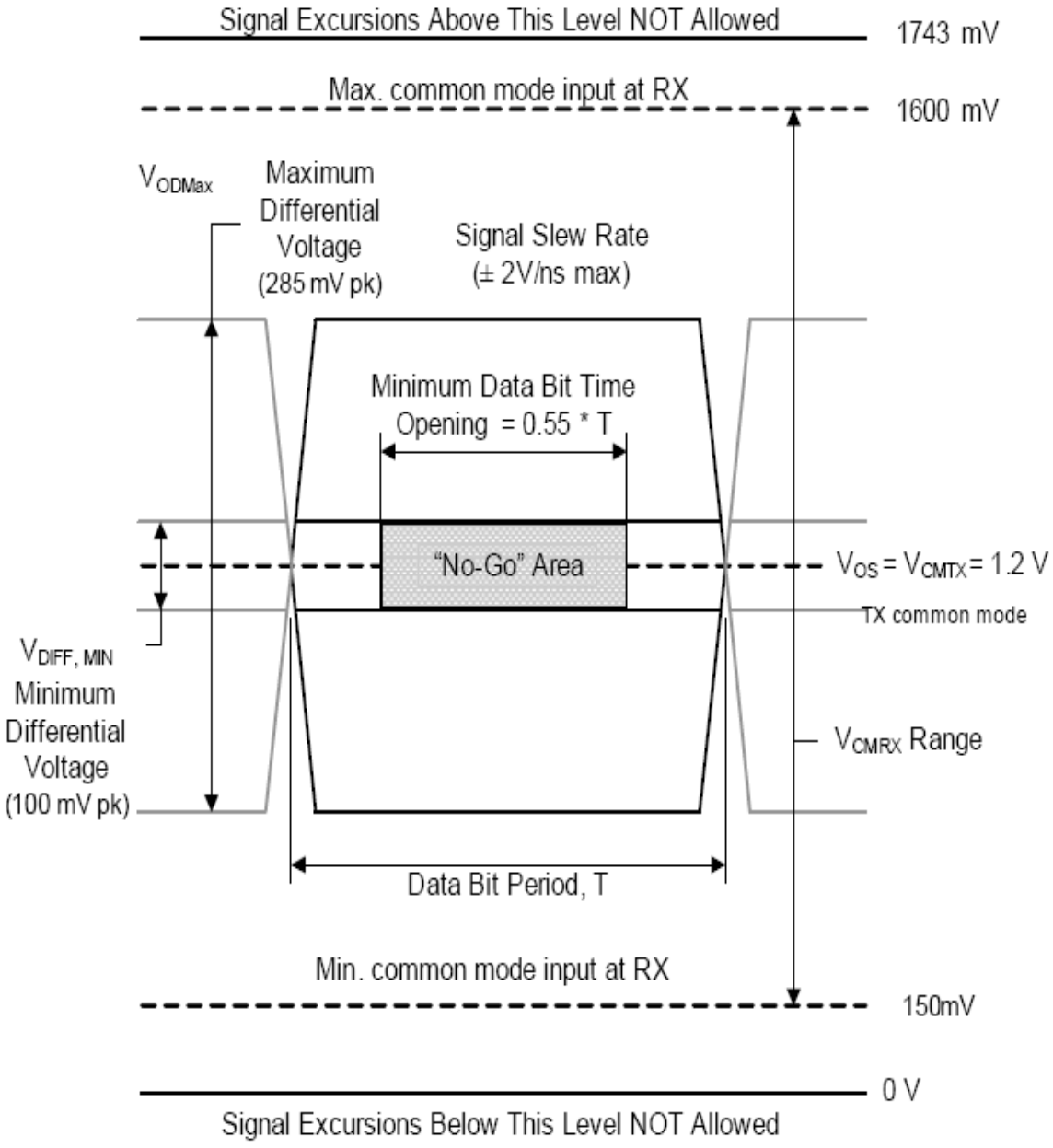


Figure 38. LFAST timing definition

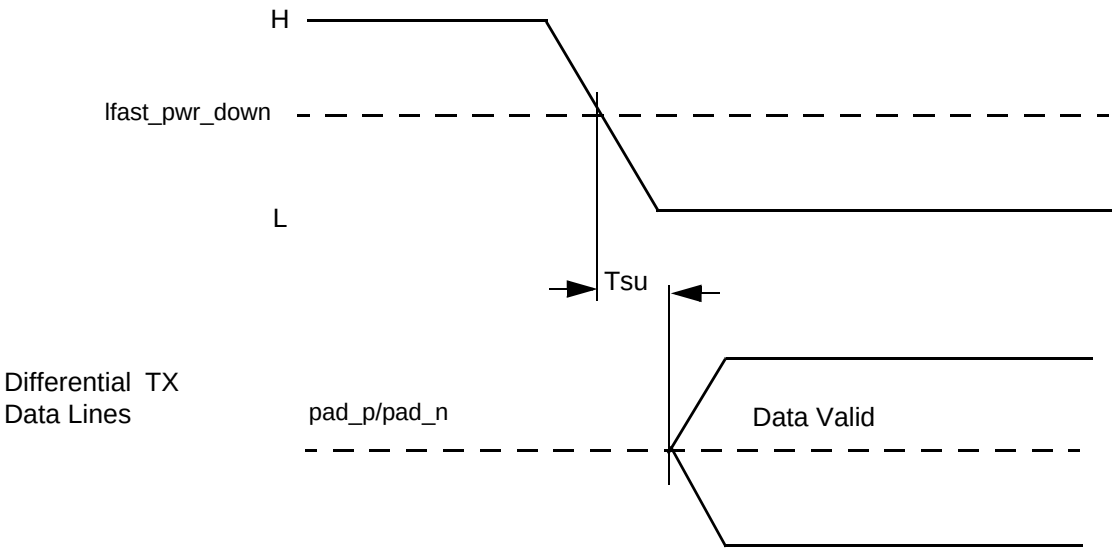


Figure 39. Power-down exit time

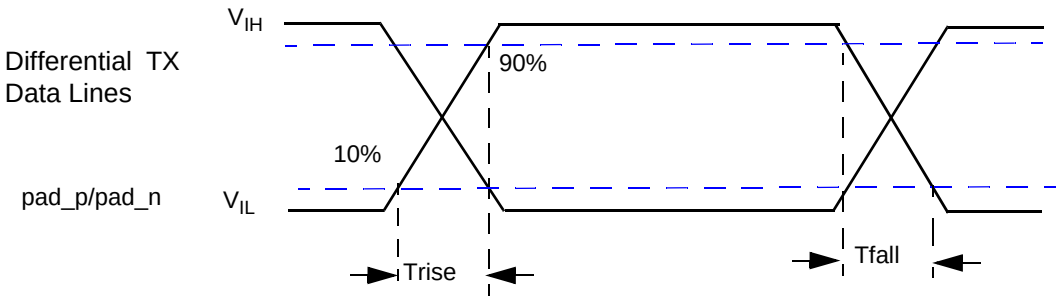


Figure 40. Rise/fall time

3.17.6.2 LFAST Interface electrical characteristics

Table 46. LFAST electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$V_{DD\_HV\_IJ}$	SR	—	Operating supply conditions		3.15	—	3.6	V
Data Rate								
DATARATE	SR	—	Data rate	—	—	312/320	Typ+0.1%	Mbps
STARTUP								
T_{STRT_BIAS}	CC	T	Bias startup time[3]	—	—	0.5	3	µs
T_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)[4]	—	—	0.2	2	µs

Table 46. LFAST electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SM2NM_TX}	CC	T	Transmitter startup time (sleep mode to normal mode)[5]	—	—	0.2	0.5	µs
T_{PD2NM_RX}	CC	T	Receiver startup time[6] (Power down to Normal mode)	—	—	20	40	ns
T_{PD2SM_RX}	CC	T	Receiver startup time[6] (Power down to Sleep mode)	—	—	20	50	ns
TRANSMITTER								
V_{OS_DRF}	CC	T	Common mode voltage	—	1.08	—	1.32	V
$\lvert\Delta_{VOD\_DRF}\rvert$	CC	D	Differential output voltage swing (terminated)	—	±100	±200	± 285	mV
T_{TR_DRF}	CC	T	Rise/Fall time (10% - 90% of swing)	—	0.26	—	1.5	ns
R_{OUT_DRF}	SR	—	Terminating resistance	$V_{DD\_HV\_IJ}$ = 5 V±10%	65	—	171	Ω
	SR	—		$V_{DD\_HV\_IJ}$ = 3 V±10%	67	—	198	Ω
C_{OUT_DRF}	SR	—	Capacitance[7]	—	—	—	5	pF
RECEIVER								
V_{ICOM_DRF}	SR	—	Common mode voltage	—	0.15[8]	—	1.6[9]	V
$\lvert\Delta_{VI\_DRF}\rvert$	SR	—	Differential input voltage	—	100	—	—	mV
V_{HYS_DRF}	CC	C	Input hysteresis	—	25	—	—	mV
R_{IN_DRF}	CC	D	Terminating resistance	$V_{DD\_HV\_IJ}$ = 5V±10%	80	100	120	Ω
		D	Terminating resistance	$V_{DD\_HV\_IJ}$ = 3 V±10%	80	115	150	Ω
C_{IN_DRF}	CC	D	Capacitance[10]	—	—	3.5	6	pF
L_{IN_DRF}	CC	D	Parasitic Inductance[11]	—	—	5	10	nH

NOTES:

1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 165 °C, unless otherwise specified
2. All values need to be confirmed during device characterization.
3. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
5. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
6. Startup time is defined as the time taken by LFAST receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.

7 Total lumped capacitance including silicon, package pin and bond wire. Application board simulation needed to verify LFAST template compliancy.

8 Absolute min = 0.15 V – (285 mV / 2) = 0 V

9 Absolute max = 1.6 V + (285 mV / 2) = 1.743 V

10 Total capacitance including silicon, package pin and bond wire

11 Total inductance including silicon, package pin and bond wire

Table 47. LFAST electrical characteristics[1]

Symbol		C	Parameter	Condition	Value			Unit
					Min	Nominal	Max	
F_{RF_REF}	SR	D	SysClk Frequency	—	10	—	26[2]	MHz
ERR_{REF}	CC	D	SysClk Frequency Error	—	–1	—	1	%
DC_{REF}	CC	D	SysClk Duty Cycle	—	45	—	55	%
C_{LOAD}	CC	D	Output Buffer Load Capacitance	—	—	—	10	pF
R_{LOAD}	CC	D	Output Buffer Load Resistance	—	10	—	—	kΩ
PN	CC	D	Integrated Phase Noise (single side band)	20 MHz	—	—	–58	dBc
	CC	D		10 MHz	—	—	–64	dBc
F_{VCO}	CC	D	PLL VCO Frequency	—	—	320	—	MHz
T_{LOCK}	CC	D	PLL Phase Lock	—	—	—	40	µs
ΔPER	CC	T	PLL Long Term Jitter (peak to peak)	—	—	—	600	ps

NOTES:
1 The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.

2 Guarantee of the 26 MHz SysClk frequency specification is pending device characterization.

3.17.7 FlexRay

3.17.7.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals.

These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

3.17.7.2 TxEN

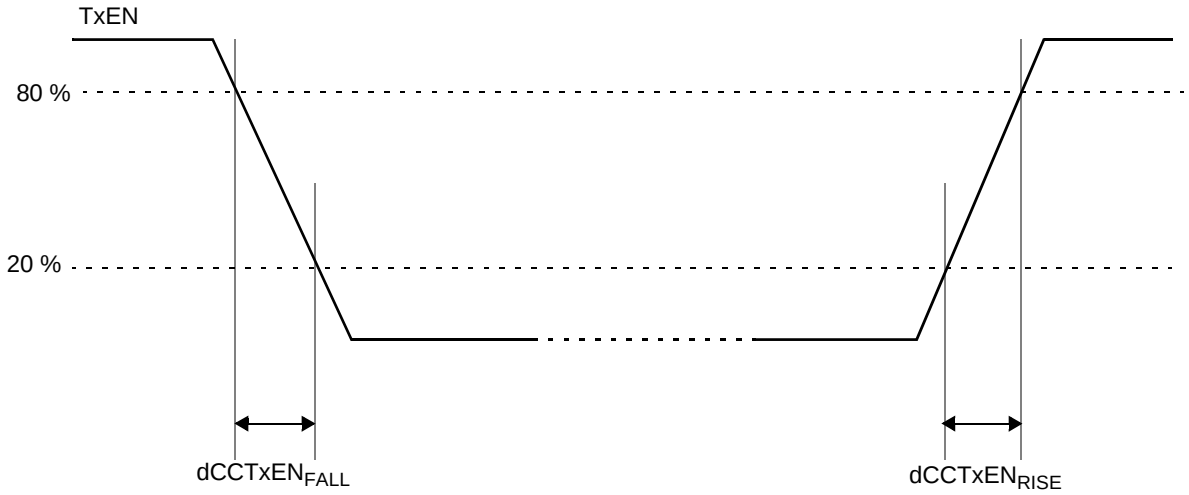


Figure 41. FlexRay TxEN signal

Table 48. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
dCCTxEN$_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN$_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN$_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN$_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

NOTES:
[1]All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +10%, T_J = –40 ^oC / 165 ^oC, TxEN pin load maximum 25 pF.

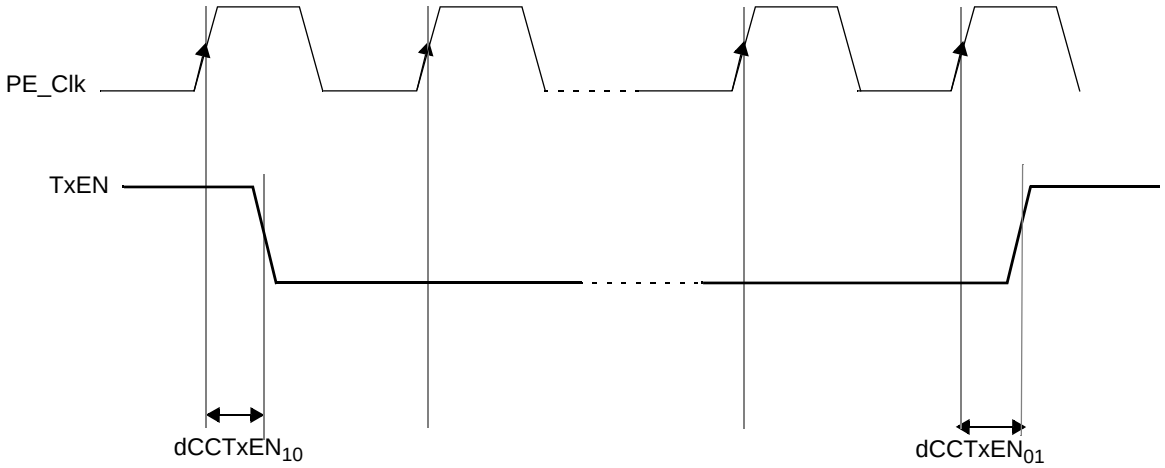


Figure 42. FlexRay TxEN signal propagation delays

3.17.7.3 TxD

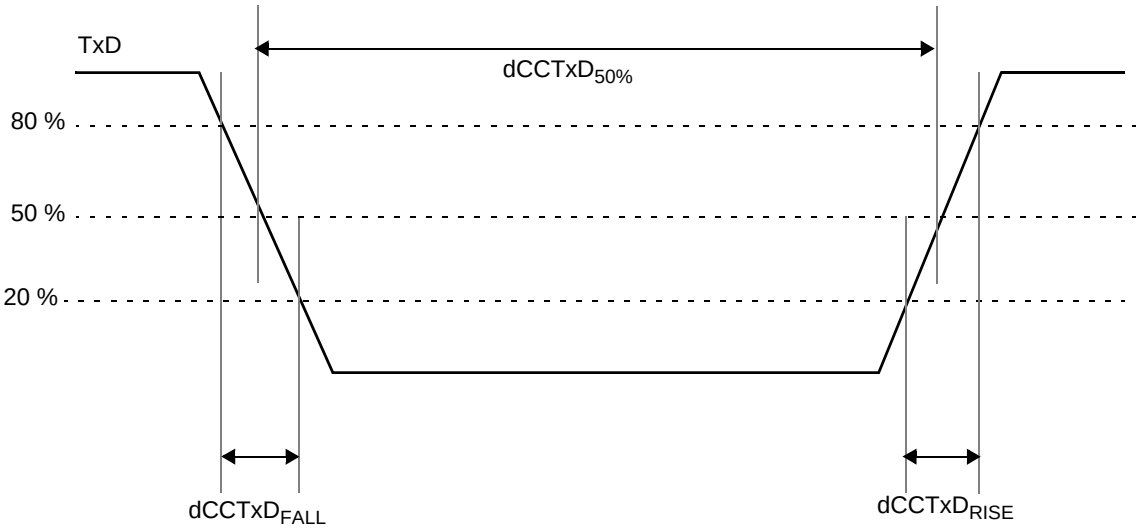
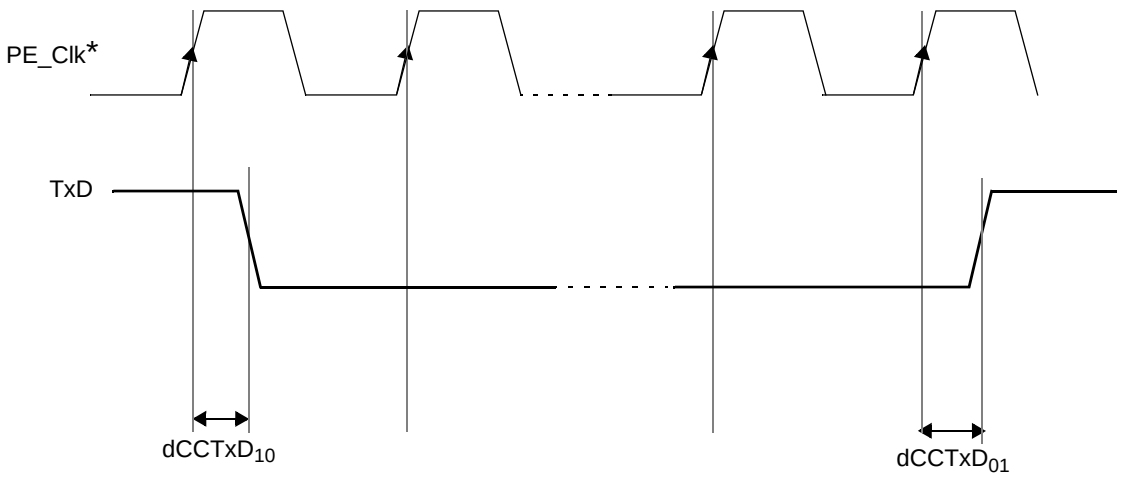


Figure 43. FlexRay TxD signal

Table 49. TxD output characteristics

Name	Description[1]	Min	Max	Unit
dCCTxAsym	Asymmetry of sending CC @ 25 pF load (=$dCCTxD_{50\%}$ - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9	ns
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

NOTES:
[1]All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +10%, T_J = –40 ^{o}C / 165 ^{o}C, TxD pin load maximum 25 pF.



*FlexRay Protocol Engine Clock

Figure 44. FlexRay TxD signal propagation delays

3.17.7.4 RxD

Table 50. RxD input characteristics

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

NOTES:
[1]All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +10%, T_J = –40 °C / 165 °C.

3.17.7.5 Receiver asymmetry

Table 51. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	-31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	-30.5	+43.0	ns

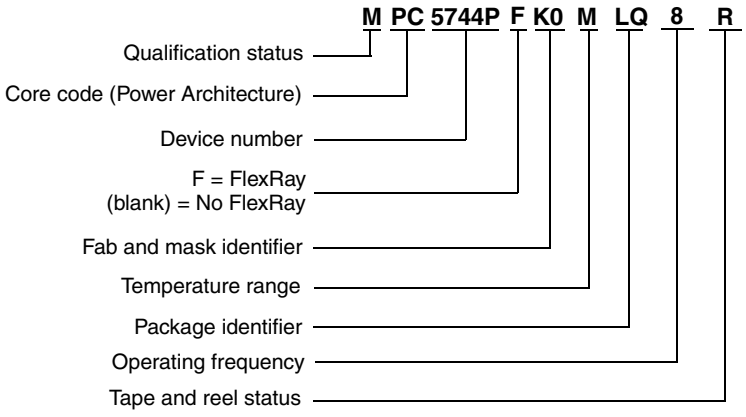
4 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASA00300D
257-ball MAPBGA	98ASA00081D

5 Ordering information



Temperature range	Package identifier	Operating frequency	Qualification status	Tape and reel status
M = –40°C to +125°C K = –40°C to +TBD°C for extended temp (+165°C T_J)	LQ = 144 LQFP MM = 257 MAPBGA KU = 176 LQFP	8 = 180 MHz 5 = 150 MHz	P = Pre-qualification M = Fully spec. qualified, general market flow S = Fully spec. qualified, automotive flow	R = Tape and reel (blank) = Trays

Note: Not all options are available on all devices. See Table 1.

Table 1. Orderable part number summary

Part number[1]	Flash/SRAM	Package	Other features[2]
PPC5744PFK0MLQ8	2.5 MB/384 KB	144 LQFP (Pb free)	–40 to +125 °C
PPC5744PFK0MKU8	2.5 MB/384 KB	176 LQFP exposed pad (Pb free)[3]	LFAST interface –40 to +125 °C
PPC5744PFK0MMM8	2.5 MB/384 KB	257 MAPBGA (Pb free)	LFAST interface Nexus Aurora –40 to +125 °C
MPC5743PFK0MLQ8	2 MB/256 KB	144 LQFP (Pb free)	–40 to +125 °C
MPC5743PFK0MMM8	2 MB/256 KB	257 MAPBGA (Pb free)	LFAST interface Nexus Aurora –40 to +125 °C
MPC5742PFK0MLQ8	1.5 MB/192 KB	144 LQFP (Pb free)	–40 to +125 °C
MPC5742PFK0MMM8	1.5 MB/192 KB	257 MAPBGA (Pb free)	LFAST interface Nexus Aurora –40 to +125 °C

NOTES:
1 All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. Not all configurations are available in the PPC parts.
2 The N33E maskset version of the device is limited to a maximum frequency of 180 MHz.
3 The 176 LQFP-EP package is not planned to be available with the N33E maskset version of the PPC5744 device. The 176 LQFP-EP package is under consideration, but not committed, for future maskset versions.

6 Document revision history

Table 52 summarizes revisions to this document.

Table 52. Revision history

Revision	Date	Description of changes
Rev. 0.3	06/2012	• Updated specifications and conditions throughout the document and added new information • Updated the name of Freescale's DigRF module to LFAST module • Updated list and format of orderable part numbers as well as information about the 176 LQFP-EP package's availability

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