HD66322T

(64-level Gray Scale Driver for High-Quality TFT Liquid Crystal Display for XGA and SXGA)

HITACHI

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Description

The HD66322T is a TFT-LCD source driver LSI, which is applicable to XGA and SXGA. The LSI receives 6-bit digital display data per pixel and outputs corresponding 64-level gray scale voltage. Since the output circuit on this LSI incorporates an operational amplifier, a positive and a negative voltage can be alternately output from each output pin. Therefore, a high-quality display with less crosstalk can be achieved without a complex circuit configuration.

Features

- High-speed operation
  - Maximum operating clock: 65 MHz (3.0V)
- Operating voltage
  - V_{CC} = 3.0 to 3.6V
  - VLCD = 10 ± 0.5V
- LCD drive voltage
  - Low voltage: 0.2 ~VLCD/2 (V)
  - High voltage: VLCD/2 ~ VLCD–0.2 (V)
- 384 LCD drive circuits
- Multicolor display

  The HD66322T receives 6-bit digital display data per pixel, and selects and outputs an LCD drive voltage among 64-level gray scale voltages. When R, G, and B color filters are added to the LCD panel, a maximum of 260 thousand colors can be displayed.
- 36 data bits (six bits of gray scale code × three dots of RGB × two pixels)
- Low output voltage deviation: Voff = ±10 mV (max)

- High-voltage asymmetrical drive

  Counter electrode does not need to be converted into AC due to a 10-V wide dynamic range and alternate output of positive and negative voltages. In addition, as positive and negative voltages are generated from the reference voltage supplied from an external device, symmetrical or asymmetrical drive can be selected according to LCD characteristics.
- Polarity inversion output to each pin

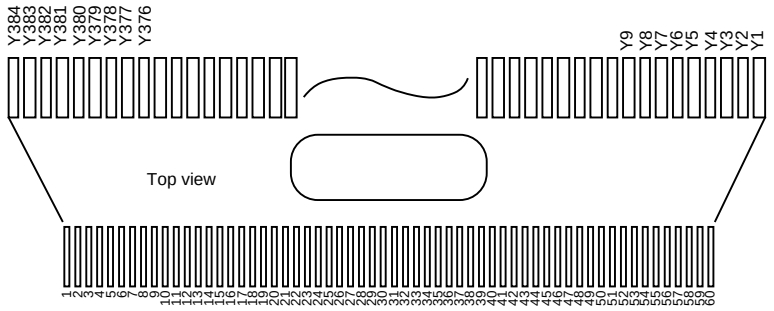
  Inversion drive for each dot can be achieved even in a one-side location configuration due to alternate output of positive and negative voltages from each output pin; this achieves a high quality display with less crosstalk.
- Operational amplifier

  An external reference voltage generator can be configured simply by adding a resistance ladder due to an operational amplifier incorporated in the output circuit of this LSI.
- Bi-directional shift
- Chip enable signal generator
- Data polarity inversion bit

  Can reduce current consumption when displaying white and black for each dot.
- Package: TCP
- Applicable system

  OA equipment such as an XGA (1024 × 768 dots)-and an SXGA (1280 × 1024 dots)-notebook personal computer or monitor

Pin Arrangement



1	$\overline{EIO2}$	11	D42	21	$\overline{TEST2}$	31	GND2	41	POL	51	D12
2	D55	12	D41	22	V_{CC}	32	V4	42	D25	52	D11
3	D54	13	D40	23	$\overline{TEST1}$	33	V3	43	D24	53	D10
4	D53	14	D35	24	SHL	34	V2	44	D23	54	D05
5	D52	15	D34	25	V9	35	V1	45	D22	55	D04
6	D51	16	D33	26	V8	36	V0	46	D21	56	D03
7	D50	17	D32	27	V7	37	GND1	47	D20	57	D02
8	D45	18	D31	28	V6	38	CL2	48	D15	58	D01
9	D44	19	D30	29	V5	39	CL1	49	D14	59	D00
10	D43	20	TESTCLK	30	VLCD	40	M	50	D13	60	$\overline{EIO1}$

Note: This figure does not specify the tape carrier package dimensions.

Figure 1 Pin Arrangement

Block Diagram

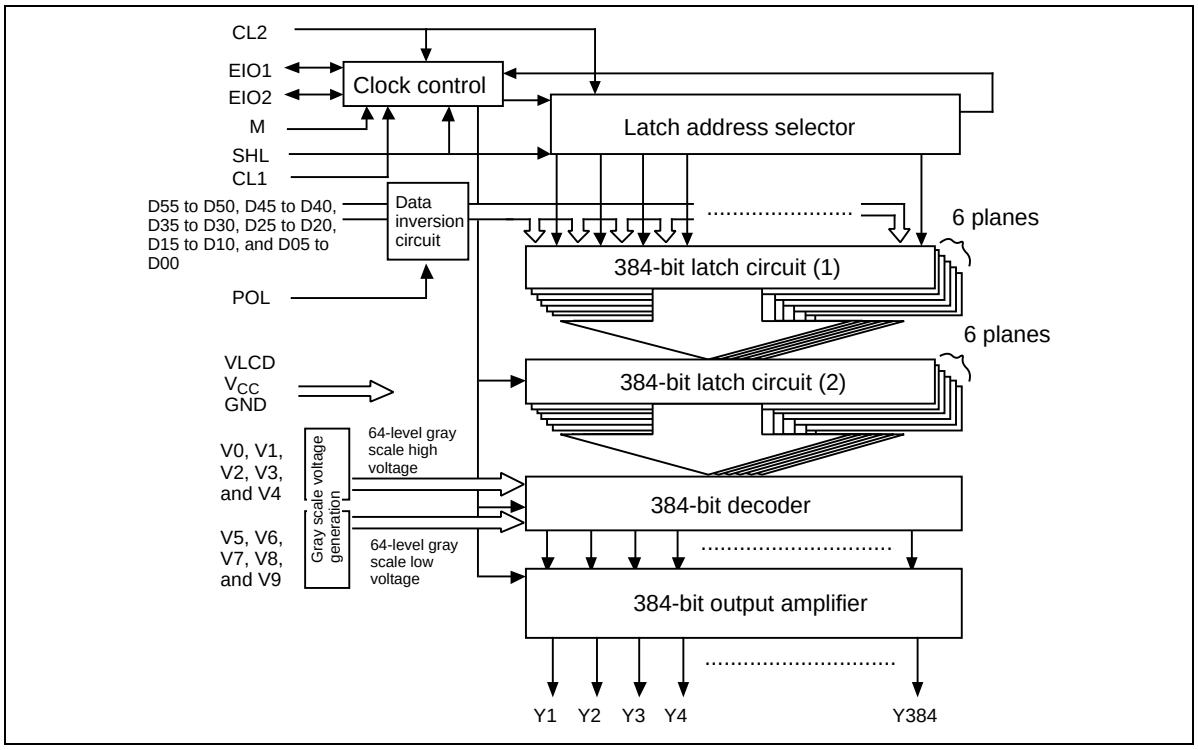


Figure 2 Block Diagram

Block Functions

Clock controller

Generates chip enable signals ($\overline{EIO2}$ and $\overline{EIO1}$) and controls the internal timing signals.

Data inversion circuit

Inverts the polarity (when the POL signal is 1) or does not invert it (when the POL signal is 0) for input data.

Latch address selector

Generates latch signals, which sequentially trigger latch operation of input display data.

Latch circuit 1

Latches 6-output × 6-bit sequentially input display data; composed of 384 × 6 bits.

Latch circuit 2

Latches 384 × 6-bit data latched in latch circuit 1 synchronously with the CL1 signal.

Decoder

Generates a 64-level gray scale voltage based on the LCD drive voltage (V8–V0) and selects the LCD applicable voltage using the 6-bit data decoded signal.

Gray scale voltage generator

Generates a 64-level gray scale high voltage or a 64-level gray scale low voltage by dividing the external input voltage by resistance.

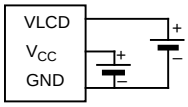
Output amplifier

Buffers and outputs the gray scale voltage selected for each output.

Pin Functions

Table 1 Pin Functions

Signal Name	Numbers	Input/Output	Function
VLCD	1	Power supply	See Figure 3.
V_{CC}	1	Power supply	
GND	1	Power supply	
V9–V5	5	Power supply	Supplies power to the LCD applicable voltage generation circuit. Voltage within the range of 5.7V to V_{EE} must be applied to V0 to V4 pins, and within the range of 0.2 to 5.0V to V5 to V9 pins.
V4–V0	5		
CL1	1	Input	While this clock is low, the LCD applicable voltage is output.
CL2	1	Input	Display data is stored at the falling edge of this signal.
POL	1	Input	Data polarity inversion signal, which saves the power supply of the data bus line in the interface. When this signal is high, display data is inverted in the driver, and when it is low, display data is input to the driver without being inverted.
D55 to D50 D45 to D40 D35 to D30 D25 to D20 D15 to D10 D05 to D00	36	Input	Inputs 6-bit (gray scale data) × 6-pixel display data.
$\overline{EIO1}$ $\overline{EIO2}$	2	Input/output	Provides chip-enable signals. Input or output depends on the SHL signal. In SHL = GND, $\overline{EIO1}$ and $\overline{EIO2}$ are input and output, and in SHL = V_{CC}, $\overline{EIO1}$ and $\overline{EIO2}$ are output and input, respectively. At any one time, the signal being used for input must go low to enable the driver to latch display data, and the signal being used for output will be driven low after 312 pixels of data have been read.
M	1	Input	An AC signal for controlling an LCD alternate drive. When this signal is 0, odd number pins (Y1, Y3, ..., Y311) output the positive LCD applicable voltage and even number pins output the negative LCD applicable voltage, and when 1, vice versa.
Y1–Y384	384	Output	Outputs LCD applicable voltages.
TEST1.2 TESTCLK	1	Input	A test pin. Normally, this signal must be set low.
SHL	1	Input	Selects the shift direction of display data. See Figure 4.



VLCD–GND: High-voltage analog power supply

V_{CC}–GND: Logic and low-voltage analog power supply

Figure 3 VLCD, V_{CC}, and GND Power Supply

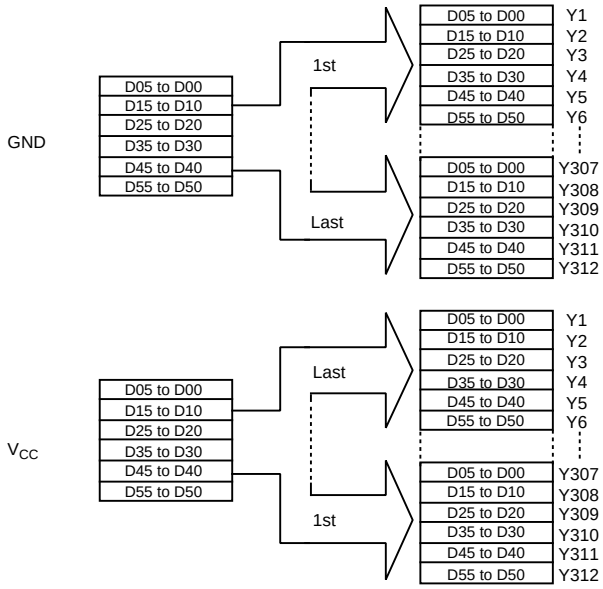


Figure 4 Display Data Shift Direction

System Overview

Figure 5 shows a block diagram of an XGA (1024 × 768)-applicable TFT color panel configured with multiple HD66322Ts. These HD66322Ts latch 6-bit data per dot, and select and output one level among 64 internally generated LCD-drive voltage levels of positive or negative polarity. When the pixels are structured using R, G, and B color filters, a maximum of 260 thousand colors can be displayed. In addition, the inversion drive for each row or for each dot can be achieved even though the HD66322Ts are located on one side as long as the inversion output function for each pin is used; this achieves a high-quality display.

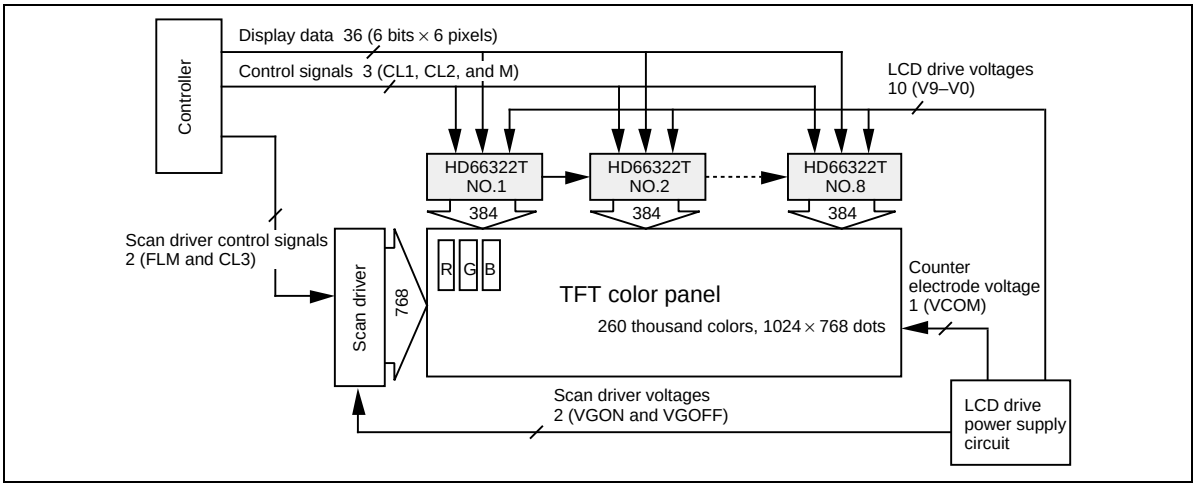
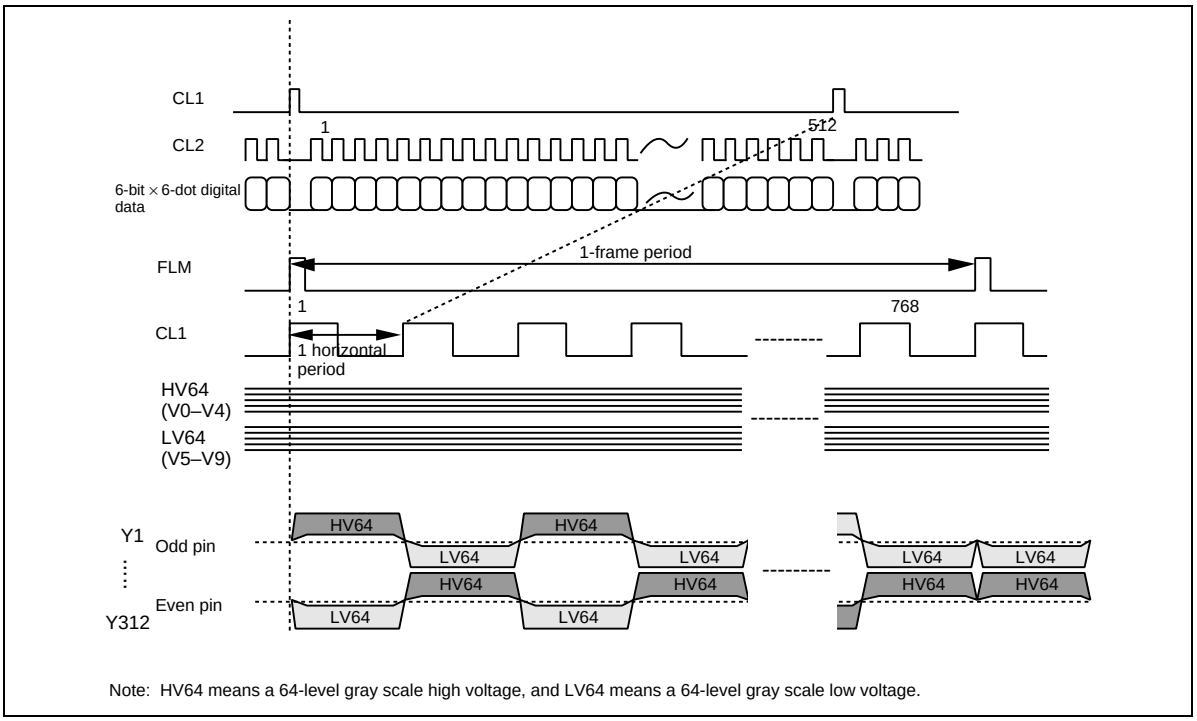


Figure 5 System Block Diagram



Note: HV64 means a 64-level gray scale high voltage, and LV64 means a 64-level gray scale low voltage.

Figure 6 Timing Chart (Example of Dot-Inversion Drive Method)

Relationship between Display Data and Output Voltage

The HD66322T outputs 64-level gray scale high voltage and 64-level gray scale low voltage generated by 10 levels of input LCD drive power supply voltage and 6-bit digital data. Figure 7 shows the relationship among the input voltages from the LCD drive power supply circuit, digital codes, and output voltages.

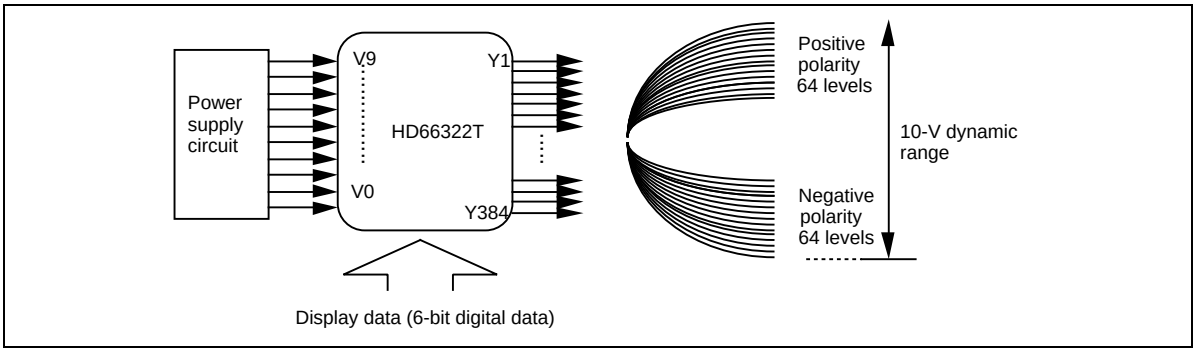


Figure 7 Selection of LCD Drive Output Level

Table 2 64-Level Gray Scale High Voltage

Display Data						
Di5	**Di4**	**Di3**	**Di2**	**Di1**	**Di0**	**64-Level Gray Scale High Voltage**
1	1	1	1	1	1	V4
1	1	1	1	1	0	V3 + 1819/2886 × (V4 – V3)
1	1	1	1	0	1	V3 + 1286/2886 × (V4 – V3)
1	1	1	1	0	0	V3 + 886/2886 × (V4 – V3)
1	1	1	0	1	1	V3 + 619/2886 × (V4 – V3)
1	1	1	0	1	0	V3 + 390/2886 × (V4 – V3)
1	1	1	0	0	1	V3 + 190/2886 × (V4 – V3)
1	1	1	0	0	0	V3
1	1	0	1	1	1	V2 + 2535/2697 × (V3 – V2)
1	1	0	1	1	0	V2 + 2377/2697 × (V3 – V2)
1	1	0	1	0	1	V2 + 2217/2697 × (V3 – V2)
1	1	0	1	0	0	V2 + 2084/2697 × (V3 – V2)
1	1	0	0	1	1	V2 + 1951/2697 × (V3 – V2)
1	1	0	0	1	0	V2 + 1818/2697 × (V3 – V2)
1	1	0	0	0	1	V2 + 1707/2697 × (V3 – V2)
1	1	0	0	0	0	V2 + 1600/2697 × (V3 – V2)
1	0	1	1	1	1	V2 + 1500/2697 × (V3 – V2)
1	0	1	1	1	0	V2 + 1400/2697 × (V3 – V2)
1	0	1	1	0	1	V2 + 1300/2697 × (V3 – V2)
1	0	1	1	0	0	V2 + 1200/2697 × (V3 – V2)
1	0	1	0	1	1	V2 + 1100/2697 × (V3 – V2)
1	0	1	0	1	0	V2 + 1000/2697 × (V3 – V2)
1	0	1	0	0	1	V2 + 900/2697 × (V3 – V2)
1	0	1	0	0	0	V2 + 800/2697 × (V3 – V2)
1	0	0	1	1	1	V2 + 700/2697 × (V3 – V2)
1	0	0	1	1	0	V2 + 600/2697 × (V3 – V2)
1	0	0	1	0	1	V2 + 500/2697 × (V3 – V2)
1	0	0	1	0	0	V2 + 400/2697 × (V3 – V2)
1	0	0	0	1	1	V2 + 300/2697 × (V3 – V2)
1	0	0	0	1	0	V2 + 200/2697 × (V3 – V2)
1	0	0	0	0	1	V2 + 100/2697 × (V3 – V2)
1	0	0	0	0	0	V2

Table 2 64-Level Gray Scale High Voltage (cont)

Display Data						
Di5	**Di4**	**Di3**	**Di2**	**Di1**	**Di0**	**64-Level Gray Scale High Voltage**
0	1	1	1	1	1	V1 + 3322/3422 × (V2 – V1)
0	1	1	1	1	0	V1 + 3222/3422 × (V2 – V1)
0	1	1	1	0	1	V1 + 3122/3422 × (V2 – V1)
0	1	1	1	0	0	V1 + 3015/3422 × (V2 – V1)
0	1	1	0	1	1	V1 + 2904/3422 × (V2 – V1)
0	1	1	0	1	0	V1 + 2793/3422 × (V2 – V1)
0	1	1	0	0	1	V1 + 2682/3422 × (V2 – V1)
0	1	1	0	0	0	V1 + 2571/3422 × (V2 – V1)
0	1	0	1	1	1	V1 + 2460/3422 × (V2 – V1)
0	1	0	1	1	0	V1 + 2349/3422 × (V2 – V1)
0	1	0	1	0	1	V1 + 2238/3422 × (V2 – V1)
0	1	0	1	0	0	V1 + 2127/3422 × (V2 – V1)
0	1	0	0	1	1	V1 + 1994/3422 × (V2 – V1)
0	1	0	0	1	0	V1 + 1861/3422 × (V2 – V1)
0	1	0	0	0	1	V1 + 1728/3422 × (V2 – V1)
0	1	0	0	0	0	V1 + 1595/3422 × (V2 – V1)
0	0	1	1	1	1	V1 + 1435/3422 × (V2 – V1)
0	0	1	1	1	0	V1 + 1275/3422 × (V2 – V1)
0	0	1	1	0	1	V1 + 1115/3422 × (V2 – V1)
0	0	1	1	0	0	V1 + 925/3422 × (V2 – V1)
0	0	1	0	1	1	V1 + 725/3422 × (V2 – V1)
0	0	1	0	1	0	V1 + 496/3422 × (V2 – V1)
0	0	1	0	0	1	V1 + 267/3422 × (V2 – V1)
0	0	1	0	0	0	V1
0	0	0	1	1	1	V0 + 3733/4000 × (V1 – V0)
0	0	0	1	1	0	V0 + 3333/4000 × (V1 – V0)
0	0	0	1	0	1	V0 + 2933/4000 × (V1 – V0)
0	0	0	1	0	0	V0 + 2533/4000 × (V1 – V0)
0	0	0	0	1	1	V0 + 2000/4000 × (V1 – V0)
0	0	0	0	1	0	V0 + 1467/4000 × (V1 – V0)
0	0	0	0	0	1	V0 + 800/4000 × (V1 – V0)
0	0	0	0	0	0	V0

Table 3 64-Level Gray Scale Low Voltage

Display Data						
Di5	**Di4**	**Di3**	**Di2**	**Di1**	**Di0**	**64-Level Gray Scale Low Voltage**
1	1	1	1	1	1	V5
1	1	1	1	1	0	V6 + 1819/2886 × (V5 – V6)
1	1	1	1	0	1	V6 + 1286/2886 × (V5 – V6)
1	1	1	1	0	0	V6 + 886/2886 × (V5 – V6)
1	1	1	0	1	1	V6 + 619/2886 × (V5 – V6)
1	1	1	0	1	0	V6 + 390/2886 × (V5 – V6)
1	1	1	0	0	1	V6 + 190/2886 × (V5 – V6)
1	1	1	0	0	0	V6
1	1	0	1	1	1	V7 + 2537/2697 × (V6 – V7)
1	1	0	1	1	0	V7 + 2377/2697 × (V6 – V7)
1	1	0	1	0	1	V7 + 2217/2697 × (V6 – V7)
1	1	0	1	0	0	V7 + 2084/2697 × (V6 – V7)
1	1	0	0	1	1	V7 + 1951/2697 × (V6 – V7)
1	1	0	0	1	0	V7 + 1818/2697 × (V6 – V7)
1	1	0	0	0	1	V7 + 1707/2697 × (V6 – V7)
1	1	0	0	0	0	V7 + 1600/2697 × (V6 – V7)
1	0	1	1	1	1	V7 + 1500/2697 × (V6 – V7)
1	0	1	1	1	0	V7 + 1400/2697 × (V6 – V7)
1	0	1	1	0	1	V7 + 1300/2697 × (V6 – V7)
1	0	1	1	0	0	V7 + 1200/2697 × (V6 – V7)
1	0	1	0	1	1	V7 + 1100/2697 × (V6 – V7)
1	0	1	0	1	0	V7 + 1000/2697 × (V6 – V7)
1	0	1	0	0	1	V7 + 900/2697 × (V6 – V7)
1	0	1	0	0	0	V7 + 800/2697 × (V6 – V7)
1	0	0	1	1	1	V7 + 700/2697 × (V6 – V7)
1	0	0	1	1	0	V7 + 600/2697 × (V6 – V7)
1	0	0	1	0	1	V7 + 500/2697 × (V6 – V7)
1	0	0	1	0	0	V7 + 400/2697 × (V6 – V7)
1	0	0	0	1	1	V7 + 300/2697 × (V6 – V7)
1	0	0	0	1	0	V7 + 200/2697 × (V6 – V7)
1	0	0	0	0	1	V7 + 100/2697 × (V6 – V7)
1	0	0	0	0	0	V7

Table 3 64-Level Gray Scale Low Voltage (cont)

Display Data						
Di5	**Di4**	**Di3**	**Di2**	**Di1**	**Di0**	**64-Level Gray Scale Low Voltage**
0	1	1	1	1	1	V8 + 3322/3422 × (V7 – V8)
0	1	1	1	1	0	V8 + 3222/3422 × (V7 – V8)
0	1	1	1	0	1	V8 + 3122/3422 × (V7 – V8)
0	1	1	1	0	0	V8 + 3015/3422 × (V7 – V8)
0	1	1	0	1	1	V8 + 2904/3422 × (V7 – V8)
0	1	1	0	1	0	V8 + 2793/3422 × (V7 – V8)
0	1	1	0	0	1	V8 + 2682/3422 × (V7 – V8)
0	1	1	0	0	0	V8 + 2571/3422 × (V7 – V8)
0	1	0	1	1	1	V8 + 2460/3422 × (V7 – V8)
0	1	0	1	1	0	V8 + 2349/3422 × (V7 – V8)
0	1	0	1	0	1	V8 + 2238/3422 × (V7 – V8)
0	1	0	1	0	0	V8 + 2127/3422 × (V7 – V8)
0	1	0	0	1	1	V8 + 1994/3422 × (V7 – V8)
0	1	0	0	1	0	V8 + 1861/3422 × (V7 – V8)
0	1	0	0	0	1	V8 + 1728/3422 × (V7 – V8)
0	1	0	0	0	0	V8 + 1595/3422 × (V7 – V8)
0	0	1	1	1	1	V8 + 1435/3422 × (V7 – V8)
0	0	1	1	1	0	V8 + 1275/3422 × (V7 – V8)
0	0	1	1	0	1	V8 + 1115/3422 × (V7 – V8)
0	0	1	1	0	0	V8 + 925/3422 × (V7 – V8)
0	0	1	0	1	1	V8 + 725/3422 × (V7 – V8)
0	0	1	0	1	0	V8 + 496/3422 × (V7 – V8)
0	0	1	0	0	1	V8 + 267/3422 × (V7 – V8)
0	0	1	0	0	0	V8
0	0	0	1	1	1	V9 + 3733/4000 × (V8 – V9)
0	0	0	1	1	0	V9 + 3333/4000 × (V8 – V9)
0	0	0	1	0	1	V9 + 2933/4000 × (V8 – V9)
0	0	0	1	0	0	V9 + 2533/4000 × (V8 – V9)
0	0	0	0	1	1	V9 + 2000/4000 × (V8 – V9)
0	0	0	0	1	0	V9 + 1467/4000 × (V8 – V9)
0	0	0	0	0	1	V9 + 800/4000 × (V8 – V9)
0	0	0	0	0	0	V9

Relationship between Input Data and Output Voltage

The HD66322T outputs gray scale voltages whose polarities are different at odd number output pins and even number output pins with respect to the LCD counter-electrode voltage. The relationship between input data and output pins is shown in Figure 8 for the following conditions:

VLCD–0.2 ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VLCD/2, and
VLCD/2 ≥ V5 ≥ V6 ≥ V7 ≥ V8 ≥ V9 ≥ 0.2V

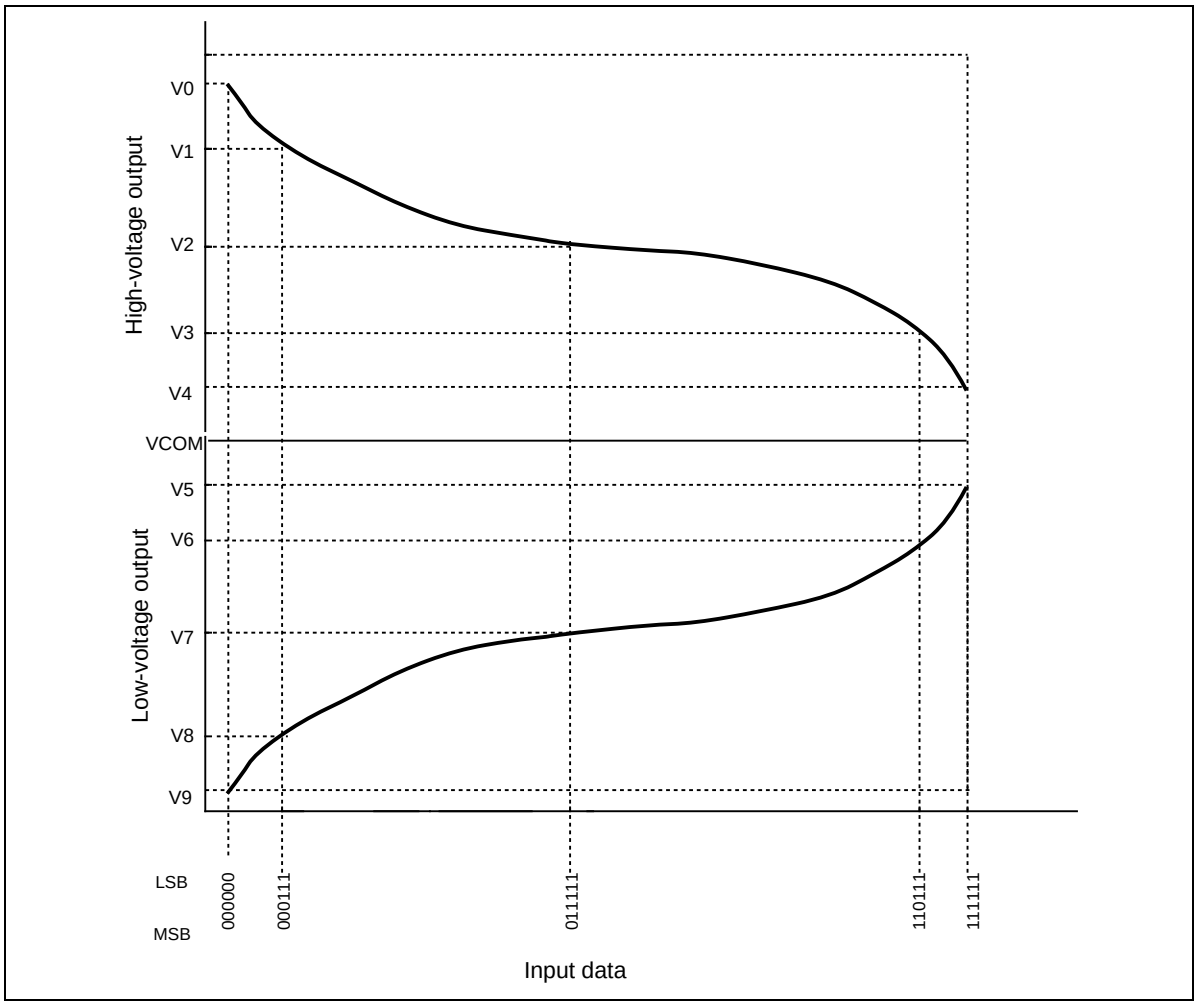


Figure 8 Relationship between Input Data and Output Voltages

Inversion Drive for Each Output Pin

The HD66322T generates a 64-level positive- or negative-polarity grayscale voltage with respect to the inversion reference voltage for each adjacent odd and even number output pin. In addition, the LCD AC drive can be controlled by switching the polarity of the M signal (refer to the section on Pin Functions).

Thus, if the HD66322Ts are located on one side of the TFT LCD panel, a dot inversion drive, which can apply the grayscale voltage with the opposite polarity to each adjacent dot, can be performed by switching the polarity of the M signal for each CL1 input. This can decrease crosstalk degrading display quality and achieve a high-quality display.

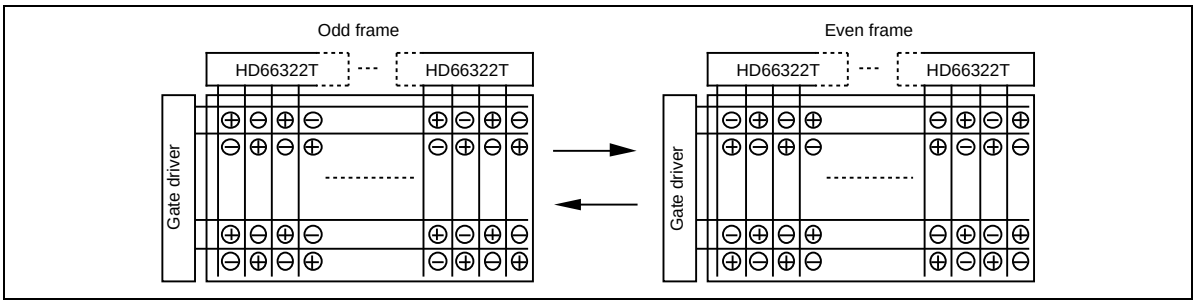


Figure 9 Dot-Inversion Drive

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit (low voltage)	V_{CC}	–0.3 to + 5.0	V	1
	LCD drive circuit (high voltage)	VLCD	–0.3 to + 12.0	V	1
Input voltage (high voltage)		Vt1	–0.3 to V_{LCD} + 0.3	V	1 and 2
Input voltage (low voltage)		Vt2	–0.3 to V_{CC} + 0.3	V	1, 3, and 4
Operating temperature		Topr	–20 to +75	°C	
Storage temperature		Tstg	–40 to +125	°C	

Notes: If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

1. Assuming GND = 0V.
2. Applies to input pins CL1, CL2, SHL, Dxx, M, and POL, and I/O pins $\overline{IO0}$ and $\overline{IO1}$ when used as input.
3. Specifies voltage to be input to the LCD drive power supply pins.
   Either of the following relationships must be held:
   V_{LCD}–0.2 ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{LCD}/2 and V_{LCD}/2 ≥ V5 ≥ V6 ≥ V7 ≥ V8 ≥ V9 ≥ 0.2V, or
   V_{LCD}–0.2 ≥ V4 ≥ V3 ≥ V2 ≥ V1 ≥ V0 ≥ V_{LCD}/2 and V_{LCD}/2 ≥ V9 ≥ V8 ≥ V7 ≥ V6 ≥ V5 ≥ 0.2V
4. The following relationship must be held for the electrical potentials of V9 to V5 and V4 to V0.
   $Vin - V_{n+1} \leq 1V$ (n = 0 to 3 or 5 to 8)

Electrical Characteristics

DC Characteristics (V_{CC}–GND = 3.0 to 3.6V, VLCD–GND = 9.5 ~ 10.5V, and Ta = –20 to +75 °C, unless otherwise stated)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	VIH	CL1, CL2, SHL, Dij, M, POL, EIO1 (I), and EIO2 (I)	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	VIL		0		$0.3 \times V_{CC}$	V		
Output high level voltage	VOH	EIO1 (O) and EIO2 (O)	$V_{CC} - 0.4$	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	VOL		—	—	0.4	V	I_{OL} = 0.4 mA	
Input leakage current (1)	I_{IL1}	CL1, CL2, SHL, Dij, M, and POL	–5	—	+5	µA		
Input leakage current (2)	I_{IL2}	EIO1 (I) and EIO2 (I)	–10	—	+10	µA		
Output offset voltage	Voff	Y1 to Y312	—	—	±10	mV	V_{EE} = 13V f_{CL1} = 53.8 kHz (1 horizontal = 18.6 µs)	1
Logic unit consumptive current	I_{CC}	V_{CC}	—	—	4.5	mA	V_{CC} = 3.3V V_{LCD} = 10V f_{CL1} = 71.7 kHz (1 horizontal = 14 µs) f_{CL2} = 65 MHz	2
Standby consumptive current	I_{ST}	V_{CC}	—	—	0.7	mA		
LCD drive power supply voltage (2)	I_{LCD}	V_{LCD}	—	—	4.5	mA		

Notes: 1 Output offset voltage Voff is defined as difference between the actual output voltage and output voltage expected.

2. Except for the current flowing in V0 to V9; outputs are unloaded.

AC Characteristics (V_{CC}–GND = 3.0 to 3.6V, VLCD–GND = 9.5 ~ 10.5V, and Ta = –20 to +75 °C, unless otherwise stated)

Item	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit	Conditions	Note
Clock cycle time	f_{max}	CL2	—	—	65	MHz		
Clock high level width	T_{cwh}	CL2	7	—	—	ns		
Clock low level width	T_{cwl}	CL2	7	—	—	ns		
Clock rise time	T_r	CL1 and CL2	—	—	4	ns		
Clock fall time	T_f	CL1 and CL2	—	—	4	ns		
Clock setup time	T_{su}	CL1 and CL2	50	—	—	ns		
Clock hold time	T_h	CL1 and CL2	300	—	—	ns		
Data setup time	T_{dsu}	Dij and CL2	3	—	—	ns		
Data hold time	T_{dh}	Dij and CL2	3	—	—	ns		
POL setup time	T_{psu}	POL and CL2	3	—	—	ns		
POL hold time	T_{ph}	POL and CL2	3	—	—	ns		
M setup time	T_{msu}	M and CL2	100	—	—	ns		
M hold time	T_{mh}	M and CL1	200	—	—	ns		
Enable setup time	T_{esu}	EIO1, EIO2, and CL2	0	—	—	ns		
Enable output delay time	T_{ed}	EIO1, EIO2, and CL2	—	—	30	ns		1
CL1 high level width	T_{cl1wh}	CL1	56	—	—	ns		
Driver output delay time	T_{dd}	CL1 and Y1 to Y384	—	—	10	µs	VLCD = 10V Ta = 25 °C	2

Notes: 1. The load conditions of an enable output pin are shown in Figure 13.
2. Defined under the conditions shown in Figure 14.

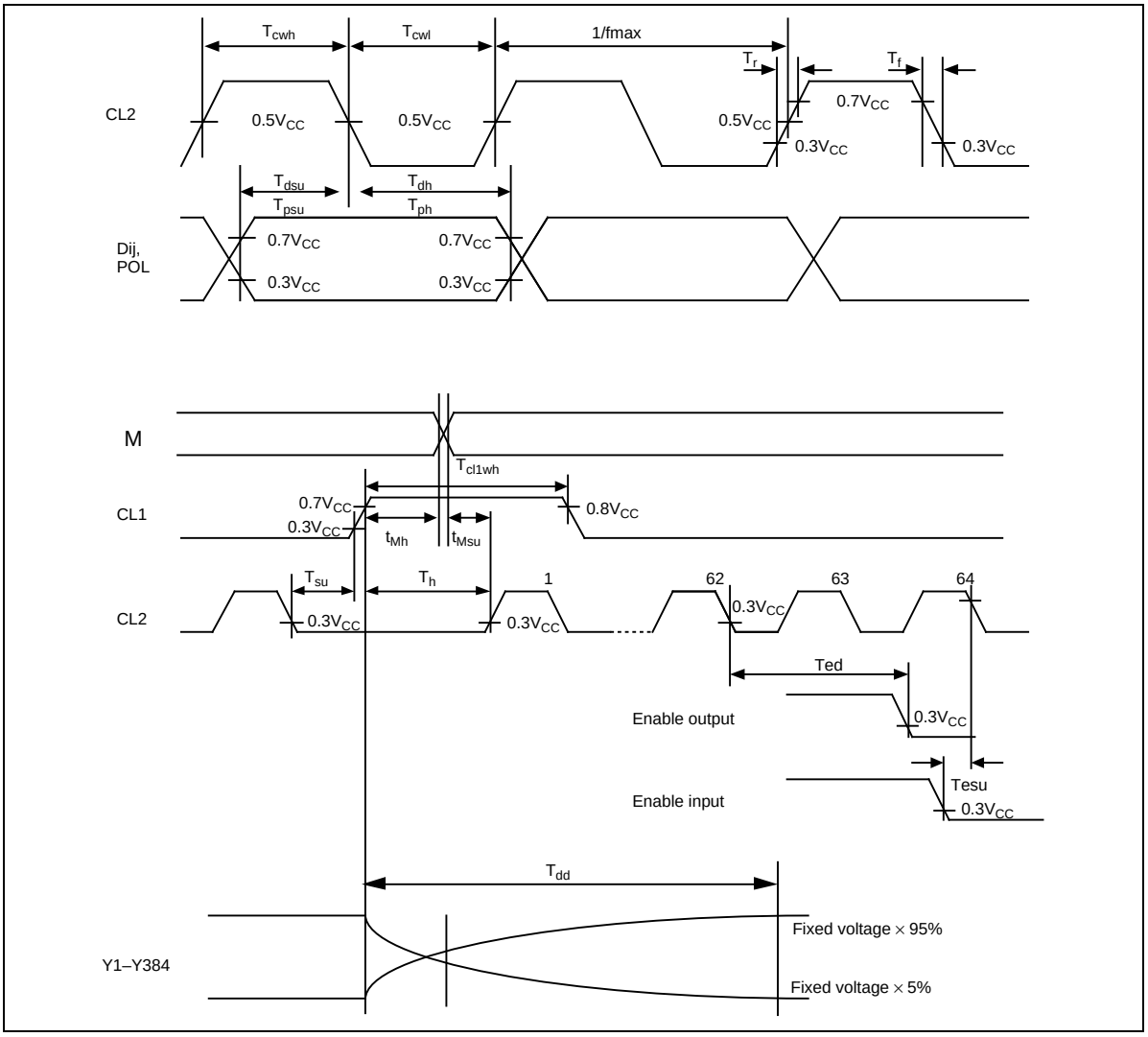


Figure 10 AC Characteristics

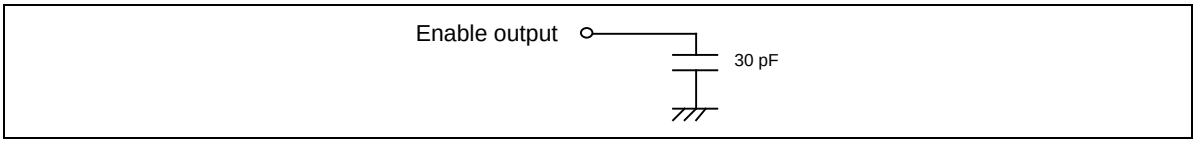


Figure 11 Load Conditions of Enable Output Pin

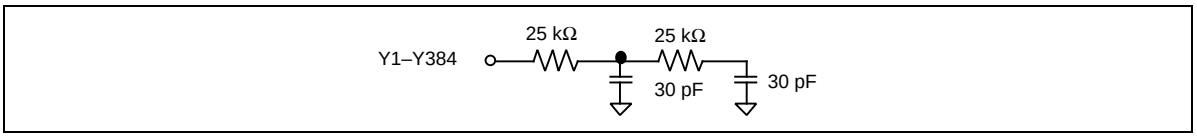


Figure 12 Load Conditions for Definition of Driver Output Delay Time