PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD6481

TIMING GENERATOR LSI FOR THREE-DIMENSION Y/C SEPARATION

The μPD6481 (TIGIII) is a timing generator for three-dimension Y/C separation. It generates clock and various kinds of timing provided to the LSI for three-dimension Y/C separation system. The μPD6481 (TIGIII) has been developed and released by selecting the required functions for three-dimension Y/C separation system from the μPD9389 (TIGIIa), which is the timing generator for EDTV. By combining with another LSI (YCSIII), signal processing system for three-dimension Y/C separation can be composed.

FEATURES

- Built-in control signal generator of field memory μPD42280
- 2 kinds of built-in clock circuits
  Burst synchronizing clock and line synchronizing clock
- Built-in various timing generators
- Built-in nonstandard signal detector
- With clock switching pin
- System clock : 14.3 MHz
- Allows data setting by serial bus control.
- Power supply : +5 V
- CMOS technology

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD6481GC-3B6	52-pin plastic QFP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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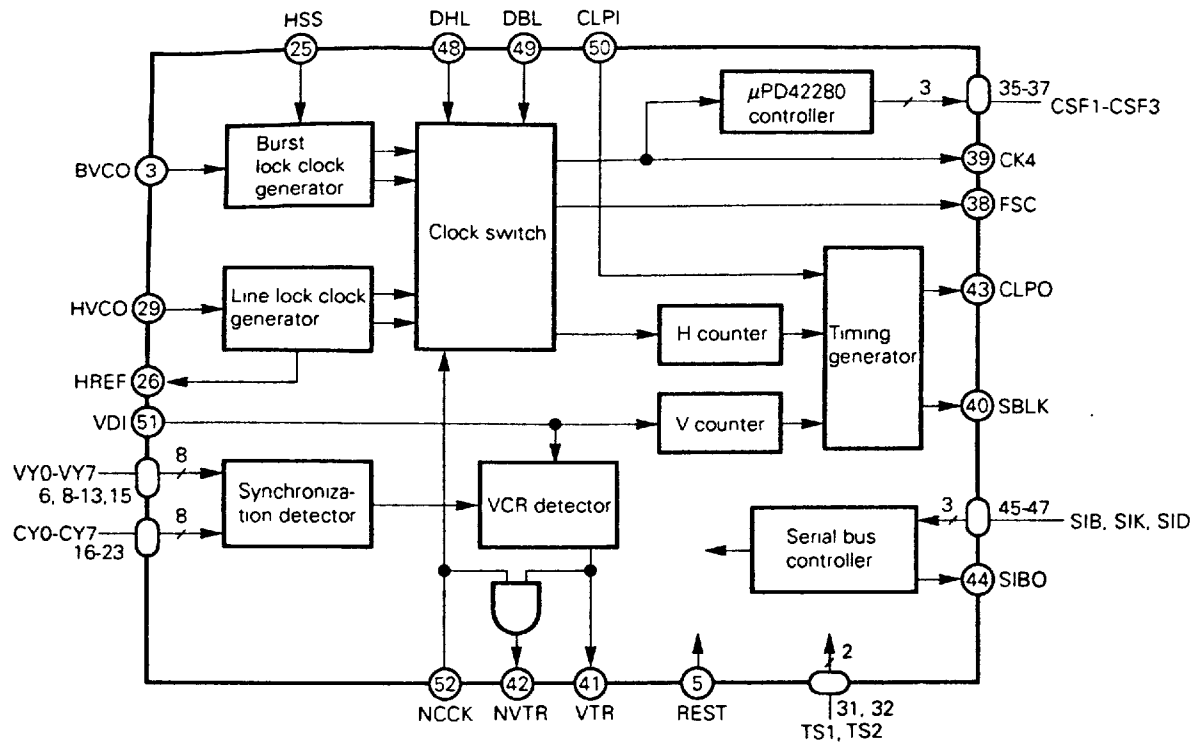
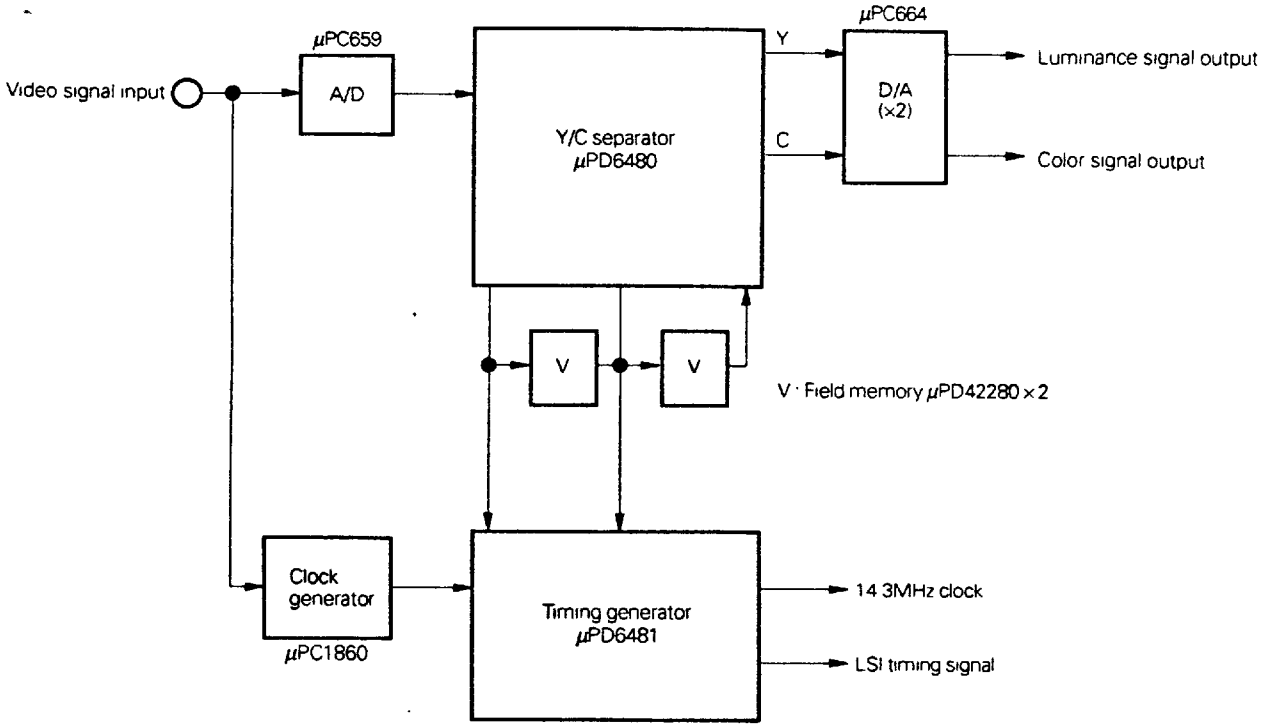
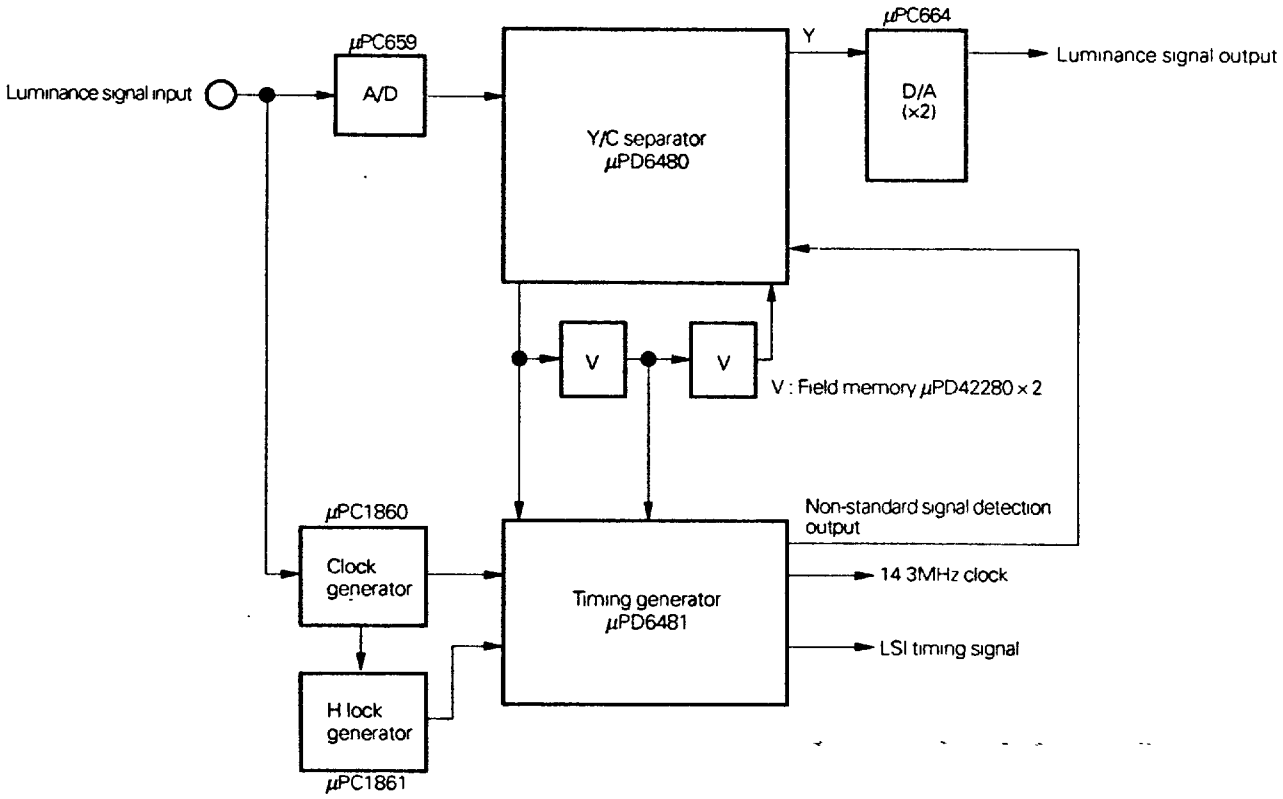
BLOCK DIAGRAM



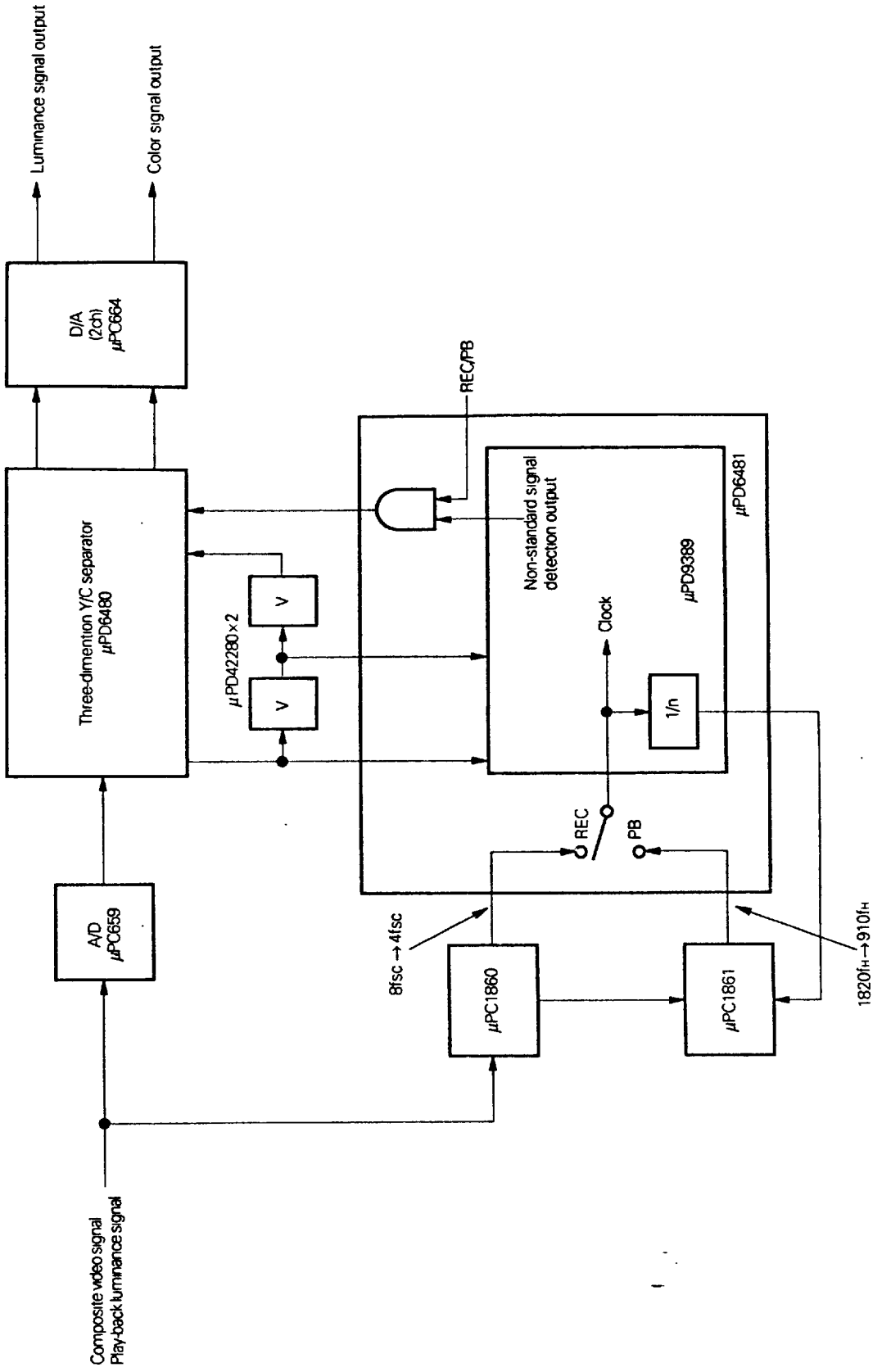
BLOCK DIAGRAM OF THREE-DIMENSION Y/C SEPARATION SYSTEM



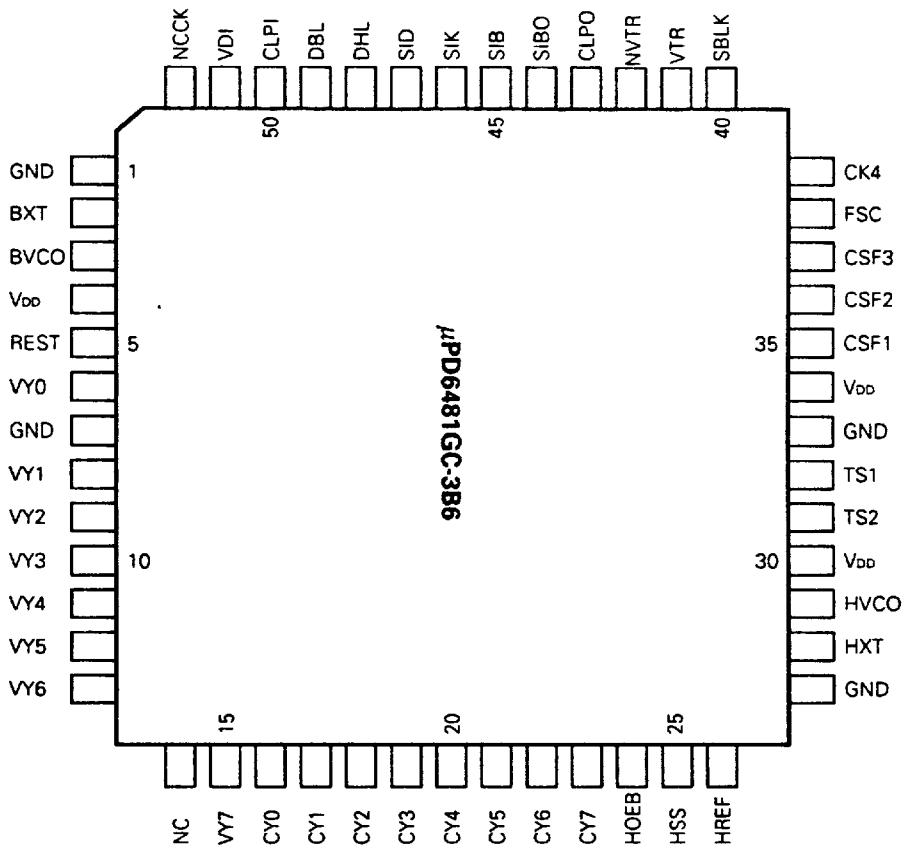
BLOCK DIAGRAM OF MOTION ADAPTIVE NOISE REDUCTION SYSTEM



APPLICATION OF THREE-DIMENSION Y/C SEPARATION SYSTEM TO VCR



PIN CONFIGURATION (Top View)



PIN NAME

Pin No.	Symbol	Name
1	GND	Ground
2	BXT	Output for testing (burst VCO oscillation output)
3	BVCO	Burst VCO oscillation input
4	V_{DD}	Power supply
5	REST	Master reset input
6	VY0	Data input A for non-standard signal detection
7	GND	Ground
8 | 13	VY1 | VY6	Data input A for non-standard signal detection
14	NC	Non-connect pin
15	VY7	Data input A for non-standard signal detection
16 | 23	CY0 | CY7	Data input B for non-standard signal detection
24	HOEB	Input for testing
25	HSS	H phase-comparison input
26	HREF	H-PLL reference output
27	GND	Ground
28	HXT	Output for testing (line VCO oscillation output)
29	HVCO	H-VCO oscillation input
30	V_{DD}	Power supply

Pin No.	Symbol	Name
31	TS2	Input for testing
32	TS1	Input for testing
33	GND	Ground
34	V_{DD}	Power supply
35 | 37	CSF1 | CSF3	Output for memory control
38	FSC	Subcarrier output
39	CK4	14 MHz clock output
40	SBLK	YCSIII blank output
41	VTR	Forced motion output
42	NVTR	Forced motion output for VCR
43	CLPO	Clamp output for A/D
44	SIBO	Serial bus busy output
45	SIB	Serial bus busy input
46	SIK	Serial bus clock input
47	SID	Serial bus data input
48	DHL	Forced line lock input
49	DBL	Forced burst lock input
50	CLPI	Clamp input
51	VDI	Vertical synchronizing signal input
52	NCCK	REC/$\overline{PB}$ mode input

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameters	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	−0.3 to +7.0	V
Input voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_d	300	mW
Operating ambient temperature	T_{opt}	−20 to +70	°C
Storage temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +70 °C)

Parameters	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Power supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		0		V_{DD}	V
Output voltage	V_O		0		V_{DD}	V
Clock input frequency	f_{CK}			14.31818		MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 0.5 V, GND = 0 V, T_a = −20 to +70 °C)

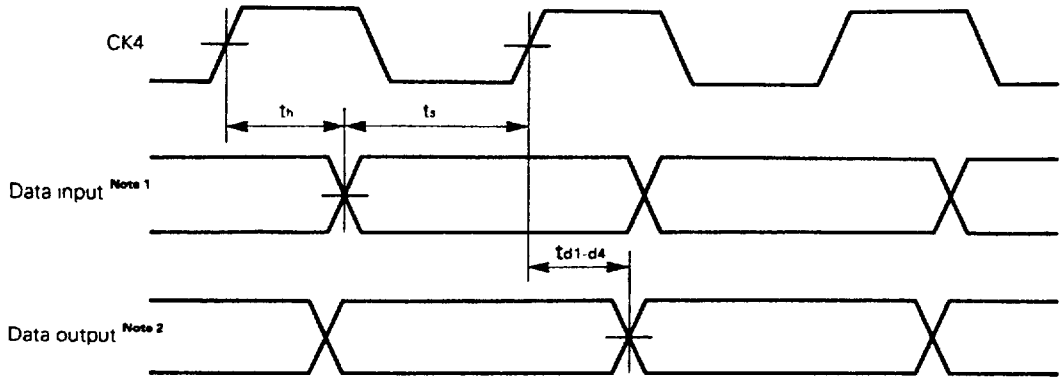
Parameters	Symbol	Conditions		Ratings			Unit
				MIN.	TYP.	MAX.	
Power supply voltage	V_{DD}			4.5	5.0	5.5	V
Current consumption	I_{DD}				30	50	mA
High level input voltage	V_{IH}	CMOS level input				0.7 V_{DD}	V
Low level input voltage	V_{IL}			0.3 V_{DD}			V
High level input voltage	V_{IH}	TTL level input				2.0	V
Low level input voltage	V_{IL}			0.8			V
High level threshold voltage	V_{T^+}	CMOS Schmitt triggered level input					
Low level threshold voltage	V_{T^-}						
Hysteresis voltage	V_H						
Input leak current	I_I	Normal input	V_I=V_{DD} or GND	−10	0	10	μA
High level input current	I_{IH}	Input with pull-down resistor	V_I=V_{DD}	40	100	270	μA
High level output current	I_{OH}	CMOS level output (−1.6/4.5 mA type)	V_{OH}=V_{DD} −0.4 V			−1.6	mA
Low level output current	I_{OL}		V_{OL}=0.4 V	4.5			mA
High level output current	I_{OH}	CMOS level output (−3.2/9.0 mA type)	V_{OH}=V_{DD} −0.4 V			−3.2	mA
Low level output current	I_{OL}		V_{OL}=0.4 V	9.0			mA
Low level output current	I_{OL}	N-ch open drain output	V_{OL}=0.4 V	9.0			mA
Output leak current	I_O	N-ch open drain output	V_O=V_{DD} or GND	−10	0	10	μA

SWITCHING CHARACTERISTICS

(V_{DD} = 5 V ± 0.5 V, GND = 0 V, CL = 15 pF, t_r = t_f = 2 ns, T_a = −20 to +70 °C)

Parameters	Symbol	Conditions		Ratings			Unit
				MIN.	TYP.	MAX.	
Clock input frequency	f_{CK}				14.31818		MHz
Rise time	t_{TLH}	CMOS level output (−1.6/4.5 mA type)	V_O="L"−"H"		7.5	16.0	ns
Fall time	t_{THL}		V_O="H"−"L"		3.6	7.8	ns
Rise time	t_{TLH}	CMOS level output (−3.2/9.0 mA type)	V_O="L"−"H"		2.5	5.5	ns
Fall time	t_{THL}		V_O="H"−"L"		1.7	3.7	ns
Propagation delay time	t_{d1}	CMOS level output	V_O="L"−"H"	5	15	40	ns
	t_{d2}		V_O="H"−"L"	5	15	40	ns
	t_{d3}	N-ch open drain output	V_O="L"−"Z"				
	t_{d4}		V_O="Z"−"L"				
Set-up time	t_s			4			ns
Hold time	t_h			10			ns
Input capacitance	C_T				5	10	pF

TIMING CHART



Note 1. VY0 - VY7 (6,8 - 13,15), CY0 - CY7 (16 - 23)

2. CLPO (43), SBLK (40), FSC (38)

PIN FUNCTIONS

	Symbol	Name	I/O characteristics			Function
			I/O	Signal level	Pull-down resistor (kΩ) I_{OH}/I_{OL} (mA)	
1	GND	Ground	—	—	—	0V : Ground potential
2	BXT	Output for testing (burst VCO oscillation output)	O	—	—	Output for testing 4 fsc is output.
3	BVCO	Burst VCO oscillation input	I	CMOS amplifier	—	VCO oscillation clock of burst lock PLL at 4 fsc (14.3 MHz) is input.
4	V_{DD}	Power Supply	—	—	—	+5 V (TYP.) Power supply voltage is applied.
5	REST	Master reset input	I	CMOS	PD:50	Input pin for forced reset Leave this pin unconnected or connect to GND in ordinary operation.
6	VY0	Data input A for non-standard signal detection	I	TTL	—	Y signal with burst signal is input. This signal is output from YCSIII (VY0 : LSB).
7	GND	Ground	—	—	—	0V : Ground potential
8 I 13	VY1 I VY6	Data input A for non-standard signal detection	I	TTL	—	Y signal with burst signal is input. This signal is output from YCSIII.
14	NC	Non-connect pin	—	—	—	Non-connect pin
15	VY7	Data input A for non-standard signal detection	I	TTL	—	Y signal with burst signal is input. This signal is output from YCSIII (VY7 : MSB).
16 I 23	CY0 I CY7	Data input B for non-standard signal detection	I	TTL	—	One field (262H) delayed signal of VY input is input (CY0 : LSB, CY7 : MSB).
24	HOEB	Input for testing	I	CMOS	PD:50	Input for testing
25	HSS	H phase-comparison input	I	CMOS	—	H signal frequency clock for AFC loop is input.
26	HREF	H-PLL reference output	O	CMOS	−1.6/4.5	Reference signal to line lock PLL is output. 910 f_H (14.3 MHz) signal input from HVCO pin is divided by 910 and is output as fH (15.734 kHz).
27	GND	Ground	—	—	—	0V : Ground potential
28	HXT	Output for testing (line VCO oscillation output)	O	—	—	Output for testing. 910 f_H is output.
29	HVCO	H-VCO oscillation input	I	CMOS amplifier	—	VCO oscillation clock of line lock PLL is input. 910 f_H (14.3 MHz) is input.

Pin No.	Symbol	Name	I/O characteristics			Function
			I/O	Signal level	Pull-down resistor (kΩ) I_{OH}/I_{OL} (mA)	
30	V_{DD}	Power supply	—	—	—	+5 V (TYP.) Power supply voltage is applied.
31	TS2	Input for testing	I	CMOS	PD:50	Input for testing Leave this pin unconnected or connect to GND in ordinary operation.
32	TS1	Input for testing	I	CMOS	PD:50	Input for testing Leave this pin unconnected or connect to GND in ordinary operation.
33	GND	Ground	—	—	—	0V: Ground potential
34	V_{DD}	Power supply	—	—	—	+5 V (TYP.) Power supply voltage is applied.
35 I 37	CSF1 I CSF3	Output for memory control	O	CMOS	-3.2/9.0	Output to control the memory for μPD6480
38	FSC	Subcarrier output	O	CMOS	-3.2/9.0	Output to FSC pin of YCP II. Reference phase output of fsc (3.58 MHz).
39	CK4	14 MHz clock output	O	CMOS	-3.2/9.0	4 fsc (14.3 MHz) clock for system
40	SBLK	YCSIII blank output	O	CMOS	-1.6/4.5	This is a signal for protecting synchronization signal of YCS III, and is input to BLK pin of YCS III (active high).
41	VTR	Forced motion output	O	CMOS	-1.6/4.5	High level is output by detecting non-standard signal, and is input to line pin of YCS III.
42	NVTR	Forced motion output for VCR	O	CMOS	-1.6/4.5	High level is output when detecting non-standard signal in three-dimension Y/C separation mode. In luminance signal NR mode, low level is output regardless of non- standard signal.
43	CLPO	Clamp output for A/D	O	CMOS	—	Pulse output for clamping the video signal immediately before A/D (active high).
44	SIBO	Serial bus busy output	O	N-ch open drain	—/9.0	Busy output for ACK response of serial bus
45	SIB	Serial bus busy input	I	CMOS Schmitt trig-gered	—	Busy input of serial bus

Pin No.	Symbol	Name	I/O characteristics			Function
			I/O	Signal level	Pull-down resistor (kΩ) I_{OH}/I_{OL} (mA)	
46	SIK	Serial bus clock input	I	CMOS Schmitt trig-gered	—	Clock input of serial bus
47	SID	Serial bus data input	I	CMOS Schmitt trig-gered	—	Data input of serial bus
48	DHL	Forced line lock input	I	CMOS	PD:50	High level switches system clock to line lock clock forcibly. Low level switches the clock auto-matically.
49	DBL	Forced burst lock input	I	CMOS	PD:50	High level switches system clock to burst lock clock forcibly. Low level switches the clock auto-matically.
50	CLPI	Clamp input	I	CMOS	—	Clamp pulse is input (active high).
51	VDI	V sync. signal input	I	CMOS	—	V sync. pulse synchronously separated from video signal is input (active low).
52	NCCK	REC/$\overline{PB}$ mode input	I	CMOS	PD:50	H : Three-dimension Y/C separation mode L : Luminance signal NR mode

FUNCTION DESCRIPTION

The μPD6481 (TIGIII) is an LSI providing clock and timing signal to μPD6480 and μPD42280, which compose three-dimension Y/C separation system. Due to the built-in non-standard signal detection circuit, the most suitable clock and signal processing mode corresponding to the signal being input are selected. Signal processing mode is selected by outputting the switching signal to each LSI for signal processing.

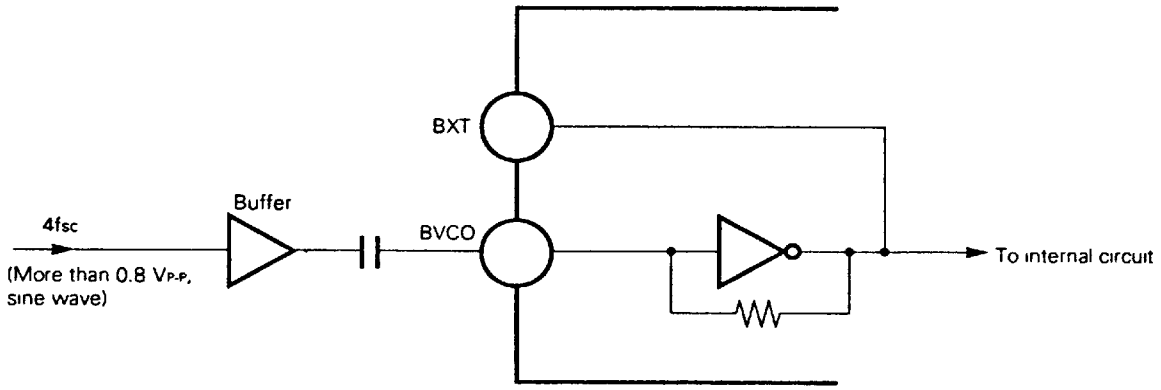
1. CLOCK GENERATION

The μPD6481 (TIGIII) has an internal frequency divider (1/910) to generate the clock synchronizing with horizontal synchronizing signal. The clock synchronizing with burst signal (4 fsc) is input from external device. These 2 clocks always oscillate, and are switched by the setting of mode switching pin (pin No.52) or detection output of the built-in nonstandard signal detection circuit.

1.1 Input Circuit of Burst Lock Clock

The clock of 14.3 MHz (4 fsc) synchronizing with burst signal is input to the μPD6481 (TIG III). The equivalent circuit of input part is shown in Fig. 1. The sine wave, amplitude of which is more than 0.8 V_{P-P}, or the square wave, duty cycle of which is 50 % should be input through the buffer and capacitor. Due to the built-in inverting amplifier with feedback resistance, the level is compensated up to CMOS level. The use of the μPC1860 is recommended for generating 4 fsc signal synchronizing with burst signal.

Fig. 1 Input Circuit of Burst Lock Clock



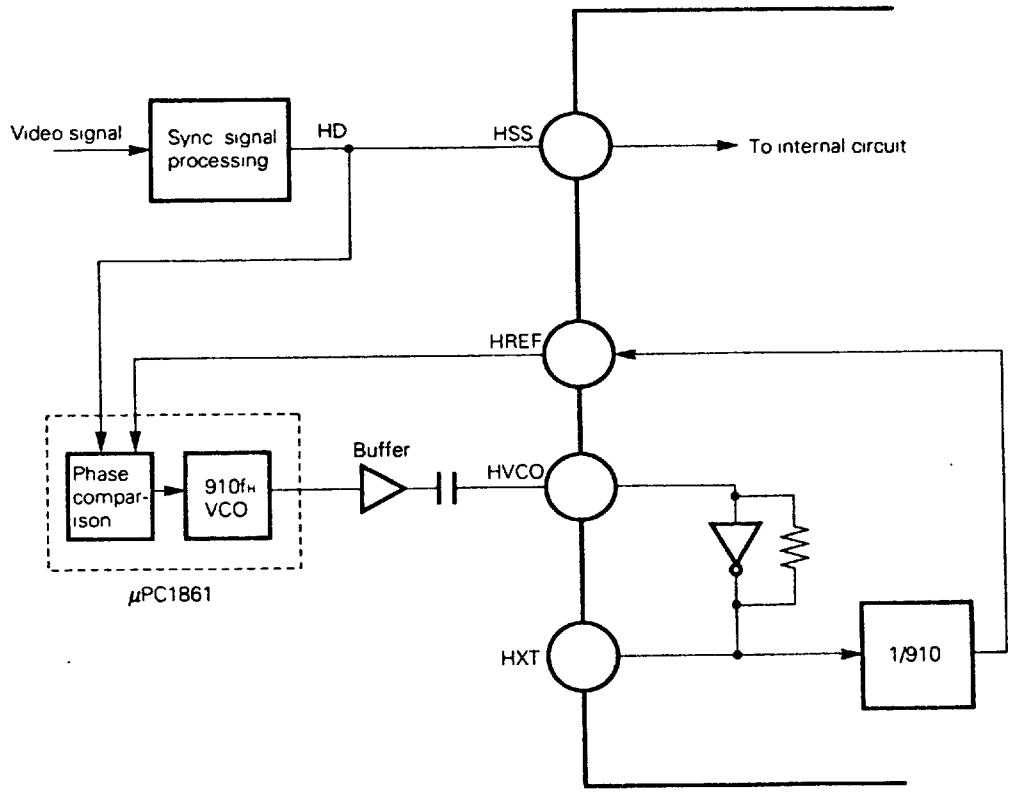
1.2 Line Lock PLL

Line lock PLL generates the clock (14.3 MHz) as 910 times as f_H from the HD signal which is phase-locked to horizontal synchronizing signal in analog sync. signal processing circuit. The 1/910 frequency divider is built in the μPD6481.

The use of the μPC1861 is recommended for phase comparison circuit to configurate PLL and 910 f_H VCO. The application circuit is shown in Fig. 2. The μPC1861 incorporates phase-comparison circuit, therefore, the circuit compares the phase of HD signal from sync. signal processing circuit with the signal devided by 910 in the μPD6481(TIGIII) (HREF output).

The input part of HVCO pin has the same configuration as Fig. 1. Therefore, the output signal of the μPC1861 through buffer and capacitor should be input.

Fig. 2 Application Using the μPC1861

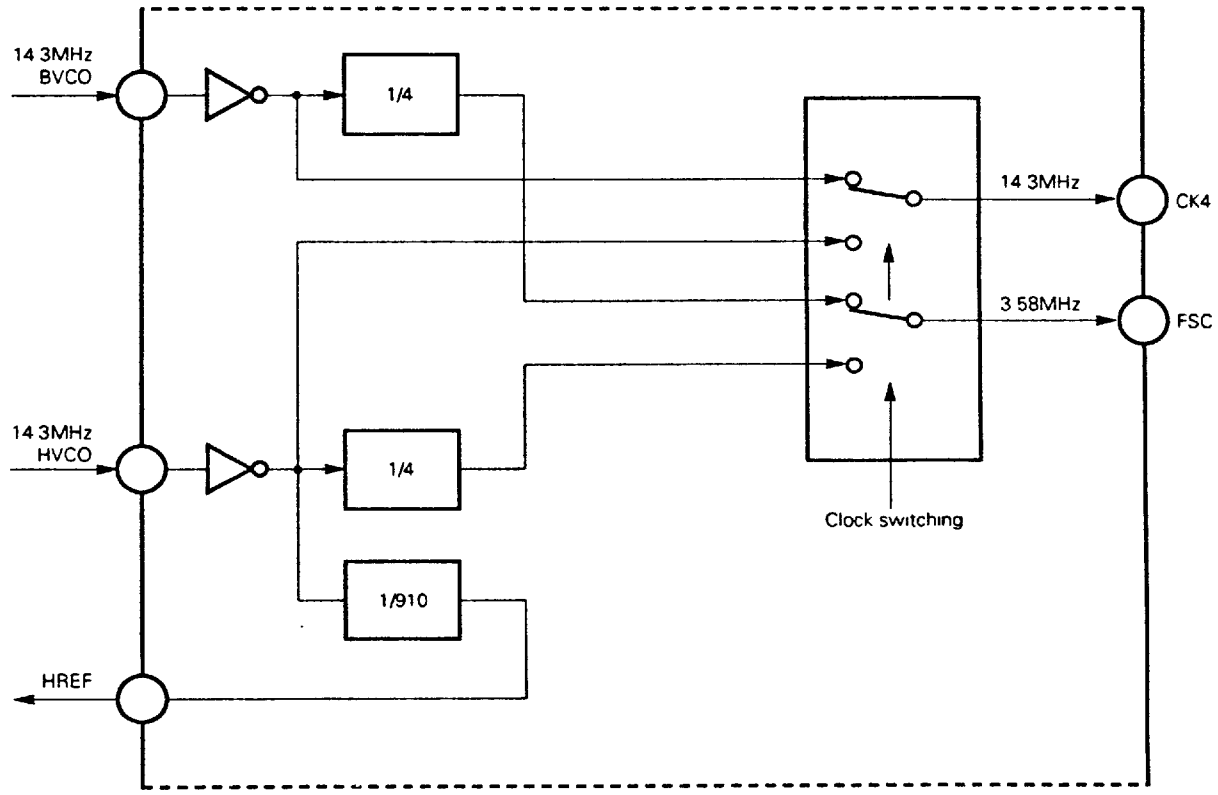


1.3 Clock Switching

The μPD6481 (TIGIII) uses 2 kinds of clocks (burst lock clock and line lock clock). These 2 clocks can be switched by setting through mode switch pin (pin No. 52) or by detecting the internal non-standard signal. Block diagram of switching part is shown in Fig. 3. In the following cases, burst lock clock is used.

- In the case that forced burst lock clock is selected through the serial bus(SA_0, D_3 = "1", D_2 = "0").
- In the case that forced burst lock clock is selected through the forced clock switching pin (DHL="L", DBL= "H").
- Three-dimension Y/C separation mode (pin No. 52 = "H") is selected through mode switching pin (pin No. 52).

Fig. 3 Block Diagram of Clock Switching



2. CONTROL OF THE μPD42280

The μPD6481 (TIGIII) incorporates a circuit to control 2M-bit field buffer μPD42280. The μPD42280 equips an internal counter circuit to generate reset pulse of the μPD42280. The counter values of each reset pulse are shown in Table 1.

Table 1 Timing for Control of the μPD42280

Pin name	Counter value
CSF1	238,420 (= 910 × 262)
CSF2 (At composite input)	237,510 (= 910 × 261)
CSF2 (At S pin input)	239,326 (= 910 × 263 – 4)
CSF3	238,419 (= 910 × 262 – 1)

3. DETECTION OF NON-STANDARD SIGNAL

The μPD6481 (TIGIII) incorporates a circuit detecting signals not based on NTSC signal specifications. This circuit is composed of the following 2 detection circuits.

(1) VCR detection circuit
(2) Sync. signal detection circuit

The result of detection is output to YCS III (μPD6480) from VTR pin.

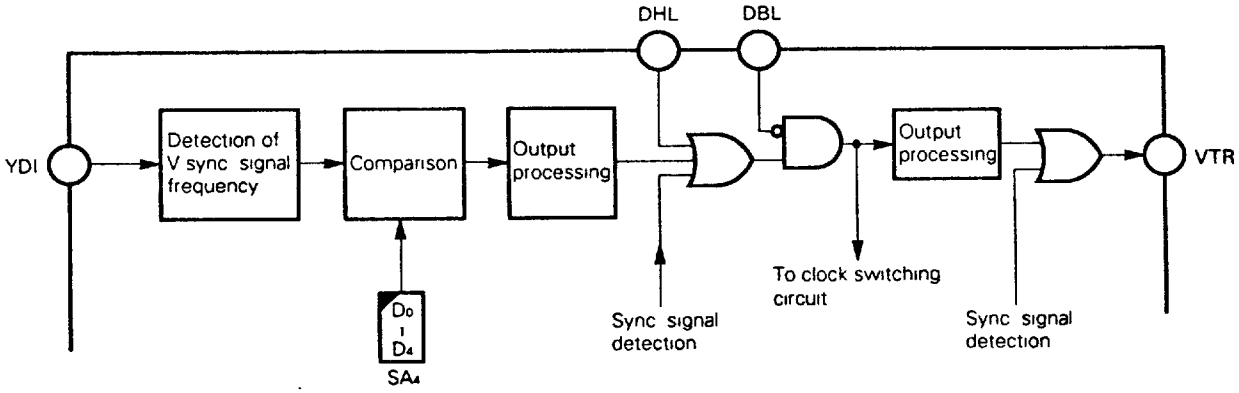
3.1 VCR Detection Circuit

The block diagram of VCR detection circuit is shown in Fig. 4. This circuit detects signals which do not have the relation of frequency interleave between color signal and vertical synchronizing signal like VCR signal, that is, the signal which can not be Y/C separated by frame correlation comb filter.

At first, vertical synchronizing frequency is detected, and the difference between the detected frequency and normal V sync. signal frequency is compared with the set value through the serial bus, then if the value is larger than the set value, input value is judged that the signal is not NTSC signal.

According to this result, system clock is to be line lock clock, and VTR pin is to be "H". When this VTR pin is connected to LINE pin of YCS III (μPD6480), inter-field Y/C separation is forcibly selected.

Fig. 4 Block Diagram of VCR Detection Circuit



3.2 Sync. Signal Detection Circuit

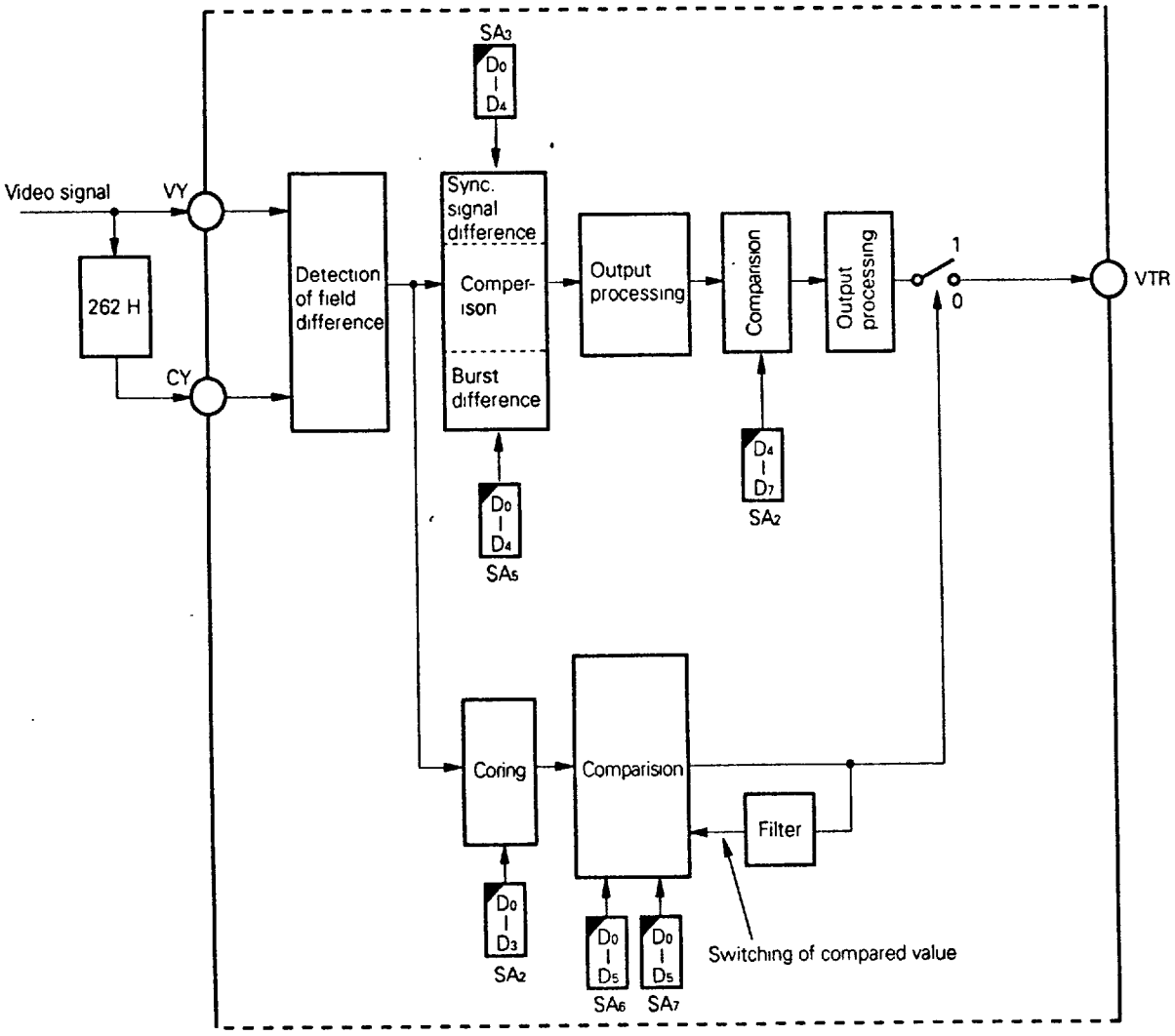
Block diagram of sync. signal detection circuit is shown in Fig. 5. This circuit detects different signals from the normal NTSC signal though this circuit has the relation of frequency interleave between color sub-carrier and horizontal synchronizing frequency in the same way as still picture data of laser disk.

To VY pin and CY pin, respectively, the signal which have time difference of 1 field (262H) is input. In the internal circuit, the difference between the horizontal synchronizing signal and burst part (difference of 1 field) is detected, and the difference is compared with the set value through serial bus to detect sync. signal.

This synchronizing signal detection circuit has a weak electric field detection circuit. Therefore, if noise is super-imposed on the output of the field difference, the circuit stops to prevent malfunction.

When sync. signal detection circuit is active, the VTR pin is to be "H". When this VTR pin is connected to LINE pin of YCSIII (μPD6480), inter-field Y/C separation is forcibly selected.

Fig. 5 Block Diagram of Synchronizing Detection Circuit



4. EXPLANATION OF SERIAL BUS INTERFACE

4.1 Explanation of Hardware

The μPD6481 (TIGIII) has a three-wire serial bus.

SID (serial data line)

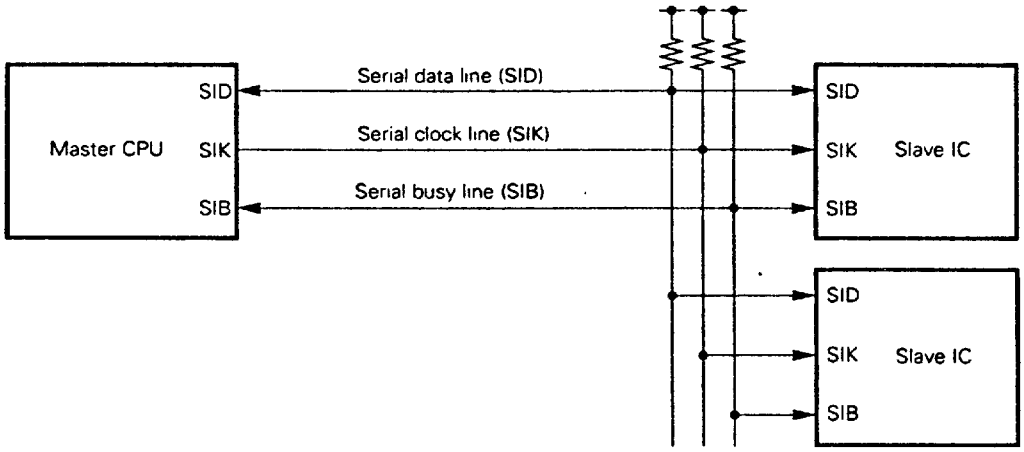
Master CPU outputs serial data synchronizing with the clock signal (SIK). The μPD6481 (TIGIII) takes in the data.

SIK (Serial clock line)

Master CPU outputs the serial clock. The μPD6481 (TIGIII) takes in the data synchronizing with this clock.

SIB (Serial busy line)

SIB is output so that master CPU operates the bus. The μPD6481 (TIGIII) starts taking in the data when this line is "L", and when the line is "H", the internal side forcibly returns to the initial status. At this time, the internal sub-address register is not initialized.



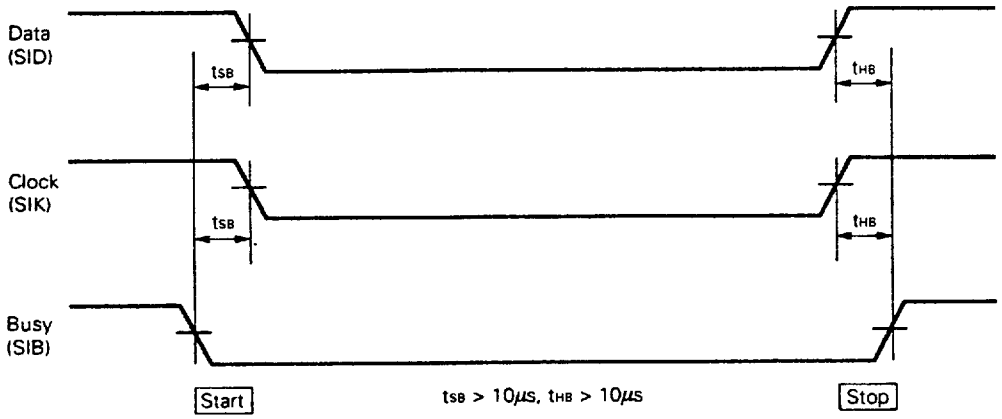
SID, SIK and SIB signals are of CMOS Schmitt triggered level input, to prevent malfunction. And SIBO output can be connected with SIB because of N-ch open drain configuration.

4.2 Software Specifications

The procedure that the master CPU controls the LSIs connected with this serial bus is explained.

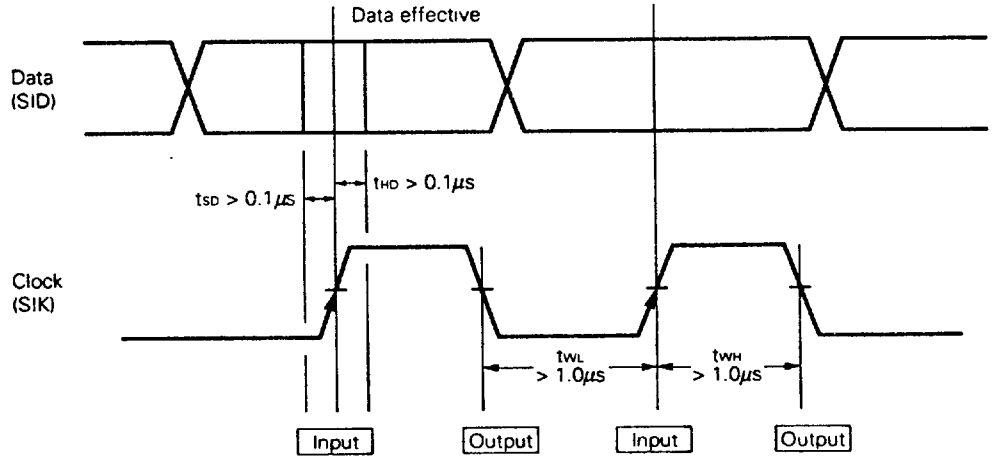
Start

At first, the master CPU falls down SIB (serial busy) line from "H" to "L" to start up this bus. At this time, SID (serial data) line and SIK (serial clock) line are "H". When SIB line is "H", the bus is forcibly reset.



Data capturing (Write mode)

In write mode, SID is taken in at rising edge of SIK. Therefore, it is the best way to execute data switching of master CPU at falling edge of SIK.



Data transfer

1 byte of data consists of a total of 10 bits: 8 bits for data, 1 bit for parity, and 1 bit for Acknowledge (ACK).

When the master CPU send 1 byte data, an address byte, a sub-address byte, and a data byte are required. However, because the μPD6481 (TIGIII) has automatic increment function of the sub-address byte counter, data bytes can be transmitted in succession.

Main address byte..... Specifies the main address of each LSI to be selected by the master CPU.
Sub-address byte..... Selects the subaddress byte and function address of each LSI selected by the master CPU with its main address.
Data byte..... Transmits data in the selected function address.

The master CPU should add a parity bit to the 9th bit position of each byte data to be sent. Even parity is used for the parity check and parity should be selected so that the total number of "1"s in the data of 9 bits including the parity bit becomes even.

The receiving μPD6481 (TIGIII) detects the parity bit. If the number of "1"s in the data is even, it sets the SIBO pin to "L" at the 10th bit. If the number of "1"s is not even, the LSI stops receiving the subsequent data, holds the SIBO pin in the high impedance state, and stops its internal operation until the next start-up of the serial bus.

Following the start-up of the serial bus, the master CPU first transmits the main address of the LSI to which data is to be sent, with a main address byte. The μPD6481 (TIGIII) will be selected if "47H" is specified as the main address.

If this main address is not the own address, the receiving LSI stops receiving data from the master CPU and stops its internal operation until the next start-up of the serial bus. If the main address is its own address, the LSI outputs a low level to the SIBO pin at the 10th clock pulse.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	P	ACK
0	1	0	0	0	1	1	1	0	0

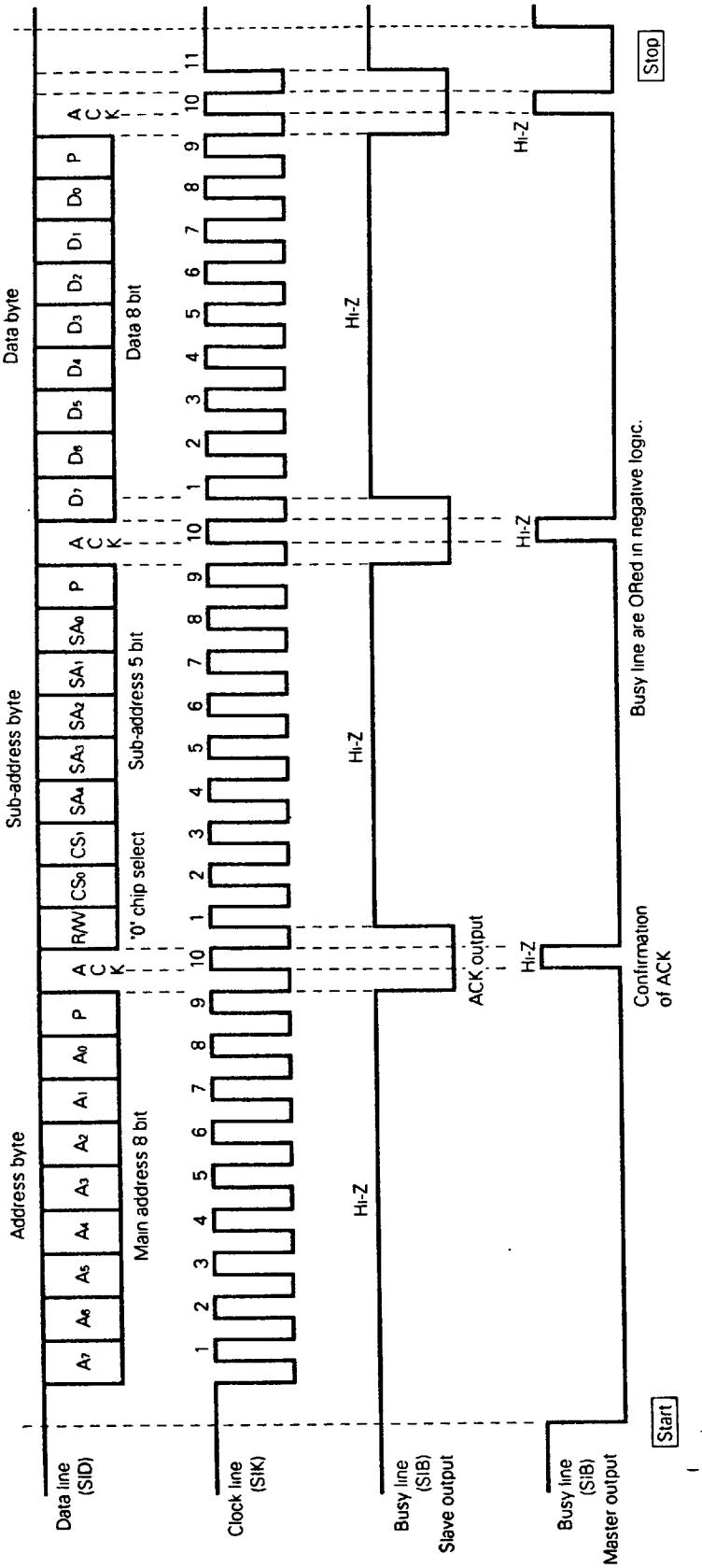
μPD6481... ... "47H" main address
P : Parity bit
ACK : Acknowledge bit

With 1 byte following the main address byte, the sub-address of the LSI selected by the main address byte is specified. The sub-address byte consists of 10 bits; 1 R/W bit, 2 chip select bits, 5 sub-address bits, 1 parity bit, and 1 acknowledge bit.

R/W bit..... Specifies the transfer direction of the data following the sub-address byte.
"L": Write mode (From master CPU to the specified LSI)
"H": Read mode (From specified LSI to master CPU)
Chip select bits..... When two or more LSI chips having the same main address are connected, these 2 bits are used to select a specific chip. With the μPD6481, the chip select bits are not used. Therefore, set these bits as follows: CS0=0, CS1=0
Sub-address bits..... Specify a function address within the LSI.
When loading initial data, data can be written successively by setting the sub-address as "00H" and using the sub-address increment function.

R/W	CS0	CS1	SA_4	SA_3	SA_2	SA_1	SA_0	P	ACK
0	0	0	0	0	0	0	0	0	0

Example of 1 byte data writing (write mode ... Master CPU writes 1 byte of data into slave IC)



List of serial bus function

Sub-address	data							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_0	3DSS (3D split selection) 0:OFF 1:ON	"0"	HREF (H-Reference shift LSB) D_0	SDSE (Sync.signal detection selection) 0:ON 1:OFF	FBCS (Forced burst clock) 0:Standard 1:ON	FHCS (Forced line clock) 0:Standard 1:ON	"0"	"0"
SA_1	HREF (H-Reference shift) "0"–"511" 0.14 μs step							
	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
SA_2	"0"	"0"	"1"	"1"	WSCO (Weak electric field detection coring)			
					D_3	D_2	D_1	D_0
SA_3	"1"	"1"	"0"	HSDR (Horizontal synchronizing signal detection reference)				
				D_4	D_3	D_2	D_1	D_0
SA_4	"0"	"0"	"0"	VTRR (VCR detection reference)				
				D_4	D_3	D_2	D_1	D_0
SA_5	"0"	"0"	"1"	BSDR (Burst synchronizing signal detection reference)				
				D_4	D_3	D_2	D_1	D_0
SA_6	"0"	"0"	WSDR1 (Weak electric field detection reference 1) Detection ON → OFF					
			D_5	D_4	D_3	D_2	D_1	D_0
SA_7	"0"	"0"	WSDR2 (Weak electric field detection reference 2) Detection OFF → ON					
			D_5	D_4	D_3	D_2	D_1	D_0
SA_8	"0"	"0"	"0"	3DSP (3D split phase) 0:Standard 1:Inverted	"0"	"0"	"0"	"0"
SA_9	"0"	"0"	"0"	"0"	"0"	"0"	"0"	STMS (S-video connector mode selection) 0:Composite 1:S-video connector

4.3 Explanation of Serial Bus Address

4.3.1 Three-dimension Y/C separation split

3DSS
(3D Y/C Split Select)

SA_0	7	0	×	×	×	×	0	0

Three-dimension Y/C separation processing on the left of the screen is set ON/OFF.

"1" .... Split mode is set ON.
Right screen : Three-dimension Y/C separation, adaptive interpolating
Left screen : Line correlation comb filter, line interpolation
(Displayed half screen side of three-dimension Y/C separation processing is switched according to SA_8, D_4)

"0" ..... Split mode is set OFF (standard).

4.3.2 Shift volume setting of H-Reference

HREF
(H-Reference)

SA_1	7	6	5	4	3	2	1	0
	MSB							
SA_0	×	0	5	×	×	×	0	0
			LSB					

The shift volume of HREF output is varied arbitrarily.
"000H"-"1FFH" can be shifted in 0.14 μs step.

4.3.3 Synchronizing signal detection selection

SDSE
(Sync Detect Select)

SA_0	×	0	×	4	×	×	0	0

ON/OFF of synchronizing signal detection circuit is selected.

"1" ....OFF
"0" ....ON(Standard)

4.3.4 Forced burst lock

FBCS
(Forced Burst Clock Select)

SA_0	×	0	×	×	3	×	0	0

Burst lock clock is forcibly selected in the inside of LSI.

"1" ....Forced burst lock clock selection
"0" ....ON (Automatic switching)

4.3.5 Forced line lock

FHCS
(Forced Line Clock Select)

SA_0

×	0	×	×	×	2	0	0

Line lock clock is forcibly selected in the inside of LSI.
"1" ····Forced line lock clock selection
"0" ····ON (Automatic switching)
In the case of SA_0, D_3="1", burst lock clock is selected, regardless of this bit.

4.3.6 Weak electric field detection coring

WSCO
(Weak Signal Coring)

SA_2

0	0	1	1	3	2	1	0
				MSB			LSB

Coring value of weak electric field detection input is set.

4.3.7 Horizontal synchronizing signal detection reference

HSDR
(H-Sync Detect Reference)

SA_3

1	1	0	4	3	2	1	0
			MSB				LSB

Reference for horizontal synchronizing signal detection is difference of horizontal synchronizing signal period between fields is compared with this set value.

4.3.8 VCR detection reference

VTRR
(VTR reference)

SA_4

0	0	0	4	3	2	1	0
			MSB				LSB

VCR detection level for non-standard signal is set. Difference of vertical sync. signal frequency and set value is compared.

4.3.9 Burst synchronizing signal detection reference

BSDR
(Burst Sync. Detect Reference)

SA_5

0	0	1	4	3	2	1	0
			MSB				LSB

Reference of burst synchronizing signal detection is set.
Field difference burst signal is compared with this set value.

4.3.10 Weak electric field detection reference set 1

WSDR1
(Weak Signal Detect Reference 1)

SA_6

0	0	5	4	3	2	1	0

MSB LSB

Weak electric field detection level which controls non-standard signal detection is set. This set value is used as reference value when weak electric field detection switches to OFF from ON.

4.3.11 Weak electric field detection reference set 2

WSDR2
(Weak Signal Detect Reference 2)

SA_7

0	0	5	4	3	2	1	0

MSB LSB

Weak electric field detection level which controls non-standard signal detection is set. This set value is used to compare when weak electric field detection changes to OFF from ON.

4.3.12 Three-dimension Y/C separation split phase inversion

3D Y/C Separation SP
(3D Y/C Split Phase Select)

SA_8

0	0	0	4	0	0	0	0

Displayed half screen side of three-dimension Y/C separation is switched.

"0" ····· Left screen is changed to three-dimension separation OFF.

"1" ····· Right screen is changed to three-dimension separation OFF.

4.3.13 S pin mode selection

STMS
(S-Terminal Mode Select)

SA_9

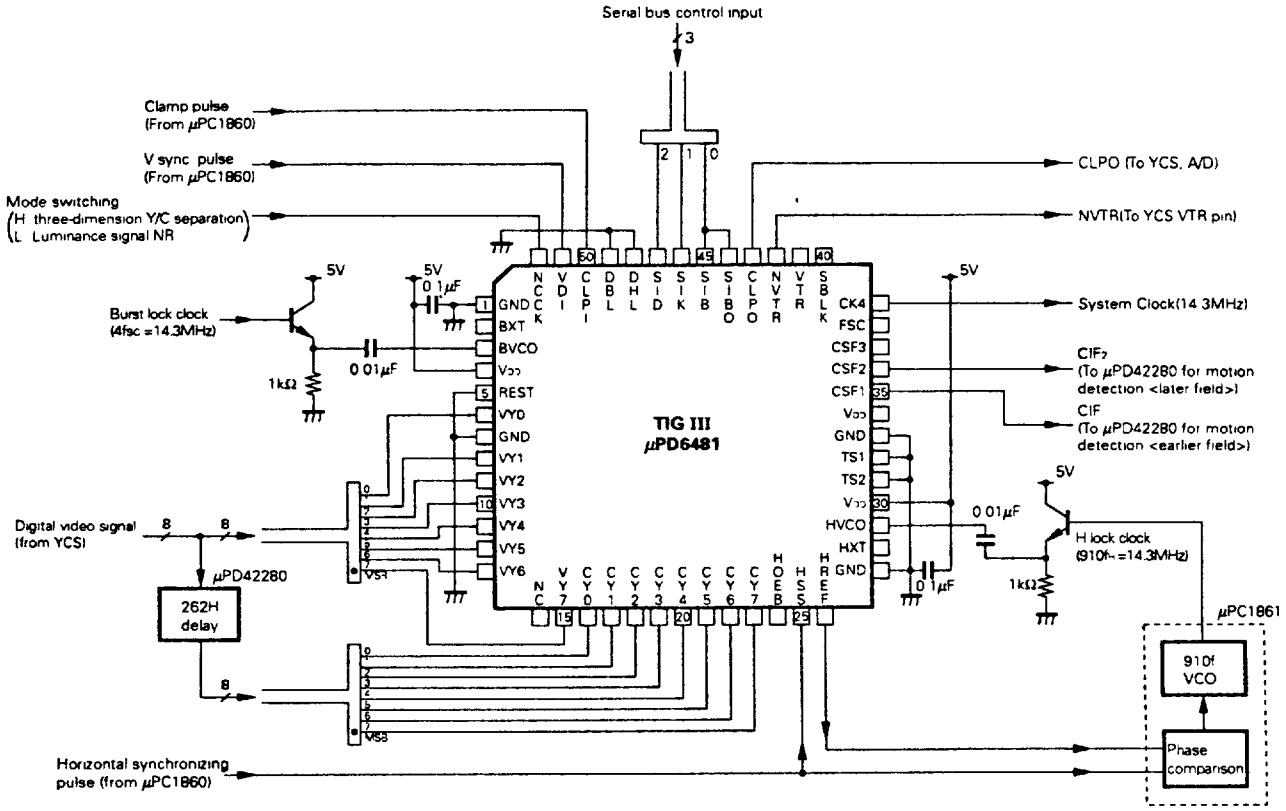
0	0	0	0	0	0	0	0

In the case of input separating Y and C (S-video connector mode), make this bit to "1", and delay length of YCS III (μPD6480) peripheral field buffer is changed.

"0" ····· Composite input

"1" ····· S-video connector input

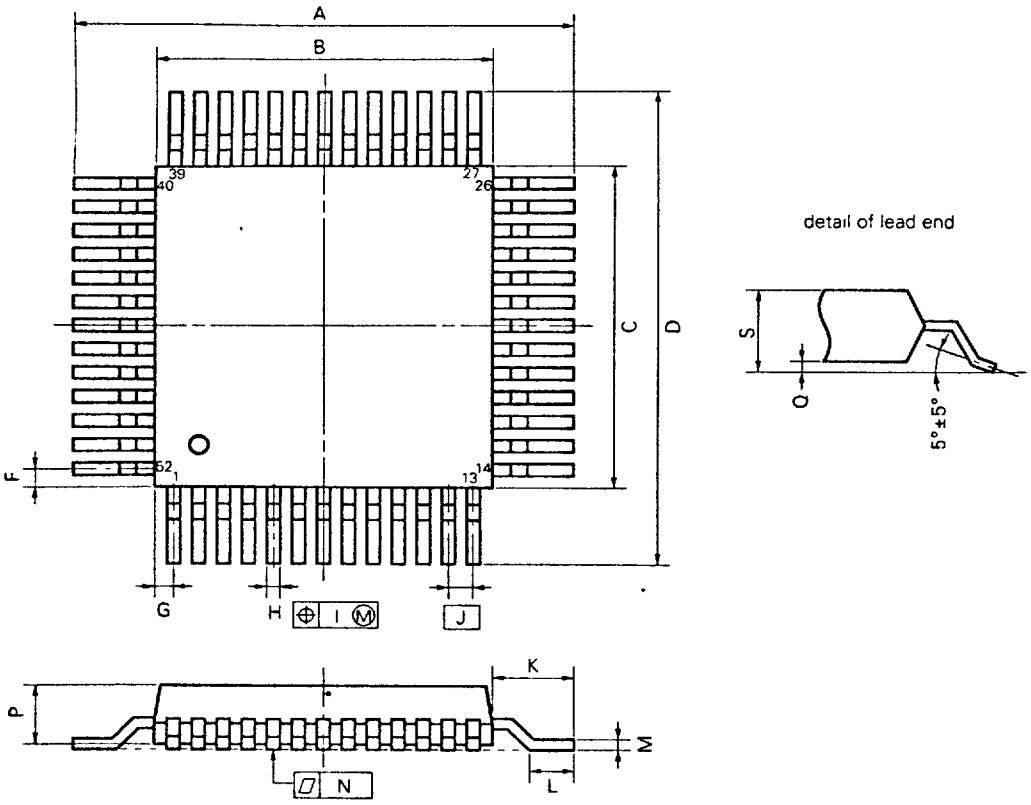
APPLICATION CIRCUIT (Three-dimension Y/C separation application ··· burst lock clock fixed mode)



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS

52 PIN PLASTIC QFP (□14)



P52GC-100-3B6,3BH-1

NOTE
Each lead centerline is located within 0 20 mm (0 008 inch) of its true position (T P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17 6±0.4	0 693±0 016
B	14 0±0 2	$0\ 551^{+0\ 009}_{-0\ 008}$
C	14 0±0 2	$0\ 551^{+0\ 009}_{-0\ 008}$
D	17 6±0 4	0 693±0 016
F	1 0	0.039
G	1.0	0.039
H	0 40±0 10	$0\ 016^{+0\ 004}_{-0\ 005}$
I	0 20	0 008
J	1.0 (T.P.)	0 039 (T.P.)
K	1.8±0.2	$0\ 071^{+0\ 008}_{-0\ 009}$
L	0 8±0 2	$0\ 031^{+0\ 009}_{-0\ 008}$
M	$0\ 15^{+0\ 10}_{-0\ 05}$	$0\ 006^{+0\ 004}_{-0\ 003}$
N	0.12	0.005
P	2 7	0 106
Q	0 1±0 1	0 004±0 004
S	3.0 MAX	0 119 MAX