TLE4998C3
TLE4998C4

Programmable Linear Hall Sensor

Sensors

Never stop thinking.

Edition 2008-12

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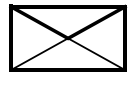
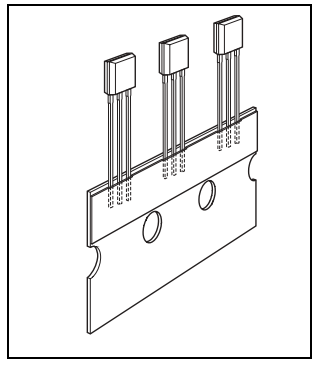
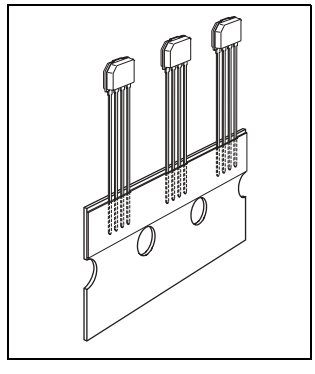


1 Overview

1.1 Features





- SPC (Short PWM Code) protocol with enhanced interface features based on SENT (Single Edge Nibble Transmission,defined by SAE J2716)
- 20-bit Digital Signal Processing (DSP)
- Digital temperature compensation
- 16-bit overall resolution
- Operates within automotive temperature range
- Low drift of output signal over temperature and lifetime
- Programmable parameters stored in EEPROM with single-bit error correction:
  - SPC protocol modes: synchronous transmission, dynamic range selection, ID selection mode
  - SPC unit time
  - Magnetic range and sensitivity (gain), polarity of the output slope
  - Offset
  - Bandwidth
  - Clamping levels
  - Customer temperature compensation coefficients
  - Memory lock
- Re-programmable until memory lock
- Supply voltage 4.5 - 5.5 V (4.1 - 16 V in extended range)
- Operation between -200 mT and +200 mT within three ranges
- Reverse-polarity and overvoltage protection for all pins
- Output short-circuit protection
- On-board diagnostics (overvoltage, EEPROM error, start up)
- Output of internal magnetic field values and temperature
- Programming and operation of multiple sensors with common power supply
- Two-point calibration of magnetic transfer function without iteration steps
- High immunity against mechanical stress, EMC, ESD

Type	Marking	Ordering Code	Package
TLE4998C3	4998C3	SP000476468	PG-SSO-3-10
TLE4998C4	4998C4	SP000440972	PG-SSO-4-1

1.2 Target Applications

- Robust replacement of potentiometers
  - No mechanical abrasion
  - Resistant to humidity, temperature, pollution and vibration
- Linear and angular position sensing in automotive applications such as pedal position, suspension control, throttle position, headlight levelling, and steering torque sensing
- Sensing of high current for battery management, motor control, and electronic fuses

1.3 Pin Configuration

Figure 1 and **Figure 2** show the location of the Hall element in the chip and the distance between Hall probe and the surface of the package.

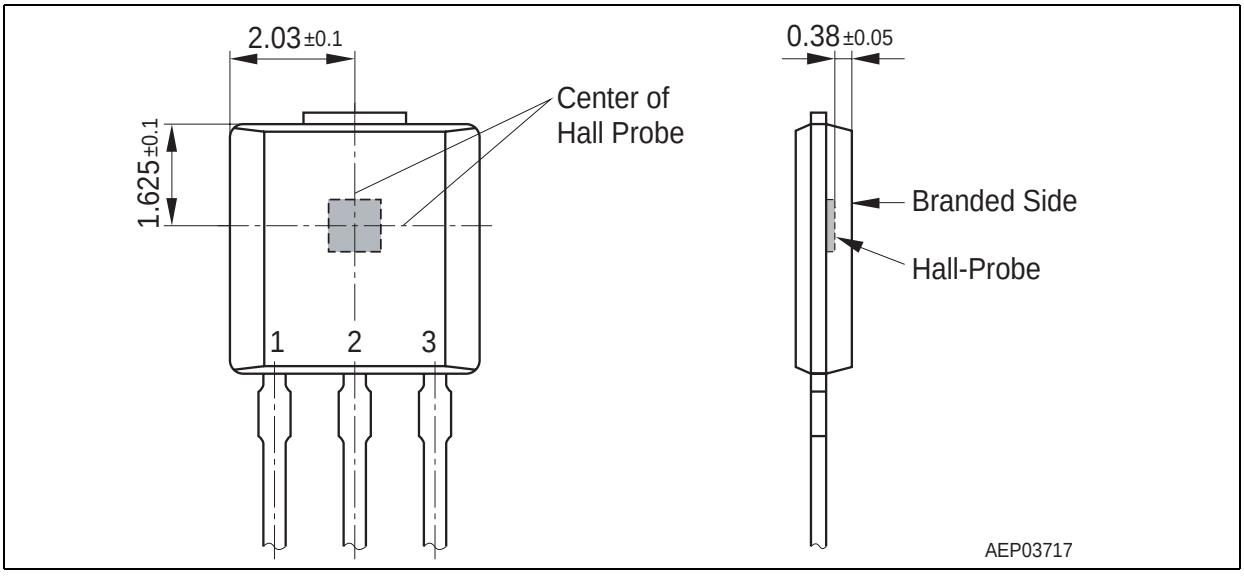


Figure 1 Hall Cell Location and Pin Configuration of PG-SSO-3-10 package

Table 1 TLE4998C3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	*VDD*	Supply voltage / programming interface
2	*GND*	Ground
3	*OUT*	Output / programming interface

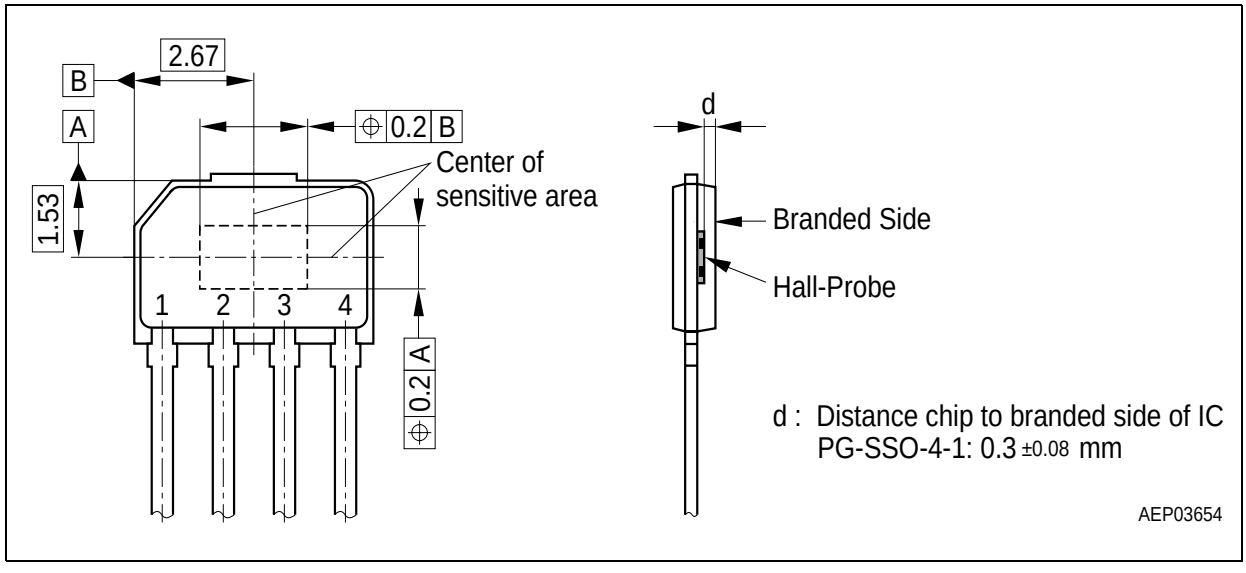


Figure 2 Hall Cell Location and Pin Configuration of PG-SSO-4-1 package

Table 2 TLE4998C4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	*TST*	Test pin (connection to *GND* is recommended)
2	*VDD*	Supply voltage / programming interface
3	*GND*	Ground
4	*OUT*	Output / programming interface

2 General

2.1 Block Diagram

Figure 3 shows a simplified block diagram.

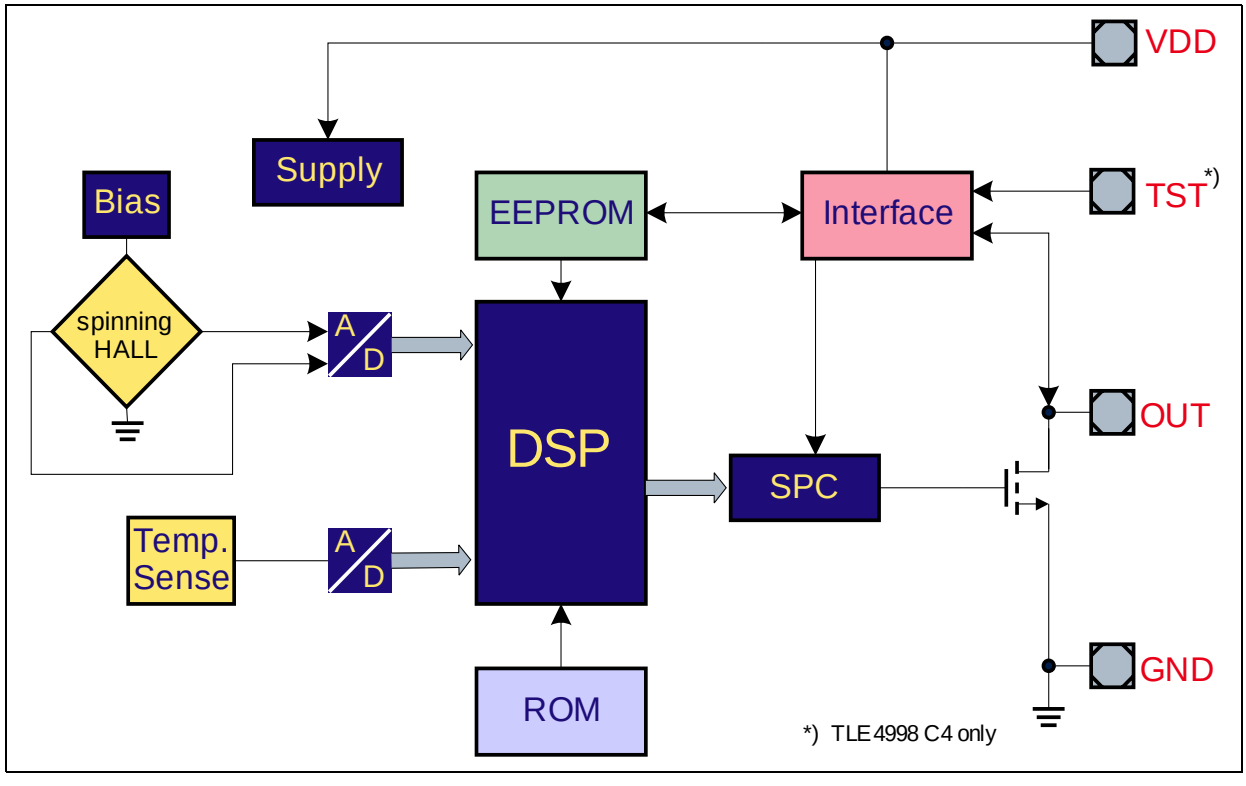


Figure 3 Block diagramm

2.2 Functional Description

The linear Hall IC TLE4998C has been designed specifically to meet the requirements of highly accurate angle and position detection as well as for current measurement applications. The sensor provides a digital SPC (Short PWM Code) signal, based on the standardized SENT (Single Edge Nibble Transmission, SAE J2716) protocol. The SPC protocol allows transmissions initiated by the ECU. Two further operation modes are available:

- “range selection” for dynamical switching of the measurement range during operation
- “ID selection” to build a bus system with up to 4 ICs on a single output line and a common supply, which can be individually accessed by the ECU.

Each transmission sequence contains an adjustable number of nibbles representing the magnetic field, the temperature value and a status information of the sensor. The interface is further described in **Chapter 13**. The output stage is an open-drain driver

pulling the output pin to low only. Therefore, the high level needs to be obtained by an external pull-up resistor. This output type has the advantage that the receiver may use an even lower supply voltage (e.g. 3.3 V). In this case the pull-up resistor must be connected to the given receiver supply.

The IC is produced in BiCMOS technology with high voltage capability, and it also has reverse-polarity protection.

Digital signal processing using a 16-bit DSP architecture together with digital temperature compensation guarantee excellent long-time stability compared to analog compensation methods.

While the overall resolution is 16 bits, some internal stages work with resolutions up to 20 bits.

2.3 Principle of Operation

- A magnetic flux is measured by a Hall-effect cell
- The output signal from the Hall-effect cell is converted from analog to digital
- The chopped Hall-effect cell and continuous-time A/D conversion ensure a very low and stable magnetic offset
- A programmable low-pass filter to reduce noise
- The temperature is measured and A/D converted, too
- Temperature compensation is done digitally using a second-order function
- Digital processing of output value is based on zero field and sensitivity value
- The output value range can be clamped by digital limiters
- The final output value is represented by the data nibbles of the SPC protocol

2.4 Transfer Functions

The examples in **Figure 4** show how different magnetic field ranges can be mapped to the desired output value ranges.

- Polarity Mode:
  - **Bipolar**: Magnetic fields can be measured in both orientations. The limit points do not necessarily have to be symmetrical around the zero field point
  - **Unipolar**: Only north- or south-oriented magnetic fields are measured
- Inversion: The gain can be set to both positive and negative values

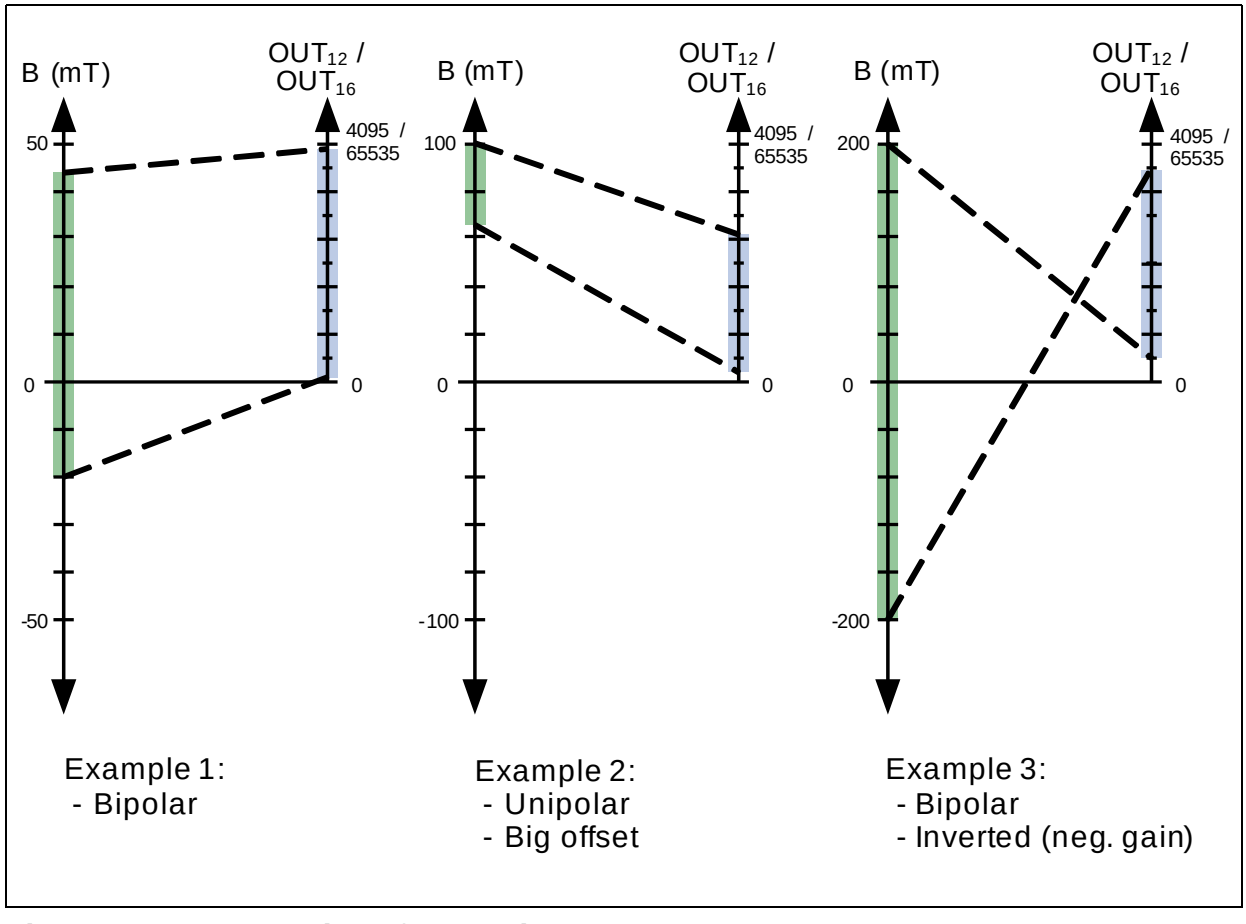


Figure 4 Examples of Operation

3 Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	- 40	150	°C	
Junction temperature	T_J	- 40	170[1)]	°C	
Voltage on V_{DD} pin with respect to ground	V_{DD}	-18	18	V	[2)]
Supply current @ overvoltage V_{DD} max.	I_{DDov}	-	15	mA	
Reverse supply current @ V_{DD} min.	I_{DDrev}	-1	0	mA	
Voltage on output pin with respect to ground	V_{OUT}	-1[3)]	18[4)]	V	
Magnetic field	B_{MAX}	-	unlimited	T	
ESD protection	V_{ESD}	-	4.0	kV	According HBM JESD22-A114-B [5)]

1) For limited time of 96 h. Depends on customer temperature lifetime cycles. Please ask for support by Infineon

2) Higher voltage stress than absolute maximum rating, e.g. 150% in latch-up tests is not applicable. In such cases, $R_{series} \geq 100\ \Omega$ for current limitation is required

3) I_{DD} can exceed 10 mA when the voltage on OUT is pulled below -1 V (-5 V at room temperature)

4) V_{DD} = 5 V, open drain permanent low, for max. 10 minutes

5) 100 pF and 1.5 kΩ

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4998C. All parameters specified in the following sections refer to these operating conditions, unless otherwise indicated.

Table 4 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.5	5.5	V	
		4.1[1)]	16[2)]	V	Extended range
Output pull-up voltage[3)]	$V_{pull-up}$	-	18	V	
Load resistance[3)]	R_L	1	-	kΩ	
Output current[3)]	I_{OUT}	0	5	mA	
Load capacitance[3)]	C_L	1	8	nF	
Junction temperature	T_J	- 40	125 150[4)]	°C	For 5000 h For 1000 h not additive

1) For reduced output accuracy

2) For supply voltages > 12 V, a series resistance $R_{series} \geq 100\ \Omega$ is recommended

3) Required output protocol characteristics depend on these parameters, R_L must be according to max. output current

4) For reduced magnetic accuracy; extended limits are taken for characteristics

Note: Keeping signal levels within the limits specified in this table ensures operation without overload conditions.

5 Electrical, Thermal, and Magnetic Parameters

Table 5 Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
SPC transmission time	t_{SPC}	-	-	1	ms	Unit time 3µs[1]
Supply current	I_{DD}	3	6	8	mA	
Output current @ OUT shorted to supply lines	I_{OUTsh}	-	95	-	mA	V_{OUT} = 5 V, max. 10 minutes
Thermal resistance TLE4998C3	R_{thJA}	-	219	-	K/W	Junction to air
	R_{thJC}	-	47	-	K/W	Junction to case
Thermal resistance TLE4998C4	R_{thJA}	-	240	-	K/W	Junction to air
	R_{thJC}	-	41	-	K/W	Junction to case
Power-on time[2]	t_{Pon}	-	0.7 15	2 20	ms	≤ ± 5% target out value ≤ ± 1% target out value
Power-on reset level	V_{DDpon}	-	3.6	4	V	
Output impedance	Z_{OUT}	20	40	70	kΩ	[3]
Output fall time	t_{fall}	2	-	4	µs	V_{OUT} 4.5 V to 0.5 V [4]
Output rise time	t_{rise}	-	20	-	µs	V_{OUT} 0.5 V to 4.5 V [4][5]
Output low saturation voltage	V_{OUTsat}	-	0.3 0.2	0.6 0.4	V	$I_{OUTsink}$ = 5 mA $I_{OUTsink}$ = 2.2 mA
Output noise (rms)	OUT_{noise}	-	1	2.5	LSB_{12}	[6]

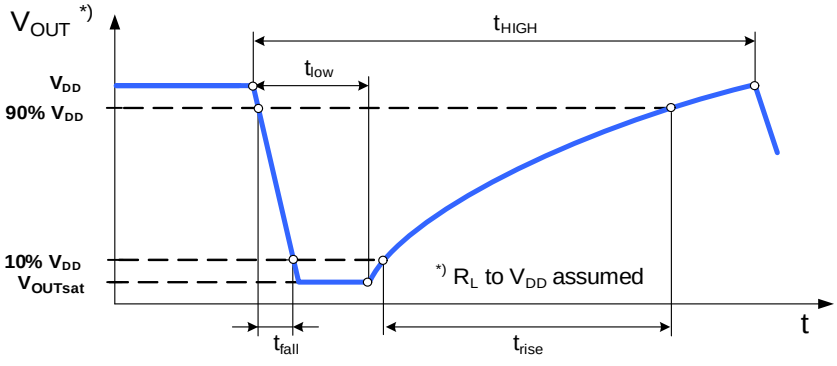
[1] Transmission time depends on the data values being sent and on int. RC oscillator frequ. variation of +/- 20%.

[2] Response time to set up output data at power on when a constant field is applied. The first value given has a ± 5% error, the second value has a ± 1% error. Measured with 640-Hz low-pass filter

[3] V_{DD} = 5V, V_{OUT}=2.6V, open drain high state

[4] For V_{DD} = 5 V, R_L = 2.2 kΩ, C_L = 4.7 nF, at room temperature, not considering condensator tolerance or influence of external circuitry

5) Depends on external R_L and C_L



6) Range 100 mT, Gain 2.23, internal LP filter 244 Hz, B = 0 mT, T = 25 °C

Calculation of the Junction Temperature

The internal power dissipation P_{TOT} of the sensor increases the chip junction temperature above the ambient temperature.

The power multiplied by the total thermal resistance R_{thJA} (Junction to Ambient) added to T_A leads to the final junction temperature. R_{thJA} is the sum of the addition of the two components, *Junction to Case* and *Case to Ambient*.

$$R_{thJA} = R_{thJC} + R_{thCA}$$
$$T_J = T_A + \Delta T$$
$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}) \quad I_{DD}, I_{OUT} > 0, \text{if direction is into IC}$$

Example (assuming no load on Vout and TLE4998C4 type):

- V_{DD} = 5 V
- I_{DD} = 8 mA
- ΔT = 240 [K/W] x (5 [V] x 0.008 [A] + 0 [VA]) = 9.6 K

For moulded sensors, the calculation with R_{thJC} is more adequate.

Magnetic Parameters

Table 6 Magnetic Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Sensitivity	S 1)	± 8.2	-	± 245	LSB_{12}/ mT	Programmable 2)
Temperature coefficient of sensitivity	TC	-150	0	150	ppm/ °C	3) See **Figure 5**
Magnetic field range	MFR	± 50	± 100 4)	± 200	mT	Programmable 5)
Integral nonlinearity	INL	- 0.1	-	0.1	%MFR	6)8)
Magnetic offset	B_{OS}	- 400	0	400	µT	7)8)
Magnetic offset drift	ΔB_{OS}	- 5	-	5	µT / °C	Error band 8)
Magnetic hysteresis	B_{HYS}	0	-	10	µT	9)

1) Defined as ΔOUT / ΔB

2) Programmable in steps of 0.024%

3) For any 1st and 2nd order polynomial, coefficient within definition in Chapter 8.

4) This range is also used for temperature and offset pre-calibration of the IC

5) Depending on offset and gain settings, the output may already be saturated at lower fields

6) Gain setup is 1.0

7) In operating temperature range and over lifetime

8) Measured at ± 100 mT range

9) Measured in 100 mT range, Gain = 1, room temperature

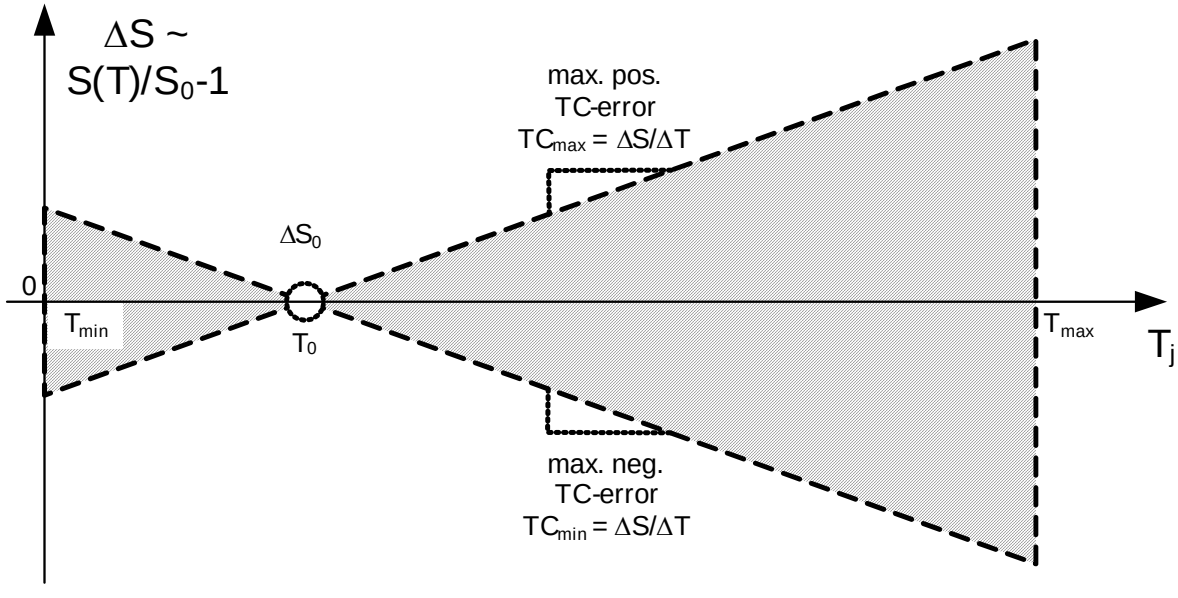


Figure 5 Drift of Temperature Coefficient

6 Signal Processing

The signal flow diagram in **Figure 6** shows the signal path and data-processing algorithm.

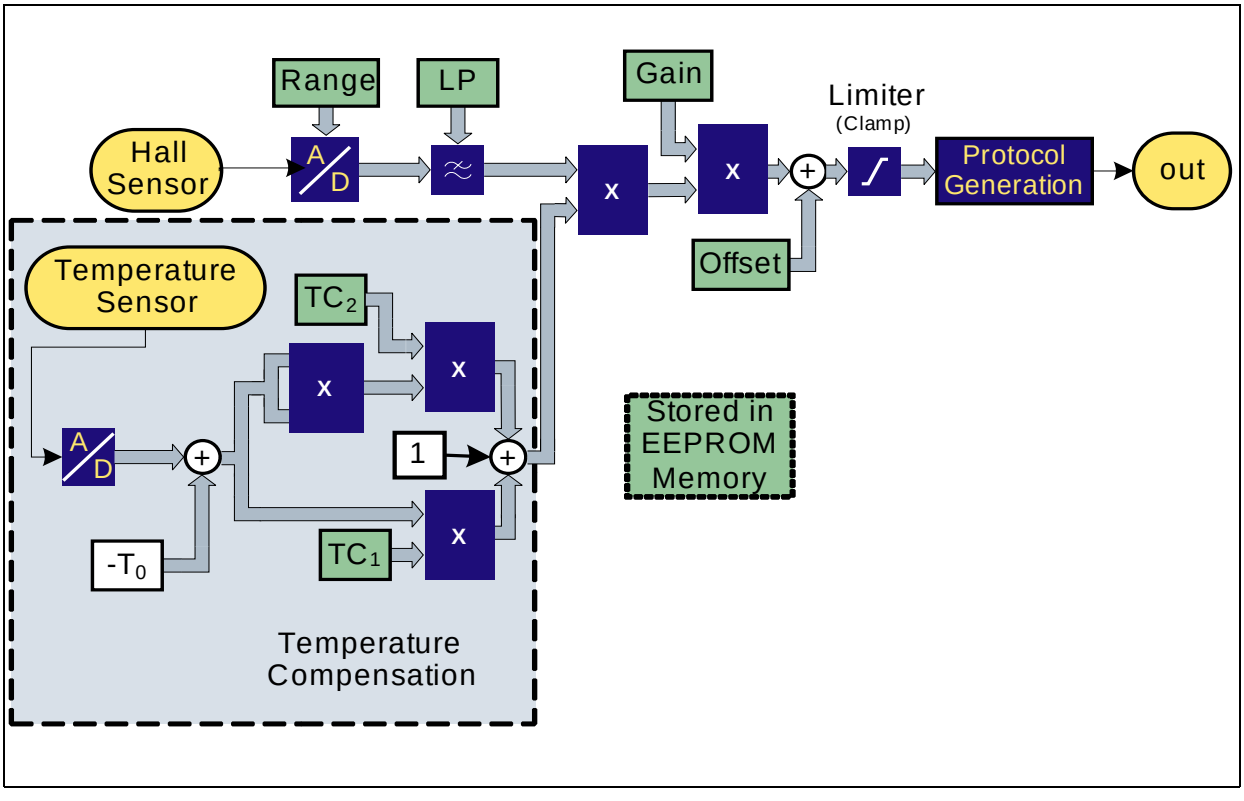


Figure 6 Signal Processing Flow

Magnetic Field Path

- The analog output signal of the chopped Hall-effect cell is converted to a digital signal in the continuous-time A/D converter. The range of the chopped A/D converter can be set in several steps either by EEPROM settings or dynamically by the master in the dynamic range mode (see **Table 7**). This gives a suitable level for the A/D converter
- After the A/D conversion, a digital low-pass filter reduces the bandwidth (**Table 11**)
- A multiplier amplifies the value depending on the gain (see **Table 9**) and temperature compensation settings
- The offset value is added (see **Table 10**)
- A limiter reduces the resulting signal to 16 bits (see **Chapter 13**) and feeds the Protocol Generation stage

Temperature Compensation

(Details are listed in **Chapter 8**)

- The output signal of the temperature cell is also A/D converted

- The temperature is normalized by subtraction of the reference temperature T_0 value (zero point of the quadratic function)
- The linear path is multiplied with the TC_1 value
- In the quadratic path, the temperature difference to T_0 is squared and multiplied with the TC_2 value
- Both path outputs are added together and multiplied with the Gain value from the EEPROM

6.1 Magnetic Field Ranges

The working range of the magnetic field defines the input range of the A/D converter. It is always symmetrical around the zero field point. Any two points in the magnetic field range can be selected to be the end points of the output value. The output value is represented within the range between the two points.

In the case of fields higher than the range values, the output signal may be distorted. In case of synchronous mode and ID selection mode the range must be set accordingly (R=0/1/3) before the calibration of offset and gain.

Table 7 Range Setting

Range	Range in mT[1)]	Parameter R
Low	± 50	3
Mid	± 100	1[2)]
High	± 200	0

1) Ranges do not have a guaranteed absolute accuracy. The temperature pre-calibration is performed in the mid range (100 mT)

2) Setting R = 2 is not used, internally changed to R = 1

Table 8 Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	R	2		bit	

6.2 Gain Setting

The overall sensitivity is defined by the range and the gain setting. The output of the ADC is multiplied with the Gain value.

Table 9 Gain

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	G	15		bit	Unsigned integer value
Gain range	$Gain$	- 4.0	3.9998	-	1)2)
Gain quantization steps	$\Delta Gain$	244.14		ppm	Corresponds to 1/4096

1) For Gain values between - 0.5 and + 0.5, the numerical accuracy decreases
To obtain a flatter output curve, it is advisable to select a higher range setting

2) A gain value of +1.0 corresponds to typical 32 LSB_{12}/mT sensitivity (100 mT range, not guaranteed). It is crucial to do a final calibration of each IC within the application using the Gain/OUT_{OS} value

The Gain value can be calculated by

$$Gain = \frac{(G - 16384)}{4096}$$

6.3 Offset Setting

The offset value corresponds to an output value with zero field at the sensor.

Table 10 Offset

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	OS	15		bit	Unsigned integer value
Offset range	OUT_{OS}	-16384	16383	LSB_{12}	1)
Offset quantization steps	ΔOUT_{OS}	1		LSB_{12}	

1) Infineon pre-calibrates the samples at zero field to 50% output value (100 mT range), but does not guarantee the value. Therefore it is crucial to do a final calibration of each IC within the application

The offset value can be calculated by:

$$OUT_{OS} = OS - 16384$$

6.4 DSP Input Low-Pass Filter

A digital low-pass filter is placed between the Hall A/D converter and the DSP, and can be used to reduce the noise level. The low-pass filter has a constant DC amplification of 0 dB (Gain of 1), which means that its setting has no influence on the internal Hall ADC value.

The bandwidth can be set to any of 8 values.

Table 11 Low Pass Filter Setting

Note: Parameter LP	**Cutoff frequency in Hz (-3dB point)[1)]**
0	80
1	240
2	440
3	640
4	860
5	1100
6	1390
7	off

1) As this is a digital filter running with an RC-based oscillator, the cutoff frequency may vary within ±20%

Table 12 Low-Pass Filter

Parameter	**Symbol**	**Limit Values**		**Unit**	**Notes**
		min.	**max.**		
Register size	LP		3	bit	
Corner frequency variation	Δf	- 20	+ 20	%	

Note: In range 7 (filter off), the output noise increases.

Figure 7 shows the filter characteristics as a magnitude plot (the highest setting is marked). The “off” position would be a flat 0 dB line. The update rate after the low-pass filter is 16 kHz.

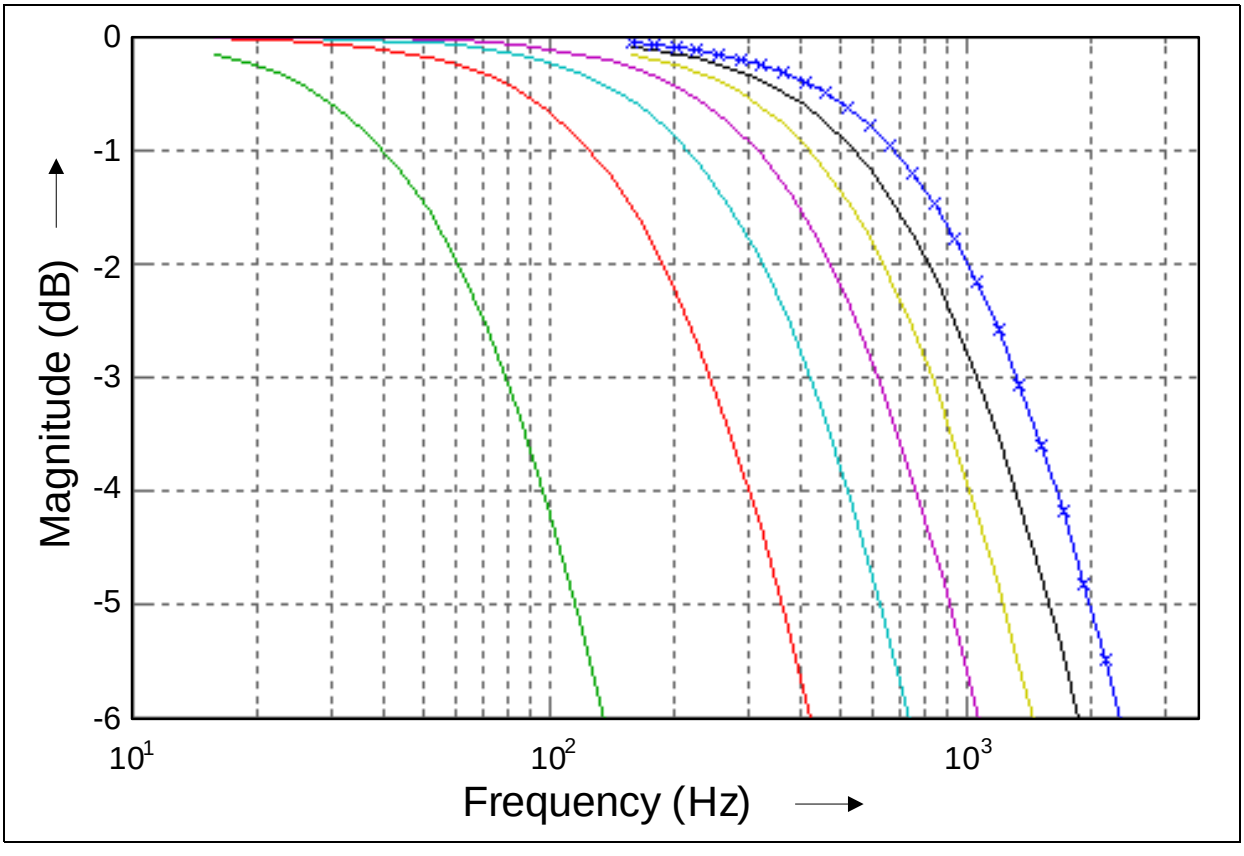


Figure 7 DSP Input Filter (Magnitude Plot)

6.5 Clamping

The clamping function is useful for separating the output range into an operating range and error ranges. If the magnetic field is exceeding the selected measurement range, the output value OUT is limited to the clamping values.

Table 13 Clamping

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	CL,CH	2 x 6		bit	(0...63)
Clamping value low	OUT_{CL}	0	65535	LSB_{16}	1)
Clamping value high	OUT_{CH}	0	65535	LSB_{16}	1) 2)
Clamping quantization steps	ΔOUT_{Cx}	1024		LSB_{16}	3)

1) For CL = 0 and CH = 63 the clamping function is disabled

2) $OUT_{CL} < OUT_{CH}$ mandatory

3) Quantization starts for CL at 0 LSB_{16} and for CH at 65535 LSB_{16}

The clamping values are calculated by:

Clamping value low (deactivated if CL=0):

$$OUT_{CL} = CL \cdot 64 \cdot 16$$

Clamping value high (deactivated if CH=63):

$$OUT_{CH} = (CH + 1) \cdot 64 \cdot 16 - 1$$

Figure 8 shows an example in which the magnetic field range between B_{min} and B_{max} is mapped to output values between 10240 LSB_{16} and 55295 LSB_{16}.

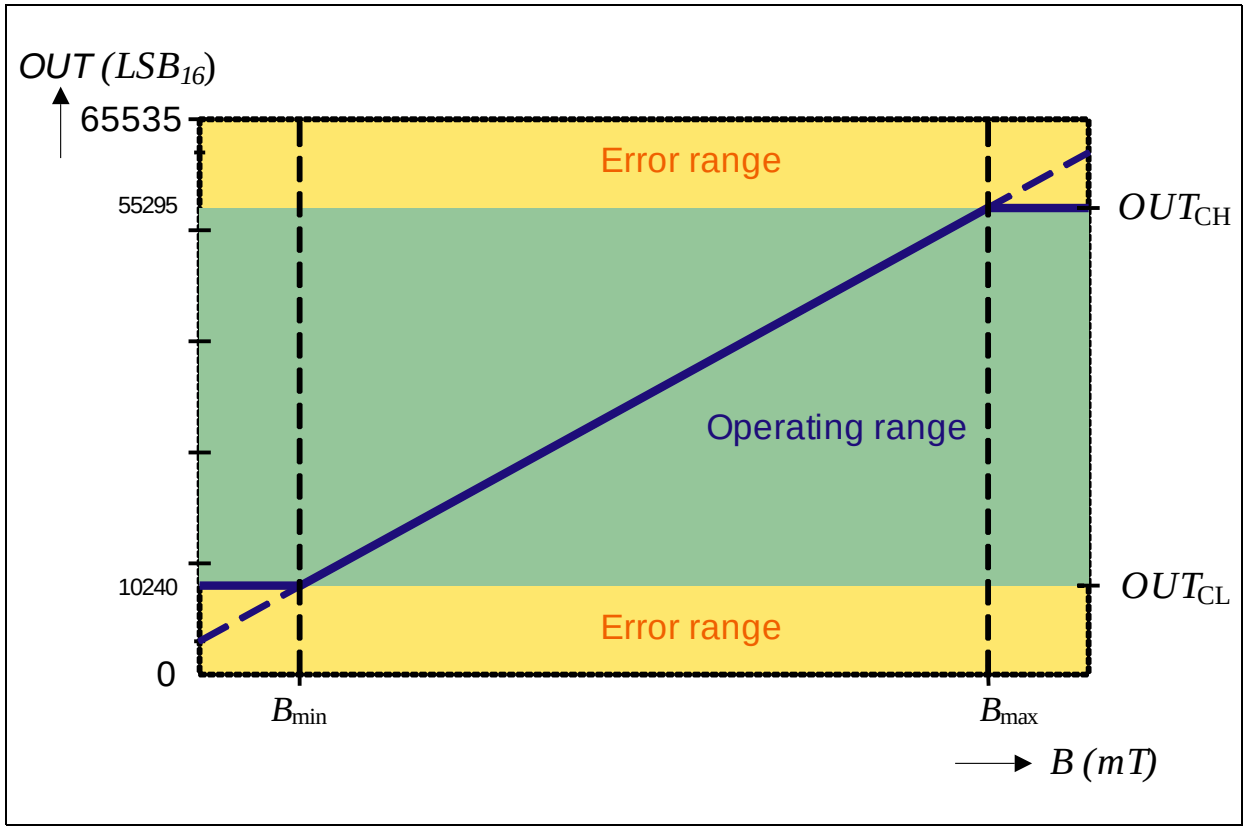


Figure 8 Clamping Example

Note: The clamping high value must be above the low value. If OUT_{CL} is set to a higher value than OUT_{CH}, the OUT_{CH} value is dominating. This would lead to a constant output value independent of the magnetic field strength.

7 Error Detection

Different error cases can be detected by the On-Board Diagnostics (OBD) and reported to the microcontroller in the status nibble (see **Chapter 13**).

7.1 Voltages Outside the Operating Range

The output signals an error condition if V_{DD} crosses the overvoltage threshold level.

Table 14 Overvoltage

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Overvoltage threshold	V_{DDov}	16.65	17.5	18.35	V	1)

1) Overvoltage bit activated in status nibble, output stays in “off” state (high ohmic)

7.2 EEPROM Error Correction

The parity method is able to correct a single bit in the EEPROM line. One other single bit error in another EEPROM line can also be detected, but not corrected. In an uncorrectable EEPROM failure, the open drain stage is disabled and kept in the off state permanently (high ohmic/sensor defect).

8 Temperature Compensation

The magnetic field strength of a magnet depends on the temperature. This material constant is specific for the different magnet types. Therefore, the TLE4998C offers a second-order temperature compensation polynomial, by which the Hall signal output is multiplied in the DSP. There are three parameters for the compensation:

- Reference temperature T_0
- A linear part (1st order) TC_1
- A quadratic part (2nd order) TC_2

The following formula describes the sensitivity dependent on the temperature in relation to the sensitivity at the reference temperature T_0:

$$S_{TC}(T) = 1 + TC_1 \times (T - T_0) + TC_2 \times (T - T_0)^2$$

For more information, please refer to the signal processing flow in **Figure 6**.

The full temperature compensation of the complete system is done in two steps:

1. **Pre-calibration in the Infineon final test**
   The parameters TC1, TC2, T0 are set to maximally flat temperature characteristics with respect to the Hall probe and internal analog processing parts.
2. **Overall system calibration**
   The typical coefficients TC1, TC2, T0 of the magnetic circuitry are programmed. This can be done deterministically, as the algorithm of the DSP is fully reproducible. The final setting of the TC1, TC2, T0 values depend on the pre-calibrated values.

Table 15 Temperature Compensation

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size TC_1	TL	-	9	bit	Unsigned integer values
1st order coefficient TC_1	TC_1	-1000	2500	ppm/ °C	1)
Quantization steps of TC_1	qTC_1	15.26		ppm/ °C	
Register size TC_2	TQ	-	8	bit	Unsigned integer values
2nd order coefficient TC_2	TC_2	- 4	4	ppm/ °C²	2)
Quantization steps of TC_2	qTC_2	0.119		ppm/ °C²	
Reference temp.	T_0	- 48	64	°C	
Quantization steps of T_0	qT_0	1		°C	3)

1) Full adjustable range: -2441 to +5355 ppm/°C, can be only used after confirmation by Infineon

2) Full adjustable range: -15 to +15 ppm/°C², can be only used after confirmation by Infineon

3) Handled by algorithm only (see Application Note)

8.1 Parameter Calculation

The parameters TC_1 and TC_2 may be calculated by:

$$TC_1 = \frac{TL - 160}{65536} \times 1000000$$

$$TC_2 = \frac{TQ - 128}{8388608} \times 1000000$$

Now the digital output for a given field B_{IN} at a specific temperature can be calculated by:

$$OUT = 2 \cdot \left(\frac{B_{IN}}{B_{FSR}} \times S_{TC} \times S_{TCHall} \times S_0 \times 4096 \right) + OUT_{OS}$$

B_{FSR} is the full-range magnetic field. It is dependent on the range setting (e.g 100 mT).

S_0 is the nominal sensitivity of the Hall probe times the Gain factor set in the EEPROM.

S_{TC} is the temperature-dependent sensitivity factor calculated by the DSP.

S_{TCHall} is the temperature behavior of the Hall probe.

The pre-calibration at Infineon is performed such that the following condition is met:

$$S_{TC}(T_J - T_0) \times S_{TCHall}(T_J) \approx 1$$

Within the application, an additional factor $B_{IN}(T) / B_{IN}(T_0)$ is given due to the magnetic system. S_{TC} then needs to be modified to S_{TCnew} so that the following condition is satisfied:

$$\frac{B_{IN}(T)}{B_{IN}(T_0)} \times S_{TCnew}(T) \times S_{TCHall}(T) \approx S_{TC}(T) \times S_{TCHall}(T) \approx 1$$

Therefore, the new sensitivity parameters S_{TCnew} can be calculated from the pre-calibrated setup S_{TC} using the relationship:

$$\frac{B_{IN}(T)}{B_{IN}(T_0)} \times S_{TCnew}(T) \approx S_{TC}(T)$$

9 Calibration

For the calibration of the sensor, a special hardware interface to a PC is required. All calibration and setting bits can be temporarily written into a Random Access Memory (RAM). This allows the EEPROM to remain untouched during the entire calibration process, since the number of the EEPROM programming cycles is limited. Therefore, this temporary setup (using the RAM only) does not stress the EEPROM.

The digital signal processing is completely deterministic. This allows a two-point calibration to be performed in one step without iterations. After measuring the Hall output signal for the two end points, the signal processing parameters Gain and Offset can be calculated.

Table 16 Calibration Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature at calibration	T_{CAL}	10	30	°C	
2 point Calibration accuracy[1)]	ΔOUT_{CAL1}	-8	8	LSB_{12}	Position 1
	ΔOUT_{CAL2}	-8	8	LSB_{12}	Position 2

1) Corresponds to ± 0.2% accuracy in each position

9.1 Calibration Data Memory

When the MEMLOCK bits are programmed (two redundant bits), the memory content is frozen and may no longer be changed. Furthermore, the programming interface is locked out and the chip remains in application mode only, preventing accidental programming due to environmental influences.

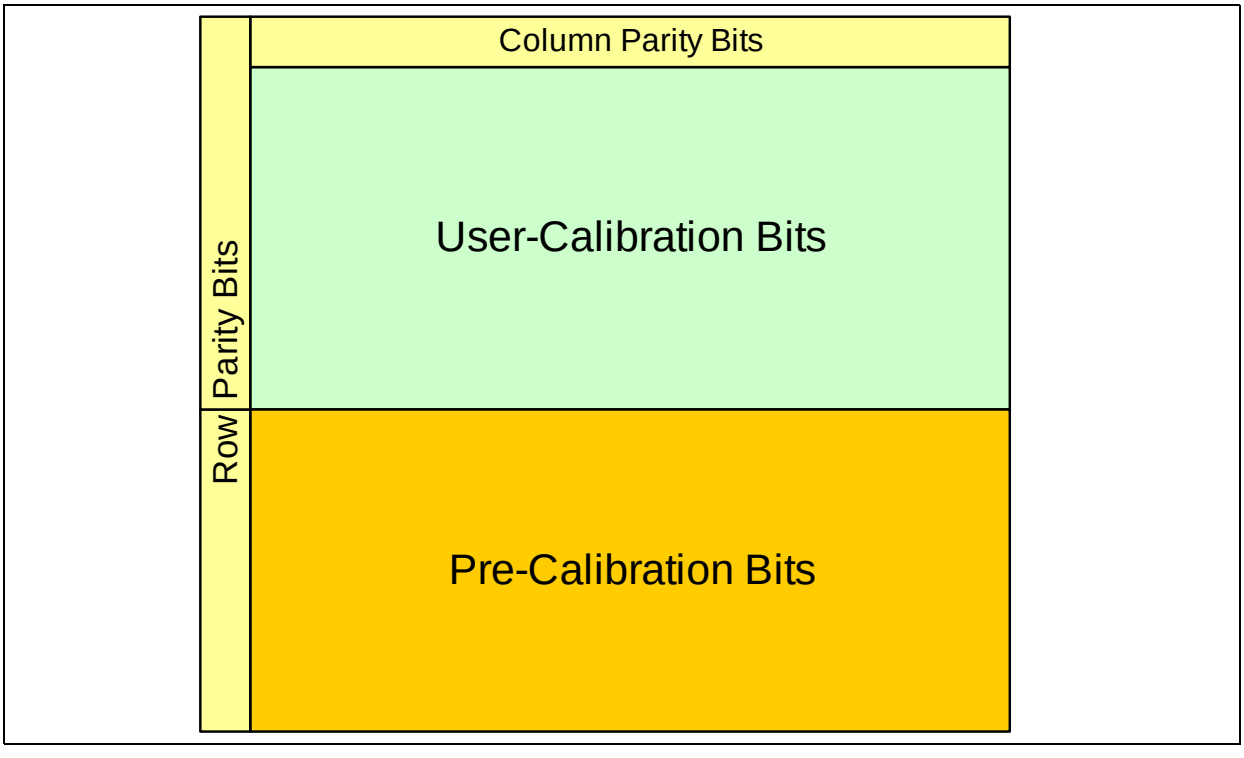


Figure 9 EEPROM Map

A matrix parity architecture allows automatic correction of any single-bit error. Each row is protected by a row parity bit. The sum of bits set (including this bit) must be an odd number (ODD PARITY). Each column is additionally protected by a column parity bit. Each bit in the even positions (0, 2, etc.) of all lines must sum up to an even number (EVEN PARITY), and each bit in the odd positions (1, 3, etc.) must have an odd sum (ODD PARITY). The parity column must have an even sum (EVEN PARITY).

This system of different parity calculations also protects against many block errors (such as erasing a full line or even the whole EEPROM).

When modifying the application bits (such as Gain, Offset, TC, etc.), the parity bits must be updated. As for the column bits, the pre-calibration area must be read out and considered for correct parity generation as well.

Note: A specific programming algorithm must be followed to ensure data retention. A detailed separate programming specification is available on request.

Table 17 Programming Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Number of EEPROM programming cycles	N_{PRG}	-	10	Cycles[1)]	Programming allowed only at start of lifetime
Ambient temperature at programming	T_{PRG}	10	30	°C	
Programming time	t_{PRG}	100	-	ms	For complete memory [2)]
Calibration memory	-	150		Bit	All active EEPROM bits
Error Correction	-	26		Bit	All parity EEPROM bits

1) 1 cycle is the simultaneous change of ≥ 1 bit

2) Depending on clock frequency at V_{DD}, write pulse 10 ms ±1%, erase pulse 80 ms ±1%

9.2 Programming Interface

The VDD pin and the OUT pin are used as a two-wire interface to transmit the EEPROM data to and from the sensor.

This allows:

- Communication with high data reliability
- The bus-type connection of several sensors and separate programming via the OUT pin

9.3 Data Transfer Protocol

The data transfer protocol is described in a separate document (User Programming Description), available on request.

9.4 Programming of Sensors with Common Supply Lines

In many automotive applications, two sensors are used to measure the same parameter.

This redundancy makes it possible to continue operation in an emergency mode. If both sensors use the same power supply lines, they can be programmed together in parallel.

10 Application Circuit

Figure 10 shows the connection of multiple sensors to a microcontroller.

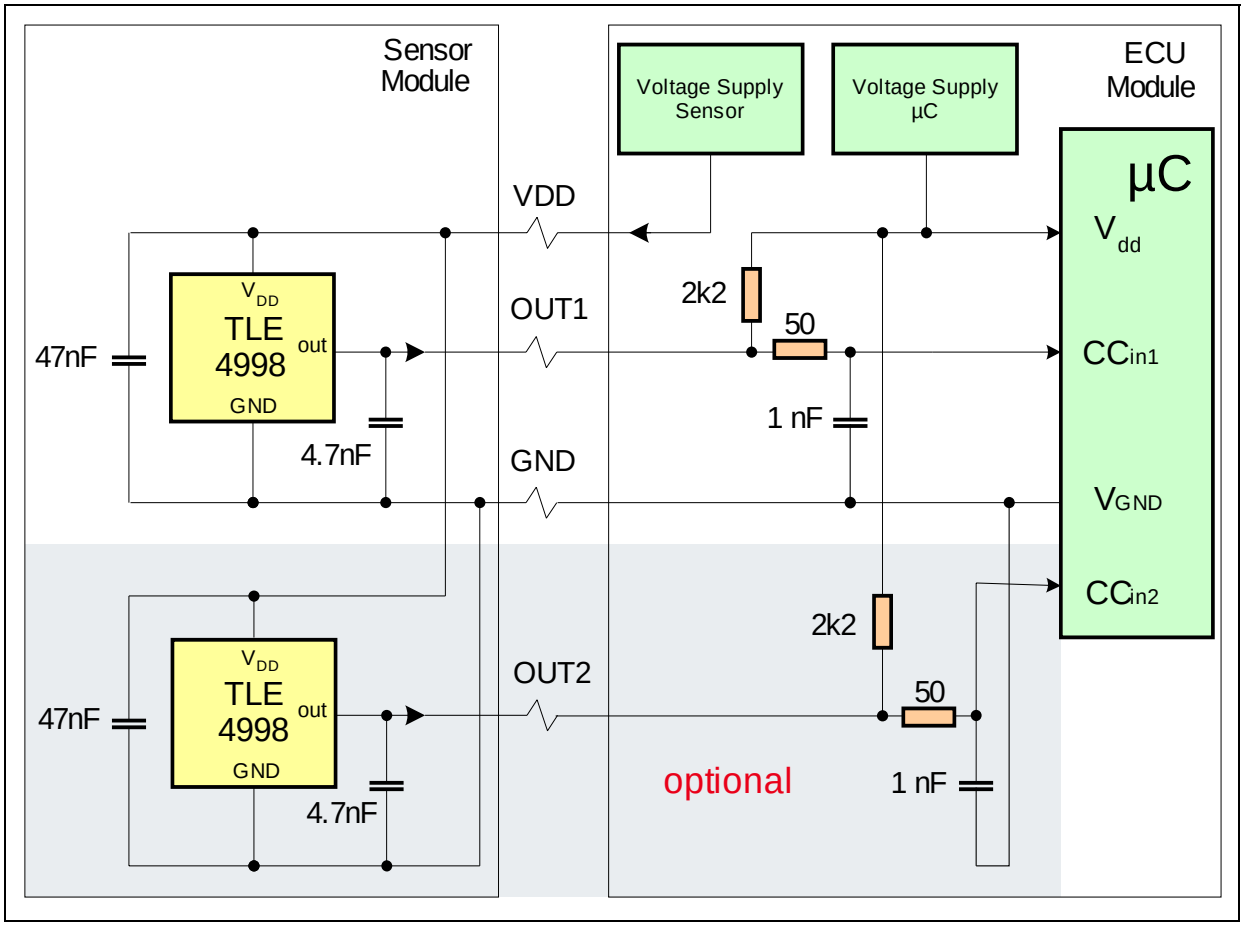
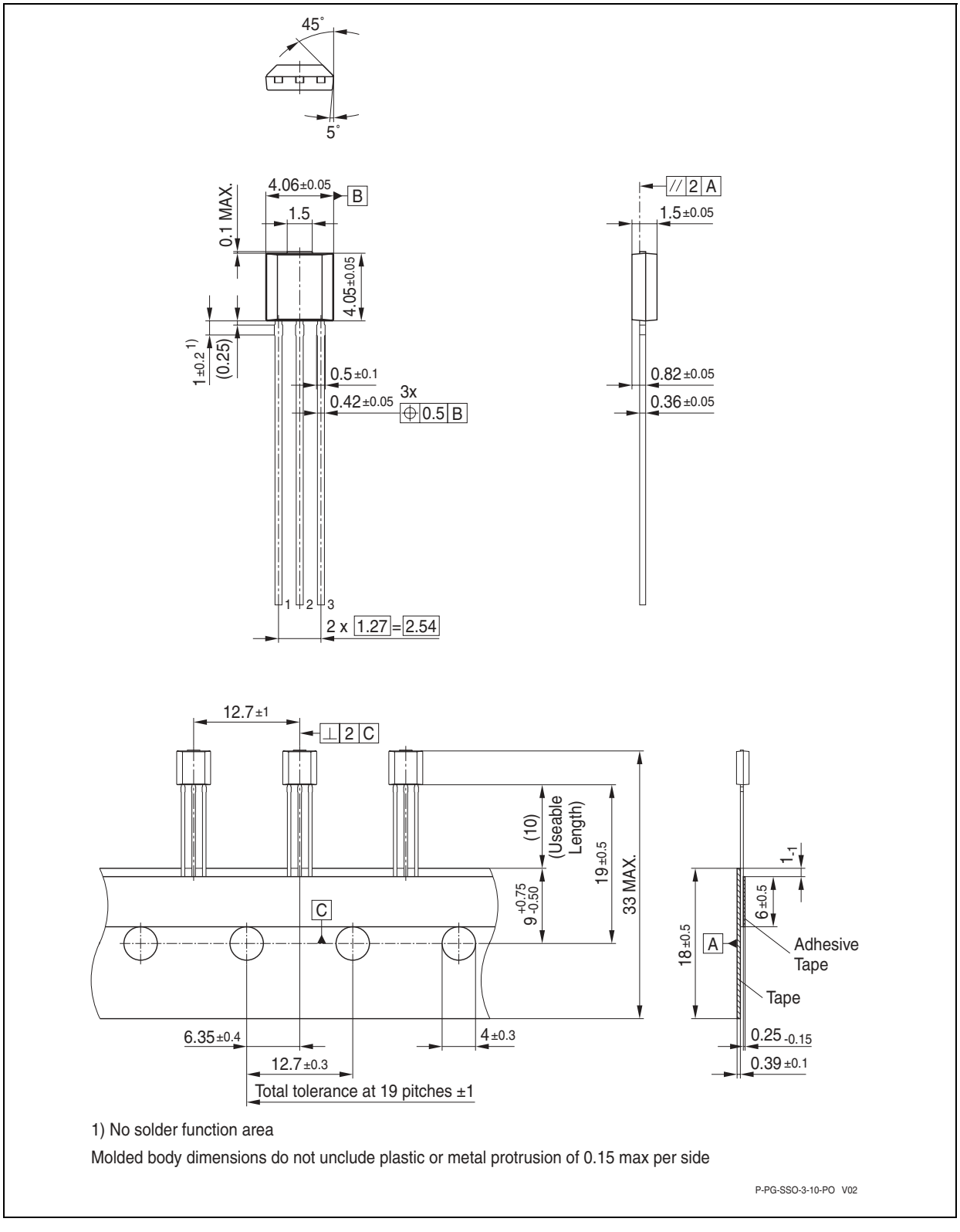


Figure 10 Application Circuit

Note: For calibration and programming, the interface has to be connected directly to the OUT pin.

The application circuit shown should be regarded as an example only. It will need to be adapted to meet the requirements of other specific applications. Further information is given in **Chapter 13**.

11 PG-SSO-3-10 Package Outlines



1) No solder function area

Molded body dimensions do not unclude plastic or metal protrusion of 0.15 max per side

P-PG-SSO-3-10-PO V02

Figure 11 **PG-SSO-3-10** (Plastic Green Single Small Outline Package)

12 PG-SSO-4-1 Package Outlines

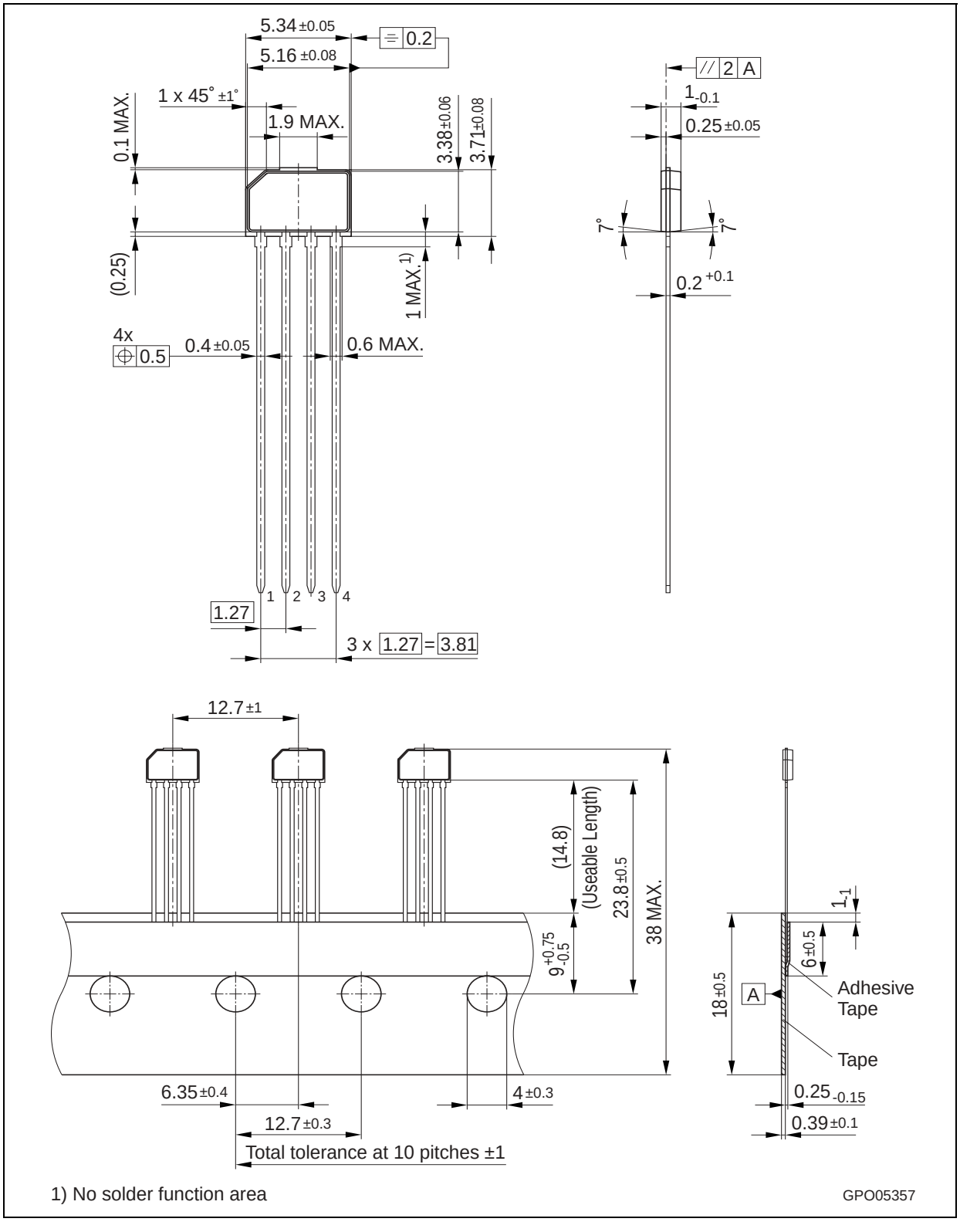


Figure 12 **PG-SSO-4-1** (Plastic Green Single Small Outline Package)

13 SPC Output Definition

The sensor supports a SPC (Short PWM Code) protocol, which enhances the standardized SENT protocol (Single Edge Nibble Transmission) defined by SAE J2716. SPC enables the use of enhanced protocol functionality due to the ability to select between “synchronous”, “range selection” and “ID selection” protocol mode. The following tables give an overview of relevant registers to chose the appropriate SPC mode.

Table 18 SPC Mode Registers

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Protocol register	*P*		2	bit	
ID register	*ID*		2	bit	1)

1) The ID register is only actively used in ID selection mode.

Table 19 SPC Mode Selection

Mode	Parameter P_{MSB}	Parameter P_{LSB}	Explanation
Synchronous	0	No effect	Section 13.4
Dynamic range selection	1	0	Section 13.5
ID selection	1	1	Section 13.6

13.1 Basic SPC Protocol Definition

As in SENT, the time between two consecutive falling edges defines the value of a four bit nibble, thus representing numbers between 0 and 15. The transmission time therefore depends on the transmitted data values. The single edge is defined by a 3 unit time (UT) low pulse on the output, followed by the high time defined in the protocol (nominal values, may vary by tolerance of internal RC oscillator, not including analog delay of the open drain output and influence by external circuitry, unit time programming see Section 13.2). All values are multiples of a unit time frame concept. A transfer consists of the following parts, depicted in Figure 13:

- A trigger pulse by the master, which initiates the data transmission
- A synchronization period of 56 UT (in parallel, a new sample is calculated)
- A status nibble of 12-27 UT
- Between 3 and 6 data nibbles of 12-27 UT each (number is programmable, see Table 21), representing the Hall value and temperature information
- A CRC nibble of 12-27 UT
- An end pulse to terminate the SPC transmission.

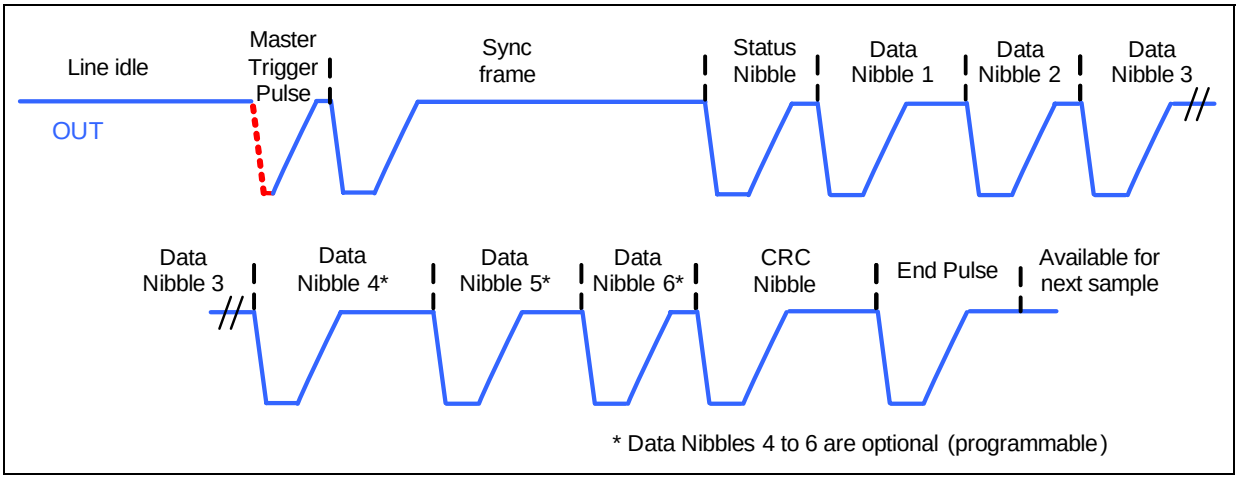


Figure 13 SPC Frame

The CRC checksum includes the status nibble and the data nibbles and can be used to check the validity of the decoded data. The sensor is available for the next sample 90µs after the falling edge of the end pulse. The sampling time (when values are taken for temperature compensation) is always defined as the beginning of the synchronization period. During this period, the resulting data is always calculated from scratch.

The number of transmitted SPC nibbles is programmable to customize the amount of information sent by the sensor. The frame contains a 16bit Hall value and an 8bit temperature value in the full configuration.

Table 20 Frame Register

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Frame register	F	2		bit	

Table 21 Frame Selection

Frame Type	Parameter F	Data Nibbles
16bit Hall, 8bit temperature	0	6 nibbles
16bit Hall	1	4 nibbles
12bit Hall, 8bit temperature	2	5 nibbles
12bit Hall	3	3 nibbles

The temperature is coded as an 8bit value. The value is transferred in unsigned integer format and corresponds to the range between -55°C and +200°C, so a transferred value

of 55 corresponds to 0°C. **Table 22** shows the mapping between junction temperature and the transmitted value in the SPC frame.

Table 22 Mapping of Temperature Value

Junction Temperature	Typ. Decimal Value from Sensor	Note
- 55°C	0	Theoretical lower limit[1)]
0°C	55	
25°C	80	
200°C	255	Theoretical upper limit[1)]

[1)] Theoretical range of temperature values, not operating temperature range

The status nibble allows to check internal states and conditions of the sensor.

- Depending on the selected SPC mode, the first two bits of the status nibble contain either the selected magnetic range or the ID of the sensor and allow therefore an easy interpretation of the received data.
- The third bit is set to “1” for the first transmission after the sensor returns from an overvoltage operation with disabled open drain stage to regular operation (see **Chapter 7.1**).
- The fourth bit is switched to “1” for the first data package transferred after a reset. This allows the detection of low-voltage situations or EMC problems of the sensor.

13.2 Unit Time Setup

The basic SPC protocol unit time granularity is defined as 3 µs. Every timing is a multiple of this basic time unit. To achieve more flexibility, trimming of the unit time can be used to:

- Allow a calibration trim within a timing error of less than 20% clock error (as given in SAE standard)
- Allow a modification of the unit time for small speed adjustments

This enables a setup of different unit times, even if the internal RC oscillator varies by ±20%. Of course, timing values that are too low could clash with timing requirements of

the application and should therefore be avoided, but in principle it is possible to adjust the timer unit for a more precise protocol timing.

Table 23 Predivider Setting

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	*Prediv*	4		bit	Predivider[1)]
Unit time	t_{UNIT}	2.0	3.88	µs	Clk_{UNIT}=8MHz[2)]

1) Prediv default is decimal = 8 for 3 µs nominal SPC unit time

2) RC oscillator frequency variation +/- 20%

The nominal unit time is calculated by:

$$t_{UNIT} = (Prediv + 16) / Clk_{UNIT}$$

$$Clk_{UNIT} = 8\text{MHz} \pm 20\%$$

13.3 Master Pulse Requirements

An SPC transmission is initiated by a Master pulse on the OUT pin. To detect a low level on the OUT pin, the voltage must be below a threshold V_{thf}. The sensor detects that the OUT line has been released as soon as V_{thr} is crossed. **Figure 14** shows the timing definitions for the master pulse. The master low time t_{mlow} as well as the total trigger time t_{mtr} are individual for the different SPC modes and are given in the subsequent sections.

It is recommended to chose the typical master low time exactly between the minimum and the maximum possible time: $t_{mlow,typ} = (t_{mlow,min} + t_{mlow,max}) / 2$. Although the allowed timing windows are larger for longer low times, the master should use a quarz clock source to provide a high timing accuracy (approx. 1%). For improved robustness, the master pulse can be adopted by the master once the effective unit time is known through the sensor's synchronisation period length. If the master low time exceeds the maximum low time, the sensor does not respond and is available for a next triggering

30µs after the master pulse crosses V_{thr}. $t_{md,tot}$ is the delay between internal triggering of the falling edge in the sensor and the triggering of the ECU.

Table 24 Master Pulse Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Falling edge threshold	V_{thf}	1.1	1.3	1.7	V	
Rising edge threshold	V_{thr}	1.25	1.43	1.8	V	
Total trigger time	t_{mtr}	10.8	13	16.3	UT	Synchronous mode 1)2)
		46.6	56	70	UT	Dyn. range mode 1)2)
		75	90	113	UT	ID selection mode 1)2)
Master delay time	$t_{md,tot}$	3.7	5.8	7.9	µs	3)

1) UT = Programmed nominal SPC unit time

2) Trigger time in the sensor is fixed to the number of unit times specified in the “typ.” column, but the effective trigger time varies due to the sensor’s clock variation

3) For V_{DD} = 5 V, R_L = 2.2 kΩ, C_L = 4.7 nF, ECU trigger level $V_{th,ECU}$ = 2V

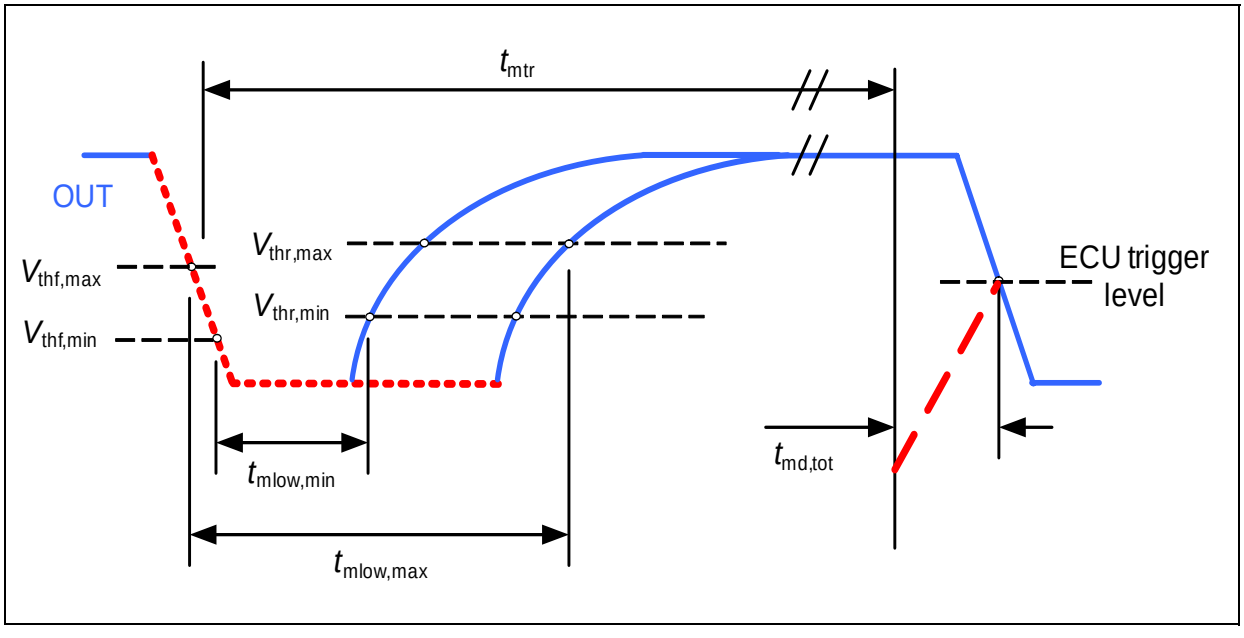


Figure 14 SPC Master Pulse Timing

13.4 Synchronous Transmission

In the “synchronous” mode, the sensor (slave) starts to transfer a complete data frame only after a low pulse is forced by the master on the OUT pin. This means that the data line is bidirectional - an open drain output of the microcontroller (master) sends the trigger pulse. The sensor then initiates a sync pulse and starts to calculate the new output data value. After the synchronization period, the data follows in form of a standard SENT frame, starting with the status, data and CRC nibbles. At the end, an end pulse allows the CRC nibble decoding and indicates that the data line is idle again. The timing diagram in **Figure 13** visualizes a synchronous transmission.

Table 25 Master Pulse Timing Requirements for Synchronous Mode

Parameter	Symbol	Limit Values			Unit[1)]	Notes
		min.	typ.	max.		
Master low time	t_{mlow}	1.5	2.75	4	UT	

1) UT = Programmed nominal SPC unit time

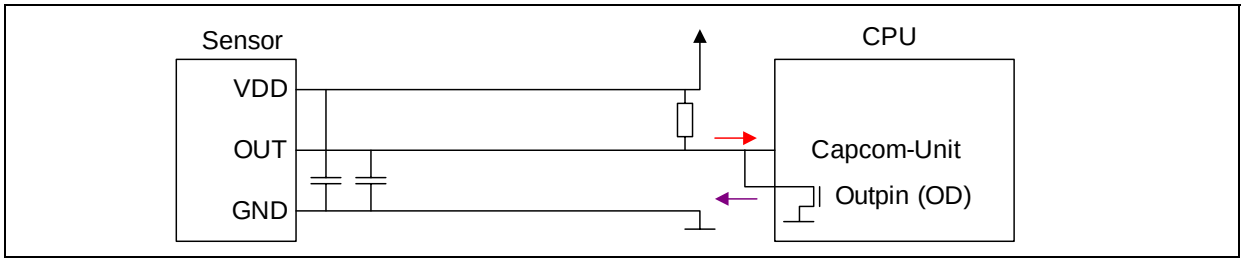


Figure 15 Bidirectional Communication in Synchronous Mode

13.5 Synchronous Transmission Including Range Selection

The low time duration of the master can be used to select the magnetic range of the sensor in SPC dynamic range selection mode.

Table 26 Master Pulse Timing Requirements for Dynamic Range Mode

Parameter	Symbol	Limit Values			Unit[1)]	Notes
		min.	typ.	max.		
Master low time	t_{mlow}	1.5	3.25	5	UT	Range = 200mT (*R*=0)
		9	12	15	UT	Range = 100mT (*R*=1)
		24	31.5	39	UT	Range = 50mT (*R*=3)

1) UT = Programmed nominal SPC unit time

The range information in the status bit can be used to determine whether the range has been properly identified. Changing the range takes some time due to the settling time of internal circuitry. The first sample after a range switch therefore still displays a value sampled with the old range setting, and the second transmission after changing the range displays the new range with reduced accuracy.

13.6 Synchronous Mode with ID Selection

This functionality is similar to the previous mode, but instead of switching the range of one sensor, one of up to four sensors are selectable on a bus (bus mode, 1 master with up to 4 slaves). This allows parallel connection of up to 4 sensors using only three lines (VDD, GND, OUT), as illustrated in **Figure 16**.

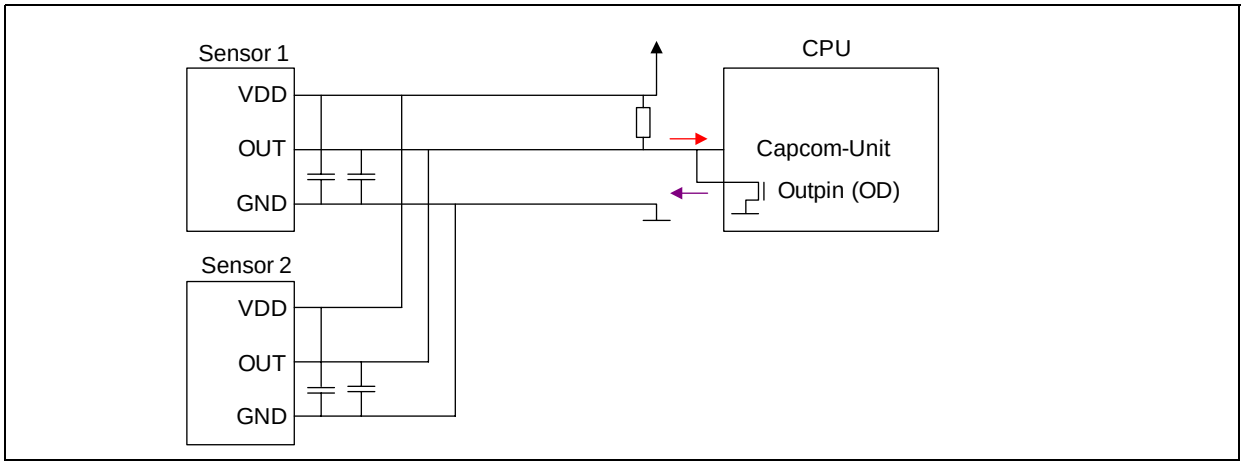


Figure 16 Bidirectional Communication with ID Selection

In this mode, the sensor starts to transfer complete packages only after receiving a master low pulse with an ID that is equivalent to the programmed value in its *ID* register. The mapping between master low time and ID is given in **Table 27**. A proper addressing requires the different sensors on a same bus to be programmed with the same nominal

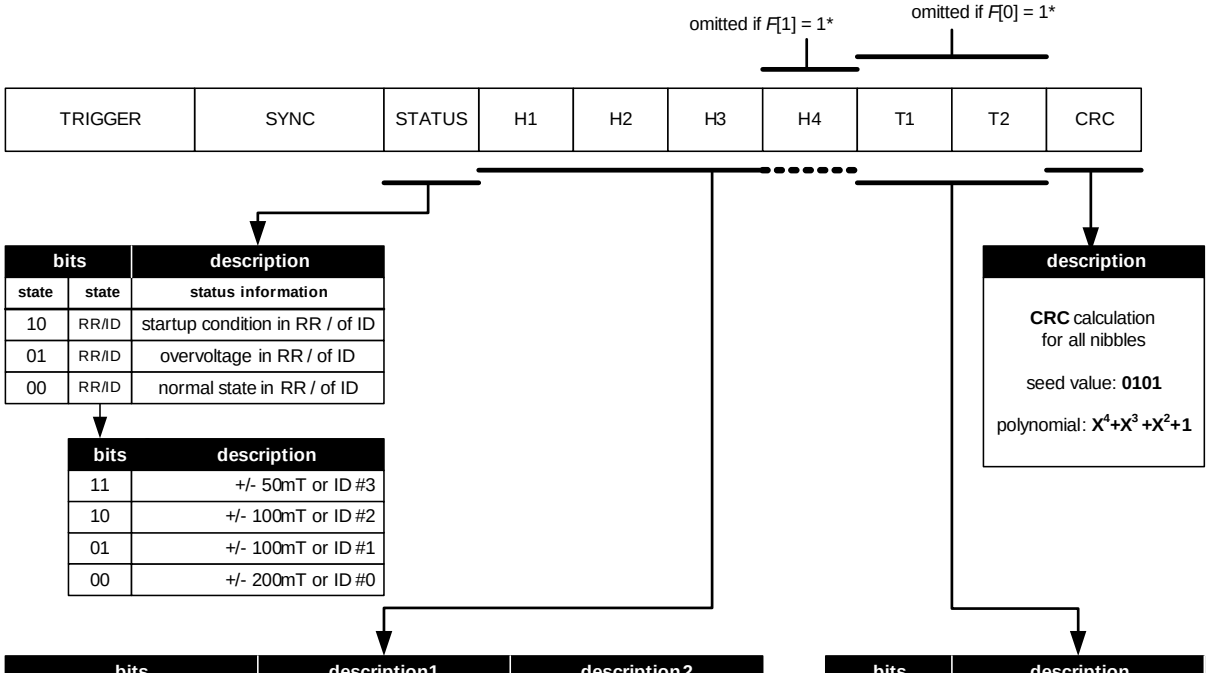
SPC unit time. Alternatively, the sensors can be trimmed using the predivider settings to further reduce their relative unit time difference for more robustness.

Table 27 Master Pulse Timing Requirements for ID Selection Mode

Parameter	Symbol	Limit Values			Unit[1)]	Notes
		min.	typ.	max.		
Master low time	t_{mlow}	9	10.5	12	UT	ID = 0
		19	21	23	UT	ID = 1
		35.5	38	40.5	UT	ID = 2
		61.5	64.5	67.5	UT	ID = 3

1) UT = Programmed nominal SPC unit time

Table 28 Content of a SPC Data Frame (5-8 Nibbles)



bits		description
state	state	status information
10	RR/ID	startup condition in RR / of ID
01	RR/ID	overvoltage in RR / of ID
00	RR/ID	normal state in RR / of ID

bits	description
11	+/- 50mT or ID #3
10	+/- 100mT or ID #2
01	+/- 100mT or ID #1
00	+/- 200mT or ID #0

description
CRC calculation for all nibbles seed value: **0101** polynomial: $X^4+X^3+X^2+1$

bits				description1	description2
H1	H2	H3	H4	decimal: OUT_{12} (= H1*256+H2*16 +H3)	decimal: OUT_{16} (= OUT12*16+H4)
1111	1111	1111	1111	4095 (FSR)	65535 (FSR)
1111	1111	1111	1110	4095	65534
1111	1111	1111	:	4095	:
1111	1111	1111	0000	4095	65520
1111	1111	1110	1111	4094	65519
1111	1111	1110	1110	4094	65518
1111	1111	1110	:	4094	:
1111	1111	1110	0000	4094	65504
1111	1111	1101	1111	4093	65503
:	:	:	:	:	:
0000	0000	0010	0000	2	32
0000	0000	0001	1111	1	31
0000	0000	0001	:	1	:
0000	0000	0001	0000	1	16
0000	0000	0000	1111	0	15
0000	0000	0000	1110	0	14
0000	0000	0000	:	0	:
0000	0000	0000	0001	0	1
0000	0000	0000	0000	0	0

bits		description
T1	T2	decimal: $TEMP_8$ (= T1*16 + T2)
1111	1111	200 °C
1111	1110	199 °C
1111	:	:
1111	0000	185 °C
1110	1111	184 °C
:	:	:
0101	0000	25 °C
0100	1111	24 °C
:	:	:
0011	0111	0°C
0011	0110	-1°C
:	:	:
0000	0001	-54 °C
0000	0000	-55 °C

Abbreviations:
TRIGGER – trigger nibble
SYNC – synchronization nibble
STATUS – status nibble
CRC – cyclic redundancy code nibble
FSR – full scale range
H1..4 – hall value
T1..2 – temperature value
OUT_{12} – 12 bit output value
OUT_{16} – 16 bit output value
$TEMP_8$ – 8 bit temperature value

* The number of nibbles is programmed in the frame register *F*

13.7 Checksum Nibble Details

The Checksum nibble is a 4-bit CRC of the data nibbles including the status nibble. The CRC is calculated using a polynomial $x^4 + x^3 + x^2 + 1$ with a seed value of 0101.

In the TLE4998C it is implemented as a series of XOR and shift operations as shown in the following flowchart:

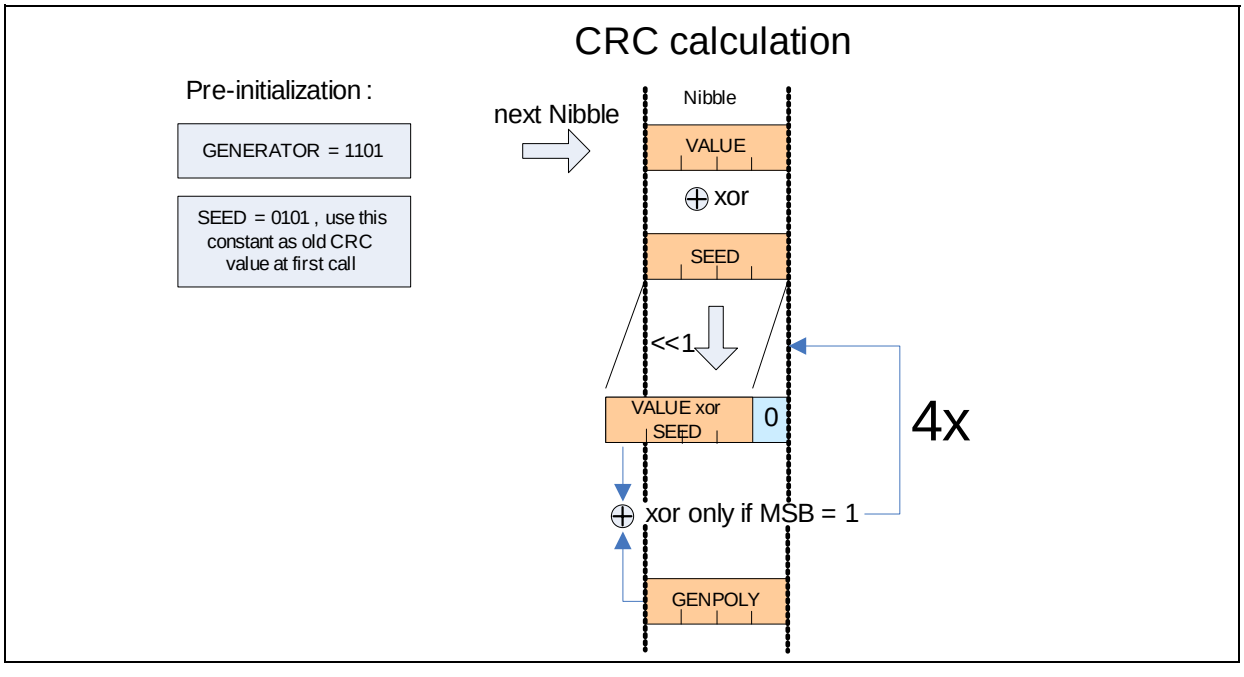


Figure 17 CRC Calculation

A microcontroller implementation may use an XOR command plus a small 4-bit lookup table to calculate the CRC for each nibble.

```
// Fast way for any µC with low memory and compute capabilities
char Data[8] = {…}; // contains the input data (status nibble, 6 data nibble, CRC)
// required variables and LUT
char CheckSum, i;
char CrcLookup[16] = {0, 13, 7, 10, 14, 3, 9, 4, 1, 12, 6, 11, 15, 2, 8, 5};
CheckSum= 5; // initialize checksum with seed "0101"
for (i=0; i<7; i++) {
   CheckSum = CheckSum ^ Data[i];
   CheckSum = CrcLookup[CheckSum];
}
; // finally check if Data [7] is equal to CheckSum
```

Figure 18 Example Code for CRC Generation

w w w . i n f i n e o n . c o m

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