1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS successive approximation 12-bit analog-to-digital converter with an on chip buried Zener reference and converting in 5 or 12 μs.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification are as follows:

Device	Part Number
−1	AD7572S(X)05/883B and AD7572S(X)12/883B
−2	AD7572T(X)05/883B and AD7572T(X)12/883B
−3	AD7572U(X)05/883B and AD7572U(X)12/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C, unless otherwise noted)

V_{DD} to DGND ..... −0.3 V, +7 V
V_{SS} to DGND ..... +0.3 V, −17 V
AGND to DGND ..... −0.3 V, V_{DD} +0.3 V
AIN to AGND ..... −15 V, +15 V
Digital Input Voltage to DGND ..... −0.3 V, V_{DD} +0.3 V
Digital Output Voltage to DGND ..... −0.3 V, V_{DD} +0.3 V
Power Dissipation (to +75°C) ..... 1000 mW
Derates above +75°C ..... 10 mW/°C
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 120°C/W for Q-24 and E-28A

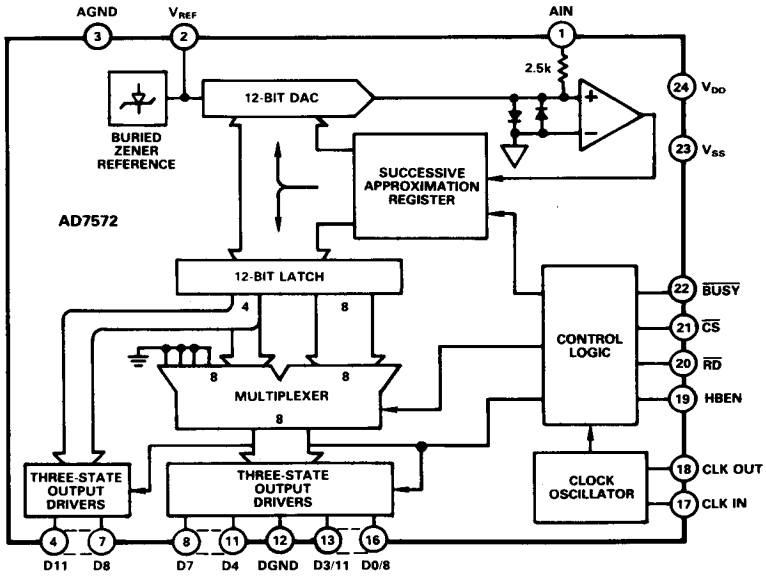
AD7572—SPECIFICATIONS

Table 1.

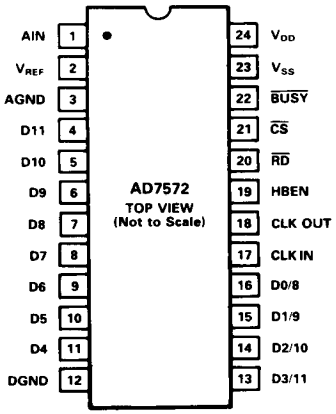
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1, 2, 3	12				Minimum Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	−1, 2	1	1	1			±LSB max
		−3	3/4	1	3/4	1/2		
Differential Nonlinearity	DNL	−1, 2, 3	1	1	1			±LSB max
Offset Error	OE	−1	6	4	6			±LSB max
		−2	5	4	5	3		
		−3	4	4	4			
Full-Scale Error[2]	FSE	−1		15				±LSB max
		−2, 3		15		10		
Full-Scale Temp Co[3]	FSTC	−1	45		45			±ppm/°C max
		−2, 3	25		25			
Analog Input Current		−1, 2, 3	3.5	3.5	3.5			mA max
V_{REF} Output	V_{REF}	−1, 2, 3		−5.25			±1%	V max
V_{REF} Temp Co	REFTC	−1	40		40			±ppm/°C max
		−2, 3	20		20			
Output Current Sink Capability		−1, 2, 3	550	550	550		External Load Should Not Change During Conversion	µA max
Digital Input Low Voltage	V_{IL}	−1, 2, 3	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IM}	−1, 2, 3	2.4	2.4	2.4			V min
Input Capacitance	C_{IN}	−1, 2, 3	10					pF max
Input Current 1	I_{IN1}	−1, 2, 3	10	10	10		$\overline{CS}$, $\overline{RD}$, HBEN	±µA max
Input Current 2	I_{IN2}	−1, 2, 3	20	20	20		CLKIN	±µA max
Digital Output Low Voltage	V_{OL}	−1, 2, 3	0.4	0.4	0.4		I_{SINK} = 1.6 mA	V max
Digital Output High Voltage	V_{OH}	−1, 2, 3	4.0	4.0	4.0		I_{SOURCE} = 200 µA	V min
Floating State Leakage Current	I_{OUT}	−1, 2, 3	10	10	10			±µA max
Floating State Output Capacitance	C_{OUT}	−1, 2, 3	15					pF max
Supply Current from V_{DD}	I_{DD}	−1, 2, 3	7	7	7			mA max
Supply Current from V_{SS}	I_{SS}	−1, 2, 3	−12	−12	−12			mA max
Conversion Time[4] Synchronous Clock	t_{CONV}	−1, 2, 3	5	5	5		f_{CLK} = 2.5 MHz	µs max
			12.5	12.5	12.5	12.5	f_{CLK} = 1 MHz	
Conversion Time[4] Asynchronous Clock	t_{CONV}	−1, 2, 3	4.8	4.8	4.8		f_{CLK} = 2.5 MHz	µs min
			5.2	5.2	5.2			µs max
Conversion Time[4] Asynchronous Clock	t_{CONV}	−1, 2, 3	12	12	12		f_{CLK} = 1 MHz	µs min
			13	13	13			µs max

NOTES
[1]V_{DD} = +5 V ± 5%, V_{SS} = −15 V ± 5%.
[2]Includes Internal V_{REF} Error.
[3]Includes Internal V_{REF} Drift.
[4]Order either AD7572YX05/883B or AD7572YX12/883B.

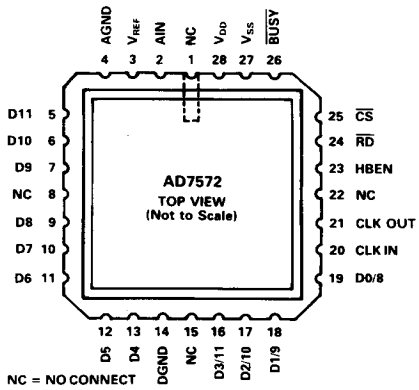
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

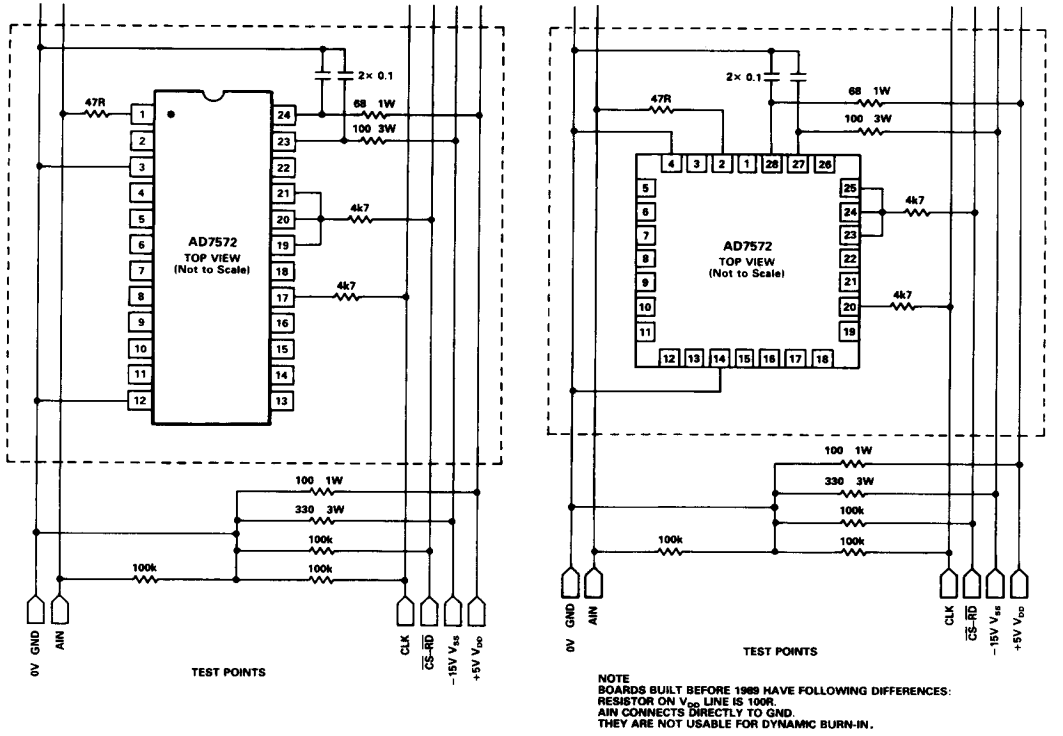


3.2.4 Microcircuit Technology Group.

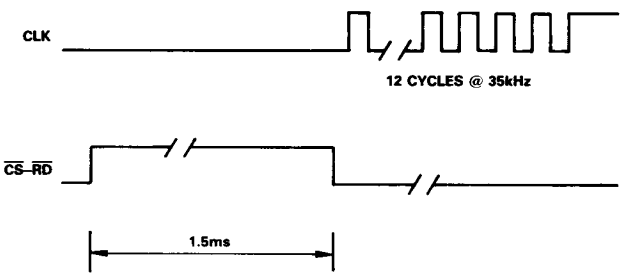
This microcircuit is covered by Technology Group (81).

4.2.1 Life Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7572 Edge Connections

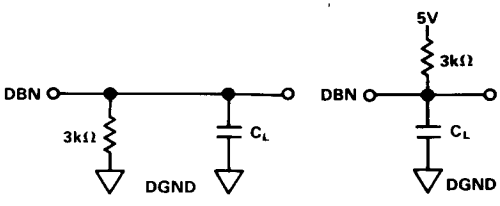


Static Burn-In Initialization

AD7572 TIMING[1]

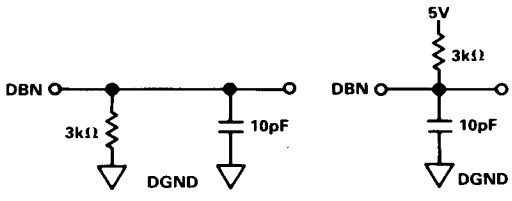
Test	Symbol	Device	Design Limit T_{min} to T_{max}	Units
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1	−1, 2, 3	0	ns min
RD to BUSY Propagation Delay	t_2	−1, 2, 3	270	ns max
Data Access Time after $\overline{RD}$, C_L=20 pF	t_3[2]	−1, 2, 3	120	ns max
Data Access Time after RD, C_L=100 pF			170	ns max
$\overline{RD}$ Pulse Width	t_4	−1, 2, 3	t_3	ns min
CS to RD Hold Time	t_5	−1, 2, 3	0	ns min
Data Setup Time after BUSY	t_6[2]	−1, 2, 3	100	ns max
Bus Relinquish Time	t_7[3]	−1, 2, 3	20	ns min
			90	ns max
HBEN to $\overline{RD}$ Setup Time	t_8	−1, 2, 3	0	ns min
HBEN to RD Hold Time	t_9	−1, 2, 3	0	ns min
Delay Between Successive Read Operations	t_{10}	−1, 2, 3	200	ns min

NOTES
[1]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_8) *b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_8)*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

6.0 Converter Details.

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit voltage mode DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 3, the AIN input connects to the comparator input via 2.5 kΩ. The DAC which has a similar 2.5 kΩ output impedance connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 80 ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 80 ns after a CLK IN edge until conversion is finished. At the end of conversion, the DAC output current balances the AIN input current. The SAR contents (12-bit data word) which represent the AIN input signal is loaded into a 12-bit latch.

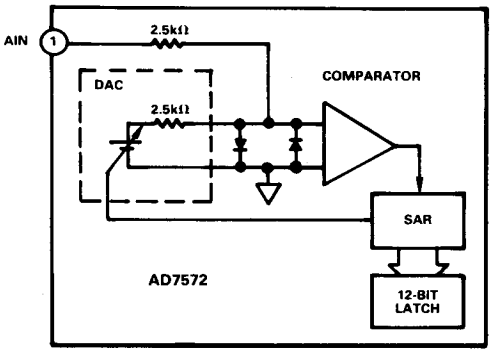


Figure 3. AD7572 AIN Input

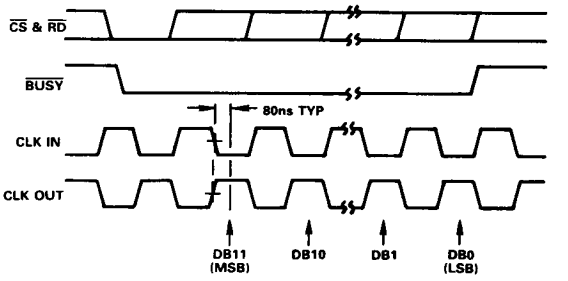


Figure 4. Operating Waveforms Using an External Clock Source for CLK IN

6.1 Driving the Analog Input.

During conversion, the AIN input current is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 2.5 MHz when CLK IN = 2.5 MHz). The analog input voltage must remain fixed during this period and as a result must be driven from an op amp or sample hold with a low output impedance. The output impedance of an op amp is equal to the open loop output impedance divided by the loop gain at the frequency of interest.

Suitable devices capable of driving the AD7572 AIN input are the AD OP-27 and AD711 op amps or the AD585 sample hold.

6.2 Control Inputs Synchronization.

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach ensures a fixed 5 μs conversion time for the AD7572XX 05 and 12.5 μs for the AD7572XX12: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT.

6.3 Unipolar Offset and Full-Scale Error Adjustment.

In applications where absolute accuracy is important, then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 5 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving AIN (i.e., A1 in Figure 5.). For zero offset error apply 0.61 mV (i.e., 1/2 LSB) at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817 V (i.e., FS –3/2 LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

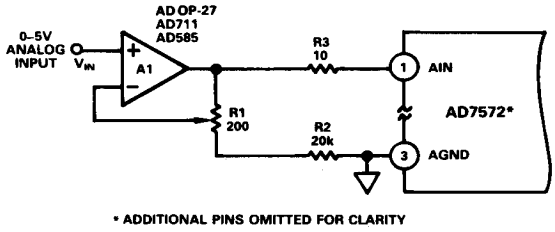


Figure 5. Unipolar 0 to +5 V Operation with Gain Error Adjust

6.4 Bipolar Operation.

Figures 6 and 7 show how bipolar operation can be achieved with the AD7572. Both circuits use an op amp to offset the analog signal (V_{IN}) by 2.5 V. Alternatively, the op amp (A1) can be replaced by a sample hold as shown in Figure 24. The op amp transfer functions are given below:

Figure 10: AIN = (V_{IN} + 2.5) volts
Figure 12: AIN = ($-V_{IN}$ + 2.5) volts

Both circuits have an analog input range of ±2.5 V and an LSB size of 1.22 mV. The output codes are offset binary for Figure 6 and complimentary offset binary for Figure 7.

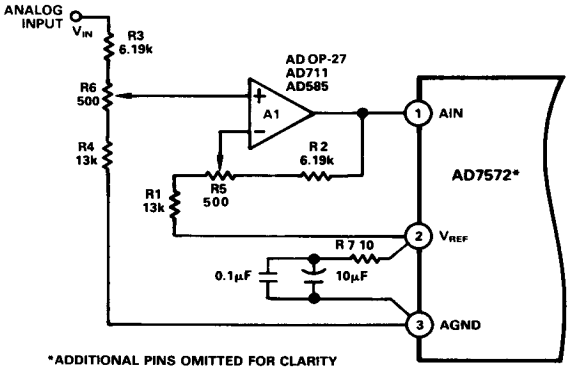


Figure 6. AD7572 Bipolar Operation – Output Code is Offset Binary

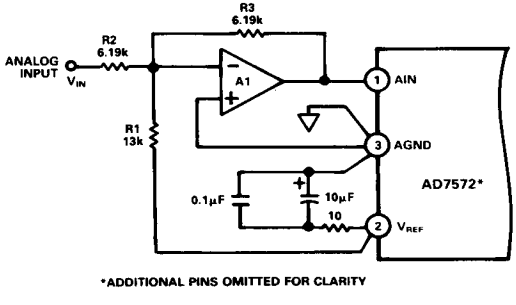


Figure 7. AD7572 Bipolar Operation – Output Code is Complementary Offset Binary

Signal ranges other than ±2.5 V are easily accommodated using different values of R3 and R4 for Figure 6, and a different R2 value for Figure 7. These resistors should be chosen such that the voltage range at AIN covers the full dynamic range (i.e., 0 V to 5 V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

In measurement applications where absolute accuracy is required, offset and full-scale error can be adjusted to zero as in Figure 8.

6.5 Bipolar Offset and Full-Scale Error Adjustment.

The bipolar circuit of Figure 6 can be adjusted for offset and full-scale errors, by including two potentiometers R5 and R6, as shown in Figure 8. Offset must be adjusted before full-scale error. This is achieved by applying an analog input of 0.61 mV (1/2 LSB) at V_{IN} and adjusting R5 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

For full-scale error adjustment, the analog input must be at 2.49817 volts (i.e., FS/2 –3/2 LSBs or last transition point). Then R6 is adjusted until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

A similar offset and full-scale error adjustment procedure may be employed for Figure 7 by making R1 and R2 variable. Offset must again be adjusted before full scale error. This is achieved by applying an analog input of 0.61 mV at V_{IN} and adjusting R1 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

For full-scale error adjust, apply a signal source of 2.49817 V at V_{IN} and adjust R2 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

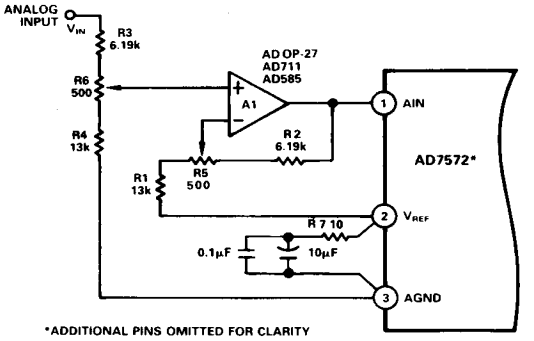


Figure 8. AD7572 Bipolar Operation with Offset and Gain Error Adjust

6.6 Internal Reference.

The AD7572 has an on-chip, buffered, temperature-compensated, buried Zener reference, which is factory trimmed to −5.25 V ± 1%. It is internally connected to the DAC and is also available at Pin 2 to provide up to 550 μA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10 μF of tantalum in parallel with 100 nF ceramic). However, large values of decoupling capacitor can affect the dynamic response and stability of the reference amplifier. A 10 Ω resistor in series with the decoupling capacitors will eliminate this problem without adversely affecting the filtering effect of the capacitors. A simplified schematic of the reference with its recommended decoupling components is shown in Figure 9.

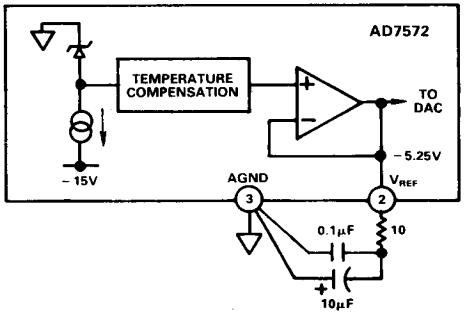


Figure 9. AD7572 Internal −5.25 V Reference