



# PRESETTABLE UP/DOWN COUNTER BINARY OR BCD-DECADE

## GENERAL DESCRIPTION

The MMC 4029 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4029 consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK,  $\overline{\text{CARRY-IN}}$  (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET

ENABLE signals. Q1, Q2, Q3, Q4 and a  $\overline{\text{CARRY OUT}}$  signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to it's zero count. The counter is advanced one count at the positive transition of the clock when the  $\overline{\text{CARRY-IN}}$  or PRESET ENABLE signals are high. Advancement is inhibited when the  $\overline{\text{CARRY-IN}}$  or PRESET ENABLE signals are high. The  $\overline{\text{CARRY-OUT}}$  signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided

the  $\overline{\text{CARRY-IN}}$  signal is low. The  $\overline{\text{CARRY-IN}}$  signal in the low state can thus be considered a CLOCK ENABLE. The  $\overline{\text{CARRY-IN}}$  terminal must be connected to  $V_{SS}$  when not in use. Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

## FEATURES

- Medium speed operation—8 MHz (typ.) at  $C_L = 50$  pF and  $V_{DD}-V_{SS} = 10$  V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "PRESET ENABLE" and individual "JAM" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode

## ABSOLUTE MAXIMUM RATINGS

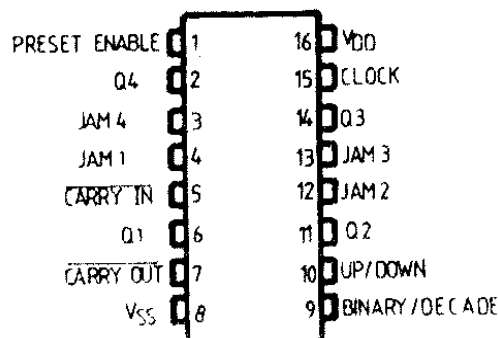
$V_{DD}^*$	Supply voltage: G and H types E and F types	-0.5 to 20 -0.5 to 18 -0.5 to $V_{DD}+0.5$	V V V
$V_i$	Input voltage		
$I_i$	DC input current (any one input)	$\pm 10$	mA
$P_{tot}$	Total power dissipation (per package) Dissipation per output transistor for $T_A =$ full package-temperature range	200	mW
$T_A$	Operating temperature : G and H types E and F types	-55 to -40	125 85 °C °C
$T_{stg}$	Storage temperature	-65 to	150 °C

\* All voltage values are referred to  $V_{SS}$  pin voltage

## RECOMMENDED OPERATING CONDITIONS

$V_{DD}^*$	Supply voltage: G and H types E and F types	3 to 18 3 to 15 0 to $V_{DD}$	V V V
$V_i$	Input voltage		
$T_A$	Operating temperature : G and H types E and F types	-55 to -40	125 85 °C °C

## CONNECTION DIAGRAM



**STATIC ELECTRICAL CHARACTERISTICS**

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>ol</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>LOW</sub>		25°C			T <sub>HIGH</sub>		
						min.	max.	min.	typ.	max.	min.		max.
I <sub>L</sub>	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150
			0/10			10		10		0.04	10		300
			0/15			15		20		0.04	20		600
			0/20			20		100		0.08	100		3000
	E, F types	0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V <sub>OH</sub>	Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95		
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V <sub>OL</sub>	Output low voltage	5 / 0		< 1	5		0.05			0.05		0.05	
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V <sub>IH</sub>	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V <sub>IL</sub>	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I <sub>OH</sub>	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15	
			0/ 5	4.6		5	-0.64		0.51	-1		-0.36	
			0/10	9.5		10	-1.6		1.3	-2.6		-0.9	
			0/15	13.5		15	-4.2		3.4	-6.8		-2.4	
		E, F types	0/ 5	2.5		5	-1.53		1.36	-3.2		-1.1	
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36	
		0/10	9.5		10	-1.3		1.1	-2.6		-0.9		
		0/15	13.5		15	3.6		3.0	-6.8		-2.4		
I <sub>OT</sub>	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36	
			0/10	0.5		10	1.6		1.3	2.6		0.9	
			0/15	1.5		15	4.2		3.4	6.8		2.4	
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36	
			0/10	0.5		10	1.3		1.1	2.6		0.9	
			0/15	1.5		15	3.6		3.0	6.8		2.4	
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current	G, H types	0/18	Any input	18		$\pm 0.1$		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$	
		E, F types	0/15		15		$\pm 0.3$		$\pm 10^{-5}$	$\pm 0.3$		$\pm 1$	
C <sub>i</sub>	Input capacitance		Any input						5	7.5		pF	

\* T<sub>LOW</sub> = -55°C for G, H devices, -40°C for E, F devices\* T<sub>HIGH</sub> = +125°C for G, H devices, +85°C for E, F devices

The Noise Margin for both "1" and "0" level is

1 V min. with V<sub>DD</sub> = 5 V2 V min. with V<sub>DD</sub> = 10 V2.5 V min. with V<sub>DD</sub> = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS**

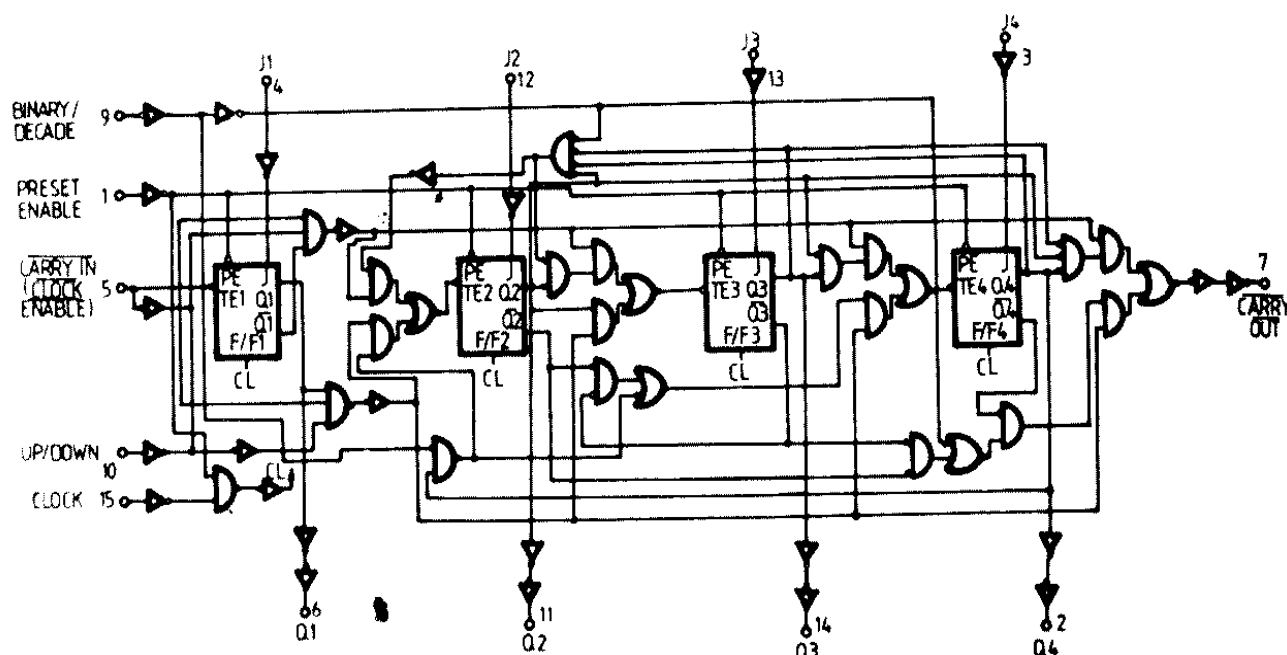
( $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$ , typical temperature coefficient for all  $V_{DD} = 0.3\%/^\circ\text{C}$ , all input rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS $V_{DD}$ (V)	VALUES			UNIT	
		min.	typ.	max.		
<b>Clocked operation</b>						
$t_{PLH}$ $t_{PHL}$	Propagation delay time (Q outputs)	5 10 15		250 120 90	500 240 180	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay time (Carry Output)	5 10 15		280 130 95	560 260 190	
$t_{TLH}$ $t_{THL}$	Transition time (Q outputs, carry output)	5 10 15		100 50 40	200 100 80	ns
$t_{W.}$	Minimum clock pulse width	5 10 15		90 45 30	180 90 60	ns
$t_r, t_f^{**}$	Clock rise and fall time	5 10 15			15 15 15	$\mu\text{s}$
$t_{setup}^{***}$	Minimum setup time (Carry input)	5 10 15		30 10 6	60 20 12	ns
$t_{setup}$	Minimum setup time (B/D or U/D)	5 10 15		170 70 50	340 140 100	
$f_{max}$	Maximum clock input frequency	5 10 15	2 4 5.5	4 8 11		MHz
<b>Preset enable</b>						
$t_{THL}$ $t_{TLH}$	Propagation delay time (Q outputs)	5 10 15		235 100 80	470 200 160	ns
$t_{PHL}$ $t_{PLH}$	Propagation delay time (Carry Output)	5 10 15		320 145 105	640 290 210	
$t_{W.}$	Minimum Preset enable (pulse width)	5 10 15		65 35 25	130 70 50	ns
$t_{rem}^{***}$	Minimum preset enable (removal time)	5 10 15		100 55 40	200 110 80	ns
<b>Carry Input</b>						
$t_{PHL}$ $t_{PLH}$	Propagation delay time (Carry output)	5 10 15		170 70 50	340 140 100	ns
$t_{setup}^{***}$	Minimum setup time (Carry input)	5 10 15		25 15 12	50 30 25	ns

PARAMETER	TEST CONDITIONS V <sub>DD</sub> (V)	VALUES			UNIT
		min.	typ.	max.	
t <sub>hold</sub> *** Minimum hold time (Carry input)	5 10 15		100 35 30	200 70 60	ns

\* If more than one unit is cascaded in the parallel clocked application, t<sub>h</sub> should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.  
 \*\*\* From Up/Down, Binary/Decade, Carry In preset Enable Control Inputs to Clock Edge.  
 \*\*\* From Carry In to Clock Edge.

**LOGIC DIAGRAM**



**TRUTH TABLES**

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
	0	1	X	$\bar{Q}$	Q
X	X	0	1	1	0
	1	1	X	Q	$\bar{Q}$ NC
	X	1	X	Q	$\bar{Q}$ NC

X = don't care

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
$\overline{\text{CARRY IN (CI)}}$ $\overline{\text{CLOCK ENABLE}}$	1 0	NO COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION