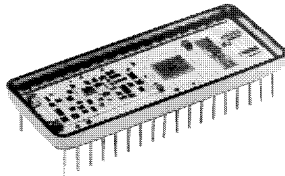


LVDT/RVDT-TO-DIGITAL CONVERTER



DESCRIPTION

The DTC-19300 is a 12- or 14-bit LVDT (Linear Variable Differential Transformer)- or RVDT (Rotary Variable Differential Transformer)-to-digital converter which also supplies the AC excitation to drive the LVDT. Internal AC excitation voltage, frequency, signal gain and resolution are all programmable for optimum system performance. Packaged in a 36-pin hybrid, the DTC-19300 also features Velocity (VEL) and Built-In-Test (BIT) outputs. The three-state digital outputs are provided in a two byte format, for easy computer interface.

The DTC-19300 has been designed precisely for use with an LVDT. Inherent characteristics of the DTC-19300, such as the input to output phase shift, have been given considerable attention. The converter's reference voltage is derived from,

and is in phase with, the LVDT output signal. Therefore, any errors due to the transducer's phase shift are virtually eliminated. Additionally, the programmability of the DTC-19300 will accommodate a broad range of LVDT's.

APPLICATIONS

The DTC-19300 provides many features previously supplied by individual system components. Because of its internal AC source, programmable features, fault indicator (BIT), and velocity output (VEL), the need for other system circuits is minimized. The DTC-19300 is an excellent choice for applications using the LVDT transducer for position feedback, such as military, commercial aerospace and industrial control systems.

FEATURES

- **Internal Oscillator:**
Programmable for Voltage and Frequency
- **Programmable Signal Gain**
- **Programmable for 12- or 14-Bit Resolution**
- **Velocity Output**
- **Built-In-Test Output**
- **Three-State, Two-Byte Digital Output**

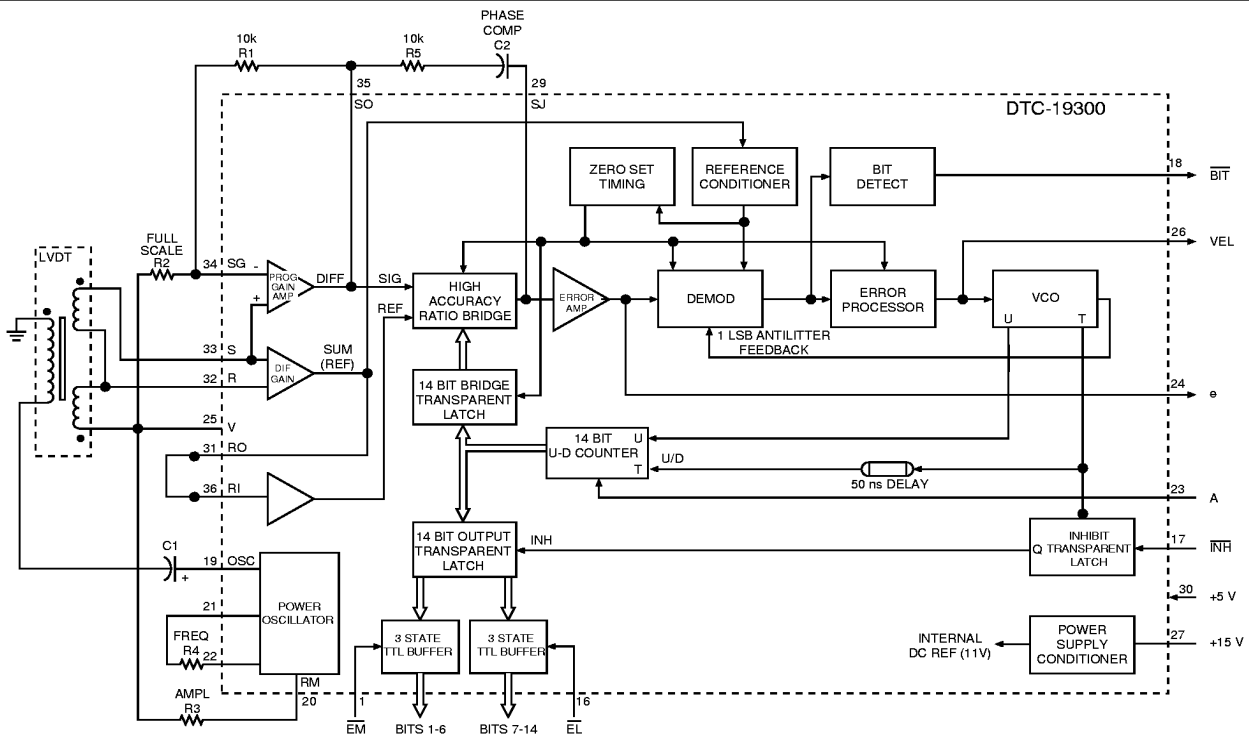


FIGURE 1. DTC-19300 BLOCK DIAGRAM

TABLE 1. DTC-19300 SPECIFICATIONS		
Specifications apply over temperature and power supply ranges.		
PARAMETER	VALUE	DESCRIPTION
RESOLUTION	12 or 14 bits	Programmable.
ACCURACY	0.25, 0.05% of Reading	See Ordering Information
REPEATABILITY	1 LSB max	
DIFFERENTIAL LINEARITY	1 LSB max	
FREQUENCY OUT (OSC Pin 19) Frequency Voltage Current Drive Protection	5 kHz $\pm 10\%$ 2.7 Vrms $\pm 20\%$ 20 mA rms min	Tunable down to 400 Hz; disable with R4 = ∞ (see Setting Up and Programming). 20% at room temp, add 20% at overtemp. Scalable down (see Setting Up and Programming). Short circuit, overcurrent, and voltage transient protected.
REFERENCE IN (RI) Full Scale Voltage Input Impedance	2 Vrms $\pm 10\%$ 20 MOhms min	Transient protected voltage follower.
REFERENCE (R) Voltage Input Impedance	1 Vrms $\pm 10\%$ 20 MOhms min	Transient protected voltage follower.
SIGNAL IN (S) Full Scale Voltage Input Impedance	2 Vrms 20 MOhms min	Transient protected voltage follower.
DIGITAL INPUTS/OUTPUTS Logic Type Inputs Loading INH (Inhibit) \overline{EM} (Enable Bits 1-6) \overline{EL} (Enable Bits 7-14) A (Resolution Control)	Logic 0 = 0.8 V max Logic 1 = 2.0 V min 10 μ A max	TTL/CMOS compatible. Pull-up current source to +5 V//5 pF, CMOS transient protected. Logic 0 inhibits, data valid within 0.5 μ s Logic 1 enables. Logic 0 enables, data valid within 150 ns. Logic 1 = high impedance, data high Z within 100 ns. Logic 1 = 14-bit resolution. Logic 0 = 12-bit resolution.
OUTPUTS Parallel Data \overline{BIT} (Built in Test) Drive Capability	12 or 14 bits Logic 0 = 1 TTL load Logic 1 = 10 TTL loads High Z = 10 μ A/5 pF max	Bipolar two's complement. Bit 1 = MSB; Bit 14 or Bit 12 = LSB. Logic 0 for BIT condition (converter malfunction). 1.6 mA at 0.4 V max +50 pF. -0.4 mA at 2.8 V min +50 pF. When in the third state.
ANALOG OUTPUTS V (Analog Ground) VEL (Velocity) Scaling Scaling TC Reversal Error Linearity Zero Offset Noise and Ripple AC peak/DC avg Load	5.5 VDC nom ± 4 V $\pm 15\%$ 200 PPM/ $^{\circ}$ C max 2% max 2% of output max 10 mV max 50 mV rms 0.5% max 40 kOhms min	VEL is with respect to V. 1 (14-bit) or 4 (12-bit) ranges per second.
DYNAMIC CHARACTERISTICS Tracking Rate Bandwidth, Closed Loop Ka A1 A2 A B Acc for 1 LSB lag Settling time - half scale step	1 full range per sec, min 18 Hz 1600 1/sec ² 0.4 1/sec 4000 1/sec 40 1/sec 20 1/sec 0.1 full ranges per sec ² 150 ms	

TABLE 1. DTC-19300 SPECIFICATIONS (CONTD)
Specifications apply over temperature and power supply ranges.

PARAMETER	VALUE	DESCRIPTION
POWER SUPPLIES +5V SUPPLY Nominal Voltage and Range Max Voltage w/o Damage Current, Peak Current, Average +15V SUPPLY Nominal Voltage and Range Max Voltage w/o Damage Current, Peak Current, Average	+5 VDC $\pm 10\%$ +8 VDC 10 mA max 10 mA max +15 VDC $\pm 5\%$ +18 VDC 25 mA max, $+\sqrt{2} \times I_{OSC}$ rms. 35 mA max, $+0.9 \times 0.5 \times I_{OSC}$ rms.	
TEMPERATURE RANGES Operating, Ambient -3XX -1XX Storage	0°C to +70°C -55°C to +125°C -65°C to +150°C	
PHYSICAL CHARACTERISTICS Size Weight	0.78 x 1.9 x 0.21 inches (20 x 48 x 5.3 mm) 1 oz (28 gm)	36-pin DDIP

INTRODUCTION

The circuit shown in FIGURE 1 (DTC-19300 Block Diagram) consists of four main parts:

1. signal input conditioner
2. feedback loop (whose elements include a high accuracy ratio bridge, a demodulator, an error processor, a VCO and an up-down counter)
3. power oscillator to excite the LVDT
4. digital interface circuit (including various latches and buffers)

In the LVDT, position output is transmitted as a differential voltage that varies linearly with changes in the core position. The DTC-19300 receives the differential and sum voltage at its inputs and internally produces a digital position δ which tracks the differential position λ to within the specified accuracy of the converter.

A high accuracy ratio bridge is used to compute $(\lambda - \delta)$, where:

λ = the LVDT's core position.

δ = the digital position contained in the converter's up-down counter.

The tracking process consists of continually adjusting δ to make $(\lambda - \delta) \rightarrow 0$, so that δ will represent the core's position, λ .

The ratio bridge output is fed to a demodulator whose output is an analog DC level proportional to $(\lambda - \delta)$. The error processor receives its input from the demodulator and integrates the error signal $(\lambda - \delta)$ which then drives a Voltage-Controlled Oscillator (VCO).

Functionally, the up-down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a type II tracking servo. In a type II servo the VCO

always settles to the counting rate which makes the $d\delta/dt$ equal to $d\lambda/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

POWER OSCILLATOR

The DTC-19300 contains an internal power oscillator. The OSC output (pin 19) can be programmed for voltage and frequency. The default output voltage is 2.7 Vrms, scalable down with an external resistor R3 connected between RM (pin 20) and V (pin 25). The default frequency is 5 kHz, tunable to 400 Hz with an external resistor R4 connected between RF1 (pin 21) and RF2 (pin 22). If desired, an external oscillator can be used in place of the internal oscillator.

SOLID STATE BUFFERED INPUTS

The signal and reference inputs are voltage follower inputs with high impedance that do not load the LVDT. The maximum transient peak voltage should not exceed 100 V.

DIGITAL INTERFACE

The digital interface circuitry has three main functions:

1. latch the output bits during an Inhibit (\overline{INH}) command allowing stable data to be read out of the DTC-19300
2. furnish parallel tri-state data formats
3. act as a buffer between the internal CMOS logic and the external TTL logic

In the DTC-19300, applying an INHIBIT (\overline{INH}) command will lock the data in the Output Transparent Latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital position always updates, and the INHIBIT can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and

the 50 ns delay are part of the Inhibit circuitry. For further information, see the INHIBIT ($\overline{\text{INH}}$, PIN 17) paragraph.

LOGIC OUTPUT

Logic outputs from the DTC-19300 consist of the LVDT core's digital position in 12 or 14 parallel data bits. All logic outputs are short-circuit proof to ground and +5 V. The internal Timing signal (T) is a positive, 0.4 to 0.7 μs pulse. Data changes approximately 50 ns after the leading edge of T, and the position is determined by the sum of the bits at logic 1. Digital outputs are three-state and are provided in two bytes: bits 1 through 6 (MSBs) which are enabled by the signal EM, and bits 7 through 14 (LSBs) which are enabled by the signal EL. Outputs are valid (logic 1 or 0) 150 ns maximum after setting EM or EL low, and are high impedance within 100 ns maximum of setting EM or EL high. Both EM and EL are internally pulled-up to +5 V at 100 nA maximum.

INHIBIT ($\overline{\text{INH}}$, PIN 17)

The $\overline{\text{INH}}$ input locks the Output Transparent Latch (See FIGURE 1) so the bits will remain stable while data is being transferred. The output is stable 0.5 μs after $\overline{\text{INH}}$ is driven to logic 0.

A logic 0 applied to the T input latches data, and a logic 1 applied to T allows the bits to change. The Inhibit Transparent Latch prevents the transmission of invalid data when there is an overlap between T (VCO clock to up-down counter) and $\overline{\text{INH}}$. While the counter is not being updated, T is at a logic 0 and the Inhibit Latch is transparent. When T goes to a logic 1, the Inhibit Latch is locked. If T occurs after $\overline{\text{INH}}$ has been applied, the latch will remain locked and its data will not change until T returns to logic 0; if $\overline{\text{INH}}$ is applied during T, the latch will not lock until the T pulse is a logic 0. The purpose of the 50 ns delay is to prevent a race condition between T and $\overline{\text{INH}}$ where the up-down counter begins to change as an $\overline{\text{INH}}$ is applied.

FIGURE 2 illustrates the Inhibit Timing. Whenever an input position change occurs, the converter changes the digital position in 1 LSB steps and generates a T pulse, delayed by 50 ns, nominal. Valid data is available at the outputs 0.2 μs after the leading

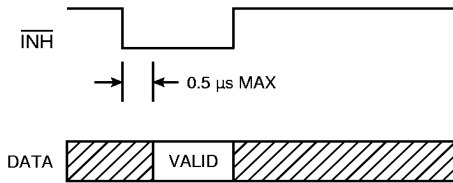


FIGURE 2. INHIBIT TIMING

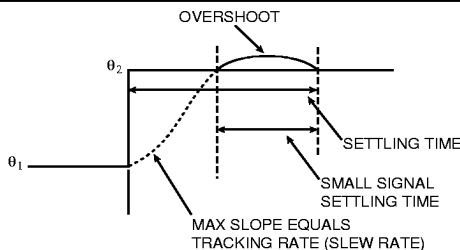


FIGURE 3. RESPONSE TO A STEP INPUT

edge of T. An $\overline{\text{INH}}$ input, regardless of its duration, does not affect the converter update.

A simple method of interfacing to a computer is:

1. apply $\overline{\text{INH}}$
2. wait 0.5 μs minimum
3. transfer data and release $\overline{\text{INH}}$

As long as the converter's maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as when power is initially applied, the response will be critically damped. FIGURE 3 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (inherent in a type II servo). The overshoot settling to final value is a function of the small signal settling to final value.

BUILT-IN-TEST ($\overline{\text{BIT}}$, PIN 18)

The $\overline{\text{BIT}}$ output monitors the level of the demodulator (D). If D exceeds approximately 65 bits, the logic level at $\overline{\text{BIT}}$ will change from logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{\text{BIT}}$ will also be set for an over-velocity condition because the converter loop cannot maintain input-output sync, or if the converter malfunctions where it cannot maintain the loop at a null.

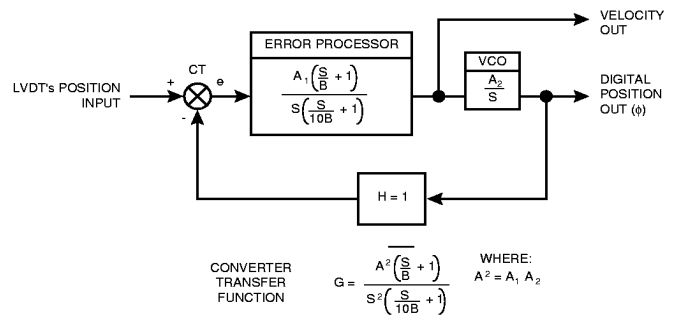


FIGURE 4. CONTROL LOOP BLOCK DIAGRAM

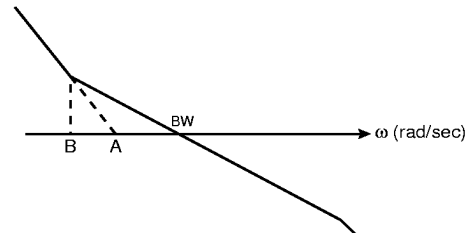


FIGURE 5. OPEN LOOP BODE PLOT

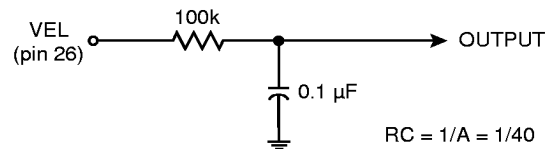
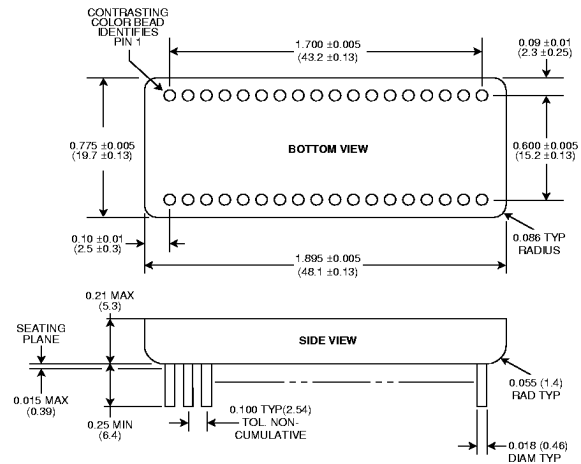


FIGURE 6. VELOCITY FILTER

BIT	WEIGHT
1 (MSB)	0.5 full range = FS
2	0.25 full range = HS
3	0.125 full range
4	0.0625 full range
5	0.03125 full range
6	0.015625 full range
7	0.0078125 full range
8	0.0039063 full range
9	0.0019531 full range
10	0.0009766 full range
11	0.0004883 full range
12	0.0002441 full range
13	0.0001221 full range
14 (LSB)	0.0000610 full range



- Notes:
1. Dimensions are in inches (millimeters).
 2. Lead identification numbers are for reference only.
 3. Lead clusters shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
 4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
 5. Case is electrically floating.

FIGURE 8. DTC-19300 MECHANICAL OUTLINE

PIN NO.	TITLE	I/O	FUNCTION
1	\overline{EM}	I	Enable MSBs. Logic 0 enables digital output bits 1-6. Logic 1 disables these bits.
2	1	O	Digital Output Bit 1 (MSB all modes).
3	2	O	Digital Output Bit 2.
4	3	O	Digital Output Bit 3.
5	4	O	Digital Output Bit 4.
6	5	O	Digital Output Bit 5.
7	6	O	Digital Output Bit 6.
8	7	O	Digital Output Bit 7.
9	8	O	Digital Output Bit 8.
10	9	O	Digital Output Bit 9.
11	10	O	Digital Output Bit 10.
12	11	O	Digital Output Bit 11.
13	12	O	Digital Output Bit 12 (LSB 12 Bit Mode).
14	13	O	Digital Output Bit 13.
15	14	O	Digital Output Bit 14 (LSB 14 Bit Mode).
16	\overline{EL}	I	Enable LSBs. Logic 0 enables digital output bits 7-14. Logic 1 disables these bits.
17	\overline{INH}	I	Inhibit. Output valid 0.5 μ s after \overline{INH} is logic 0.
18	\overline{BIT}	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds approximately 65 bits.
19	OSC	O	Power oscillator output.
20	RM	I	Reference Magnitude. Power amplifier amplitude adjust.
21	RF1	I	Reference Frequency. Power amplifier frequency adjust.
22	RF2	I	Reference Frequency. Power amplifier frequency adjust.
23	A	I	Resolution Control. Sets resolution to 12 or 14 bits. Set for 14 bit mode by connecting the \overline{BIT} (pin 18) to A (pin 23). Set for 12-bit mode by grounding A.
24	e	O	AC Error.
25	V	O	Internal DC reference voltage +5.5 V.
26	VEL	O	Velocity.
27	+15 V	I	Supply Voltage.
28	GND	—	Ground.
29	SJ	I	Summing Junction.
30	+5 V	I	Supply Voltage.
31	RO	O	Reference Out.
32	R	I	LVDT Reference input.
33	S	I	LVDT Signal input.
34	SG	I	Signal Amplifier Gain Point.
35	SO	O	Signal Amplifier Output.
36	RI	I	Full Scale Reference Input.

ORDERING INFORMATION

DTC-19300-XXXX

Supplemental Process Requirements:

- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Accuracy:

- 1 = 0.25% of Full Scale reading + 3 LSB (at room temp.)
- 2 = 0.05% of Full Scale reading + 3 LSB (at room temp.)

Process Requirements:

- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:

- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—