

Signetics

54F190, 54F191 Counters

T.45.23.09

54F190 Asynchronous Presettable BCD/Decade Up/Down Counter
54F191 Asynchronous Presettable 4-Bit Binary Up/Down Counter

Military FAST Products

Product Specification

FEATURES

- Synchronous, reversible counting
- BCD/decade — 54F190
4-bit binary — 54F191
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single up/down control input

DESCRIPTION

The 54F190 is an asynchronous presettable up/down BCD decade counter. It

contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The 54F191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data Inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load (PL) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

ORDERING INFORMATION

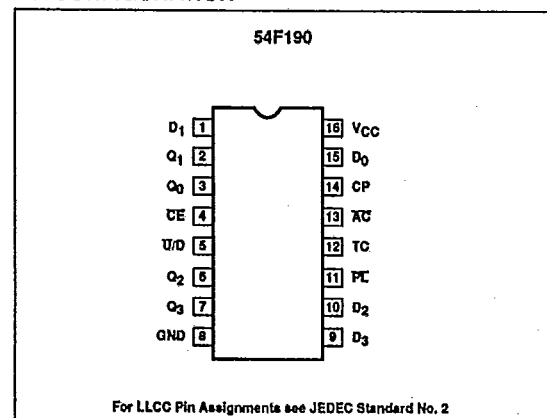
DESCRIPTION	ORDER CODE
Ceramic DIP	54F190/BEA 54F191/BEA
Ceramic Flat Pack	54F190/BFA 54F191/BFA
Ceramic LLCC	54F190/B2A 54F191/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

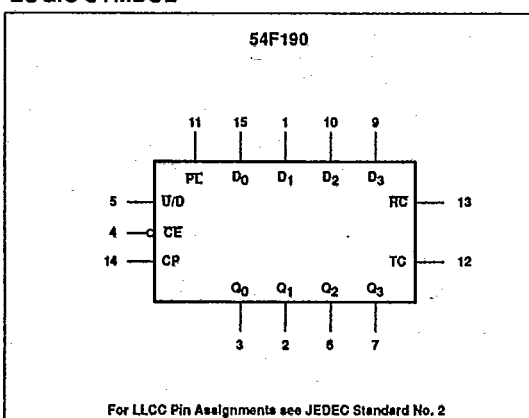
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CE	Count enable input (active low)	1.0/3.0	20 μ A/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
$D_0 - D_3$	Parallel data inputs	1.0/1.0	20 μ A/0.6mA
PL	Asynchronous parallel load input (active low)	1.0/1.0	20 μ A/0.6mA
U/D	Up/down count control input	1.0/1.0	20 μ A/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
RC	Ripple clock output (active low)	50/33	1.0mA/20mA
TC	Terminal count output (active high)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL

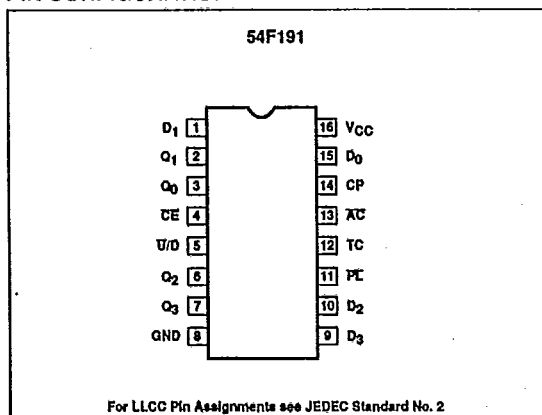


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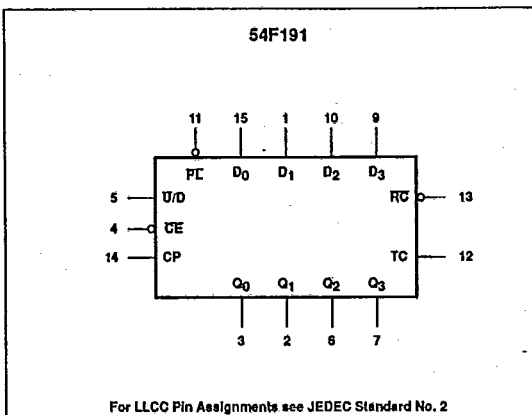
Counters

54F190, 54F191

PIN CONFIGURATION



LOGIC SYMBOL



Counting is inhibited by a High level on the Count Enable (CE) input. When CE is Low, internal state changes are initiated.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock (RC). The TC output is normally Low and goes High when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 54F190 and reaches "15" in the count-up mode for 54F191. The TC output will remain High until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the RC output. When TC is High and CE is Low, the RC follows the Clock Pulse (CP) delayed by two gate delays. The RC output essentially duplicates the Low clock pulse width, although

delayed in time by two gate delays. This feature simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each RC output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on CE inhibits the RC output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

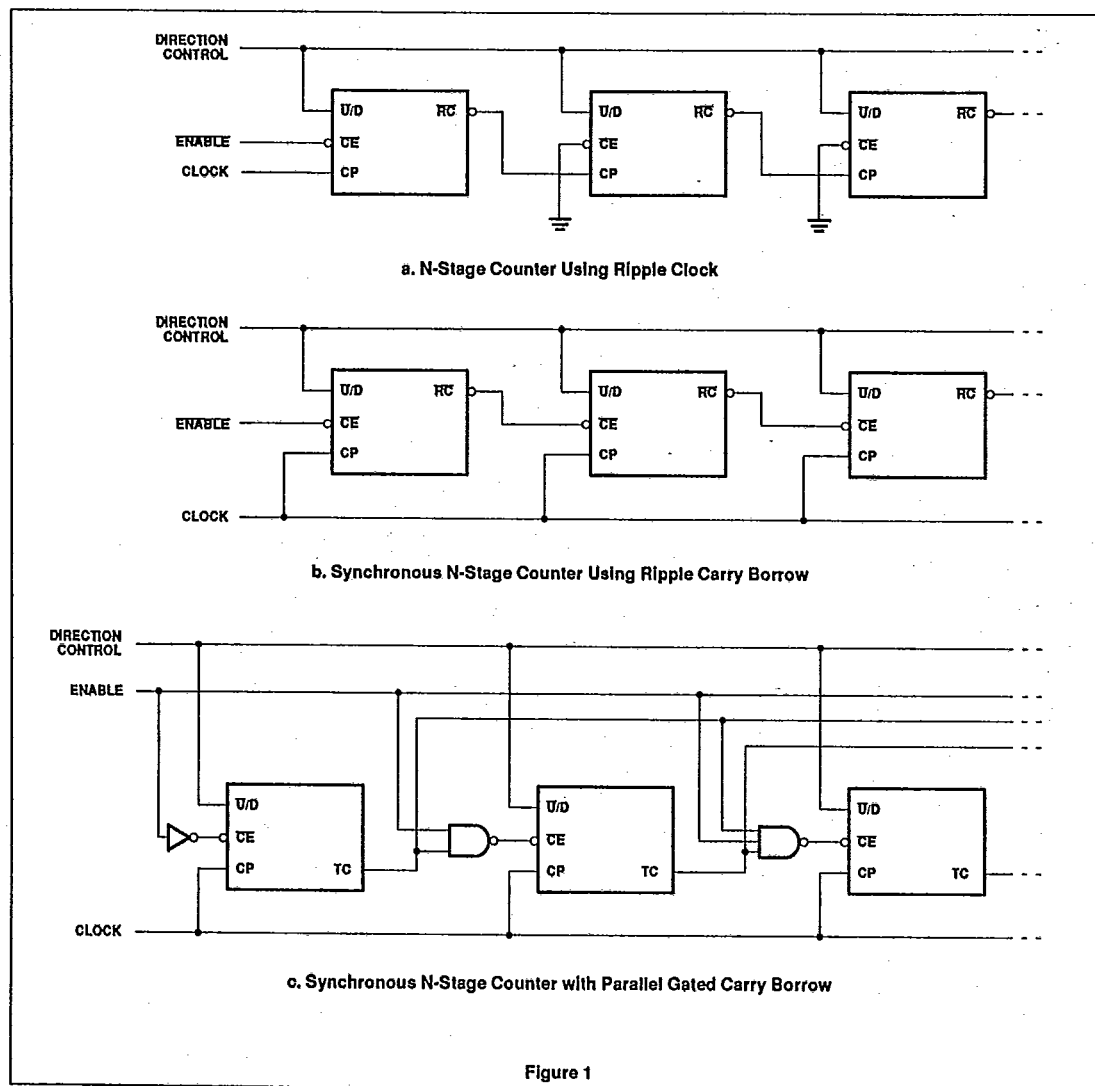
Figure 1b shows a method of causing state changes to occur simultaneously in all stages.

The RC outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the RC output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the CE input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own CE, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.

Counters

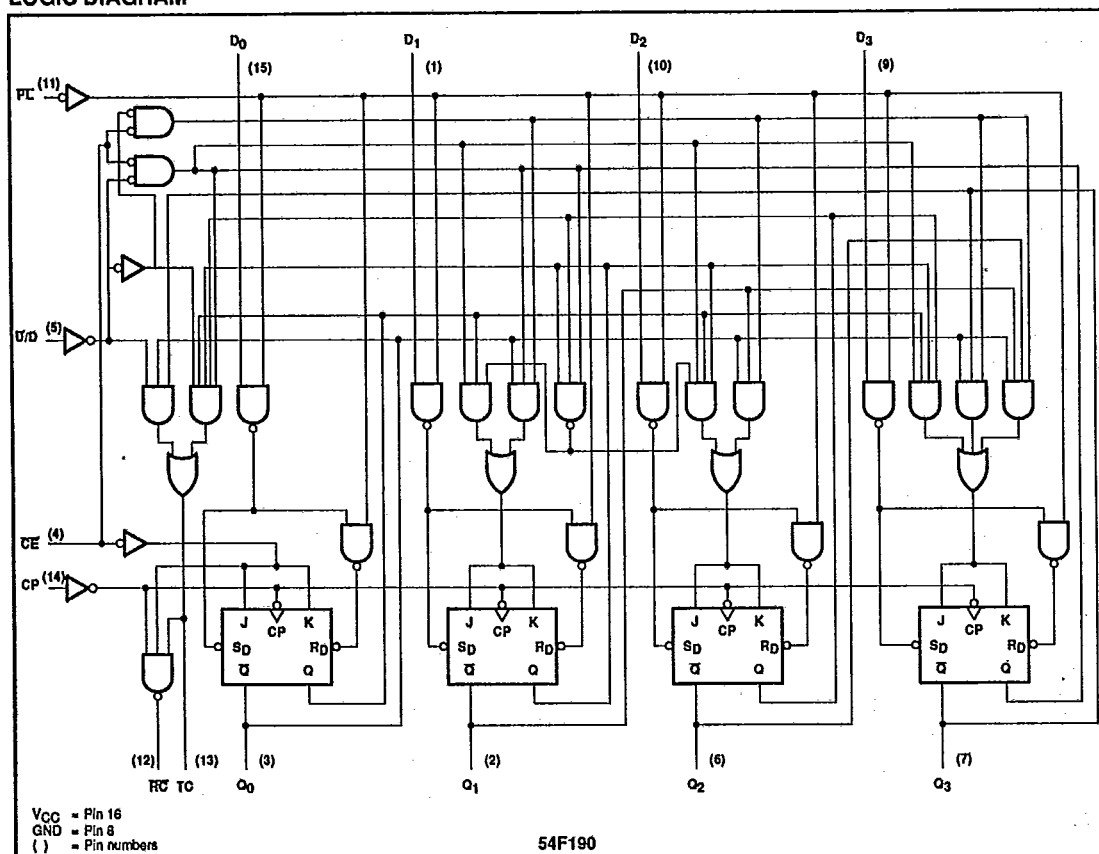
54F190, 54F191



Counters

54F190, 54F191

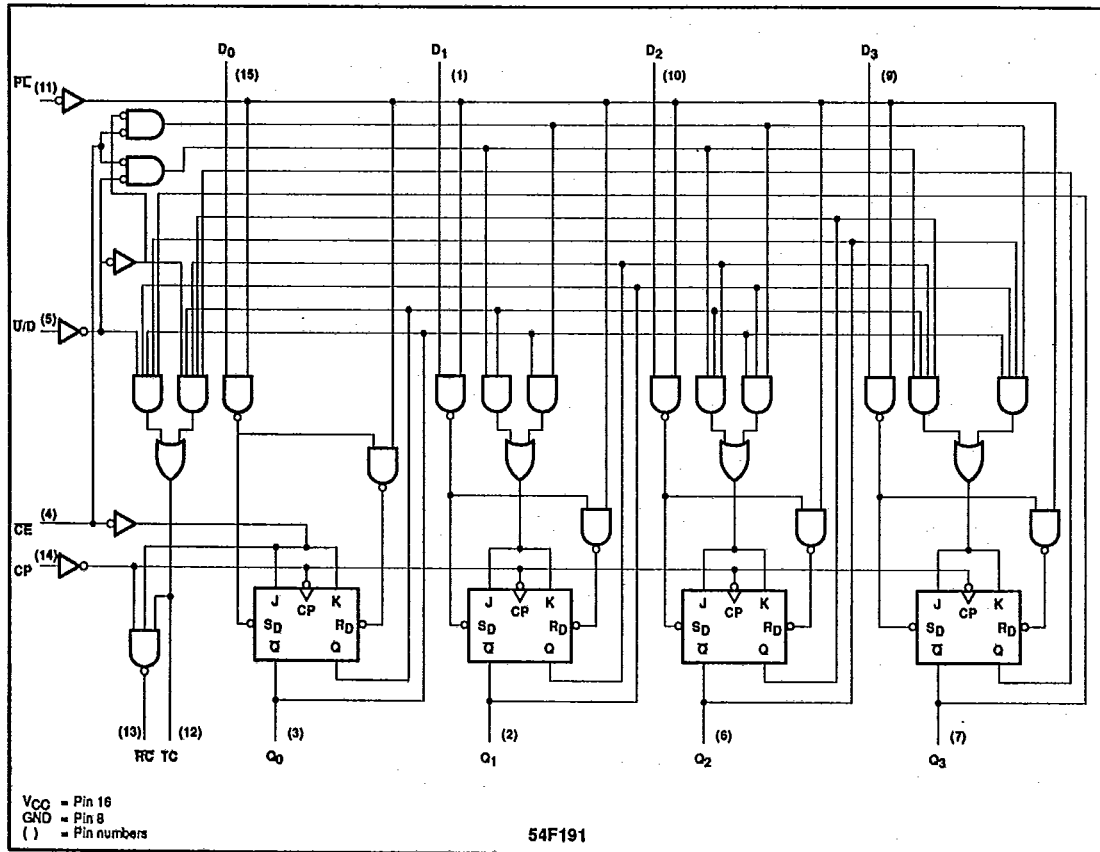
LOGIC DIAGRAM



Counters

54F190, 54F191

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE, 54F190, 54F191

OPERATING MODE	INPUTS					OUTPUTS
	PL	U/D	CE	CP	D _n	Q _n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	I	↑	X	count up
Count down	H	H	I	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

Counters

54F190, 54F191

TC AND RC FUNCTION TABLE, 54F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	CE	CP	Q ₀	Q ₁	Q ₂	Q ₃	TC	RC
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	↑	H	X	X	H	↓	↑
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	↑	L	L	L	L	↓	↑

TC AND RC FUNCTION TABLE, 54F191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	CE	CP	Q ₀	Q ₁	Q ₂	Q ₃	TC	RC
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	↑	H	H	H	H	↓	↑
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	↑	L	L	L	L	↓	↑

H = High voltage level steady state

L = Low voltage level steady state

↑ = Low voltage level one set-up time prior to Low-to-High clock transition

X = Don't care

↑ = Low-to-High clock transition

↑ = Low pulse

↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5.0	mA
V _O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _H	High-level input voltage	2.0			V
V _L	Low-level input voltage			0.8	V
I _K	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	-55		+125	°C

Counters

54F190, 54F191

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OL} = Max, V _{IH} = Min		0.35	0.50	V
V _K	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{H2}	Input current at maximum input voltage	V _{CC} = Max, V _I = 7.0V			0.3	mA
					0.1	mA
I _{H1}	High-level input current	V _{CC} = Max, V _I = 2.7V			60	μA
					20	μA
I _L	Low-level input current	V _{CC} = Max, V _I = 0.5V			-1.8	mA
					-0.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = Max	-60		-150	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		38	55	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			Min	Typ	Max	Min	Max		
t _{MAX}	Maximum clock frequency (Q _n)	Waveform 1	100	125		80 ⁵		MHz	
f _{MAX}	Maximum clock frequency (RC)	Waveform 2	85	95		75 ⁵		MHz	
t _{PLH} t _{PHL}	Propagation delay CP to Q _n	Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.5	ns ns	
t _{PLH} t _{PHL}	Propagation delay CP to TC	Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay CP to RC	Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay CE to RC	Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay U/D to RC	Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay U/D to TC	Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n	Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.5	ns ns	
t _{PLH} t _{PHL}	Propagation delay PL to Q _n	Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	11.0 12.5	ns ns	
t _{PLH} t _{PHL}	Propagation delay D _n to RC	Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	21.0 15.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay D _n to TC	Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay PL to TC	Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	14.5 15.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay PL to RC	Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	22.0 14.5	ns ns	

Counters

54F190, 54F191

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low D _n to PC	Waveform 6	4.5 4.5			5.0 6.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low D _n to PC	Waveform 6	2.0 2.0			2.0 3.0		ns ns
t _s (L)	Setup time, High or Low CE to CP	Waveform 6	10.0			10.0		ns
t _h (L)	Hold time, High or Low CE to CP	Waveform 6	0			0.5		ns
t _s (H) t _s (L)	Setup time, High or Low U/D to CP	Waveform 6	12.0 12.0			12.0 12.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low U/D to CP	Waveform 6	0 0			0 0		ns ns
t _w (L)	PC Pulse width	Waveform 5	6.0			6.0		ns
t _w (H) t _w (L)	CP Pulse width	Waveform 1	3.5 6.0			3.5 6.0		ns ns
t _{rec}	Recovery time, PC to CP	Waveform 5	6.0			8.0		ns

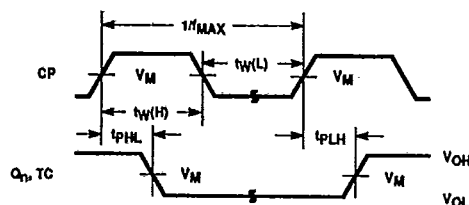
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

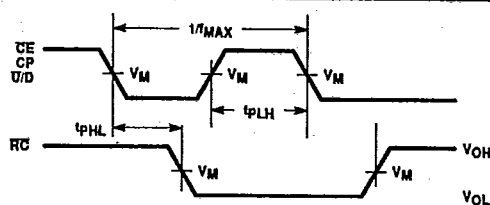
Counters

54F190, 54F191

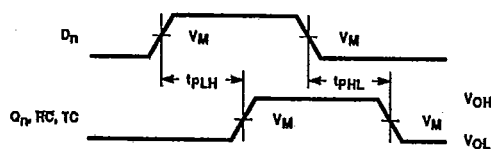
AC WAVEFORMS



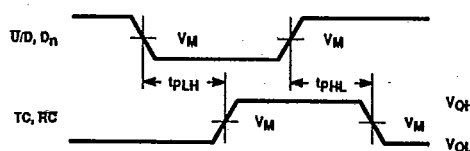
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency.



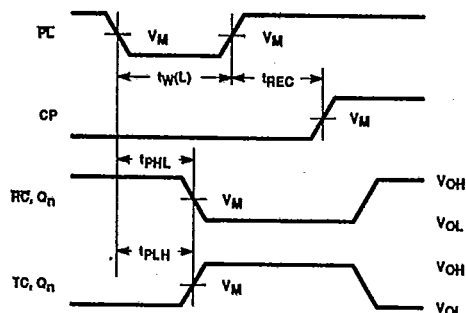
Waveform 2. Propagation Delay, Clock or Clock Enable to Ripple Clock Output and Maximum Clock Frequency



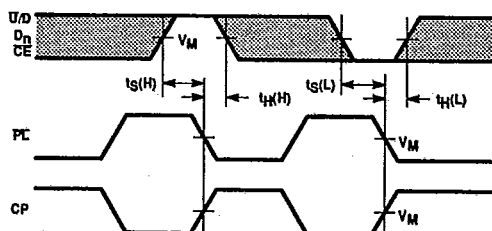
Waveform 3. Non-Inverting Propagation Delays



Waveform 4. Inverting Propagation Delay



Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time

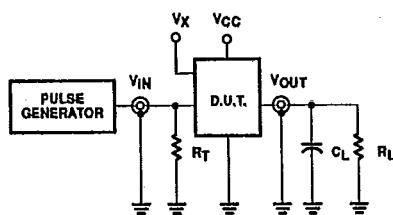
Waveform 6. Set-Up Time and Hold Time for D_n to PL , U/D to CP and CE to CP $V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable performance.

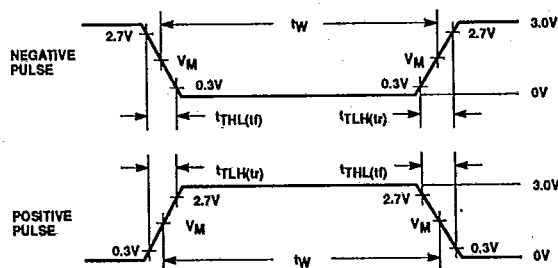
Counters

54F190, 54F191

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



VM = 1.5V

Input Pulse Definition

DEFINITIONS:

- RL = Load Resistor; see AC Characteristics for value.
- CL = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- RT = Termination resistance should be equal to ZOUT of pulse generators.
- VX = Undocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	tPLH	tPHL
54F	1MHz	500ns	≤2.5ns	≤2.5ns