

54AC11802, 74AC11802 TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS

D3593, JULY 1990

- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

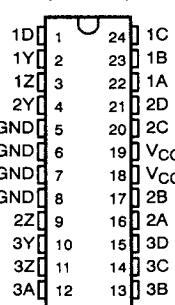
The 'AC11802 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic $Y = A + B + C + D$ and $Z = \overline{A} + \overline{B} + \overline{C} + \overline{D}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54AC11802 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11802 is characterized for operation from -40°C to 85°C .

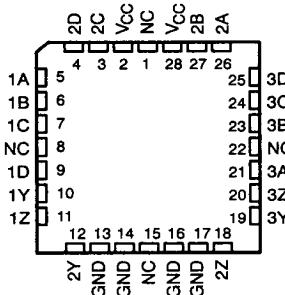
FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y	Z
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	L	H

54AC11802... JT PACKAGE
74AC11802... DW OR NT PACKAGE
(TOP VIEW)



54AC11802... FK PACKAGE
(TOP VIEW)



NC - No internal connection

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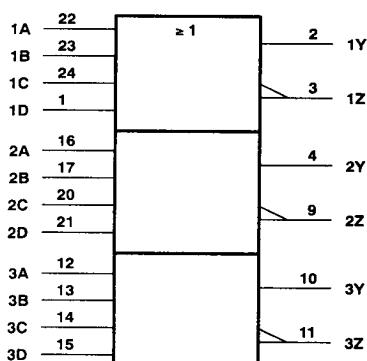


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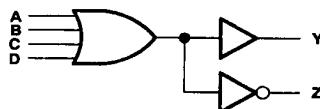
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logic symbol†



logic diagram (positive logic) (one section)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 150 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			54AC11802		74AC11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y		5.6						ns
t _{PHL}				5.1						

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			54AC11802		74AC11802		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y		3.8						ns
t _{PHL}				3.8						

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $TA = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
	C _L = 50 pF	f = 1 MHz		
C _{pd} Power dissipation capacitance per gate			27	pF

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