REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Technical changes in table I. Editorial changes throughout.	94-09-21	M. L. Poelking

REV																			
SHEET																			
REV					A	A	A	A											
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
90-09-27

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CHMOS, 16-BIT MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89982
A	67268	

SHEET 1 OF 22

DESC FORM 193
JUL 94

5962-E288-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0003903 120

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89982	01	Z	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C196KB	12 MHz CHMOS 16-bit microcontroller
02	80C196KB-12	12 MHz CHMOS 16-bit microcontroller

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Z	CMGA3-P68	68	pin grid array package
Y	see figure 1	68	leaded chip carrier package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Voltage on any pin with respect to ground	-0.5 V to +7.0 V
Storage temperature range	-65°C to +150°C
Case operating temperature range (T_C)	-55°C to +125°C
Power dissipation (P_D)	1.5 W 1/
Lead temperature (soldering 10 seconds)	265°C
Junction temperature (T_J)	150°C
Thermal resistance, junction-to-case (Θ_{JC}):	See MIL-STD-1835

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C 2/
Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Digital circuit ground (V_{SS})	0.0 V dc
Analog supply voltage (V_{REF})	4.5 V dc to 5.5 V dc
Frequency of operation (f_O)	3.5 to 12 MHz
High level input voltage:	
Excluding XTAL1, RESET (V_{IH})	1.9 V dc to 6.0 V dc
XTAL1 (V_{IH1})	3.15 V dc to 6.0 V dc
RESET (V_{IH2})	2.2 V dc to 6.0 V dc
Low level input voltage (V_{IL})	-0.5 V dc to 0.8 V dc

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2/ Case temperatures are "instant on".

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All	-0.5	0.8	V
Input high voltage (all except RESET and XTAL1)	V_{IH}			01	$0.2V_{CC}$ +1.0	V_{CC} +0.5	V
				02	$0.2V_{CC}$ +1.1	V_{CC}+0.5	
Input high voltage XTAL1	V_{IH1}			All	0.7 V_{CC}	V_{CC} +0.5	V
Input high voltage on RESET	V_{IH2}			All	2.2	V_{CC}+0.5	V
Output low voltage	V_{OL}	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA		All		0.3 0.45 1.5	V
Output high voltage (standard outputs)	V_{OH}	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA		All	V_{CC} 0.3 V_{CC} 0.7 V_{CC} 1.5		V
Output high voltage (quasi-bidirectional outputs)	V_{OH1}	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA		All	V_{CC} -0.3 V_{CC} -0.7 V_{CC} -1.5		V
Input leakage current (standard inputs)	I_{LI}	$0.0 \le V_{IN} \le V_{CC}$ -0.3 V		All		±10	µA
Input leakage current (port 0)	I_{LI1}	$0.0 \le V_{IN} \le V_{REF}$		All		±3	
1 to 0 transition current (QBD) pins	I_{TL}	V_{IN} = 2.0 V		01		-650	
				02		-800	
Logical 0 input current (QBD) pins	I_{IL}	V_{IN} = 0.45 V		All		-50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Logical 0 input current in RESET (ALE, RD, WR, BHE, INST, P2.0	I_{IL1}	V_{IN} = 0.45 2/	1, 2, 3	01		-850	mA
				02		-7	
Active mode current RESET	I_{CC}	XTAL1 = 12MHz $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V		All		60	mA
A/D converter reference current	I_{REF}			All		5	
Idle mode current	I_{IDLE}	XTAL1 = 12 MHz $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V		01		22	
				02		25	
Active mode current	I_{CC1}	XTAL1 = 3.5 MHz		01		22	
				02		30	
Power down mode current	I_{PD}	XTAL1 = 12MHz $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V		All		50	µA
Reset pull-up resistor	R_{RST}		4, 5, 6	All	6K	50K	Ω
Pin capacitance (any pin to V_{SS})	C_S	f_{TEST} = 1.0 MHz see 4.3.1c	4	All		10	pF
Address valid to READY setup	t_{AVYV}	Capacitance load on all pins = 100 pF, rise and fall time = 10 ns, f_{OSC} = 12 MHz, see figure 4	9, 10, 11	All		$2t_{OSC}$-85	ns
ALE low to READY setup	t_{LLYV}			All		t_{OSC}-75	
Non READY time	t_{YLYH}			All	No upper limit		
READY hold after CLKOUT low	t_{CYLX}			All	0	t_{OSC}-30	
READY hold after ALE low	t_{LLYX}			All	t_{OSC}-15	$2t_{OSC}$-40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Address valid to BUS WIDTH setup	t_{AVGV}	Capacitive load on all pins = 100 pF, rise and fall time = 10 ns, f_{OSC} = 12 MHz, see figure 4	9, 10, 11	All		$2t_{OSC}-85$	ns
ALE low to BUS WIDTH setup	t_{LLGV}			All		$t_{OSC}-70$	ns
BUS WIDTH hold after CLKOUT low	t_{CLGX}			All	0		ns
Address valid to input data valid	t_{AVDV}			All		$3t_{OSC}-67$	ns
RD active to input data valid	t_{RLDV}			All		$t_{OSC}-23$	ns
CLKOUT low to input data valid	t_{CLDV}			All		$t_{OSC}-50$	ns
End of RD to input data float	t_{RHDZ}			All		$t_{OSC}-20$	ns
Data hold after RD inactive	t_{RXDX}			All	0		ns
Frequency on XTAL1	f_{XTAL}			All	3.5	12	MHz
$1/f_{XTAL}$	t_{OSC}			All	83	286	ns
XTAL1 high to CLKOUT high or low 3/	t_{XHCH}			01	35	110	
				02	20	110	
CLKOUT cycle time 4/	t_{CLCL}			All	$2t_{OSC}$		
CLKOUT high period	t_{CHCL}				$t_{OSC}-10$	$t_{OSC}+10$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
CLKOUT falling edge to ALE rising	t_{CLLH}	Capacitive load on all pins = 100 pF, rise and fall time = 10 ns, f_{OSC} = 12 MHz See figure 4	9, 10, 11	01	-5	15	ns
				02	-10	10	
ALE high period	t_{LHLL}			All	t_{OSC}-12	t_{OSC}+12	ns
Address setup to ALE falling edge	t_{AVLL}			All	t_{OSC}-20		ns
Address hold after ALE falling edge	t_{LLAX}			All	t_{OSC}-40		ns
ALE falling edge to RD falling edge	t_{LLRL}			All	t_{OSC}-40		ns
RD low to CLKOUT falling edge	t_{RLCL}			01	5	30	ns
				02	4	25	
ALE falling edge to CLKOUT rising	t_{LLCH}			All	-15	15	ns
ALE cycle time 4/	t_{LHLH}			All	$4t_{OSC}$		ns
RD low period	t_{RLRH}			All	t_{OSC}-5		
RD rising edge to rising edge 5/	t_{RHLH}			All	t_{OSC}	t_{OSC}+25	
RD low to address float	t_{RLAZ}			All		10	
ALE falling edge to WR falling edge	t_{LLWL}			All	t_{OSC}-10		
CLKOUT low to WR falling edge	t_{CLWL}			All	0	25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Data stable to WR rising edge	t_{QVWH}	Capacitance load on all pins = 100 pF, rise and fall time = 10 ns, f_{OSC} = 12 MHz, see figure 4	9, 10, 11	All	t_{osc}-23		ns
Data hold after WR rising edge	t_{WHQX}			01	t_{osc}-10		ns
				02	t_{osc}-15		
WR rising edge to ALE rising edge 5/	t_{WHLH}			01	t_{osc}-10	t_{osc}+15	ns
				02	t_{osc}-15	t_{osc}+10	
BHE, INST holg after WR rising edge	t_{WHBX}			01	t_{osc}-10		ns
				02	t_{osc}-15		
Oscillator frequency	$1/t_{XLXL}$			All	3.5	12.0	MHz
CLKOUT high to WR rising edge	t_{CHWH}			01	-10	10	ns
				02	-5	15	
WR low period	t_{WLWH}			All	t_{osc}-30		ns
Oscillator period	t_{OP}			All	83	286	ns
High time	t_{HT}			All	32		
Low time	t_{LT}			All	32		
Rise time	t_{RT}			All		10	
Fall time	t_{FT}			All		10	
Serial port clock period (BRR ≥ 8002H) 3/	t_{XLXL}			All	$6t_{osc}$		
Serial port clock falling edge to rising edge (BRR ≥ 8002H) 3/	t_{XLXH}			All	$4t_{osc}$±50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Output data setup to clock rising edge 3/	t_{QVXH}	Capacitive load on all pins = 100 pF, rise and fall time = 10 ns, f_{OSC} = 12 MHz, See figure 4.	9, 10, 11	All	$2t_{OSC}-50$		ns
Output data hold after clock rising edge 3/	t_{XHQX}			All	$2t_{OSC}-50$		
Next output data valid after clock rising edge 3/	t_{XHQV}			All		$2t_{OSC}+50$	
Serial port clock period (BRR = 8001H) 3/	t_{XLXL}			All	$4t_{OSC}$		
Serial port clock falling edge to (BRR = 8001H) 3/	t_{XLXH}			All	$2t_{OSC}\pm50$		
Input data setup to clock rising edge 3/	t_{DVXH}			All	$t_{OSC}+50$		
Input data hold after clock rising edge 3/	t_{XHDX}			All	0		
Last clock rising to output float 3/	t_{XHQZ}			All		t_{OSC}	
Resolution		Clock prescaler on mode 2 V_{REF} = 5.120 V, XTAL1 = 12 MHz	1, 2, 3	All	256	1024 10	level bits
Absolute error				All	0	±4	LSBs
Non-linearity				All	0	±4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Differential non-linearity			1, 2, 3	All	0	±2	LSBs
Channel to channel matching				All	0	±1	LSBs
Off isolation 3/ 6/			4, 5, 6	All	-60		dB
Input resistance 3/				01	1K	5K	Ω
				02	750	1.2K	
DC input leakage			1, 2, 3	All	0	3.0	µA

1/ The following pins are active low: $\overline{\text{RESET}}$, $\overline{\text{EA}}$, ADV of ALE/$\overline{\text{ADV}}$, $\overline{\text{RD}}$ $\overline{\text{WR}}$/$\overline{\text{WRL}}$, and $\overline{\text{BHE}}$/$\overline{\text{WRH}}$. Case temperatures are instant on. QBD (quasi-bidirectional pins) include port 1, P2.6 and P2.7. Standard outputs include AD0-15, RD , WR, ALE, BHE, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, ports 3 and 4, TXD/P2.0, and RXD (in serial mode 0). The V_{OH} specifications is not valid for RESET. Ports 3 and 4 are open drain outputs. Standard inputs include HSI pins, EA, READY, BUS WIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RSTP2.4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45 V or V_{OH} is held below V_{CC} -0.7 V:
I_{OL} on output pins: 10 mA.
I_{OH} on quasi-bidirectional pins: Self limiting.
I_{OH} on standard output pins: 10 mA.
Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
During normal (non-transient) conditions, the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH}: is self limiting
HSO, P2.0, RXD, $\overline{\text{RESET}}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, WR, BHE	I_{OL}: 13 ma	I_{OH}: 11 mA
AD0-AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
RD, ALE, INST-CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

2/ Holding these pins below V_{IH} in RESET may cause the part to enter test modes.

3/ Guaranteed if not tested, to the limits specified in table I.

4/ CLKOUT is directly generated as a divide by 2 of the oscillator, ALE is directly generated as a divde by 4 of the oscillator.

5/ Assuming back-to-back bus cycles.

6/ DC to 100 KHz. Multiplexer break-before-make guaranteed.

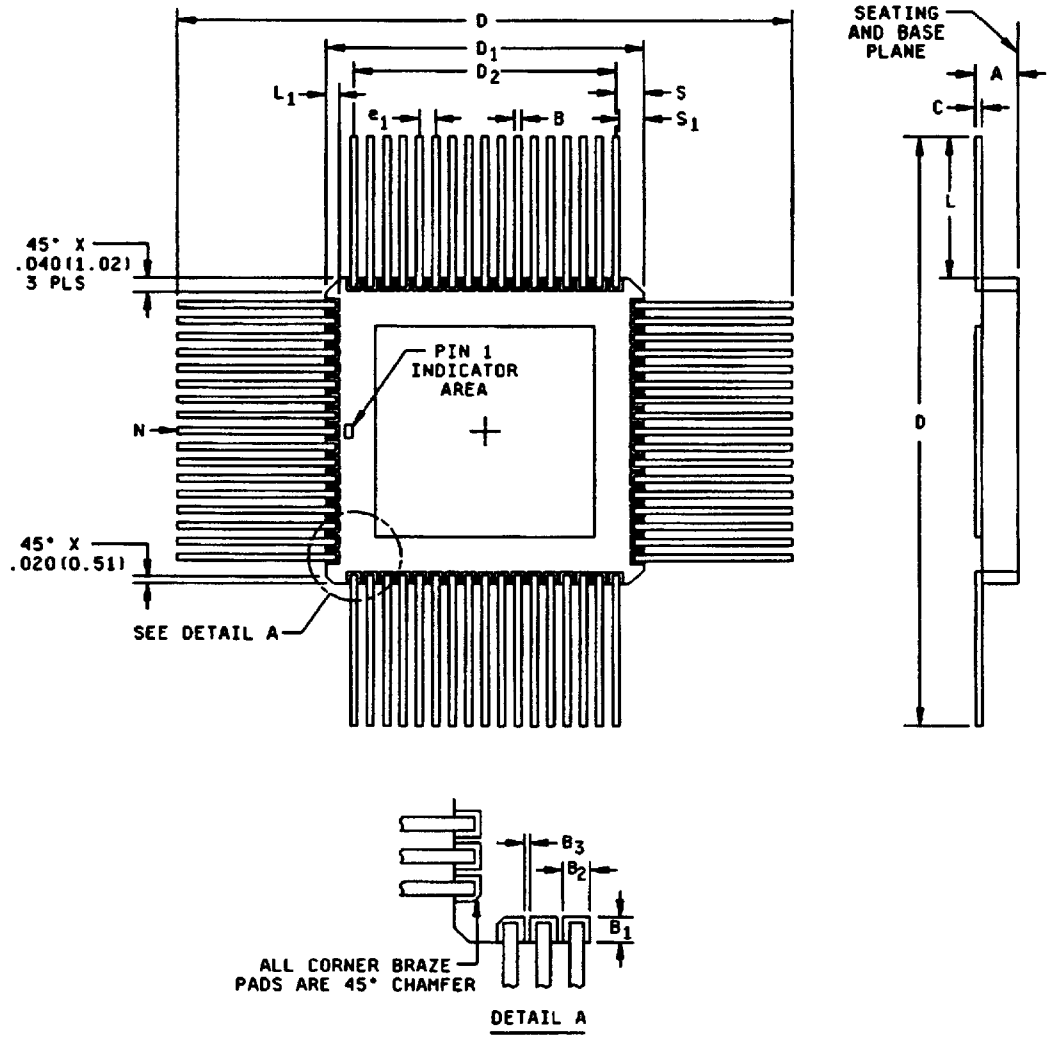

FIGURE 1. Case outline Y.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89982
		REVISION LEVEL A	SHEET 11

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.69	.080	.106
B	0.41	0.51	.016	.020
B_1	1.02	1.52	.040	.060
B_2	0.76	1.02	.030	.040
B_3	0.13	0.51	.005	.020
C	0.20	0.31	.008	.012
D	41.66	47.50	1.640	1.870
D_1	23.75	24.64	.935	.970
D_2	20.32 BSC		.800 BSC	
e1	1.27 BSC		.050 BSC	
L	9.52	11.43	.375	.450
L_1	1.02	1.52	.040	.060
N	68		68	
S	1.68	2.21	.066	.087
S_1	1.27	---	.050	---

NOTES:
1. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurements. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline Y - continued

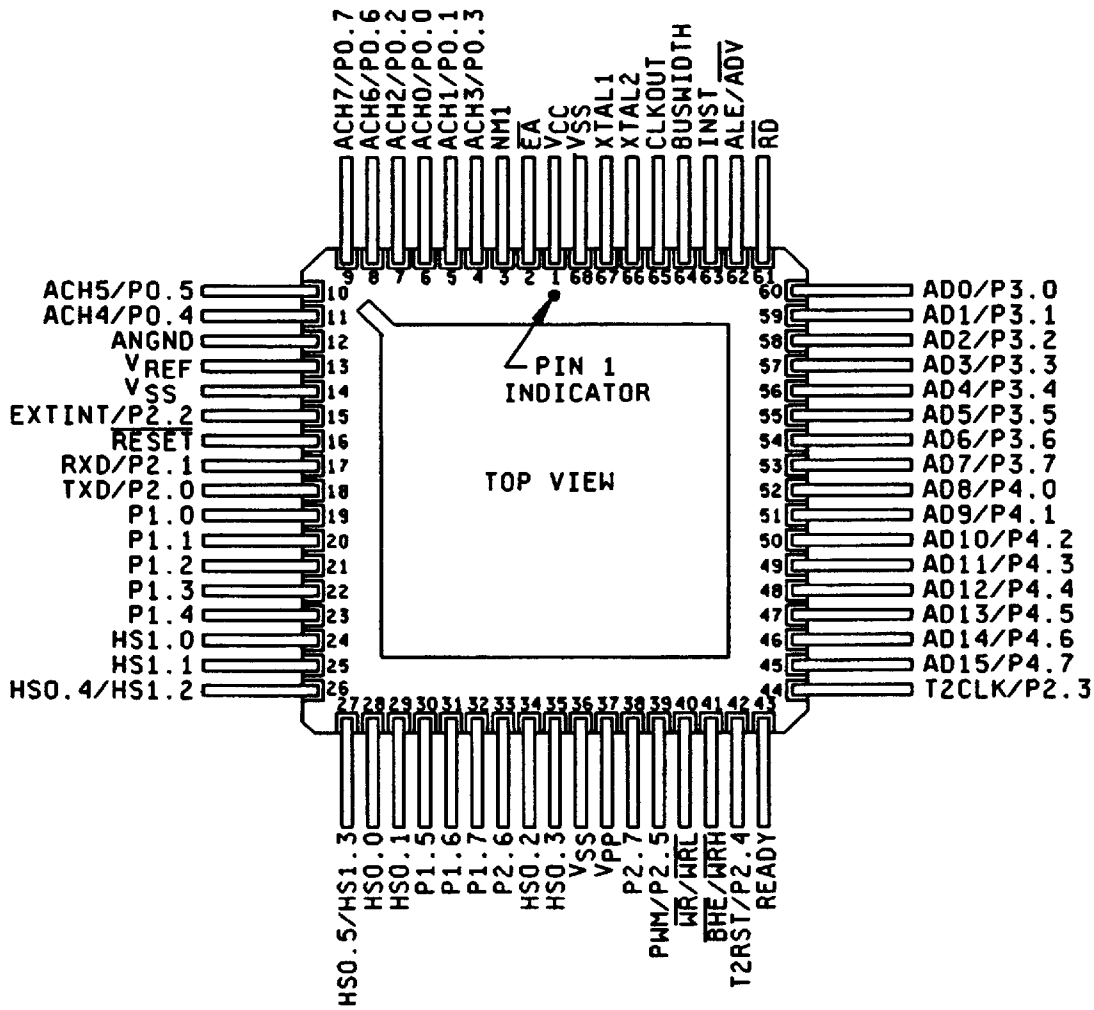

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89982
		REVISION LEVEL	SHEET 13

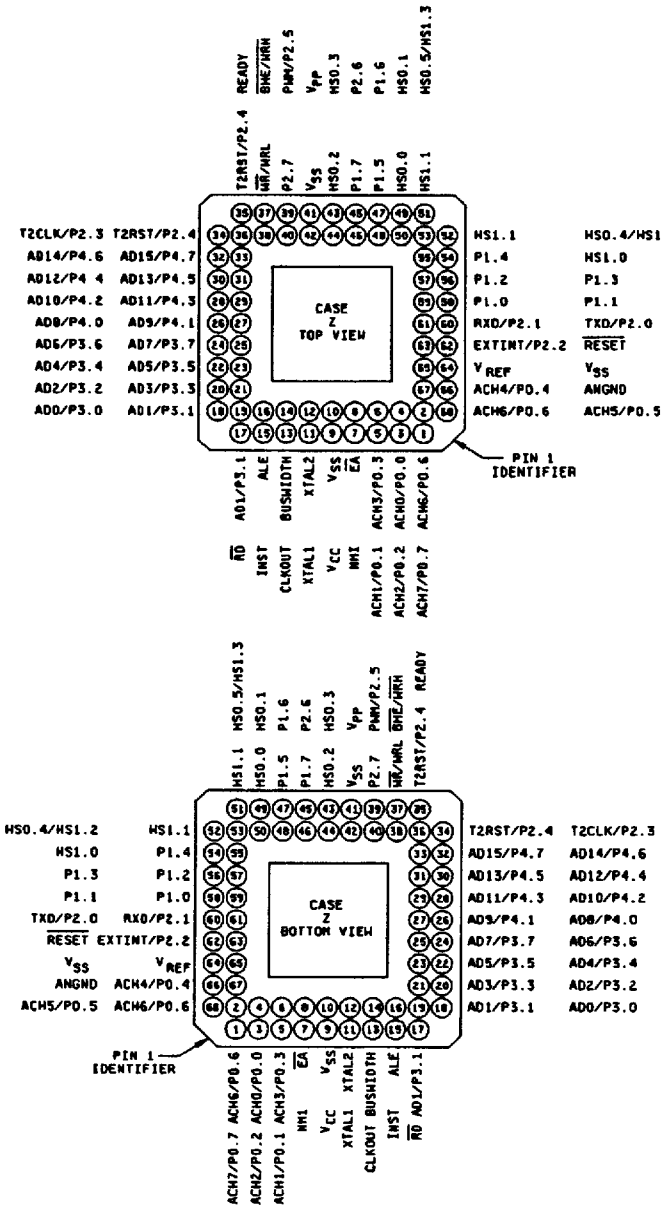

FIGURE 2. Terminal connections - continued

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89982
		REVISION LEVEL	SHEET 14

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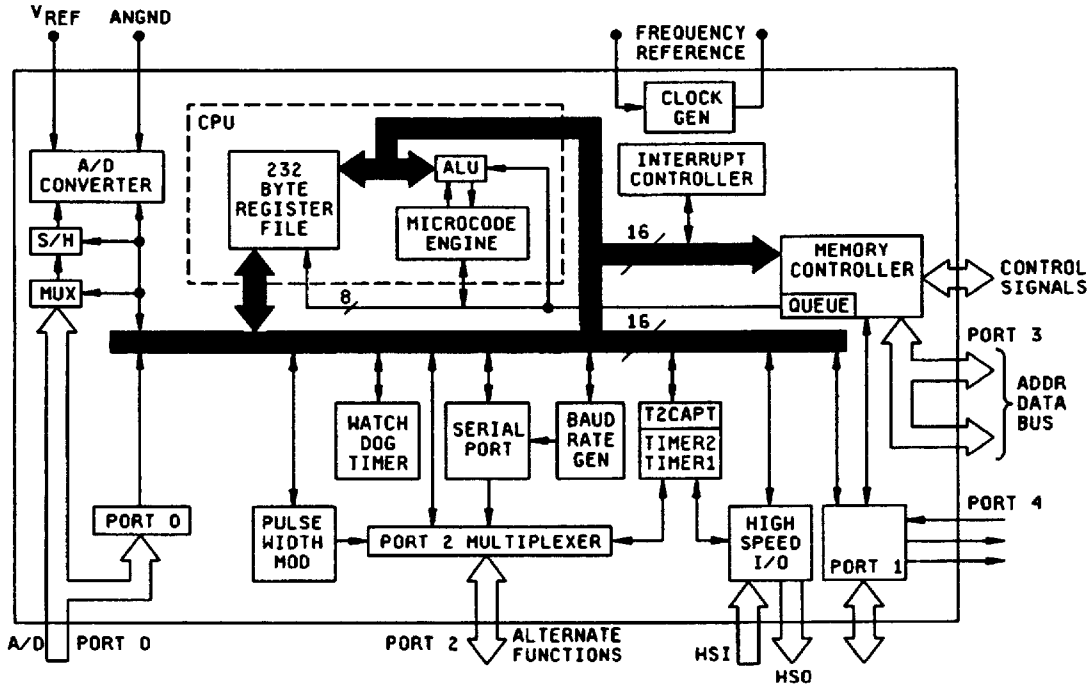
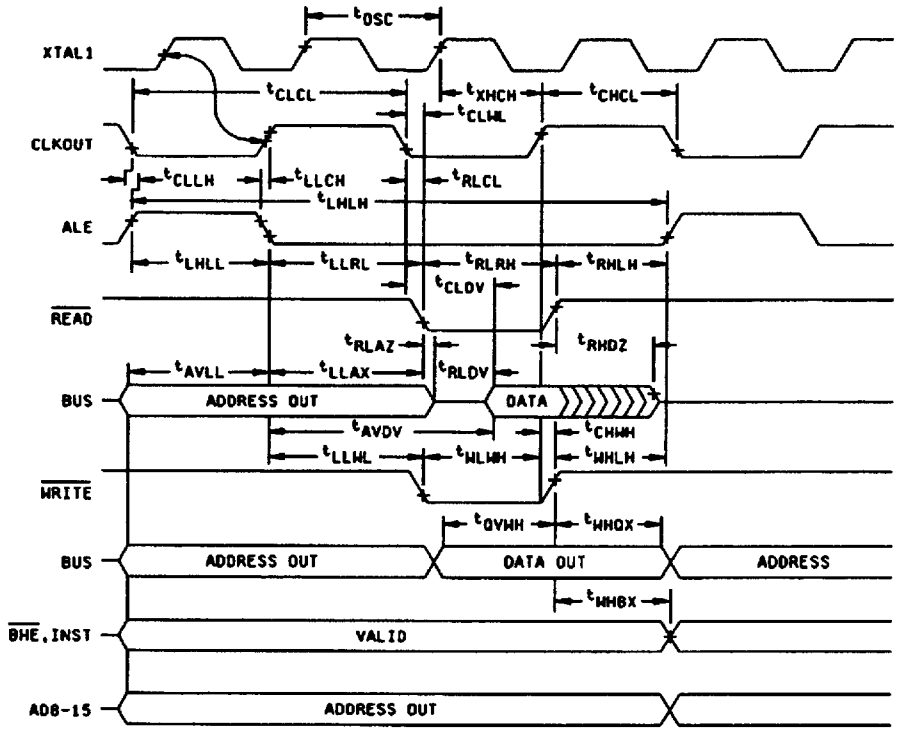
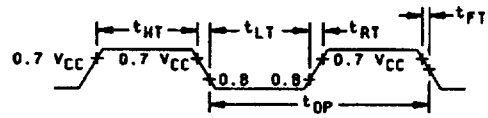
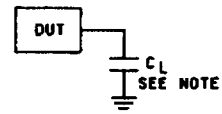


FIGURE 3. Functional block diagram.

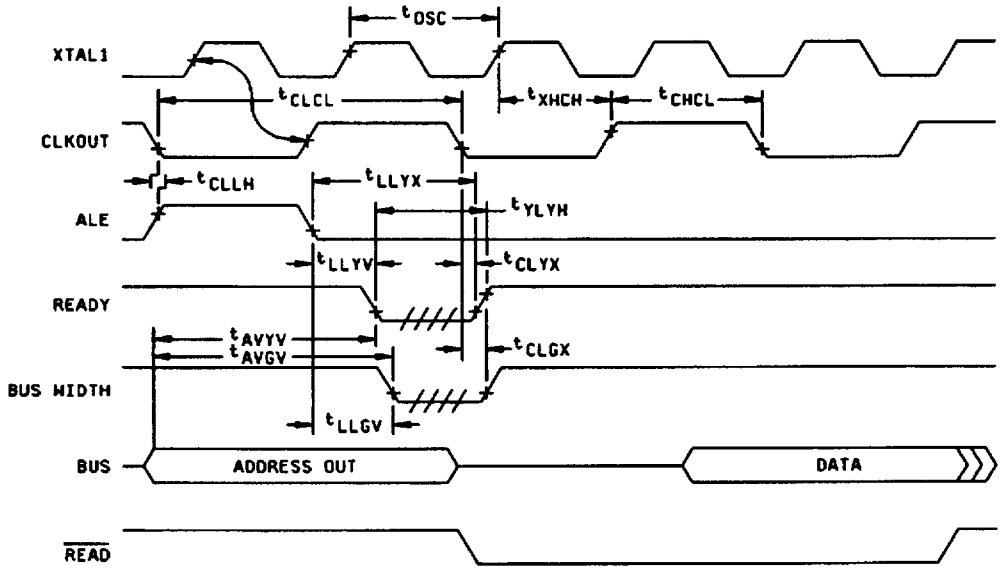






C_L = 100 pF, unless otherwise specified.

FIGURE 4. Switching waveforms and test circuit.



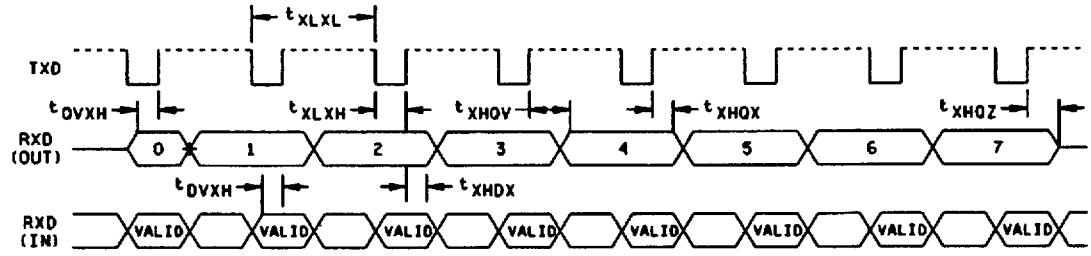
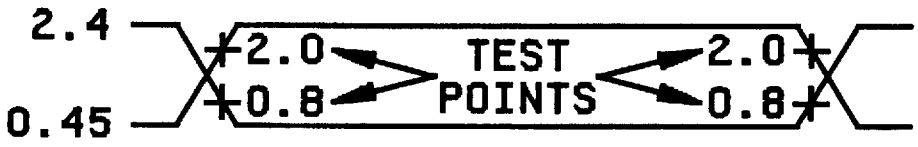


FIGURE 4. Switching waveforms and test circuit - continued



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs I_{OL}/I_{OH} ±15 mA.

FIGURE 4. Switching waveforms and test circuit - continued

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*,2,3,7*8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,7,9

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5765, or telephone (513) 296-8525.

TABLE III. Pin functions.

Pin name	Function
V_{CC}	Main supply voltage (5.0 V).
V_{SS}	Digital circuit ground (0.0 V). There are two V_{SS} pins, both must be connected.
V_{REF}	Reference voltage for the A/D converter (5.0 V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read port 0. Must be connected for A/D and port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from power down circuit. Connect this pin with a 1 µF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is one-half the oscillator frequency. It has a 50 percent duty cycle.
$\overline{\text{RESET}}$	Reset input to the chip. Input low for at least four state times to reset the chip . The subsequent low-to-high transition resynchroizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump location to location 2080H is excuted. Input high for normal operation. RESET has an internal pull-up.
BUS WIDTH	Input for BUS WIDTH selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUS WIDTH is a 1, a 16-bit bus cycle occurs. If BUS WIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	$\overline{\text{EA}}$ must be tied low. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to locations 2000H through 3FFF to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address latch enable or address valid output as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory addresses.

6.6 Pin descriptions. Microcircuits conforming to this drawing shall have pin functions as specified in table III.

TABLE III. Pin functions - continued

Pin name	Function
$\overline{RD}$	Read signal output to external memory . $\overline{RD}$ is activated only during external memory reads.
WR/$\overline{WRL}$	Write and write low output to external memory, as selected by the CCR WR will go low only for external writes where an even byte is being written. WR/WRL is actvated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus high enable or write high output to external memory, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to high byte of the data bus. AO = 0 selects the the bank of memory that is connected to the low byte of the data bus. Thus acesses to a 16-wide memory can be to the low byte only (AO = 0, $\overline{BHE}$ = 1), to the high byte only (AO = 1, $\overline{BHE}$ = 0), or both bytes (AO = 0, $\overline{BHE}$ = 0). If the WRH function is selected the pin will go low if the bus cycle is writing to an odd memory location. BHE/WRH is valid only during 16-bit external memory write cycles.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory contoller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR.
HSI	Inputs to high speed input unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2, HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO unit. The HSI pins are also used as the SID in SLAVE programming mode.
HSO	Outputs from high speed output unit. Six HSO pins are available: HSO.0, HSO.1 HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HS1 unit.
port 0	8-bit high impedance input only port. Three pins can be used as a digital inputs and /or as analog inputs to the on-chip A/D converter These pins set the programming mode.
PORT 1	8-bit quasi-bidirectional I/O port.
PORT 2	8-bit multifunctional port. All of its pins are shared with other functions in the 01 device.
PORT 3, PORT 4	8-bit bi-directional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pull-ups.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.