NCP4896

1.0 Watt Audio Power Amplifier with Earpiece Driving Capability

The NCP4896 is an audio power amplifier designed for portable communication device applications such as mobile phones. This part is capable of delivering 1.0 W of continuous average power to an 8.0 Ω BTL load from a 5.0 V power supply and, 250 mW to a 4.0 Ω BTL from 2.6 V power supply. It also provides the control of driving a single−ended earpiece and delivers 90 mW from a 5.0 V power supply to a 32 Ω load.

This device provides high quality audio while requiring few external components and minimal power consumption. It features a low−power consumption shutdown mode, which is achieved by driving the shutdown pin with logic Low.

The NCP4896 contains circuitry to prevent from “pop and click” noise that would otherwise occur during turn−on and turn−off transitions. It is also efficient when switching modes from BTL to SE and SE to BTL.

For maximum flexibility, the part provides an externally controlled gain (with resistors), as well as an externally controlled turn−on time (with bypass capacitor).

Due to its excellent PSRR, it can be directly connected to the battery, saving the use of an LDO.

Features

- Single−Ended or Differential Control
- 1.0 W to an 8.0 Ω BTL Load from a 5.0 V Power Supply
- Excellent PSRR: Direct Connection to the Battery
- Ultra Low Current Shutdown Mode
- 2.2 V−5.5 V Operation
- External Gain Configuration Capability
- External Turn−on Time Configuration Capability
- Thermal Overload Protection Circuitry
- Up to 1.0 nF Capacitive Load Driving Capability
- “Pop and Click” Noise Protection Circuit
- This is a Pb−Free Device

Typical Applications

- Portable Electronic Devices
- PDAs
- Mobile Phones

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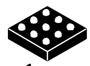
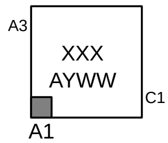
MARKING DIAGRAM

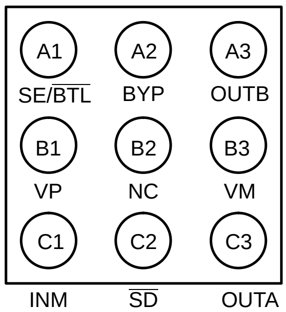


9−PIN FLIP−CHIP
FC SUFFIX
CASE 499AL



XXX	= Specific Device Code	
A	= Assembly Location	
Y	= Year	
WW	= Work Week	

PIN CONNECTIONS
9−PIN FLIP−CHIP CSP



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

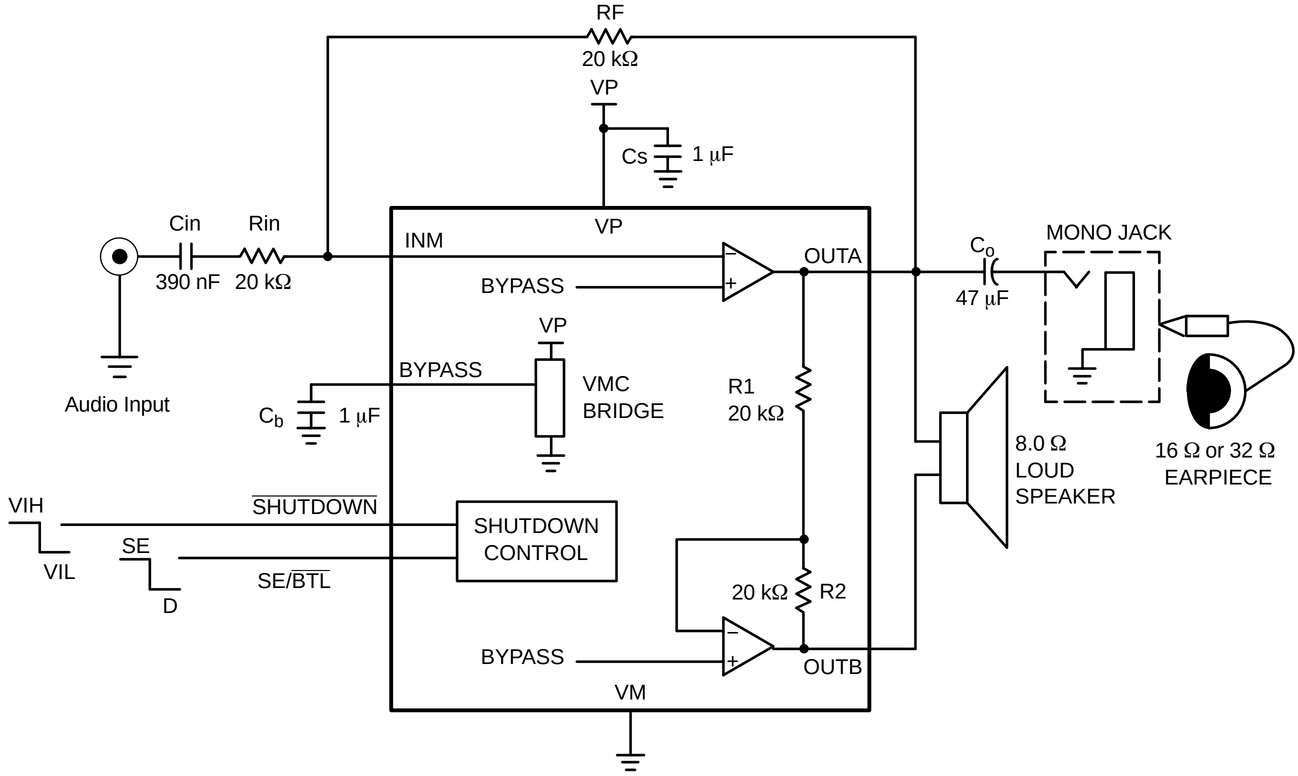


Figure 1. Typical NCP4896 Application Circuit with Single−Ended Input

PIN DESCRIPTION

Pin	Type	Symbol	Description
A1	I	SE/$\overline{\text{BTL}}$	When this pin is Low , the audio amplifier is in differential mode. If a High level is applied, the configuration is in Single−Ended Mode
A2	I	BYP	Bypass capacitor pin which provides the common mode voltage (VP/2).
A3	O	OUTB	Positive output of the amplifier. In high impedance state when the device is in Single−Ended mode.
B1	I	VP	Positive analog supply of the cell.
B2		NC	Not connected.
B3	I	VM	Ground.
C1	I	INM	Audio Input Signal.
C2	I	$\overline{\text{SD}}$	The device enters in shutdown mode when a low level is applied to this pin.
C3	O	OUTA	Negative output of the amplifier. This is the active output dedicated to a SE load when this configuration is activated.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	VP	6.0	V
Operating Supply Voltage	Op VP	2.2 to 5.5 V	−
Input Voltage	V_{in}	−0.3 to Vcc +0.3	V
Max Output Current	Iout	500	mA
Power Dissipation (Note 2)	Pd	Internally Limited	−
Operating Ambient Temperature	T_A	−40 to +85	°C
Max Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance Junction−to−Air	$R_{\theta JA}$	90 (Note 3)	°C/W
ESD Protection Human Body Model (HBM) (Note 4) Machine Model (MM) (Note 5)	−	> 2000 > 200	V
Latch Up Current at T_A = 85°C (Note 6)	−	±100 mA	−

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
2. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation.
3. For the 9−Pin Flip−Chip CSP package, the $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with a 500 mm^2 area.
4. Human Body Model, 100 pF discharge through a 1.5 kΩ resistor following specification JESD22/A114.
5. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
6. Maximum ratings per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS Limits apply for T_A between −40°C to +85°C (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Supply Quiescent Current	I_{dd}	VP = 3.0 V, No Load VP = 5.0 V, No Load $\overline{\text{BTL}}$	– –	1.7 1.8	–	mA
		VP = 3.0 V, 8.0 Ω, $\overline{\text{BTL}}$ VP = 5.0 V, 8.0 Ω, $\overline{\text{BTL}}$	– –	1.8 2.0	– 4.0	
		VP = 5.0 V, No Load, SE	–	1.0	2.5	
		VP = 5.0 V, 32 Ω, SE	–	1.1	–	mA
Common Mode Voltage	V_{cm}	–		VP/2	–	V
Shutdown Current	I_{SD}	For VP Between 2.2 V to 5.5 V $\overline{\text{SD}}$ = Low T_A = +25°C T_A = −40°C to +85°C	 – – –	 – 20 –	 – 600 2.0	 nA µA
Shutdown Voltage High	V_{SDIH}	–	1.4	–	–	V
Shutdown Voltage Low	V_{SDIL}	–	–	–	0.4	V
SE Select	$V_{BTL/SE}$	–	1.4	–	–	V
DE Select	$V_{SE/BTL}$	–	–	–	0.4	V
Turning On Time (Note 8)	T_{WU}	C_{by} = 1.0 µF	–	140	–	ms
Turning Off Time (Note 8)	T_{SD}	–	–	20	–	ms
Output Swing	$V_{loadpeak}$	VP = 3.0 V, 8.0 Ω, BTL VP = 5.0 V, 8.0 Ω, BTL	2.3 –	2.57 4.3	– –	V
		VP = 5.0 V, 32 Ω, SE	–	4.9	–	V
Rms Output Power	P_O	VP = 5.0 V, 32 Ω, SE THD + N < 0.1% VP = 5.0 V, 16 Ω, SE THD + N < 0.1% VP = 5.0 V, 8.0 Ω, BTL THD + N < 0.1%	– – –	92 176 1080	– – –	mW
Output Offset Voltage	V_{os}	For VP between 2.2 V to 5.5 V BTL and SE	−30	1.0	30	mV
Power Supply Rejection Ratio	PSRR V+	RF = Ri = 20 kΩ VP_{ripple_pp} = 200 mV C_{by} = 1.0 µF Input Terminated with 10 Ω f = 217 Hz to 1.0 khz VP = 5.0 V, 8.0 Ω, BTL VP = 3.0 V, 8.0 Ω, BTL VP = 5.0 V, 32 Ω, SE VP = 3.0 V, 32 Ω, SE	 – – – –	 −66 −67 −69 −70	 – – – –	dB
Efficiency	η	VP = 3.0 V, 8.0 Ω, BTL P_{orms} = 380 mW VP = 5.0 V, 8.0 Ω, BTL P_{orms} = 1.0 W	 – –	 64 63	 – –	%
Thermal Shutdown Temperature	T_{sd}	–	–	160	–	°C
Total Harmonic Distortion	THD + N	RF = Ri = 20 kΩ VP = 3.6 V, f = 1.0 kHz P_{out} = 400 mW, 8.0 Ω, BTL P_{out} = 40 mW, 16 Ω, BTL P_{out} = 40 mW, 32 Ω, SE	 – – –	 0.02 0.01 0.003	 – – – 	%

7. Min/Max limits are guaranteed by design, test or statistical analysis.
8. See section “Application Information” for a theoretical approach of this parameter.

TYPICAL PERFORMANCE CHARACTERISTICS

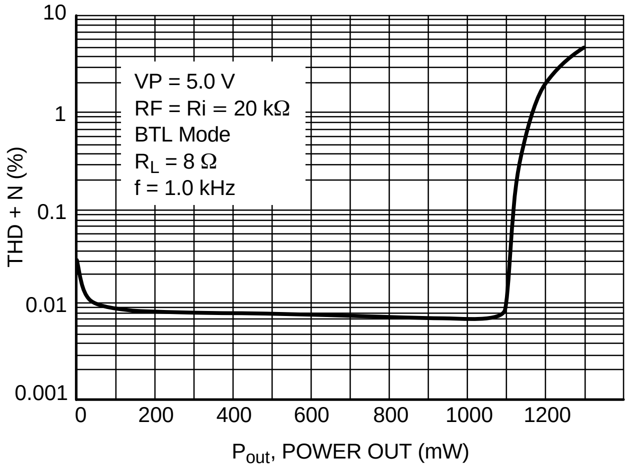


Figure 2. THD + N vs. Power Out (BTL Mode)

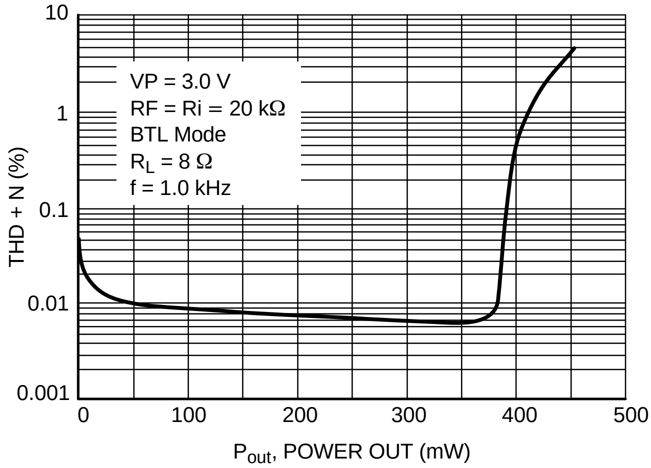


Figure 3. THD + N vs. Power Out (BTL Mode)

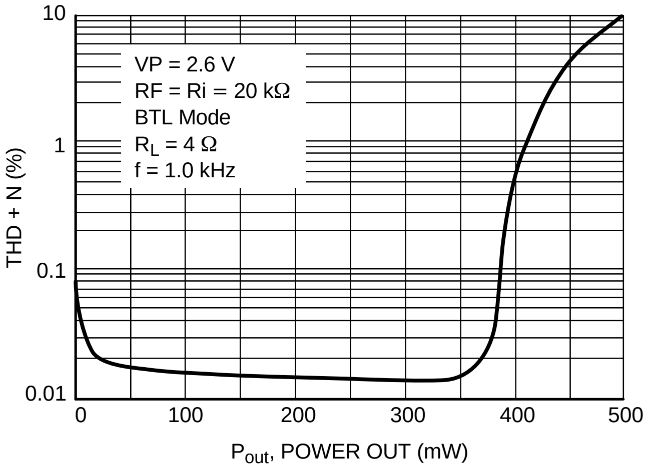


Figure 4. THD + N vs. Power Out (BTL Mode)

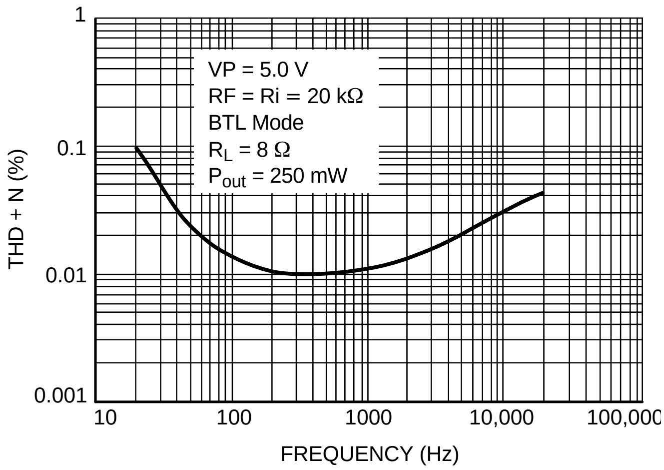


Figure 5. THD + N vs. Frequency (BTL Mode)

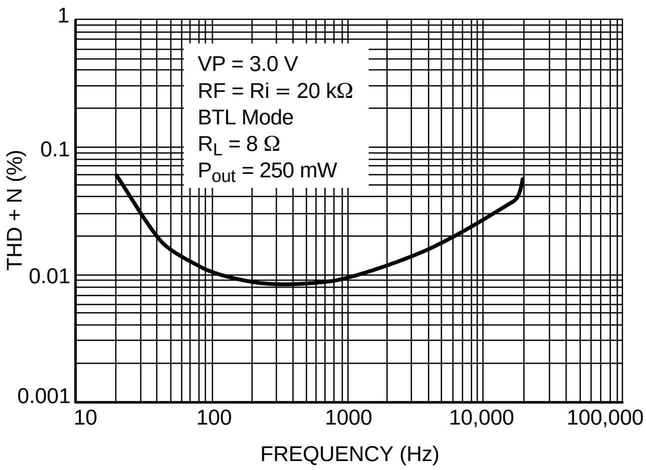


Figure 6. THD + N vs. Frequency (BTL Mode)

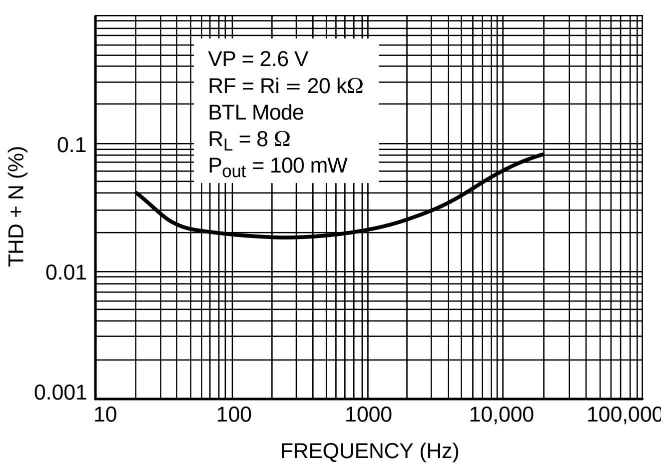


Figure 7. THD + N vs. Frequency (BTL Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

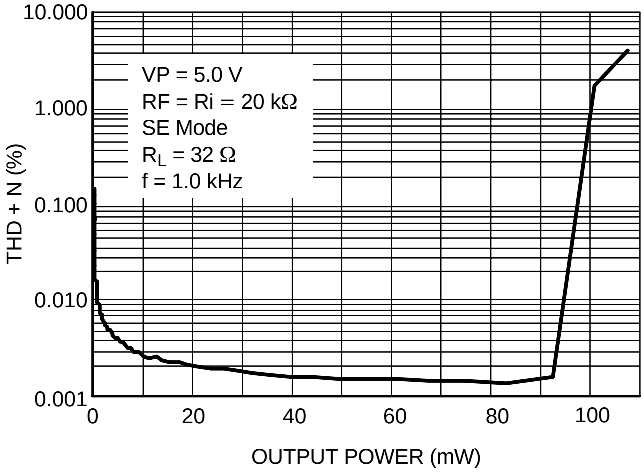


Figure 8. THD + N vs. Output Power (SE Mode)

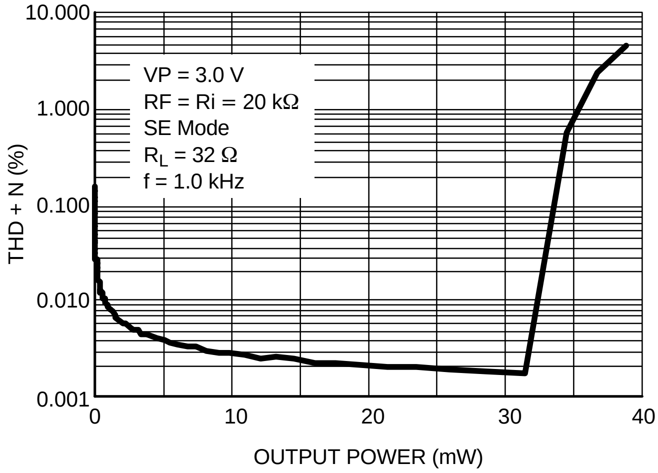


Figure 9. THD + N vs. Output Power (SE Mode)

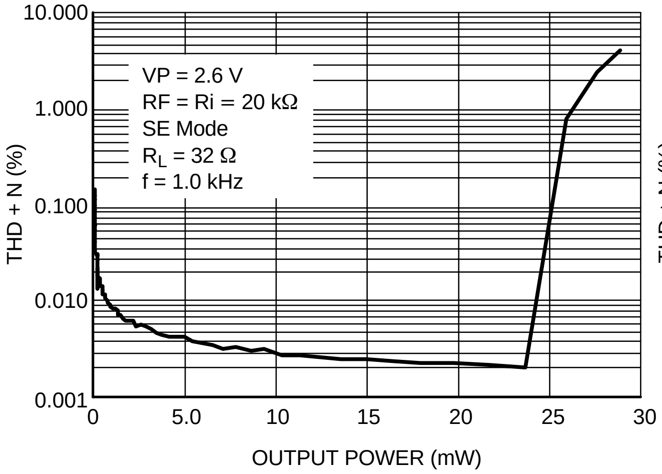


Figure 10. THD + N vs. Output Power (SE Mode)

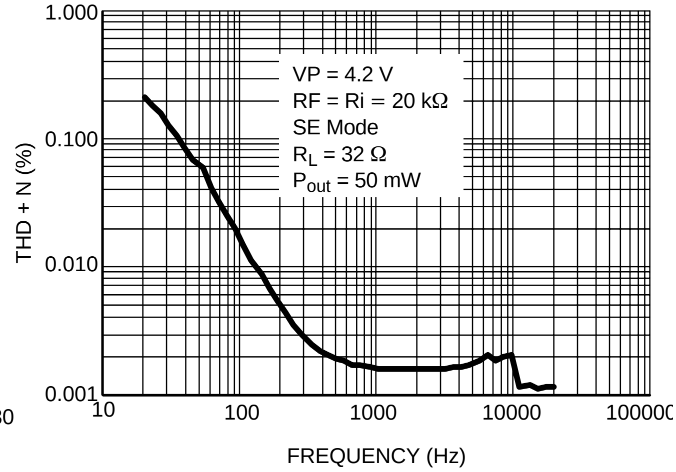


Figure 11. THD + N vs. Frequency (SE Mode)

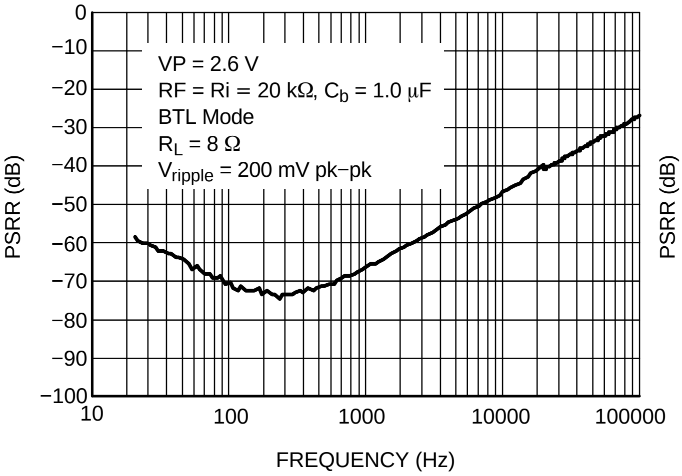


Figure 12. PSRR (BTL Mode) @ VP = 2.6 V

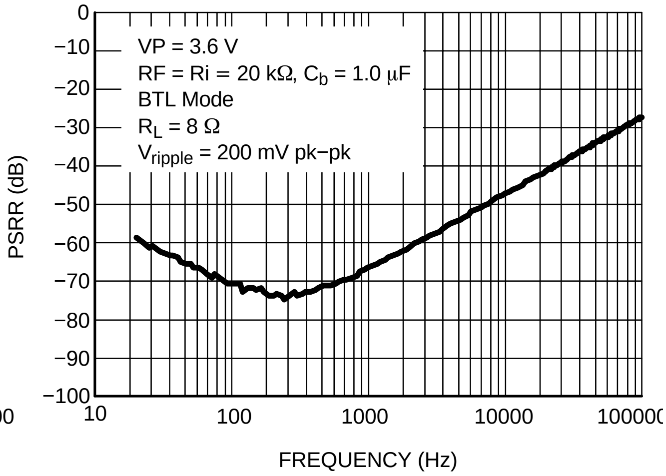


Figure 13. PSRR (BTL Mode) @ VP = 3.6 V

TYPICAL PERFORMANCE CHARACTERISTICS

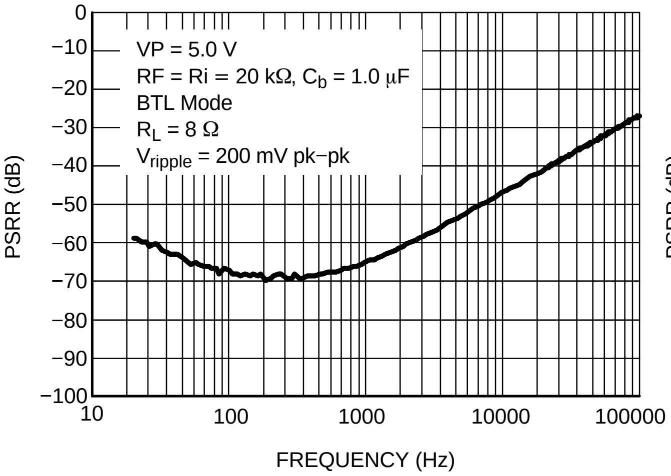


Figure 14. PSRR (BTL Mode) @ VP = 5.0 V

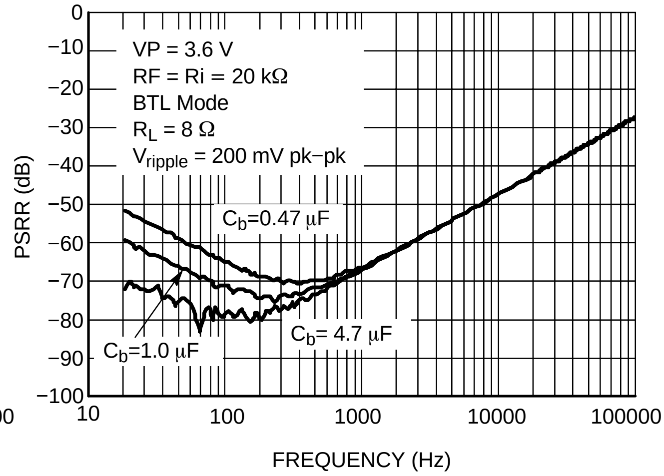


Figure 15. PSRR vs. C_b (BTL Mode) @ VP = 3.6 V

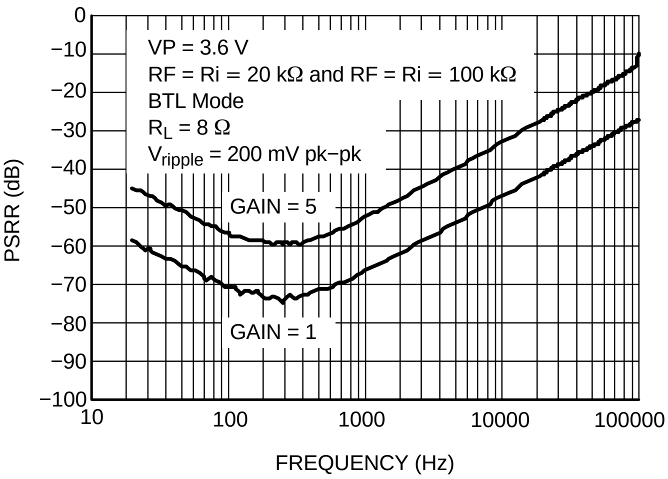


Figure 16. PSRR vs. Gain (BTL Mode) @ VP = 3.6 V

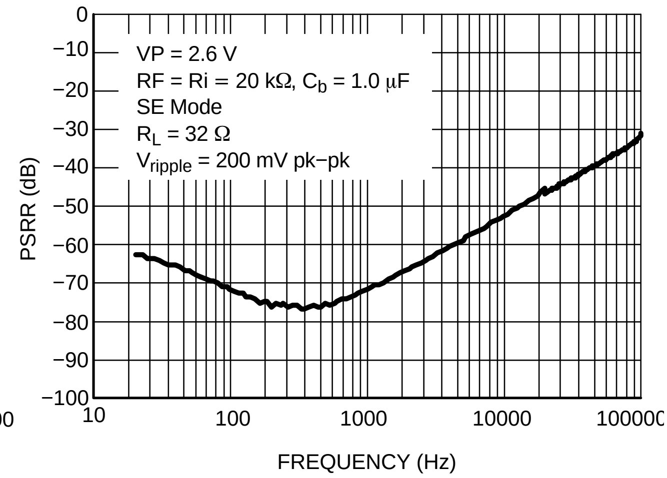


Figure 17. PSRR (SE Mode) @ VP = 2.6 V

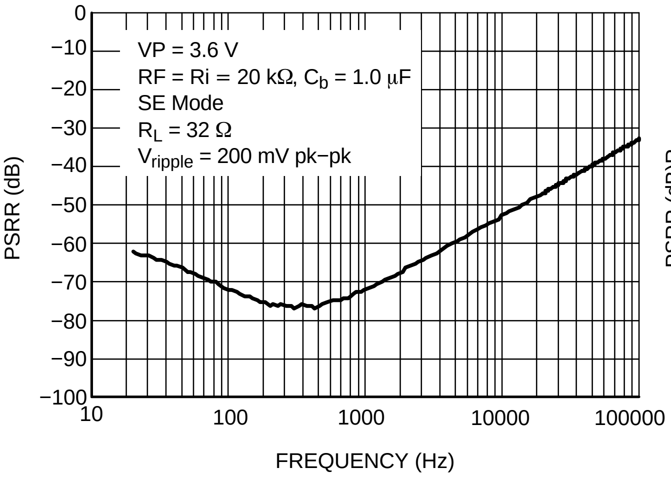


Figure 18. PSRR (SE Mode) @ VP = 3.6 V

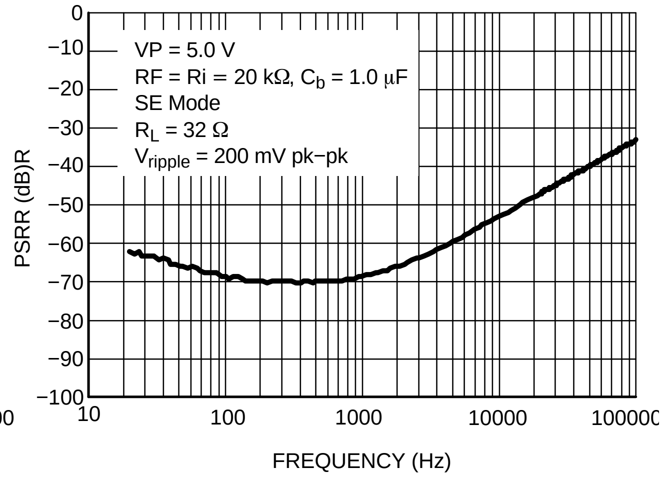


Figure 19. PSRR (SE Mode) @ VP = 5.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

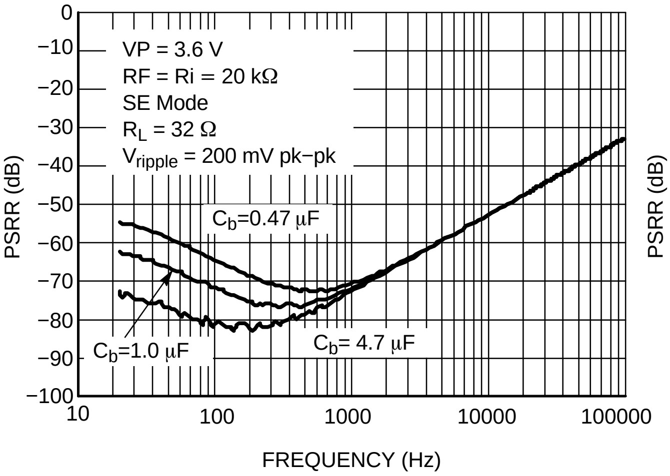


Figure 20. PSRR vs. C_b (SE Mode) @ VP = 3.6 V

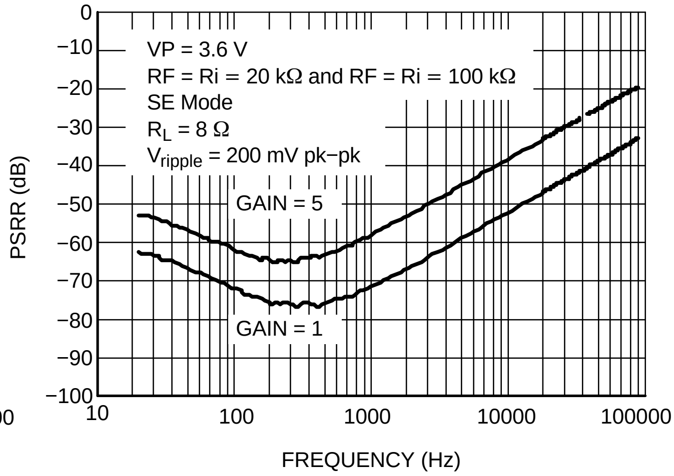


Figure 21. PSRR vs. Gain (SE Mode) @ VP = 3.6 V

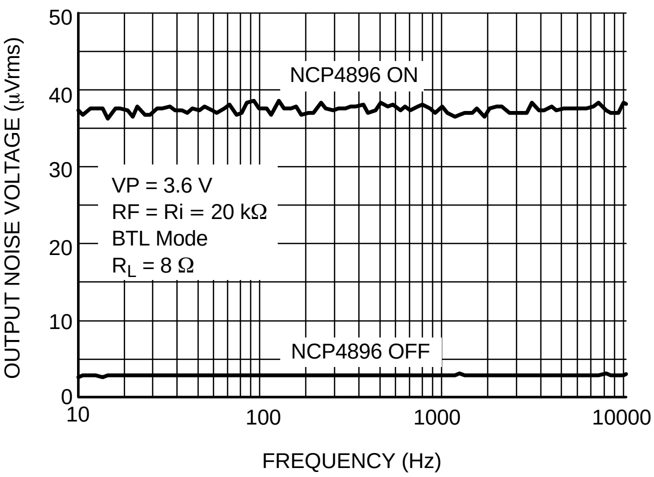


Figure 22. Output Noise Voltage (BTL Mode) @ VP = 3.6 V

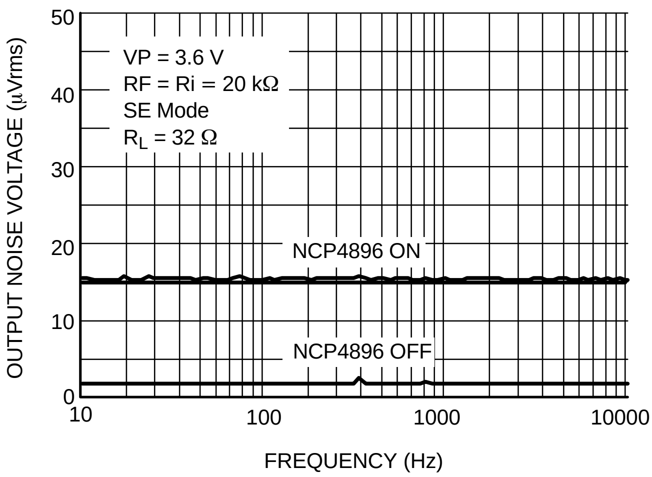


Figure 23. Output Noise Voltage (SE Mode) @ VP = 3.6 V

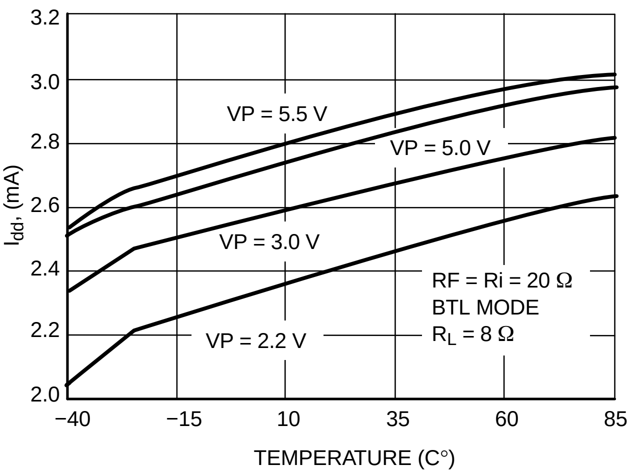


Figure 24. Quiescent Current (BTL Mode) vs. VP

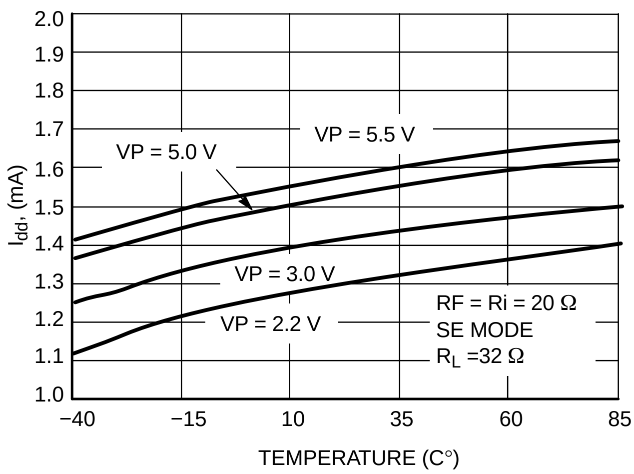


Figure 25. Quiescent Current (SE Mode) vs. VP

TYPICAL PERFORMANCE CHARACTERISTICS

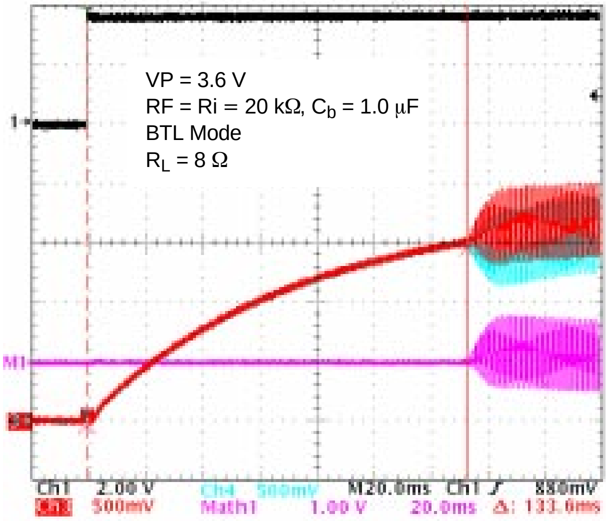


Figure 26. Turn On Sequence (BTL Mode) @ VP = 3.6 V

TYPICAL PERFORMANCE CHARACTERISTICS

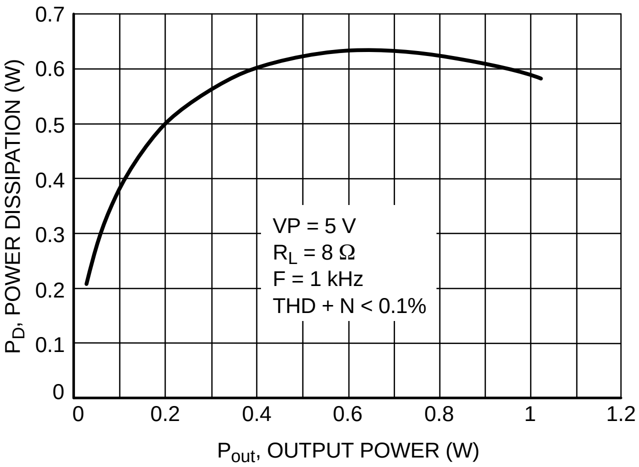


Figure 27. Power Dissipation vs. Output Power

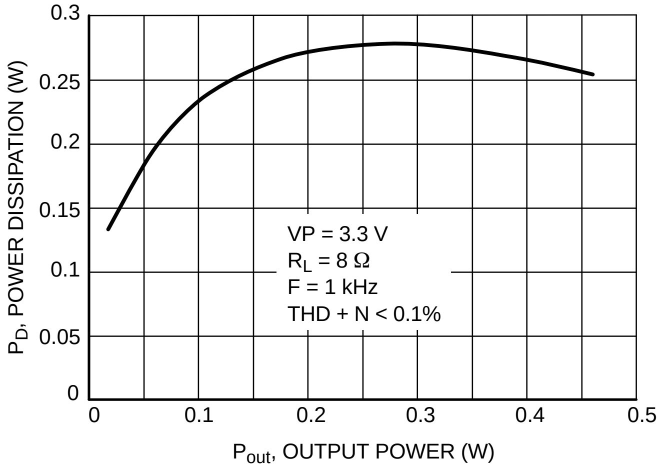


Figure 28. Power Dissipation vs. Output Power

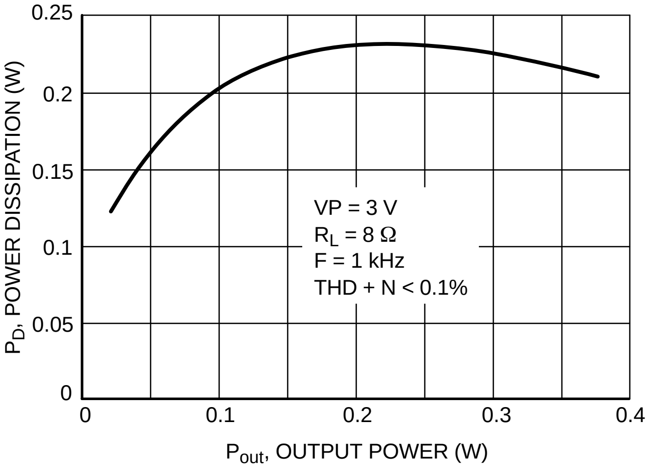


Figure 29. Power Dissipation vs. Output Power

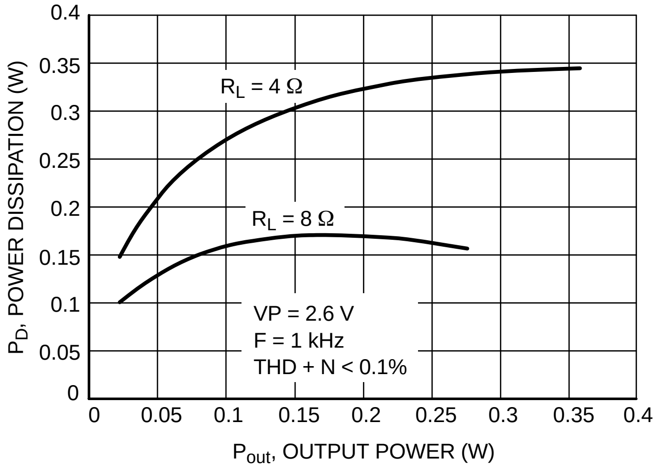


Figure 30. Power Dissipation vs. Output Power

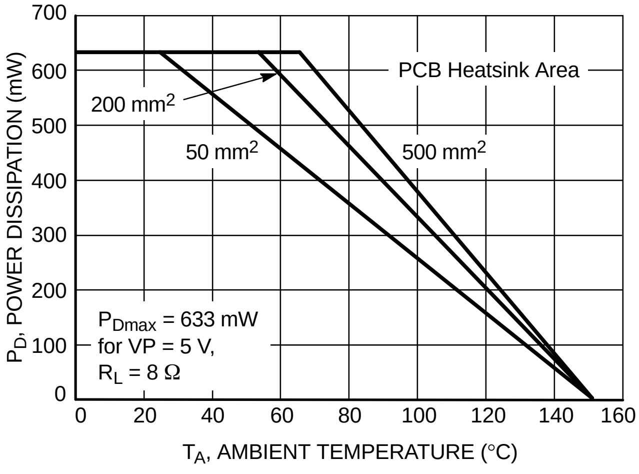


Figure 31. Power Derating − 9−Pin Flip−Chip CSP

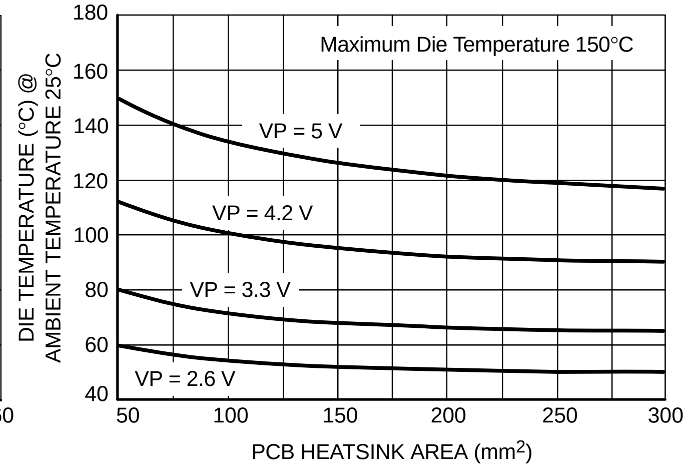


Figure 32. Maximum Die Temperature vs. PCB Heatsink Area

APPLICATION INFORMATION

Detailed Description

The NCP4896 audio amplifier can operate from 2.2 V until 5.5 V power supply. It delivers 320 mW rms output power to 4.0 Ω load (VP = 2.6 V) and 1.0 W rms output power to 8.0 Ω load (VP = 5.0 V).

The structure of the NCP4896 is basically composed of two identical internal power amplifiers. Both are externally configurable with gain−setting resistors R_{in} and RF (the closed−loop gain is fixed by the ratios of these resistors). So the load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor.

Internal Power Amplifier

The output Pmos and Nmos transistors of the amplifier were designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the Nmos and Pmos transistors does not exceed 0.6 Ω when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

Turn−On and Turn−Off Transitions

A cycle with a turn−on and turn−off transition is illustrated with plots that show both single ended signals on the previous page.

In order to eliminate “pop and click” noises during transitions, output power in the load must be slowly established or cut. When logic high is applied to the shutdown pin, the bypass voltage begins to rise exponentially and once the output DC level is around the common mode voltage, the gain is established slowly (20 ms). This way to turn−on the device is optimized in terms of rejection of “pop and click” noises.

A theoretical value of turn−on time at 25°C is given by the following formula.

C_{by}: bypass capacitor

R: internal 150 k resistor with a 25% accuracy

$T_{on} = 0.95 * R * C_{by}$

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. During the shutdown mode, amplifier outputs are connected to the ground. However, to cut totally the output audio signal, you only need to wait for 20 ms.

Shutdown Function

The device enters shutdown mode when the shutdown signal is low. During the shutdown mode, the Dc quiescent current of the circuit is typically 10 nA.

Current Limit Circuit

The maximum output power of the circuit (Porms = 1.0 W, VP = 5.0 V, R_L = 8.0 Ω) requires a peak current in the load of 500 mA.

In order to limit the excessive power dissipation in the load when a short−circuit occurs, the current limit in the load is fixed to 800 mA. The current in the four output MOS transistors are real−time controlled, and when one current exceeds 800 mA, the gate voltage of the MOS transistor is clipped and no more current can be delivered.

Single−Ended Operation

In SE mode, the load is driven from the primary amplifier output (OUTA). The gain is set by the ration between RF and Ri.

$$\text{SE Gain} = -\left(\frac{Rf}{Ri}\right)$$

In this SE mode, an output capacitor (Co) is required to block the common mode voltage at the output of the amplifier, thus avoiding DC currents in the load. As for the high pass filter due to the input capacitor and the Ri resistor, the load gives with Co another first order high pass filter, the cut−off frequency of which is given by:

$$Fc = \frac{1}{2\pi R_L \cdot Co}$$

SE/$\overline{\text{BTL}}$ Operation

Due to the internal control of each amplifier through SE/$\overline{\text{BTL}}$ pin, the NCP4896 allows a cost saving for application which requires to drive a example an 8.0 Ω BTL and a 32 Ω Single−Ended load.

The internal circuitry avoids “pop and click” noises that could occur in both $\overline{\text{BTL}}$ and Singled−Ended loads during transitions from SE to $\overline{\text{BTL}}$ and $\overline{\text{BTL}}$ to SE.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceeds 160°C, and will be switched on again only when the temperature decreases below 140°C.

The NCP4896 is unity−gain stable and requires no external components besides gain−setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application.

Both internal amplifiers are externally configurable (RF and R_{in}) with gain configuration.

The differential−ended amplifier presents two major advantages:

− The possible output power is four times larger (the output swing is doubled) as compared to a single−ended amplifier under the same conditions.

− Output pins (OUTA and OUTB) are biased at the same potential VP/2, this eliminates the need for an output coupling capacitor required with a single−ended amplifier configuration.

The differential closed loop−gain of the amplifier is given by $A_{vd} = * \frac{R_f}{R_{in}} = \frac{V_{orms}}{V_{inrms}}$. V_{orms} is the rms value of the voltage seen by the load and V_{inrms} is the rms value of the input differential signal.

Output power delivered to the load is given by $P_{orms} = \frac{(Vopeak)^2}{2 * R_L}$ (Vopeak is the peak differential output voltage).

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500 mA $I_{opeak} = \frac{V_{opeak}}{R_L}$.

Gain−Setting Resistor Selection (R_{in} and RF)

R_{in} and RF set the closed−loop gain of both amplifier.

In order to optimize device and system performance, the NCP4896 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance.

An input resistor (R_{in}) value of 22 kΩ is realistic in most of applications, and doesn’t require the use of a too large capacitor C_{in}.

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with Rin, the cut−off frequency is given by $fc = \frac{1}{2 * \Pi * R_{in} * C_{in}}$.

The value of the capacitor must be high enough to ensure good coupling at low frequencies without attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage (VP/2) and can increase the turn−on pops.

An input capacitor value between 0.1 μ and 0.39 μF performs well in many applications (With R_{in} = 22 kΩ).

Bypass Capacitor Selection (Cby)

The bypass capacitor Cby provides half−supply filtering and determines how fast the NCP4896 turns on.

This capacitor is a critical component to minimize the turn−on pop. A 1.0 μF bypass capacitor value (C_{in} = < 0.39 μF) should produce clickless and popless shutdown transitions. The amplifier is still functional with a 0.1 μF capacitor value but is more susceptible to “pop and click” noises.

Thus, a 1.0 μF bypassing capacitor is recommended.

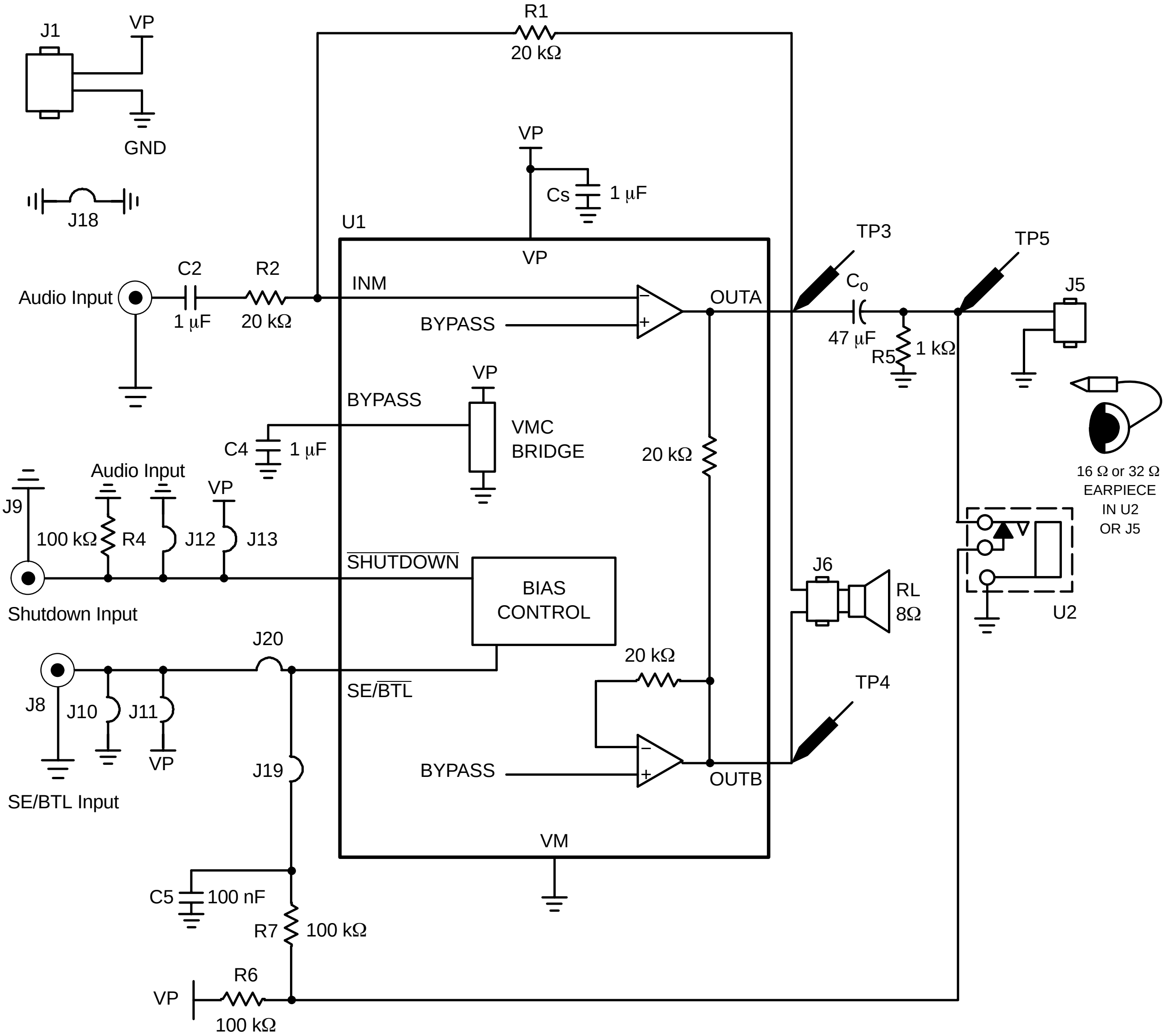
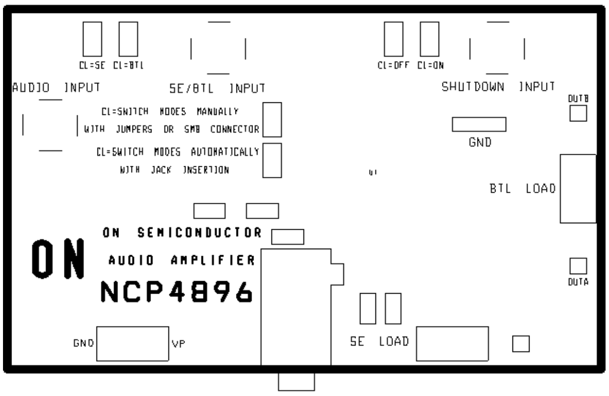
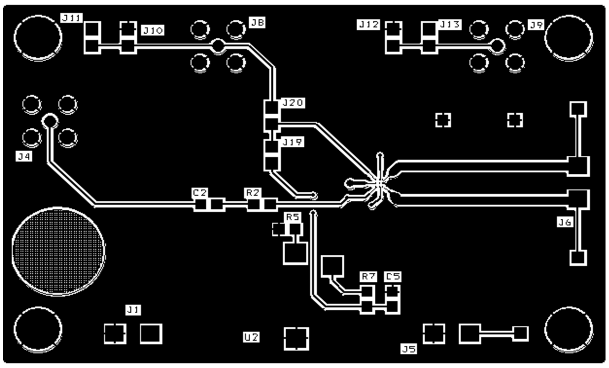


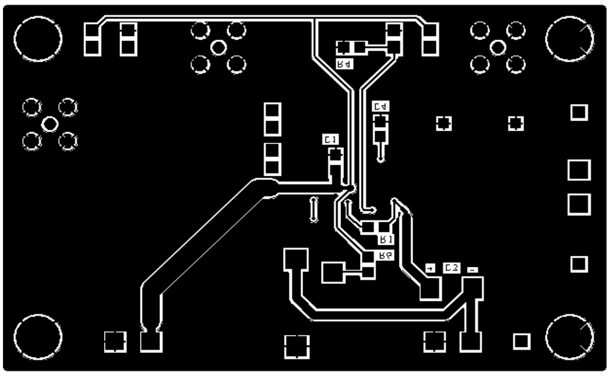
Figure 33. Typical NCP4896 Application Circuit with Single−Ended Input



Silkscreen Layer



Top Layer



Bottom Layer

Figure 34. Demonstration Board for 9−Pin Flip−Chip CSP Device − PCB Layers

BILL OF MATERIAL

Item	Part Description	Ref	PCB Footprint	Manufacturer	Manufacturer Reference
1	NCP4896 Audio Amplifier	U1			NCP4896
2	3.5 mm PCB Jack Connector	U2		Decelect−Forgos (Eurosab)	IEM101−3
3	SMD Resistor 20 kΩ	R1, R2	0805	Vishnay−Draloric	CRCW0805
4	SMD Resistor 100 kΩ	R4, R6, R7	0805	Vishnay−Draloric	CRCW0805
5	SMD Resistor 1.0 kΩ	R5	0805	Vishnay−Draloric	CRCW0805
6	Ceramic Capacitor 1.0 μF, 16 V, X7R	C1, C2, C4	0805	Murata	GRM21 Series GRM21BR71C105KA01L
7	Tantalum Capacitor 47 μF, 6.3 V	C3	B Size	AVX	TPS Series
8	Ceramic Capcitor 100 nF, 50 V, X7R	C5	0805	Murata	GRM21 Series GRM21BR71H104KA01L
9	Jumper Header Vertical Mount, 2*1, 100 mils	J10, J11, J12, J13, J19, J20			
10	Jumper Connector, 400 mils	J18			
11	I/O Connector. It Can be Plugged by BLZ5.08/2 (Weidmuller Reference)	J1, J5, J6		Weidmuller	SL5.08/2/90B
12	SMB Connector	J4, J8, J9		Radiall	R114665000
13	Test Point	TP3, TP4, TP5		Keystone	5000

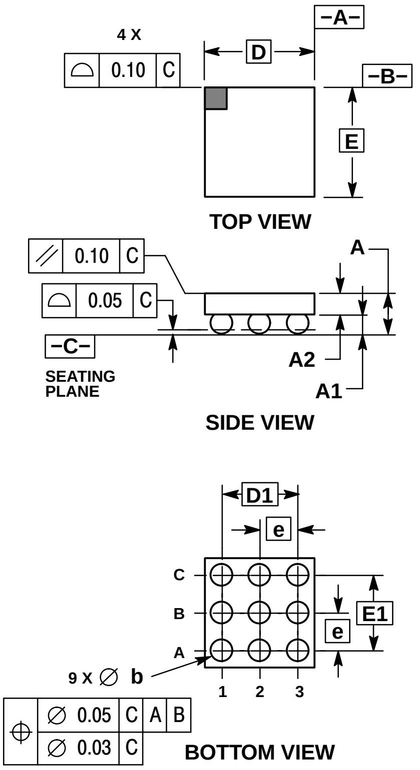
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP4896FCT1G	MAM	9−Pin Flip−Chip (Pb−Free)	3000/Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

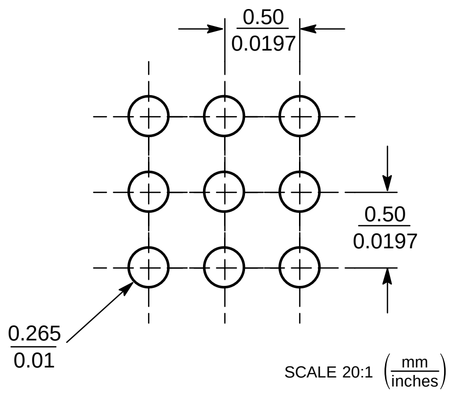
9−PIN FLIP−CHIP
FC SUFFIX
CASE 499AL−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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