Quad Static Shift Right/Shift Left Shift Register
Last In First Out Buffer
LIFO

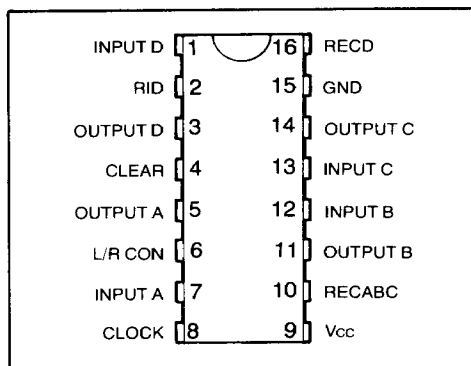## FEATURES

☐ COMPLAMOS® N-Channel Silicon Gate Technology.
☐ Quad 81 bit or Quad 133 bit
☐ Directly Compatible with T²L, MOS
☐ Operation Guaranteed from DC to 1.0MHz
☐ Recirculate logic on-chip
☐ Single +5.0V power supply
☐ Low clock input capacitance
☐ Single phase clock at T²L levels
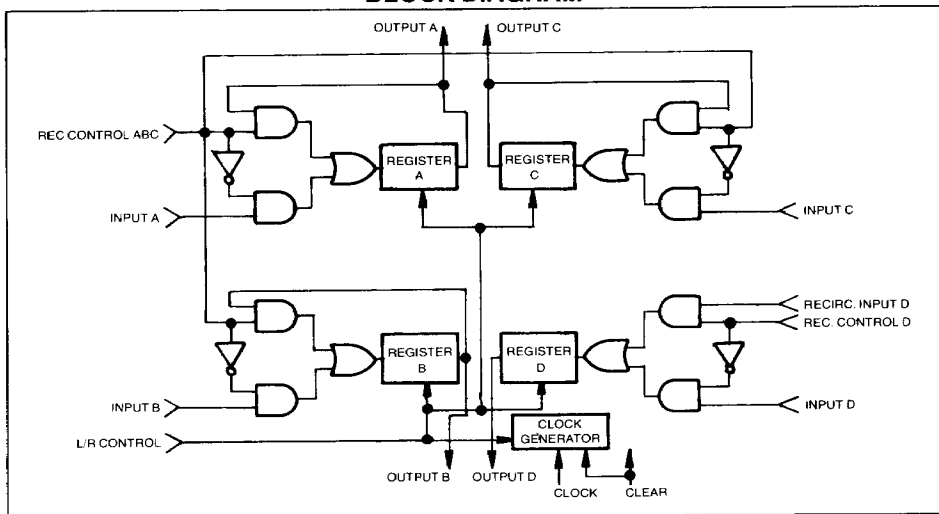☐ Clear function
☐ 16-pin Ceramic DIP Package

APPLICATIONS

☐ Bi-Directional Printer
☐ Computers—Push Down Stack—LIFO
☐ Buffer data storage—memory buffer
☐ Delay lines—delay line processing
☐ Digital filtering
☐ Telemetry Systems
☐ Terminals
☐ Peripheral Equipment

PIN CONFIGURATION

INPUT D	1	16	RECD
RID	2	15	GND
OUTPUT D	3	14	OUTPUT C
CLEAR	4	13	INPUT C
OUTPUT A	5	12	INPUT B
L/R CON	6	11	OUTPUT B
INPUT A	7	10	RECABC
CLOCK	8	9	Vcc

BLOCK DIAGRAM

SECTION VIII

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General Description

The SMC SR 5017 and SR 5018 are quad 133 (SR 5017) and quad 81 (SR 5018) bit static shift registers utilizing SMC's COPLAMOS® N channel silicon gate process. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and requires only a single +5 volt power supply.

These shift registers can be driven by either T²L circuits or by MOS circuits and provide driving capability to MOS to T²L circuits.

This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information right or left. This shift left/shift right (L/R Control) control input is common to all registers.

The recirculate control input is common for registers A, B, and C. Register D has an independent recirculate control input as well as a Recirculate Input.

A Clear input has been provided that will cause the shift register to be cleared when the input is at Vcc. A single T²L clock input is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 or 133 are available for flag storage.
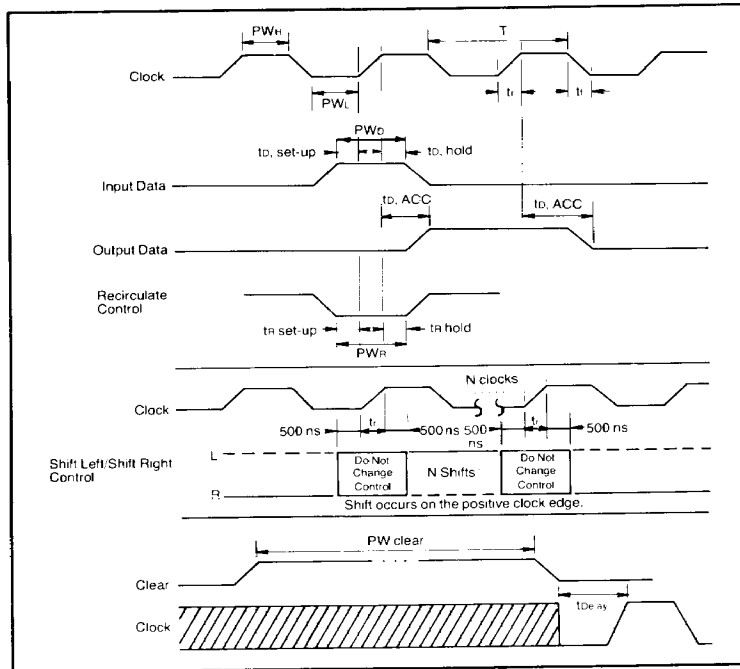
MAXIMUM GUARANTEED RATINGS*
Operating Temperature Range .... 0°C to + 70°C
Storage Temperature Range .... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) .... +325°C
Positive Voltage on any Pin, with respect to ground .... +8.0V
Negative Voltage on any Pin, with respect to ground .... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (TA = 0°C to 70°C, Vcc = +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V$_{IL}$			0.8	V	
High Level, V$_{IH}$	Vcc—1.5		Vcc	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V$_{OL}$			0.4	V	I$_{OL}$=1.6ma
High Level, V$_{OH}$	Vcc—1.5	4.0		V	I$_{OH}$=100μa
INPUT LEAKAGE CURRENT			1.0	μa	V$_{IN}$=Vcc
CLOCK, CLEAR			25	pf	
All Other			10	pf	
POWER SUPPLY CURRENT			100	ma	
A.C. Characteristics					TA= +25°C
CLOCK					
PW$_H$	300			ns	
PW$_L$	600			ns	
Transition, t$_r$, t$_f$		0.02	1.0	μs	
Repetition Rate, 1/T	0		1.0	MHz	
t Delay	500			ns	
INPUT DATA					
t$_D$, set-up	150			ns	
t$_D$, hold	150			ns	
PW$_D$	300			ns	
OUTPUT DATA					
t$_D$, ACC		200	350	ns	
RECIRCULATE CONTROL					
t$_R$, set-up	200			ns	
t$_R$, hold	300			ns	
PW$_R$	500			ns	
CLEAR					
PW$_{CLEAR}$	20			μs	

Timing Diagram

Description of Pin Functions

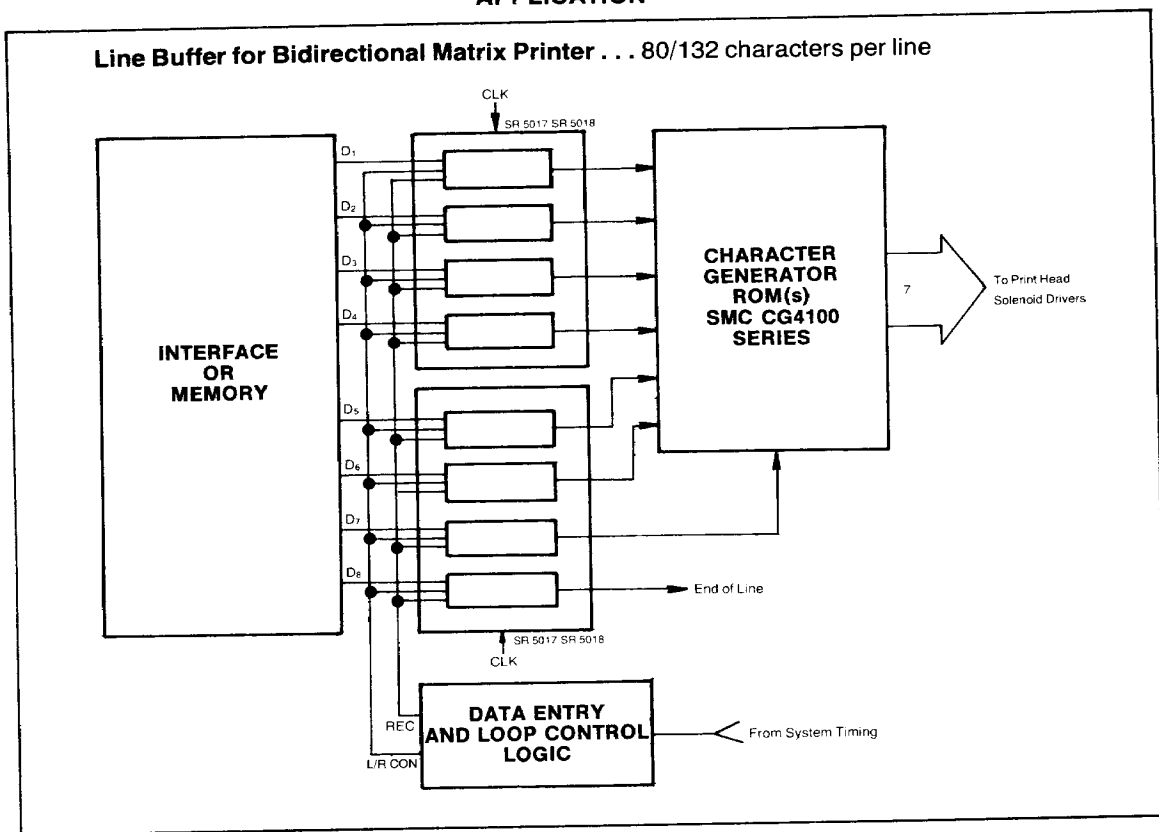| Symbol	Name	Pin	Function
D	Input D	1	Input signal for D register.
RID	Recirculate Input D	2	Input signal which is the input to the D register when recirculate control D is high: RECD = 1.
O$_D$	Output D	3	Output signal for D register.
CLR	Clear	4	Input signal when high forces outputs to a low state immediately and clears all the registers.
O$_A$	Output A	5	Output signal for A register.
L/R CON	Shift Left/Shift Right Control	6	Input signal which is low for loading data and for shifting right. When L/R CON is high, the register will shift left.
A	Input A	7	Input signal which is either high or low depending on what word is to be loaded into shift register.
CLK	Clock Input	8	Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock.
V$_{CC}$	5 Volt	9	5 volt power supply.
RECABC	Recirculate ABC	10	Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs.
O$_B$	Output B	11	Output signal for B register.
B	Input B	12	Input signal for B register.
C	Input C	13	Input signal for C register.
O$_C$	Output C	14	Output signal for C register.
GND	GND	15	Ground.
RECD	Recirculate Control D	16	Input signal which is normally low and, when goes high, disconnects Input D to register and connects RECIRCULATE INPUT D to register.

Logic Diagram
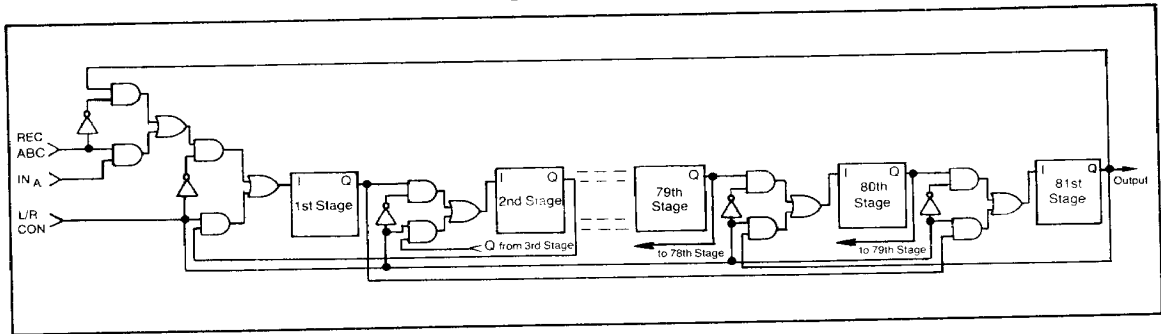
APPLICATION

Line Buffer for Bidirectional Matrix Printer . . . 80/132 characters per line