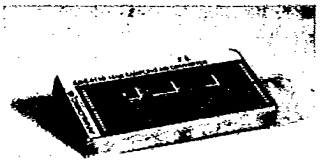


ANALOGIC®

ADC4110/4111

16-Bit Extended Temperature Range Sampling A/D Converters

Description T-51-10-16

Analogic's ADC4110/4111 are 16-bit analog-to-digital converters (ADCs) with integral sample-and-hold amplifiers (S/H) that offer significantly improved stability and reduced power dissipation over previous converters of similar architecture. Their low noise, low power dissipation, and guaranteed end-to-end S/H plus A/D performance over a wide temperature range make them ideal for applications requiring high precision in severe environments, such as seismic exploration and field testing. Both combine a precision S/H circuit and a high accuracy A/D converter with tri-state output buffers in a single module, eliminating the interface problems that often accompany the integration of individual modules. (See Figure 1).

The ADC4110/4111 feature exceptional accuracy and stability over temperature, including a maximum Differential Nonlinearity Tempco of ±1 ppm/°C, clock stability of ±0.03%/°C maximum, and rapid stabilization at power up. Offering guaranteed performance over the temperature range of −25°C to +85°C, the ADC4111 satisfy the most stringent industrial and geophysical data acquisition requirements. Low power dissipation (1.0W), very low noise (75 μV rms), and wide dynamic range (16 bits) allow the user to perform sophisticated measurements with a much higher level of confidence in the results than would otherwise be possible in these severe environments.

The ADC4110/4111 are fully shielded in 2" x 4" x 0.37" metal packages. Each is fully tested and supplied with its documented test data.

Features

- **Guaranteed performance over extended temperature range** (−25°C to +85°C)
- **Low noise** 50 μV (ADC)
- **Low differential nonlinearity** ±0.0015% FSR maximum
- **Low drift** ±1 ppm/°C differential nonlinearity tempco
- **Low power** 0.9W
- **Byte-selectable HCT tri-state buffered outputs**
- **High throughput rate** 12.5 kHz
- **Pin-programmable input voltage range** 0V to +5V, 0V to +10V, ±5V, ±10V

Applications

For severe temperature environments including:

- **Seismic Data Acquisition**
- **Portable Field-Test Equipment**
- **Automatic Test Equipment**
- **Materials Testing**

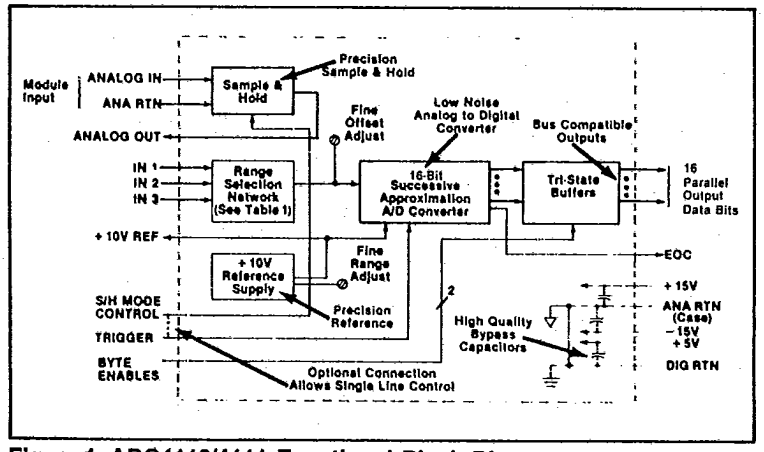


Figure 1. ADC4110/4111 Functional Block Diagram.

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

SPECIFICATIONS

T-51-10-16

(Includes combined S/H and A/D performance, and applies to both ADC4110-M and ADC4111-M except where noted)
(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Full Scale Range (FSR)
0V to +5V, 0V to +10V, ±5V, ±10V (see Table 1)

Maximum Input Without Damage
±15V

Impedance
100 Megohm / / 5 pF

Bias Current
1 nA maximum

ACCURACY

Absolute Accuracy (Traceable to NBS)
Calibrated to ±0.006% FSR

Relative Accuracy
±0.003% FSR maximum

Differential Nonlinearity
±0.0015% FSR maximum

Quantizing Error
±1/2 LSB

Noise (S/H plus A/D)
75 μV rms, ±10V range

Noise (A/D only)
50 μV rms, ±10V range

Monotonicity
Guaranteed

STABILITY

Tempco of Differential Nonlinearity
±3 ppm/°C FSR maximum (ADC4110),
±1 ppm/°C FSR maximum (ADC4111)

Gain Tempco
±8 ppm/°C FSR maximum

Offset Tempco
±30 μV/°C typical, ±80 μV/°C maximum (ADC4110)
±30 μV/°C typical, ±60 μV/°C maximum (ADC4111)

Clock Stability
±0.03%/°C maximum

Power Supply Sensitivity
±0.001% FSR per 1% change in supply voltage

Warm-up Time to Specified Accuracy
1 minute

Recommended Recalibration Interval
6 months

DYNAMIC PERFORMANCE

Maximum Throughput Rate
12,500 measurements/second

S/H Acquisition Time
15 μs maximum

A/D Conversion Time
65 μs maximum

S/H Aperture Delay
50 ns

S/H Aperture Uncertainty
1 ns

S/H Hold Mode Feedthrough Rejection
90 dB minimum, measured with 20V p-p 10 kHz sinewave input

S/H Droop Rate
0.2 μV/μs at 25°C, doubles every 10°C

S/H Dielectric Absorption Error
±0.005% of input voltage change at maximum throughput rate. Error decreases as sampling time is decreased.

DIGITAL OUTPUTS

End of Conversion (EOC)
Positive true, 2 unit loads/line, (see Figure 3 for timing) CMOS

Parallel Data Codes
Positive true, tri-state buffered HCT; 2's complement unipolar binary, 2's complement offset binary (see Table 1)

DIGITAL INPUTS

General
Standard TTL, one unit load/line

S/H Mode Control
Sample = Logic 1
Hold = Logic 0 (minimum = conversion time)
Logic 1 to logic 0 transition time 10 ns maximum

A/D Trigger
Negative-going edge; logic 1 to logic 0 transition 50 ns maximum

Low/High Byte Enable
Logic 0 = enable
Logic 1 = 3.5V minimum @ 1 μA, HCT
Logic 0 = 1.5V maximum @ 1 μA, HCT

POWER REQUIREMENTS

+15V, ±3%
37 mA maximum

−15V, ±3%
35 mA maximum

+5V, ±5%
9 mA maximum

Power Dissipation
1.0W

ENVIRONMENTAL AND MECHANICAL

Operating Temperature
0°C to +70°C (ADC4110-M)
−25°C to +85°C (ADC4111-M)

Storage Temperature
−25°C to +85°C

Relative Humidity
5% to 95% noncondensing to 40°C

Shielding
Electrostatic (RFI) 6 sides;
Electromagnetic (EMI) 5 sides

Package Size
2.0" x 4.0" x 0.375"
(50.8 x 101.6 x 9.53 mm)

Specifications subject to change without notice.

Operation T-51-10-16

The ADC4110/4111 interface directly to most commonly available input devices (multiplexers, amplifiers, etc.). The high input impedance of the fast, fully-buffered unity gain S/H amplifier minimizes source loading errors; the hold mode feedthrough rejection and droop rate allow optimum performance in multichannel systems.

The parallel binary data information is HCT tri-state buffered allowing access as either two 8-bit bytes or as a single 16-bit (including B1) data word. (If the tri-state feature is not needed, normal two's complement binary outputs can be obtained by connecting the byte enable pins to ground.)

For operation with a single external control pulse, the S/H mode control input may be connected to the A/D trigger. Figure 3 shows the timing requirements for the digital control signals.

Input voltage range is established by connecting the S/H output to the appropriate A/D input pins (see Table 1). These pins provide access to the S/H output for arbitrary signal processing prior to analog-to-digital conversion. In addition, the S/H may be bypassed for applications requiring direct input to the A/D converter.

Applications

Designed to operate within the −25°C to +85°C temperature range (0°C to +70°C ADC4110-M) with high accuracy and low drift, the ADC4111-M can serve a variety of applications, including field testing, such as portable multichannel seismic data acquisition systems to provide rapid, highly-linear, and stable A/D conversion. In these systems, geophones receive artificially induced shock waves reflected off the different subsurface strata at various angles and velocities. The weakest signals may travel up to 5 miles through the lithosphere, and are difficult to distinguish from the noise and interference caused by ground roll. After appropriate front-end preamplification and filtering, the analog signals are converted to digital form and stored for processing. The ADC4110/4111 provide the low noise and required throughput to digitize data from 16 channels, while maintaining a 780 Hz-per-channel sampling rate.

Table 1

RANGE PROGRAMMING AND OUTPUT CODING

A/D Input Connections

Full Scale Range	Connect IN 1 to	Connect IN 2 to	Connect IN 3 to	Input Impedance
0 to +5V	S/H ANA OUT	S/H ANA OUT	S/H ANA OUT	1.25kΩ
0 to +10V	ANA RTN	S/H ANA OUT	S/H ANA OUT	2.5kΩ
−5V to +5V	S/H ANA OUT	+10V REF	ANA RTN	2.5kΩ
−10V to +10V	ANA RTN	+10V REF	S/H ANA OUT	5.0kΩ

Output Codes

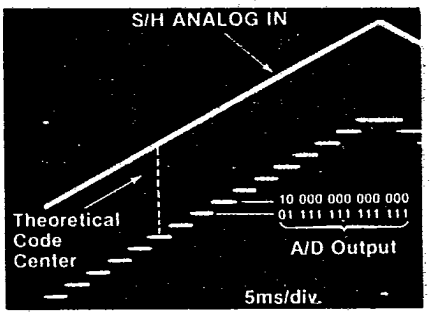
Two's Complement

UNIPOLAR

0V to +5V	0V to +10V	Code
+4.99992	+9.99985	0 111 111 111 111 111
0.00000	0.00000	1 000 000 000 000 000

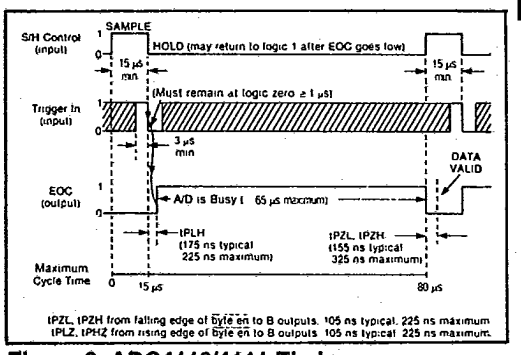
BIPOLAR

±5V	±10V	Code
+4.99985	+9.99969	0 111 111 111 111 111
0.00000	0.00000	0 000 000 000 000 000
−5.00000	−10.00000	1 000 000 000 000 000



The upper trace shows an input that ramps repetitively from −2.44 mV to +2.44 mV and back very slowly in relation to the module's 12.5 kHz sampling rate. The module output is used to drive a digital-to-analog converter, whose output is then shown on the lower trace. Thus each level on the staircase corresponds to a set of conversions made around a code center voltage, and the transitions show when the module toggles its LSB. This type of plot may be used to measure differential non-linearity (the most significant A/D performance parameter for most applications) and to determine by inspection the existence of errors such as wide code, narrow code, missing code, non-monotonicity, etc. Because the input is dynamically changing, this type of test simulates actual operation very well.

Figure 2. ADC4111-M Crossplot Shows Highly Linear Performance.



tPZL, tPZH from falling edge of $\overline{\text{byte en}}$ to B outputs. 105 ns typical, 225 ns maximum
tPLZ, tPHZ from rising edge of $\overline{\text{byte en}}$ to B outputs. 105 ns typical, 225 ns maximum.

Figure 3. ADC4110/4111 Timing.

Calibration

Due to excellent long-term stability, these modules will rarely require re-calibration. They should, however, be re-adjusted when the selected FSR is changed. Offset should be zeroed prior to trimming the range.

Offset Zeroing Procedure

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Offset pot until the module output code corresponds to 0V, with the LSB alternating equally between 0 and 1.

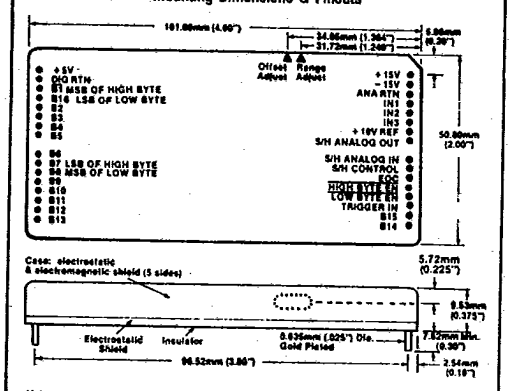
Range Trimming Procedure (Gain Adjust)

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Gain pot until the module output code is all 1's, with the LSB alternating equally between 0 and 1.

Input Voltages for Calibration

	ADC4110/4111-M	
Nominal FSR	Offset	Range
0 to + 5V	38 μV	+4.99989V
0 to + 10V	76 μV	+9.99977V
−5 to + 5V	76 μV	+4.99977V
−10 to 10V	153 μV	+9.99854V

Mounting Dimensions & Pinouts



Notes
- Pin spacing on 2.54 mm (0.10") centers. Double spacing between pins 8 & 9 as shown.
- Modupac™ may be mounted in any orientation.

Ordering Guide

Simply Specify

☐ **ADC4110-M**	**Commercial Temp**
☐ **ADC4111-M**	**Industrial Temp**