19-1452; Rev 1; 10/99

MAXIM

Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

General Description

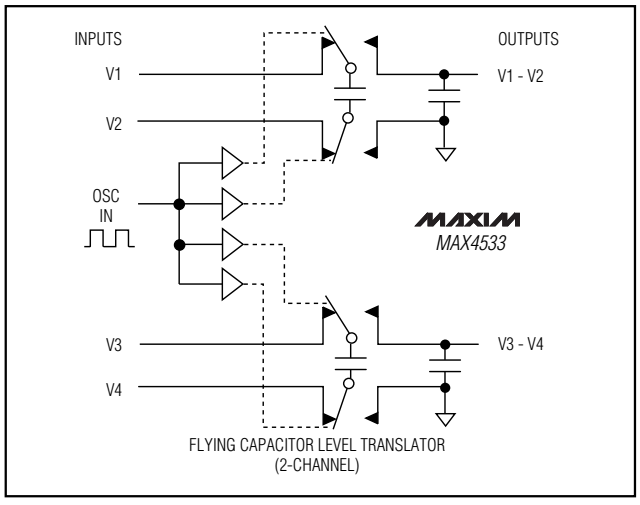
The MAX4533 quad, single-pole/double-throw (SPDT), fault-protected analog switch is pin-compatible with the industry-standard MAX333 and MAX333A. The MAX4533 features fault-protected inputs and Rail-to-Rail® signal handling. The normally open (NO_) and normally closed (NC_) terminals are protected from overvoltage faults up to ±25V with power on and up to ±40V with power off. During a fault condition, NO_ and NC_ become high impedance with only nanoamperes of leakage current flowing to the source. In addition, the output (COM_) clamps to the appropriate polarity supply rail and provides up to ±10mA of load current. This ensures unambiguous rail-to-rail outputs when a fault occurs.

The MAX4533 operates from dual ±4.5V to ±18V power supplies or a single +9V to +36V supply. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility when using ±15V supplies or a +12V supply. On-resistance is 175Ω max and is matched between switches to 10Ω max. The off-leakage current is only 0.5nA at T_A = +25°C and 10nA at T_A = +85°C.

Applications

Redundant/Backup Systems	Portable Instruments
Test Equipment	Data-Acquisition Systems
Communications Systems	
Industrial and Process Control	Avionics Systems

Typical Operating Circuit



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.
† Patent Pending

Features

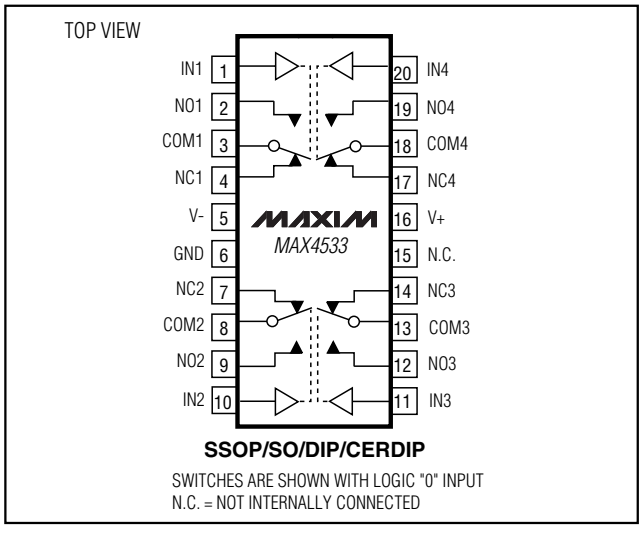
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **±40V Fault Protection with Power Off**
  ±25V Fault Protection with ±15V Supplies
- ♦ **All Switches Off with Power Off**
- ♦ **No Power-Supply Sequencing Required During Power-Up or Power-Down**
- ♦ **Output Clamped to Appropriate Supply Voltage During Fault Condition—No Transition Glitch**
- ♦ **1kΩ (typ) Output Clamp Resistance During Overvoltage**
- ♦ **175Ω (max) Signal Paths with ±15V Supplies**
- ♦ **20ns (typ) Fault Response Time**
- ♦ **±4.5V to ±18V Dual Supplies**
  +9V to +36V Single Supply
- ♦ **Pin-Compatible with Industry-Standard MAX333/MAX333A**
- ♦ **TTL/CMOS-Compatible Logic Inputs with ±15V or Single +9V to +15V Supplies**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4533CAP	0°C to +70°C	20 SSOP
MAX4533CWP	0°C to +70°C	20 Wide SO

Ordering Information continued at end of data sheet.

Pin Configuration/ Functional Diagram



SSOP/SO/DIP/CERDIP

SWITCHES ARE SHOWN WITH LOGIC "0" INPUT
N.C. = NOT INTERNALLY CONNECTED

Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +44.0V
V- .....-44.0V to +0.3V
V+ to V-.....-0.3V to +44.0V
COM_, IN_ (Note 1) ..... (V- - 0.3V) to (V+ + 0.3V)
NC_, NO_ (Note 2).....(V+ - 40V) to (V- + 40V)
NC_, NO_ to COM_ .....-40V to +40V
NC_, NO_ Overvoltage with Switch Power On
(supplies at ±15V).....-30V to +30V
NC_, NO_ Overvoltage with Switch Power Off .....-40V to +40V
Continuous Current into Any Terminal.....±30mA
Peak Current into Any Terminal
(pulsed at 1ms,10% duty cycle).....±50mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 10.53mW/°C above +70°C) 842mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C).....889mW
Operating Temperature Ranges
MAX4533C_ _ .....0°C to +70°C
MAX4533E_ _ .....-40°C to +85°C
MAX4533M_ _.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: COM_ and IN_ pins are not fault protected. Signals on COM_ or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: NC_ and NO_ pins are fault protected. Signals on NC_ or NO_ exceeding -25V to +25V may damage the device. These limits apply with power applied to V+ or V-. The limit is ±40V with V+ = V- = 0.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Fault-Free Analog Signal Range (Note 2)	$V_{NO\_}$, $V_{NC\_}$	V+ = +15V, V- = -15V, $V_{NO\_}$ or $V_{NC\_}$ = ±15V	C, E, M	V-		V+	V
COM_ to NO_ or COM_ to NC_ On-Resistance	R_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = ±10V, $I_{COM\_}$ = 1mA	+25°C		125	175	Ω
			C, E			200	
			M			250	
COM_ to NO_ or COM_ to NC_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = ±10V, $I_{COM\_}$ = 1mA	+25°C		1	6	Ω
			C, E			10	
			M			15	
On-Resistance Flatness		$V_{COM\_}$ = +5V, 0, -5V, $I_{COM\_}$ = 1mA	+25°C		4		Ω
NO_ or NC_ Off-Leakage Current (Note 5)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	$V_{NO\_}$ or $V_{NC\_}$ = ±14V, $V_{COM\_}$ = ∓14V	+25°C	-0.5	0.02	0.5	nA
			C, E	-10		10	
			M	-200		200	
COM_ On-Leakage Current (Note 5)	$I_{COM\_(ON)}$	$V_{COM\_}$ = ±14V, $V_{NO\_}$ or $V_{NC\_}$= ±14V or floating	+25°C	-0.5	0.01	0.5	nA
			C, E	-20		20	
			M	-400		400	
FAULT							
Fault-Protected Analog Signal Range (Note 2)	$V_{NO\_}$, $V_{NC\_}$	Applies with power on	+25°C	-25		+25	V
		Applies with power off	+25°C	-40		+40	
COM_ Output Leakage Current, Supplies On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, no connection to "ON" channel	+25°C	-10		10	nA
			C, E	-200		200	
			M	-10		10	µA
NO_ or NC_ Off Input Leakage Current, Supplies On	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, $V_{COM\_}$ = ∓10V	+25°C	-20		20	nA
			C, E	-200		200	
			M	-10		10	µA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
NO_ or NC_ Input Leakage Current, Supplies Off	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±40V, V+ = 0, V- = 0	+25°C	-20	0.1	20	nA
			C, E	-200		200	
			M	-10		10	µA
COM_ On-Clamp Output Current, Supplies On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = +25V	+25°C	8	11	13	mA
		$V_{NO\_}$ or $V_{NC\_}$ = -25V	+25°C	-12	-10	-7	
COM_ On-Clamp Output Resistance, Supplies On	$R_{COM\_}$	$V_{NO\_}$ or V_{NC} = ±25V	+25°C		1.0	2.5	kΩ
			C, E, M			3	
±Fault Output Clamp Turn-On Delay Time (Note 6)		R_L = 10kΩ, $V_{NO\_}$ or $V_{NC\_}$ = ±25V	+25°C		20		ns
±Fault Recovery Time (Note 6)		R_L = 10kΩ, $V_{NO\_}$ or $V_{NC\_}$ = ±25V	+25°C		2.5		µs
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E, M	2.4			V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E, M			0.8	V
IN_ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}	$V_{IN\_}$ = +0.8V or +2.4V	+25°C	-1	0.03	1	µA
			C, E, M	-5		5	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = ±10V, R_L = 2kΩ; Figure 2	+25°C		100	250	ns
			C, E			400	
			M			600	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = ±10V, R_L = 2kΩ; Figure 2	+25°C		60	150	ns
			C, E			300	
			M			450	
Break-Before-Make Time Delay	t_{BBM}	$V_{COM\_}$ = ±10V, R_L = 1kΩ; Figure 3	+25°C	10	50		ns
Charge Injection (Note 6)	Q	C_L = 100pF, $V_{COM\_}$ = 0; Figure 4	+25°C		1.5		pC
NO_ or NC_ Off-Capacitance	$C_{N\_(OFF)}$	f = 1MHz; Figure 5	+25°C		5		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz; Figure 5	+25°C		12		pF
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 1MHz; Figure 6	+25°C		-62		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 1MHz; Figure 6	+25°C		-66		dB
POWER SUPPLY							
Power-Supply Range	V+, V-			±4.5		±18	V
V+ Supply Current	I+	All $V_{IN\_}$ = 0 or +5V, $V_{NO\_}$ = $V_{NC\_}$ = 0	+25°C			600	µA
			C, E, M			1000	
V- Supply Current	I-	All $V_{IN\_}$ = 0 or +5V, $V_{NO\_}$ = $V_{NC\_}$ = 0	+25°C			400	µA
			C, E, M			600	
GND Supply Current	I_{GND}	All $V_{IN\_}$ = 0 or +5V, $V_{NO\_}$ = $V_{NC\_}$ = 0	+25°C			300	µA
			C, E, M			450	

Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Fault-Free Analog Signal Range (Note 2)	$V_{NO\_}$, $V_{NC\_}$	V+ = +12V, V- = 0, $V_{NO\_}$ or $V_{NC\_}$ = +12V or 0	C, E, M	0		V+	V
COM_ to NO_, COM_ to NC_ On-Resistance	R_{ON}	V+ = +12V, $V_{NO\_}$ or $V_{NC\_}$ = +10V, $I_{COM\_}$ = 1mA	+25°C		260	390	Ω
			C, E			450	
			M			525	
COM_ -NO_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = +12V, $V_{NO\_}$ or $V_{NC\_}$ = +10V, $I_{COM\_}$ = 1mA	+25°C		4	10	Ω
			C, E			20	
			M			30	
NO_ or NC_ Off-Leakage Current (Notes 5, 9)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = +12V, $V_{COM\_}$ = +10V, +1V, $V_{NO\_}$ or $V_{NC\_}$ = +1V, +10V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
			M	-200		200	
COM_ On-Leakage Current (Notes 5, 9)	$I_{COM\_(ON)}$	V+ = +12V, $V_{COM\_}$ = +10V, $V_{NO\_}$ or $V_{NC\_}$= +10V or floating	+25°C	-0.5	0.01	0.5	nA
			C, E	-20		20	
			M	-400		400	
FAULT							
Fault-Protected Analog Signal Range (Note 2)	$V_{NO\_}$, $V_{NC\_}$	Applies with power on	+25°C	-25		+25	V
		Applies with power off	+25°C	-40		+40	
COM_ Output Leakage Current, Supply On (Note 9)	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, V+ = +12V, no connection to “ON” channel	+25°C	-10		10	nA
			C, E	-200		200	
			M	-10		10	µA
NO_ or NC_ Off Input Leakage Current, Supply On (Note 9)	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, $V_{COM\_}$ = 0, V+ = +12V	+25°C	-20		20	nA
			C, E	-200		200	
			M	-10		10	µA
NO_ or NC_ Input Leakage Current, Supply Off (Note 9)	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±40V, V+ = 0, V- = 0	+25°C	-20	0.1	20	nA
			C, E	-200		200	
			M	-10		10	µA
COM_ On-Clamp Output Current, Supply On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, V+ = +12V	+25°C	2	3	5	mA
COM_ On-Clamp Output Resistance, Supply On	$R_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, V+ = +12V	+25°C		2.4	5	kΩ
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E, M	2.4			V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E, M			0.8	V
IN_ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}	$V_{IN\_}$ = +0.8V or +2.4V	+25°C	-1	0.03	1	µA
			C, E, M	-5		5	

ELECTRICAL CHARACTERISTICS—Single Supply (continued)

(V+ = +12V, V- = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = +10V, R_L = 2kΩ; Figure 2	+25°C		200	500	ns
			C, E, M			1000	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = +10V, R_L = 2kΩ; Figure 2	+25°C		100	300	ns
			C, E, M			900	
Break-Before-Make Time Delay	t_{BBM}	$V_{COM\_}$ = +10V, R_L = 1kΩ; Figure 3	+25°C	5	100		ns
Charge Injection	Q	C_L = 100pF, $V_{COM\_}$ = 0; Figure 4	+25°C		2		pC
NO_ or NC_ Off-Capacitance	$C_{N\_(OFF)}$	f = 1MHz; Figure 5	+25°C		5		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz; Figure 5	+25°C		15		pF
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{NO\_}$ = $1V_{RMS}$, f = 1MHz; Figure 6	+25°C		-62		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{NO\_}$ = $1V_{RMS}$, f = 1MHz; Figure 6	+25°C		-65		dB
POWER SUPPLY							
Power-Supply Range	V+		C, E, M	9		36	V
V+ Supply Current	I+	All $V_{IN\_}$ = 0 or +5V, $V_{NO\_}$ = $V_{NC\_}$ = 0	+25°C			350	µA
			C, E, M			550	
V- and GND Supply Current	I_{GND}	All $V_{IN\_}$ = 0 or +12V, $V_{NO\_}$ = $V_{NC\_}$ = 0	+25°C			200	µA
			C, E, M			350	
		All $V_{IN\_}$ = 0 or +5V, $V_{NO\_}$ = $V_{NC\_}$ = 0	+25°C			350	µA
			C, E, M			550	

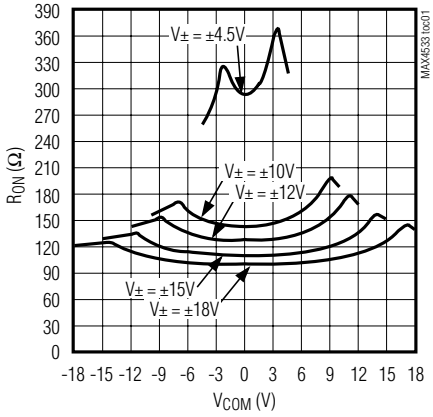
Note 3: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 4: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.
Note 5: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at T_A = +25°C.
Note 6: Guaranteed by design.
Note 7: Off-isolation = 20log10($V_{COM\_}$ / $V_{NO\_}$), $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.
Note 8: Between any two analog inputs.
Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

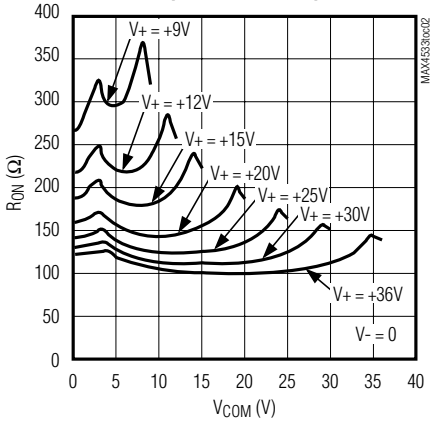
Typical Operating Characteristics

(V+ = +15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

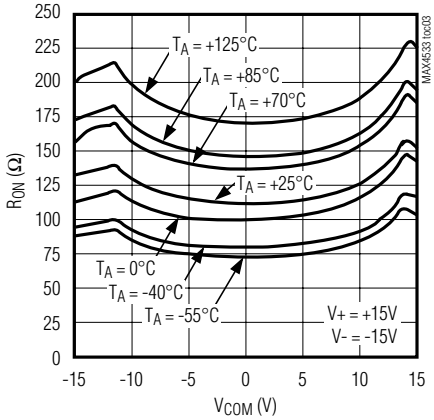
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



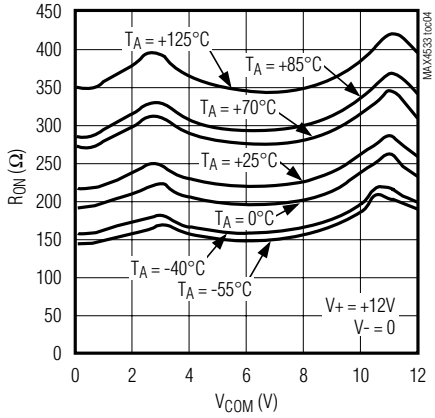
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



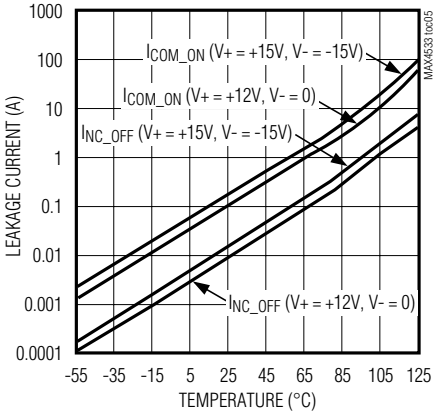
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



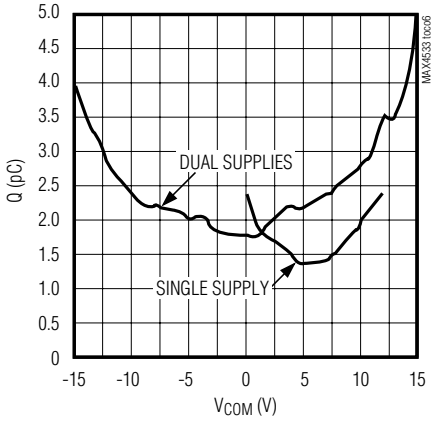
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



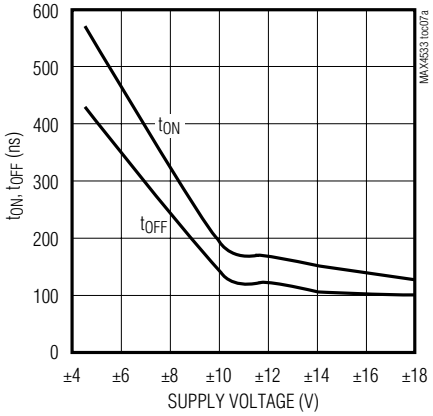
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



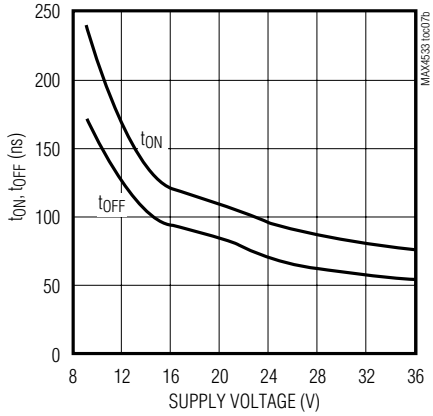
CHARGE INJECTION vs. V_{COM}



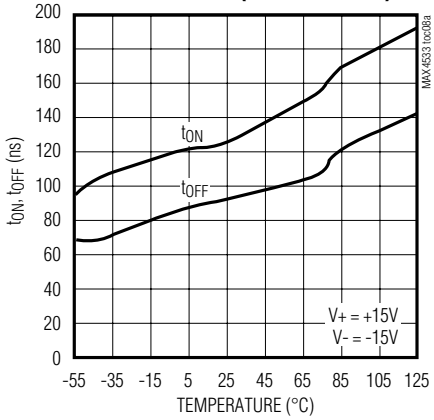
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE (DUAL SUPPLIES)



TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE (SINGLE SUPPLY)



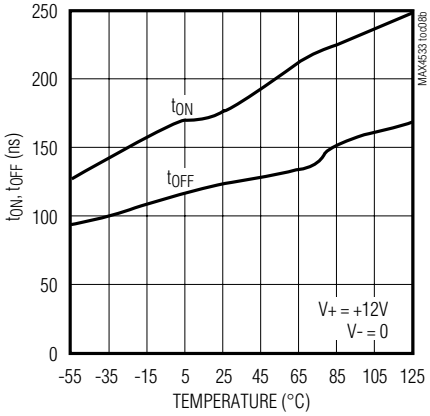
TURN-ON/TURN-OFF TIME vs. TEMPERATURE (DUAL SUPPLIES)



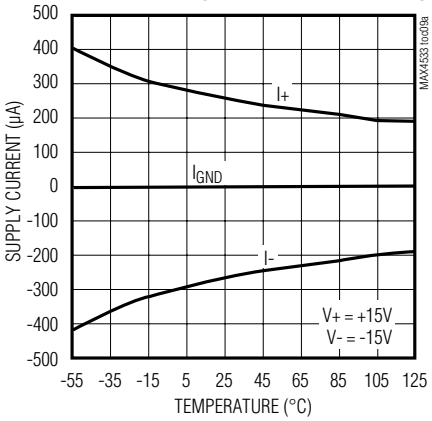
Typical Operating Characteristics (continued)

(V+ = +15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

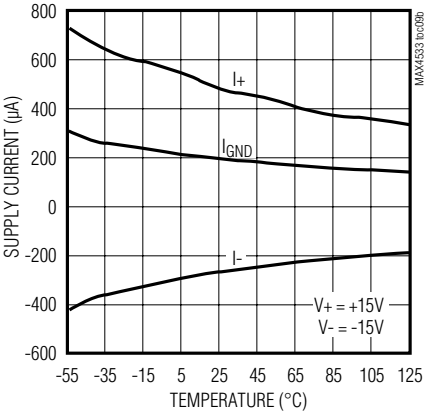
TURN-ON/TURN-OFF TIME vs. TEMPERATURE (SINGLE SUPPLY)



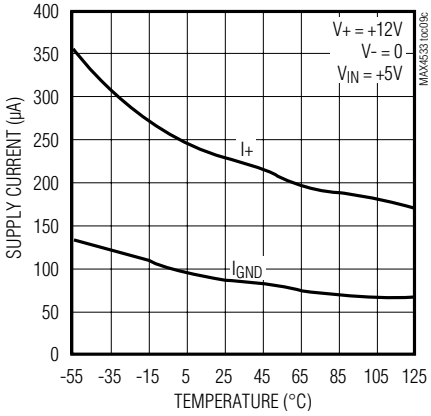
POWER-SUPPLY CURRENT vs. TEMPERATURE (DUAL SUPPLIES, V_{IN} = 0)



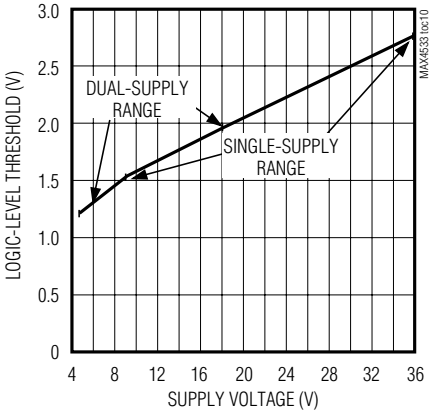
POWER-SUPPLY CURRENT vs. TEMPERATURE (DUAL SUPPLIES, V_{IN} = +5V)



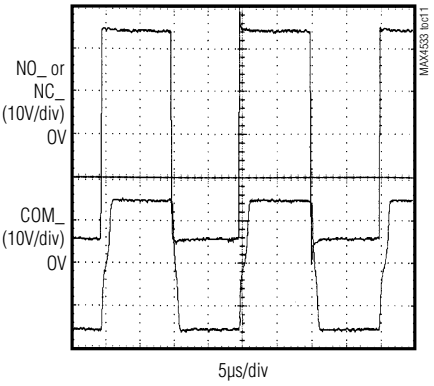
POWER-SUPPLY CURRENT vs. TEMPERATURE (SINGLE SUPPLY)



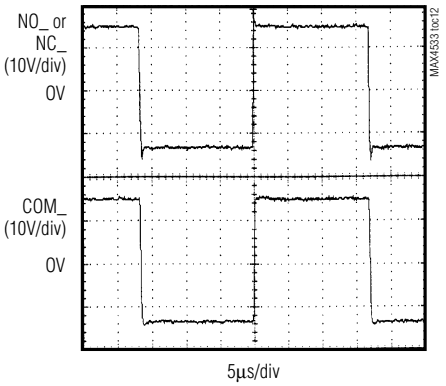
LOGIC-LEVEL THRESHOLD vs. SUPPLY VOLTAGE



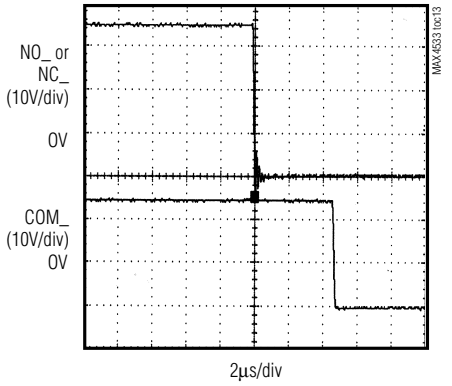
OVERVOLTAGE WITH ±25V INPUT



FAULT-FREE SIGNAL WITH ±15V INPUT



FAULT RECOVERY TIME

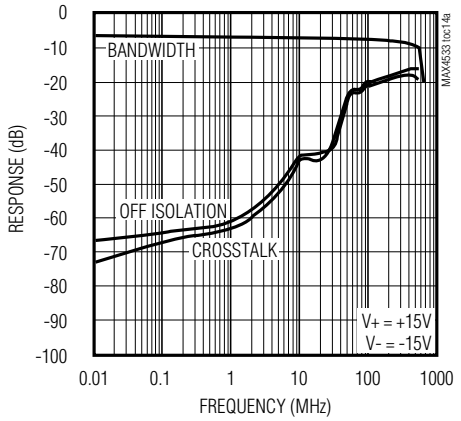


Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

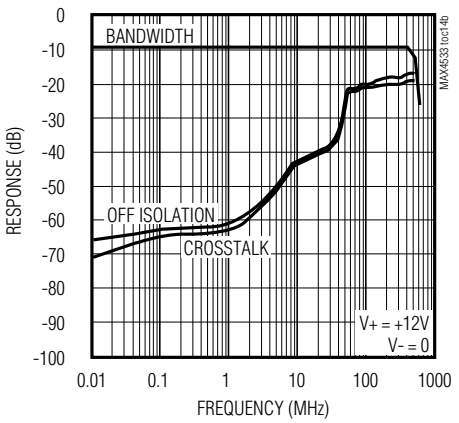
Typical Operating Characteristics (continued)

(V+ = +15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

FREQUENCY RESPONSE (DUAL SUPPLIES)



FREQUENCY RESPONSE (SINGLE SUPPLY)



Pin Description

PIN	NAME	FUNCTION
1, 10, 11, 20	IN1, IN2, IN3, IN4	Logic Control Digital Inputs
2, 9, 12, 19	NO1, NO2, NO3, NO4	Normally Open Inputs*
3, 8, 13, 18	COM1, COM2, COM3, COM4	Analog Switch Common Outputs*
4, 7, 14, 17	NC1, NC2, NC3, NC4	Normally Closed Inputs*
5	V-	Negative Analog Supply Voltage Input
6	GND	Digital Ground
15	N.C.	No Connection. Not internally connected.
16	V+	Positive Analog and Digital Supply-Voltage Input

**When the voltage on NO_ or NC_ does not exceed V+ or V-, NO_ (or NC_) and COM_ pins are bidirectional.*

Detailed Description

The MAX4533 is a fault-protected analog switch with special operation and construction. Traditional fault-protected switches are constructed using three-series CMOS devices. This combination produces good fault protection but fairly high on-resistance when the signals are within about 3V of each supply rail. These series devices are not capable of handling signals up to the power-supply rails.

The MAX4533 differs considerably from traditional fault-protected switches, with three advantages. First, it is constructed with two parallel FETs, allowing very low on-resistance when the switch is on. Second, they allow signals on the NC_ or NO_ pins that are within or slightly beyond the supply rails to be passed through the switch to the COM_ terminal, allowing rail-to-rail signal operation. Third, when a signal on NC_ or NO_ exceeds the supply rails by about 150mV (a fault condition), the voltage on COM_ is limited to the appropriate polarity supply voltage. Operation is identical for both fault polarities. The fault-protection extends to ±25V with power on and ±40V with power off.

The MAX4533 has a parallel N-channel and P-channel MOSFET switch configuration with input voltage sensors. The simplified internal structure is shown in Figure 1. The parallel N1 and P1 MOSFETs form the switch element. N3 and P3 are sensor elements to sample the input voltage and compare it against the power-supply rails.

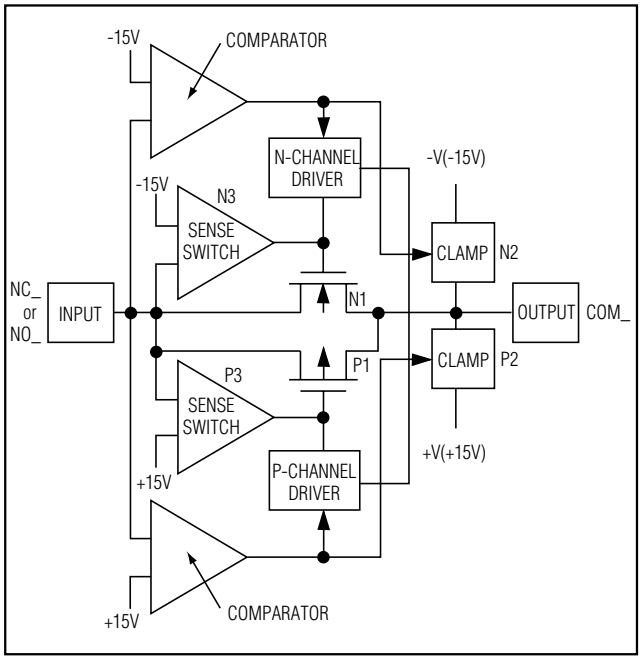


Figure 1. Simplified Internal Structure

During normal operation of a conducting channel, N1 and P1 remain on with a typical 125Ω on-resistance between NO_ (or NC_) and COM_. If the input voltage exceeds either supply rail by about 150mV, the parallel combination switches (N1, P1) are forced off through the driver and sensing circuitries. At the same time, the output (COM_) is clamped to the appropriate supply rail by the clamp circuitries (N2, P2). Two clamp circuits limit the output voltage to the supply voltages.

For simplicity, Figure 1 shows only one side of the SPDT switch configuration. The complete circuit is composed of two channels with their outputs connected.

Normal Operation

Two comparators continuously compare the voltage on the NO_ (or NC_) pin with V+ and V- supply voltages. When the signal on NO_ (or NC_) is between V+ and V-, the switch behaves normally, with FETs N1 and P1 turning on and off in response to NO_ (or NC_) signals (Figure 1). For any voltage between the supply rails, the switch is bidirectional; therefore, COM_ and NC_ (or NO_) are interchangeable. Only NO_ and NC_ can be exposed to overvoltages beyond the supply range and within the specified breakdown limits of the device.

Fault Condition

The MAX4533 protects devices connected to its output (COM_) through its unique fault-protection circuitry. When the input voltage is raised above either supply rail, the internal sense and comparator circuitries (N3 and N-channel driver or P3 and P-channel driver) disconnect the output (COM_) from the input (Figure 1).

If the switch driven above the supply rail has an on state, the clamp circuitries (N2 or P2) connect the output to the appropriate supply rail. Table 1 summarizes the MAX4533's operation under normal and fault conditions. Row 5 shows a negative fault condition when the supplies are on. It shows that with supplies of ±15V, if the input voltage is between -15V and -25V, the output (COM_) clamps to the negative supply rail of -15V. With this technique, the SPDT switch is capable of withstanding a worse-case condition of opposite fault polarities at its inputs.

Transient Fault Condition

When a fast rising or falling transient on NO_ (or NC_) exceeds V+ or V-, the output (COM_) follows the input (IN_) to the supply rail by only a few nanoseconds. This delay is due to the switch on-resistance and circuit capacitance to ground. However, when the input transient returns to within the supply rails there is a longer recovery time. For positive faults, the recovery time is typically 2.5µs. For negative faults, the recovery time is typically 1.3µs. These values depend on the COM_ output resistance and capacitance. The delays are not dependent on the fault amplitude. Higher COM_ output resistance and capacitance increase the recovery times.

Fault Protection, Voltage, and Power Off

The maximum fault voltage on the NO_ or NC_ pins is ±40V from ground when the power is off. With ±15V supply voltages, the highest voltage on NO_ (or NC_) can be +25V, and the lowest voltage on NO_ (or NC_) can be -25V. Exceeding these limits can damage the chip.

IN_ Logic-Level Thresholds

The logic-level thresholds are TTL/CMOS-compatible when V+ is +15V. Raising V+ increases the threshold slightly; when V+ reaches +25V, the level threshold is 2.8V—higher than the TTL output high-level minimum of 2.4V, but still compatible with CMOS outputs (see the *Typical Operating Characteristics*).

Increasing V- has no effect on the logic-level thresholds, but it does increase the gate-drive voltage to the signal FETs, reducing their on-resistance.

Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

Table 1. Switch States in Normal and Fault Conditions

POWER SUPPLIES (V+, V-)	INPUT RANGE	NC_	NO_	OUTPUT
On	Between Rails	On	Off	NC_
On	Between Rails	Off	On	NO_
On	Between V+ and (+40V - V+)	On	Off	V+
On	Between V+ and (+40V - V+)	Off	On	V+
On	Between V- and (-40V - V-)	On	Off	V-
On	Between V- and (-40V - V-)	Off	On	V-
Off	Between Rails	Off	Off	Follows the load terminal voltage.

Failure Modes

The MAX4533 is not a lightning arrester or surge protector. Exceeding the fault-protection voltage limits on NO_ or NC_, even for very short periods, can cause the device to fail.

Applications Information

Ground

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the switches. This drive signal is the only connection between the power supplies and the analog signals. GND, IN_, and COM_ have ESD protection diodes to V+ and V-.

Supply Current Reduction

When the logic signals are driven rail-to-rail from 0 to +12V or -15V to +15V, the supply current reduces to approximately half of the supply current when the logic input levels are at 0 to 5V.

Power Supplies

The MAX4533 operates with bipolar supplies between ±4.5V and ±18V. The V+ and V- supplies need not be symmetrical, but their difference can not exceed the absolute maximum rating of +44V. The MAX4533 operates from a single supply between +9V and +36V when V- is connected to GND.

Test Circuits/Timing Diagrams

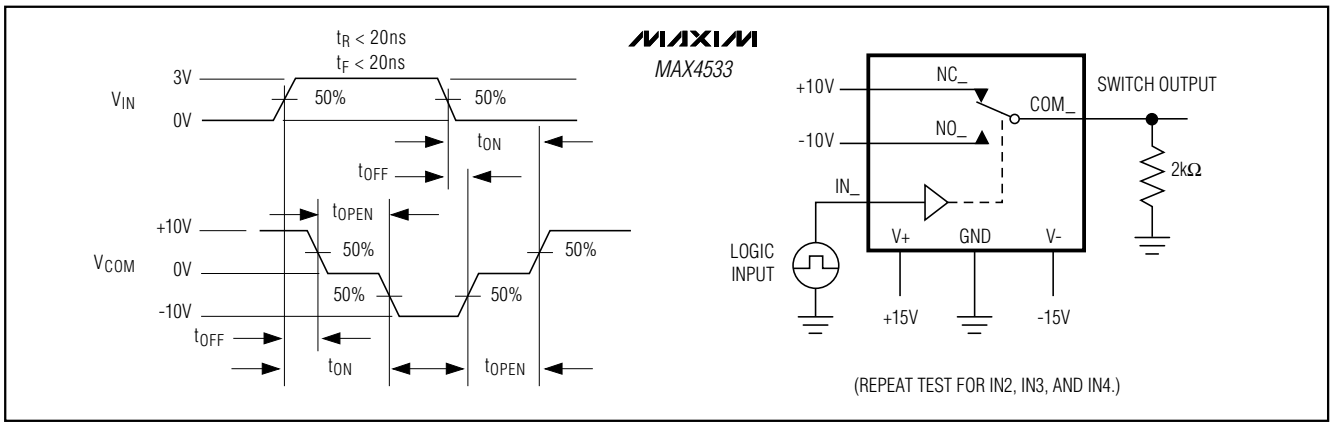


Figure 2. Switching-Time Test Circuit

Test Circuits/Timing Diagrams (continued)

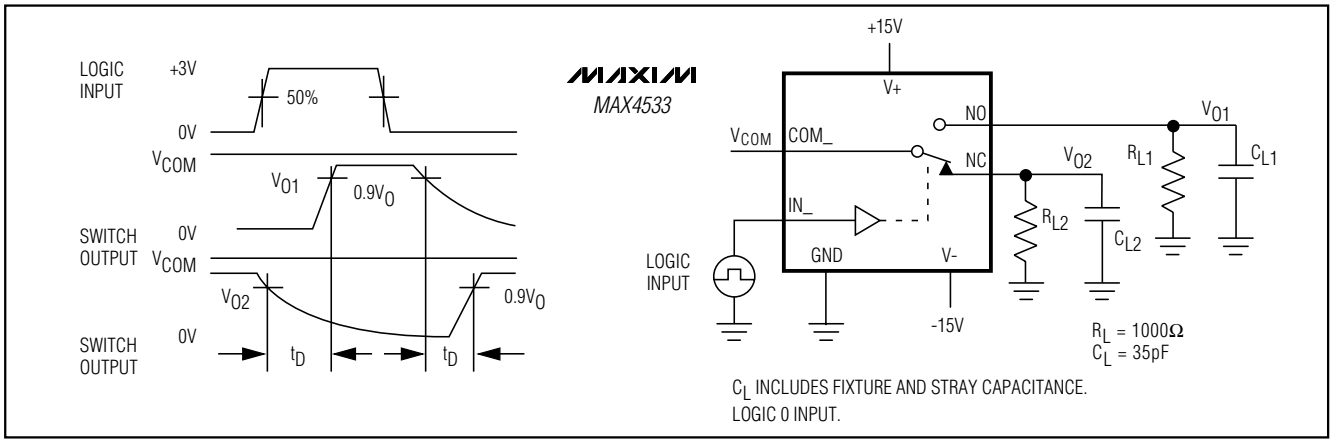


Figure 3. Break-Before-Make

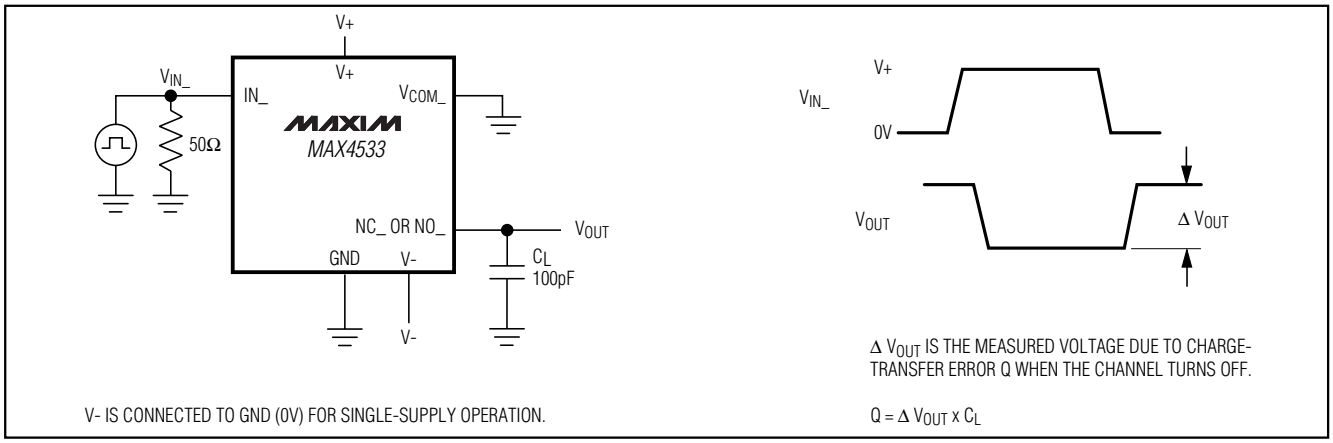


Figure 4. Charge Injection

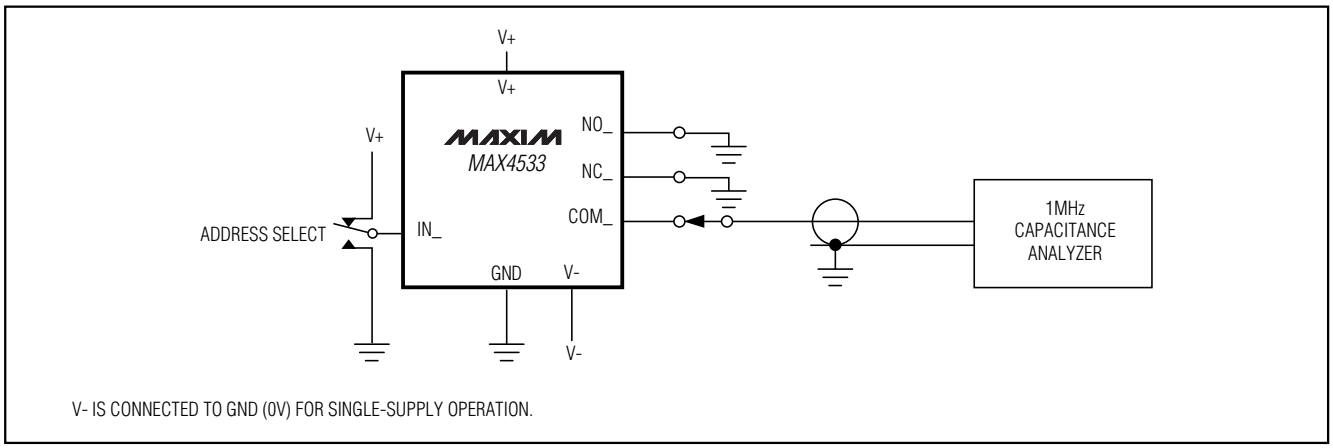
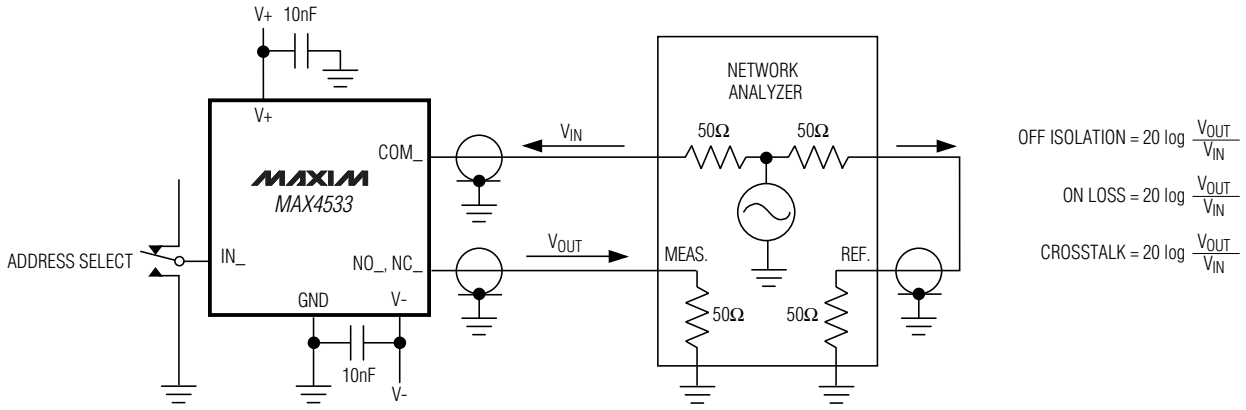


Figure 5. COM_, NO_, NC_ Capacitance

Quad, Rail-to-Rail, Fault-Protected, SPDT Analog Switch

Test Circuits/Timing Diagrams (continued)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORTS AT SOCKET TERMINALS.
OFF ISOLATION IS MEASURED BETWEEN COM_ AND "OFF" NO_ OR NC_ TERMINALS.
ON LOSS IS MEASURED BETWEEN COM_ AND "ON" NO_ OR NC_ TERMINALS.
CROSSTALK IS MEASURED BETWEEN COM_ TERMINALS WITH ALL SWITCHES ON.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.
V- IS CONNECTED TO GND (0V) FOR SINGLE-SUPPLY OPERATION.

Figure 6. Frequency Response, Off-Isolation, and Crosstalk

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4533CPP	0°C to +70°C	20 Plastic DIP
MAX4533EAP	-40°C to +85°C	20 SSOP
MAX4533EWP	-40°C to +85°C	20 Wide SO
MAX4533EPP	-40°C to +85°C	20 Plastic DIP
MAX4533MJP	-55°C to +125°C	20 CERDIP

Chip Information

TRANSISTOR COUNT: 448

MAX4533

Part Number Table

Notes:

1. See the MAX4533 QuickView Data Sheet for further information on this product family or download the MAX4533 full data sheet (PDF, 224kB).
2. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
3. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See full data sheet or Part Naming Conventions.
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX4533C/D					RoHS/Lead-Free: No
MAX4533CPP+			PDIP;20 pin;.300" Dwg: 21-0043D (PDF) Use pkgcode/variation: P20+2*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533EPP+			PDIP;20 pin;.300" Dwg: 21-0043D (PDF) Use pkgcode/variation: P20+2*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533CPP			PDIP;20 pin;.300" Dwg: 21-0043D (PDF) Use pkgcode/variation: P20-2*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4533EPP			PDIP;20 pin;.300" Dwg: 21-0043D (PDF) Use pkgcode/variation: P20-2*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4533CWP+T			SOIC;20 pin;.300" Dwg: 21-0042B (PDF) Use pkgcode/variation: W20+4*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533CWP+			SOIC;20 pin;.300" Dwg: 21-0042B (PDF) Use pkgcode/variation: W20+4*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis

MAX4533CWP-T			SOIC;20 pin;.300" Dwg: 21-0042B (PDF) Use pkgcode/variation: W20-4*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4533CWP			SOIC;20 pin;.300" Dwg: 21-0042B (PDF) Use pkgcode/variation: W20-4*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4533EWP			SOIC;20 pin;.300" Dwg: 21-0042B (PDF) Use pkgcode/variation: W20-4*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4533EWP-T				-40C to +85C	RoHS/Lead-Free: No
MAX4533CAP			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20-2*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4533CAP+T			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20+2*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533CAP+			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20+2*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533CAP-T			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20-2*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX4533EAP+			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20+2*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533EAP+T			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20+2*	-40C to +85C	RoHS/Lead-Free: Yes Materials Analysis
MAX4533EAP			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20-2*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX4533EAP-T			SSOP;20 pin;.209" Dwg: 21-0056C (PDF) Use pkgcode/variation: A20-2*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis

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