32K x 8 Bit High-Speed CMOS Static RAM (3.3V Operating)

FEATURES

- Fast Access Time 15, 17ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 0.1mA(Max.)
  - Operating KM68V257C - 15 : 90mA(Max.)
  - KM68V257C - 17 : 80mA(Max.)
- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V (Min)
- Standard Pin Configuration
  - KM68V257CJ : 28-SOJ-300
  - KM68V257CTG : 28-TSOP1-0813, 4F

GENERAL DESCRIPTION

The KM68V257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68V257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V257C is packaged in a 300mil 28-pin plastic SOJ or TSOP1 forward.

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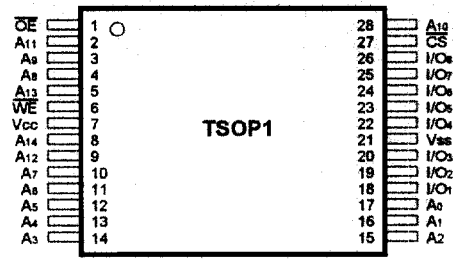
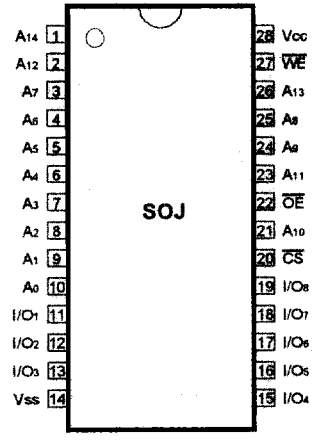
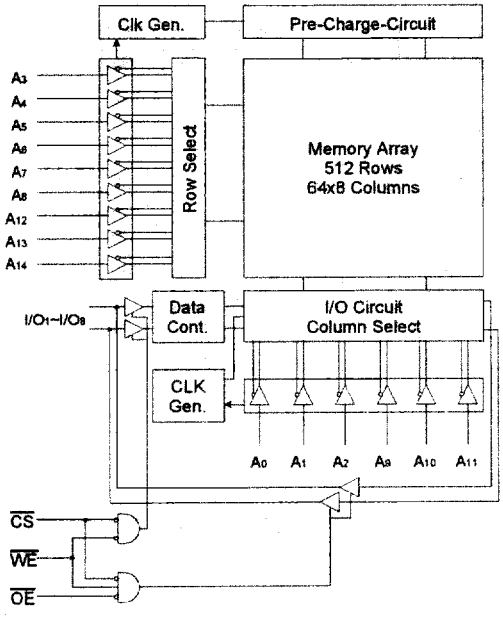
PIN CONFIGURATION *(Top View)*





FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION

Pin Name	Pin Function
A0 - A14	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width≤12ns) for I≤20mA
** V_{IH}(Max) = V_{CC}+2.0V(Pulse Width≤12ns) for I≤20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C,Vcc= 3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	90	mA
			17ns	-	80	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V		-	0.1	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

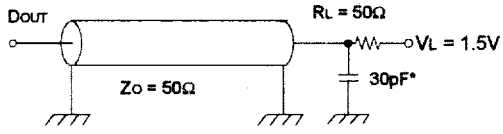
* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise noted.)

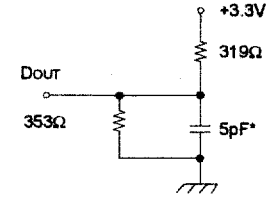
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE

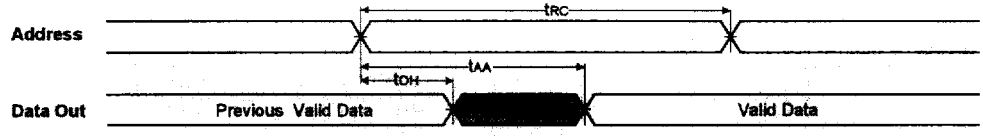
Parameter	Symbol	KM68V257C-15		KM68V257C-17		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	17	-	ns
Address Access Time	t_{AA}	-	15	-	17	ns
Chip Select to Output	t_{CO}	-	15	-	17	ns
Output Enable to Valid Output	t_{OE}	-	7	-	8	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	ns
Chip Selection to Power DownTime	t_{PD}	-	15	-	17	ns

WRITE CYCLE

Parameter	Symbol	KM68V257C-15		KM68V257C-17		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15	-	17	-	ns
Chip Select to End of Write	t_{CW}	11	-	12	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	15	-	17	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	6	0	6	ns
Data to Write Time Overlap	t_{DW}	8	-	8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	0	-	0	-	ns

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



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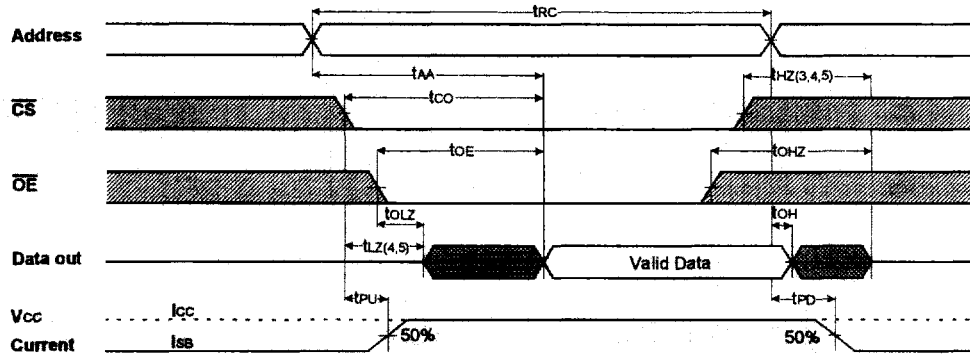
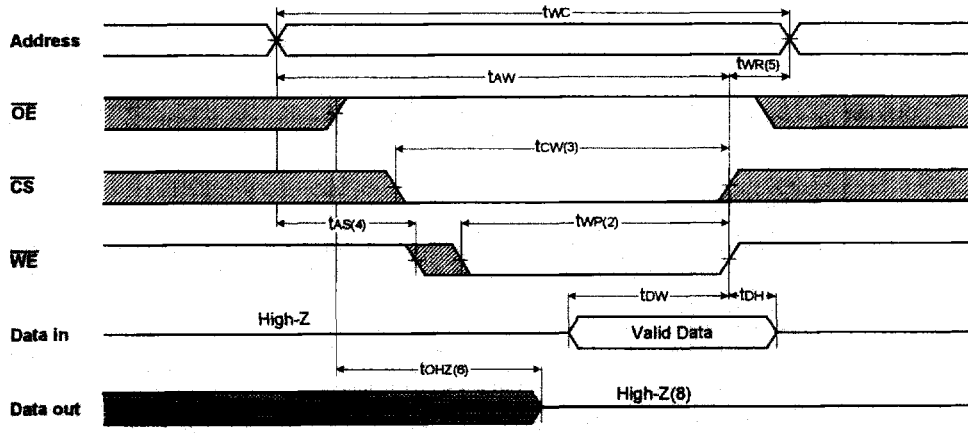
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$= Clock)



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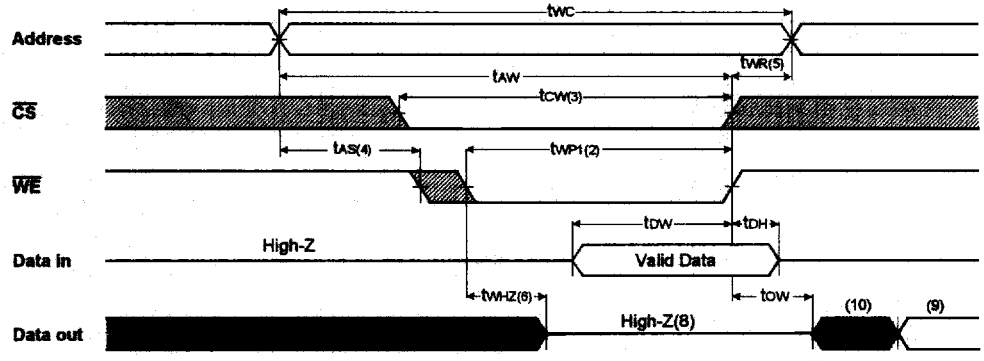
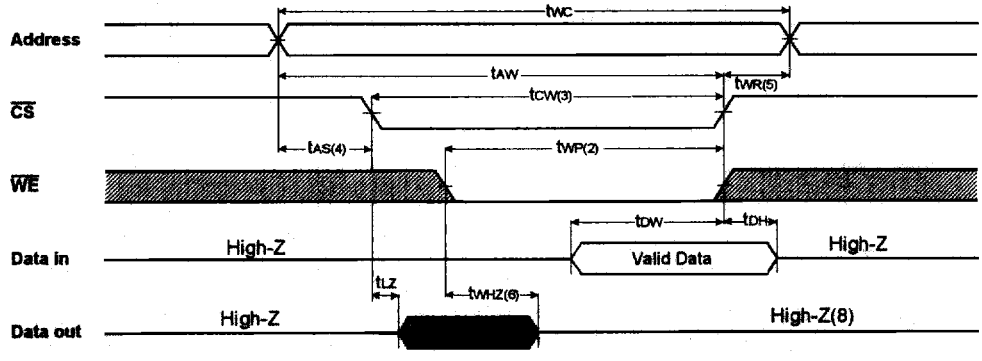
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$= Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V	-	-	0.07	mA
Data Retention Set-Up Time	t_{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t_{RDR}		5	-	-	ms

DATA RETENTION WAVE FORM