FM 1208S FRAM® Memory

4,096-Bit Nonvolatile Ferroelectric RAM
Product Specification

Features

- 4,096 Bit Bytewide Nonvolatile Ferroelectric RAM
  Organized as 512 x 8
- CMOS Technology with Integrated Ferroelectric Storage Cells
- Fully Synchronous Operation
  - 250ns Read Access
  - 500ns Read/Write Cycle Time
  - Minimum of 10^8 Endurance Cycles
- On Chip Data Protection Circuit
- 10 Year Data Retention without Power
- Single 5 Volt ±10% Supply
- Low Power Consumption
  - Active Current: 10mA
  - Standby Current: 100µA
- CMOS/TTL Compatible I/O Pins
- 24 Pin Ceramic/Plastic DIP and Skinny DIP, and Plastic SOP Packages
- 0 to 70°C Ambient Operating Temperature Range

Description

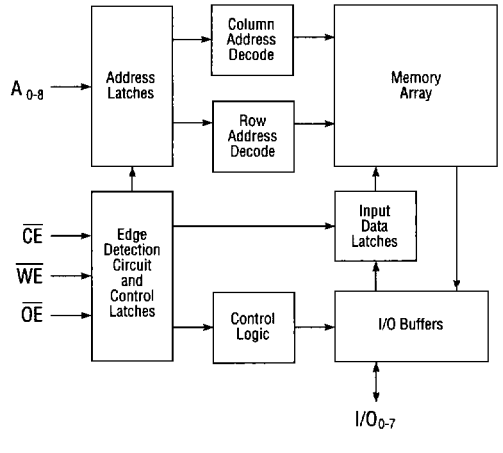
The FM 1208S is a bytewide ferroelectric RAM, or FRAM® product organized as 512 x 8. FRAM memory products from Ramtron combine the read/write characteristics of semiconductor RAM with the nonvolatile retention of magnetic storage.

This product is manufactured in a 1.5 micron Si gate CMOS technology with the addition of integrated thin film ferroelectric storage cells developed and patented by Ramtron.

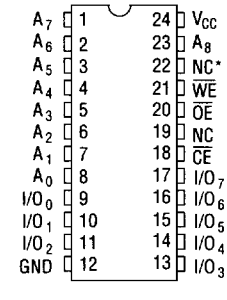
The ferroelectric cells are polarized on each read or write cycle, therefore no special store recall sequence is required. The memory is always static and nonvolatile.

Ramtron's FRAM products operate from a single +5 volt power supply and are TTL/CMOS compatible on all inputs and outputs. The FM 1208S utilizes the JEDEC standard bytewide SRAM pinout.

Functional Diagram



Pin Configuration



* Must be Unconnected or Tied to GND

© Ramtron International Corporation, 1850 Ramtron Drive, Colorado Springs, CO 80921
Telephone (800) 545-FRAM, (719) 481-7000, **Fax** (719) 488-9095

Pin Names

Pin Names	Function
A_0 - A_8	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	+5 Volts
GND	Ground
NC	No Connect

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	0 to 70°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	0 to 3 V
Input Rise and Fall Time	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 50pF

Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Parameter	Description	Max	Test Condition
$C_{I/O}$ (1)	Input/Output Capacitance	8pF	$V_{I/O}$ = 0V
C_{IN} (1)	Input Capacitance	6pF	$V_{I/O}$ = 0V

(1) This parameter is periodically sampled and not 100% tested.

DC Operating Conditions

T_A = 0° to 70°C Unless Otherwise Noted

Symbol	Parameters	Min	Max	Test Condition
V_{CC}	Power Supply Voltage	4.75V	5.25V	
I_{CC1}	Power Supply Current - Active		10mA	V_{CC} = Max, $\overline{CE}$ and $\overline{OE}$ Cycling at Minimum Cycle Time $\overline{WE}$ = V_{CC}, CMOS Input Levels and I/Os Unloaded
I_{CC2}	Power Supply Current - Standby		100µA	V_{CC} = Max, $\overline{CE}$ = V_{CC} Other Inputs Can Cycle at Minimum Cycle Time
I_{IL}	Input Leakage Current		10µA	V_{IN} = GND to V_{CC}
I_{OL}	Output Leakage Current		10µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	-1V	0.8V	
V_{IH}	Input High Voltage	2.0V	V_{CC} + 1V	
V_{OL}	Output Low Voltage		0.4V	I_{OL} = 4.2mA
V_{OH}	Output High Voltage	2.4V		I_{OH} = -2mA

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Function
H	X	X	Standby/Precharge
↘	X	X	Latch Address
L	H	L	Read
L	L	X	Write

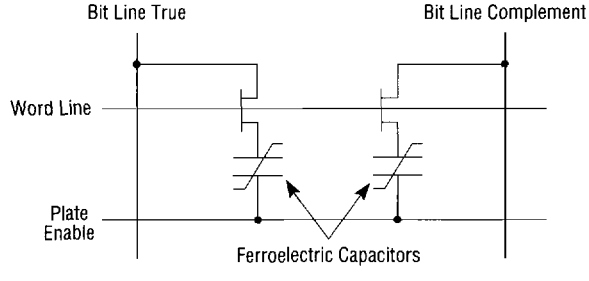
Theory of Operation

The FM 1208S memory uses a two transistor, two capacitor memory structure illustrated below.

The FRAM memory utilizes the bistable characteristic of the ferroelectric cell to store data.

During a write operation, data is transferred from the I/O pins to the bit lines. When the word line pass transistor is enabled and the common plate is pulsed, the data will be stored by polarizing the ferroelectric cell in one of two states. To read data, the pass transistor is enabled and the sense amplifier senses the difference in polarization of the ferroelectric cells to determine the stored data state. Since the read operation is destructive, the data is then automatically rewritten back to the ferroelectric cell by switching the polarization. The memory can be cycled up to 10^8 cycles without degrading the data retention characteristics of the memory.

Dual Memory Capacitor Cell

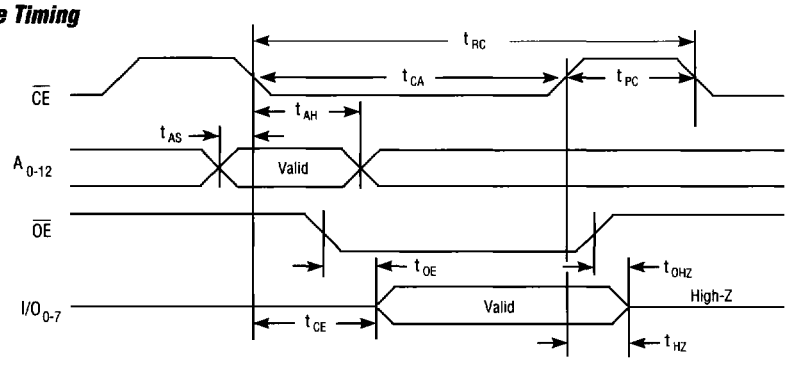


Read Cycle

The FRAM memory operates synchronously using the CE signal as the clock. The memory read cycle time t_{RC} is measured between falling edges of CE. The CE signal must be active for time t_{CA}. The memory requires a minimum precharge time t_{PC} to precharge the internal busses between operations.

The memory latches the address internally on the falling edge of CE. The address data must meet a minimum setup time t_{AS} and hold time t_{AH} relative to a clock edge. Read data is valid a maximum access time t_{CE} after the beginning of the read cycle. The OE signal is used to gate the data to the I/O pins. It must be enabled time t_{OE} prior to the time data is required on the I/O pins. Output data remains valid on the outputs until disabled by either the rising edge of OE or CE. The output becomes high-Z after time t_{HZ} from the CE signal or time t_{OHZ} from the OE signal. The WE signal should be high during the entire read operation.

Read Cycle Timing



Read Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V ± 10% Unless Otherwise Noted

Symbol	Parameter	JEDEC Symbol	Min	Max	Unit
			-250		
t_{RC}	Read Cycle Time	t ELEL	500		ns
t_{CA}	Chip Enable Active Time	t ELEH	250	10,000	ns
t_{PC}	Precharge Time	t EHEL	250		ns
t_{AS}	Address Setup Time	t AVEL	0		ns
t_{AH}	Address Hold Time	t ELAX	30		ns
t_{CE}	Chip Enable Access Time	t ELQV		250	ns
t_{OE}	Output Enable Access Time	t OLQV		30	ns
t_{HZ}	Chip Enable to Output High-Z	t EHQZ		45	ns
t_{OHZ}	Output Enable to Output High-Z	t OHQZ		35	ns

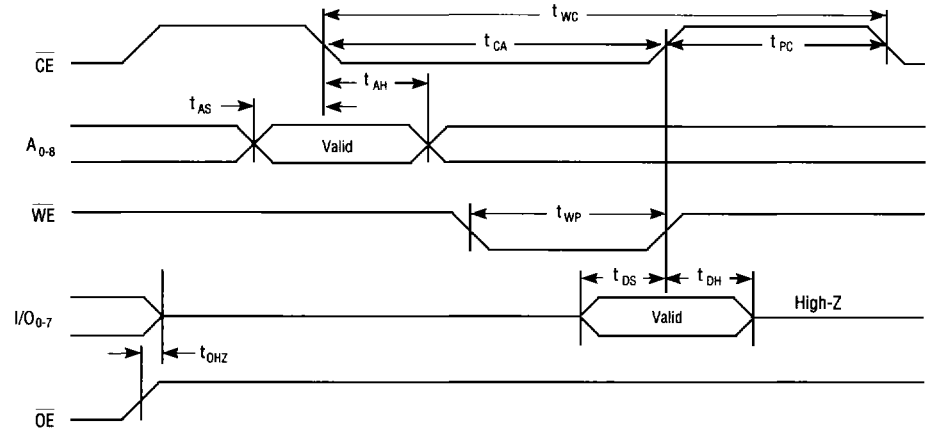
Write Cycle

The FM 1208S operates synchronously using the CE signal as a clock. The memory write cycle time t_{WC} is measured between falling edges of CE. The CE signal must be active for time t_{CA}. The memory requires a minimum precharge time t_{PC} to precharge the internal busses between operations.

The memory latches the addresses internally on the falling edge of $\overline{CE}$. The address data must meet a minimum setup time t_{AS} and hold time t_{AH} relative to the clock edge.

The data must be valid on the I/O pins time t_{DS} prior to the rising edge of $\overline{WE}$ and held time t_{DH} after $\overline{WE}$. $\overline{WE}$ must be stable time t_{WP} prior to the rising edge of CE. The $\overline{OE}$ signal must disable the chip outputs time t_{OHZ} prior to placing data on the I/O pins to prevent a data conflict.

Write Cycle Timing



Write Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 5V ± 10% Unless Otherwise Noted

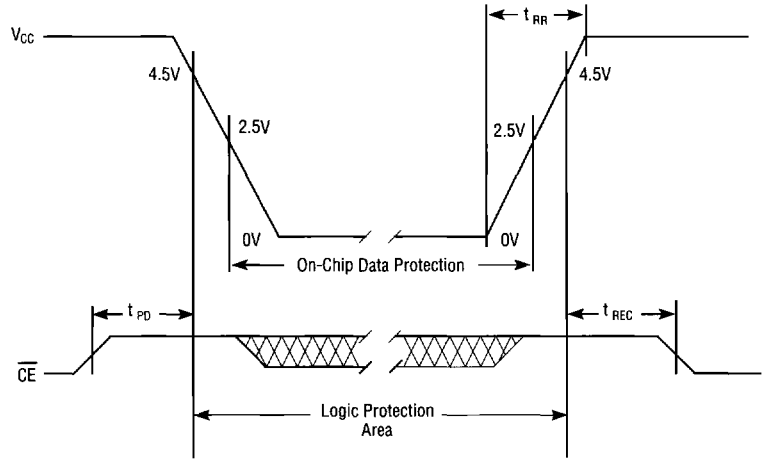
Symbol	Parameter	JEDEC Symbol	Min	Max	Unit
			-250		
t_{WC}	Write Cycle Time	t_{ELEL}	500		ns
t_{CA}	Chip Enable Active Time	t_{ELEH}	250	10,000	ns
t_{PC}	Precharge Time	t_{EHEL}	250		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		ns
t_{AH}	Address Hold Time	t_{ELAX}	30		ns
t_{WP}	Write Enable Pulse Width	t_{WLWH}	80		ns
t_{DS}	Data Setup Time	t_{DVWH}	80		ns
t_{DH}	Data Hold Time	t_{WHDX}	5		ns
t_{OHZ}	Output Enable to Output High-Z	t_{OHQZ}		35	ns

Power-Down/Power-Up Conditions

Care must be taken during power sequencing to prevent data loss resulting from memory operations during out of spec voltage conditions. This is managed by detecting power failure with sufficient time to disable memory operation time t_{PD} prior to V_{CC} reaching its lower specification, +4.5 volts. During power up, the memory operation should be disabled until time t_{REC} after V_{CC} reaches its operating voltage, +4.5 volts.

The memory has an on-chip data protection circuit which prevents memory operation when V_{CC} is less than +2.5 volts. This will protect the data in CMOS systems where the system control logic continues to function to +2.5 volts. However, external circuitry is required to force CE to a high level in systems with control logic that does not operate to +2.5 volts to prevent false memory operations from being initiated by the system control logic during this unspecified voltage range. There are a number of precision DC voltage detector circuits available to implement this function.

Power-Down/Power-Up Conditions

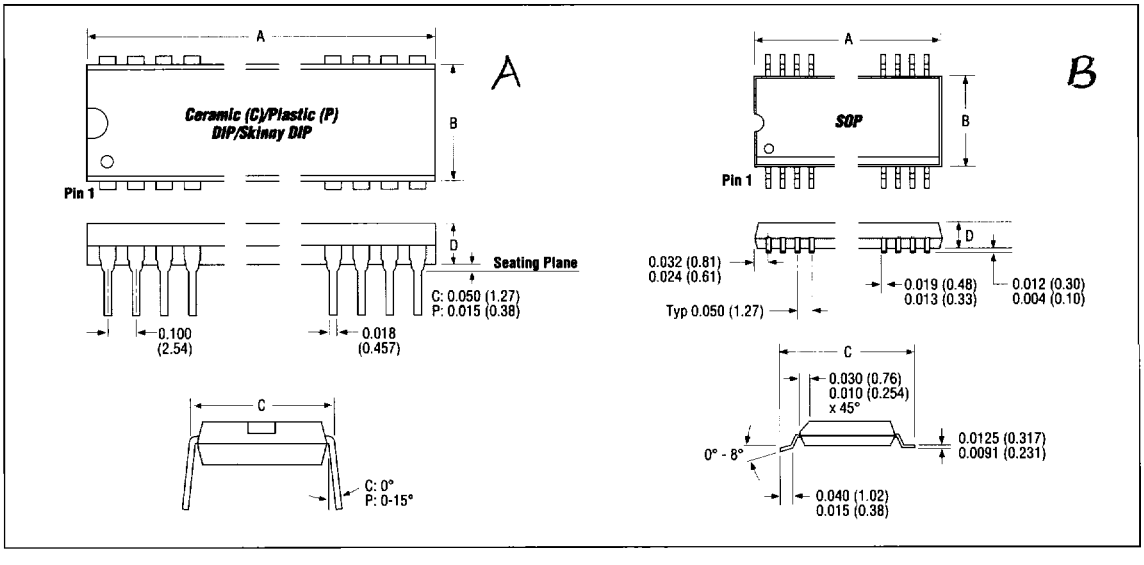


Power-Down/Power-Up AC Parameters

Symbol	Parameter	Min	Max	Unit
t_{PD}	Control Signals Stable to Power-Down	250		ns
t_{REC}	Power-Up to Operation		250	ns
t_{RR}	Power-Up Ramp Rate (0-5V)	100		µs

Packaging Information

Package	Type	Dimensions in Inches (Millimeters)			
		FM 1208S 24-Pin			
		A	B	C	D
Ceramic DIP	D 1	1.200 (30.48)	0.595 (15.113)	0.600 (15.24)	0.100 (2.54)
Ceramic Skinny DIP	DS 2	1.200 (30.48)	0.295 (7.49)	0.300 (7.62)	0.100 (2.54)
Plastic DIP	P 3	1.250 (31.75)	0.540 (13.72)	0.600 (15.24)	0.150 (3.81)
Plastic Skinny DIP	PS 4	1.185 (30.10)	0.260 (6.60)	0.300 (7.62)	0.130 (3.30)
Plastic SOP	S B	0.614 (15.59) 0.598 (15.19)	0.300 (7.62) 0.287 (7.29)	0.416 (10.57) 0.398 (10.11)	0.094 (2.34) 0.090 (2.29)



Ordering Information