SRAM

128K x 8 SRAM
WITH OUTPUT ENABLE

FEATURES
- High speed: 12*, 15*, 17, 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS — MARKING
- Timing
  - 12ns access — -12*
  - 15ns access — -15*
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
  - 45ns access — -45
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ

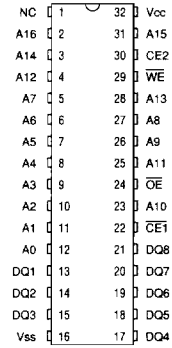
NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention — L
- 2V data retention, low power — LP
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C1008DJ-25 LP IT

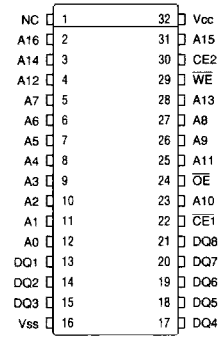
*Preliminary

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-7, SA-8)



32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

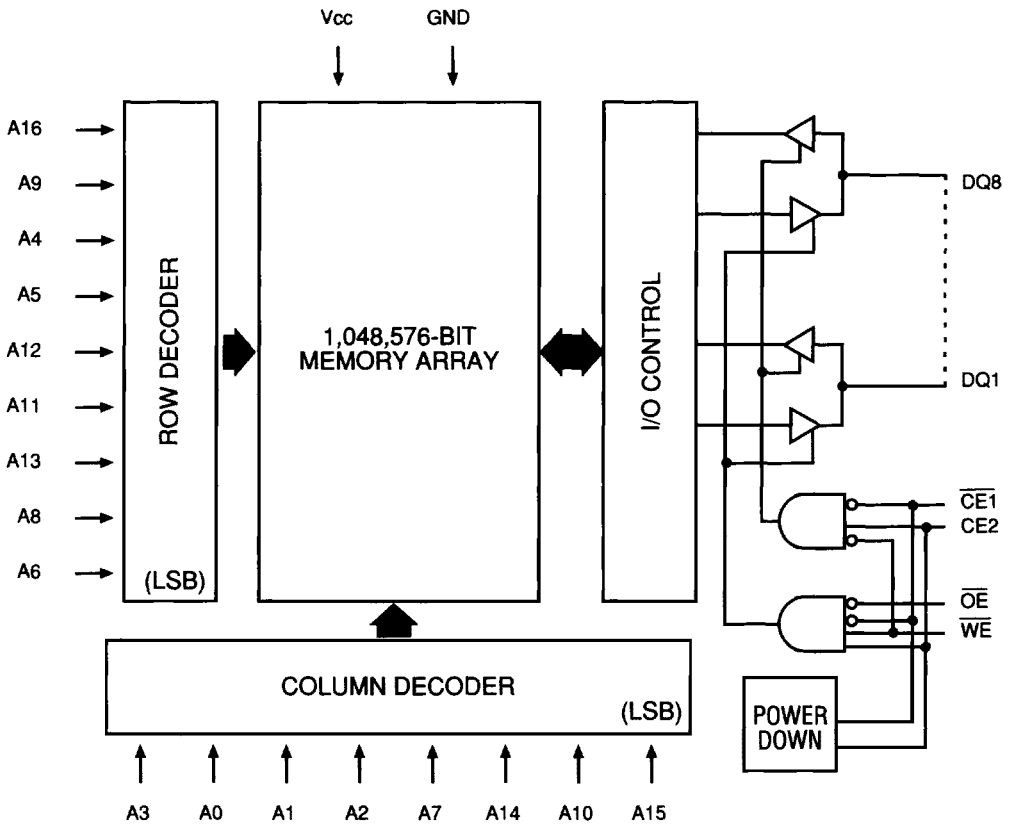
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and an output enable ($\overline{OE}$). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers reduced power standby modes when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12+	-15+	-17	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$CE2 \ge V_{IH}$; $\overline{CE1} \le V_{IL}$; V_{CC} = MAX; f = MAX = 1/ ^tRC; Outputs Open	I_{CC}	95	190	165	155	140	125	115	110	mA	3, 15
Power Supply Current: Standby	$CE2 \le V_{IH}$ or $\overline{CE1} \ge V_{IH}$; V_{CC} = MAX; f = MAX = 1/ ^tRC; Outputs Open	I_{SB1}	17	45	40	40	35	30	25	25	mA	15
	"LP" Version Only	I_{SB1}	1.3	3	3	3	3	3	3	3	mA	15
	$CE2 \le V_{SS}$ +0.2V; $\overline{CE1} \ge V_{CC}$ -0.2V; V_{CC} = MAX; $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	5	5	5	mA	15
	"L" and "LP" Versions Only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	15

+Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12*		-15*		-17		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	12		15		17		20		25		35		45		ns	
Address access time	^tAA		12		15		17		20		25		35		45	ns	
Chip Enable access time	^tACE		12		15		17		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		7		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		17		20		25		35		45	ns	
Output Enable access time	^tAOE		4		5		5		6		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		5		6		10		12		15	ns	6
WRITE Cycle																	
WRITE cycle time	^tWC	12		15		17		20		25		35		45		ns	
Chip Enable to end of write	^tCW	8		10		12		12		15		20		25		ns	
Address valid to end of write	^tAW	8		10		12		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		12		15		20		25		ns	
WRITE pulse width	$^tWP2$	10		12		13		15		15		20		25		ns	
Data setup time	^tDS	6		7		8		8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		15		18	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

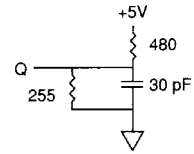


Fig. 1 OUTPUT LOAD EQUIVALENT

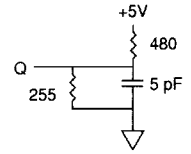


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

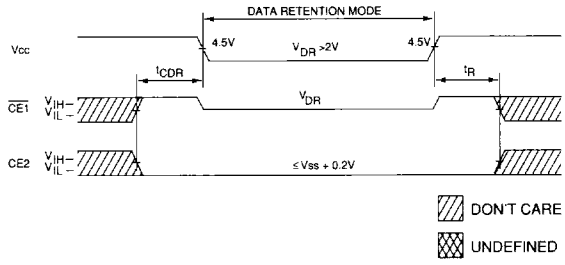
1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
15. Typical values are measured at 5V, 25°C and 25ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

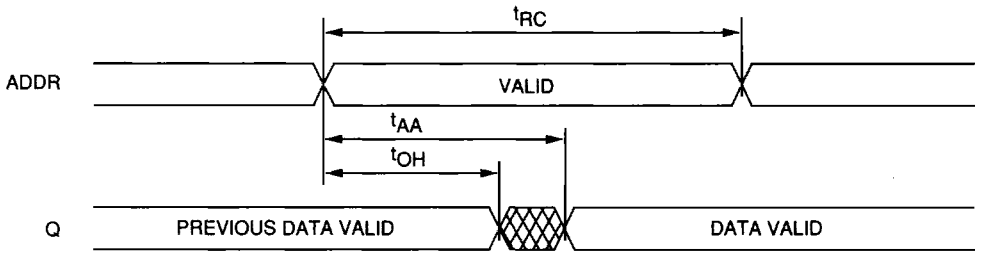
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	150	µA	
		Vcc = 3V			60	250	µA	
		Vcc = 3V*			30	100	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

*Preliminary

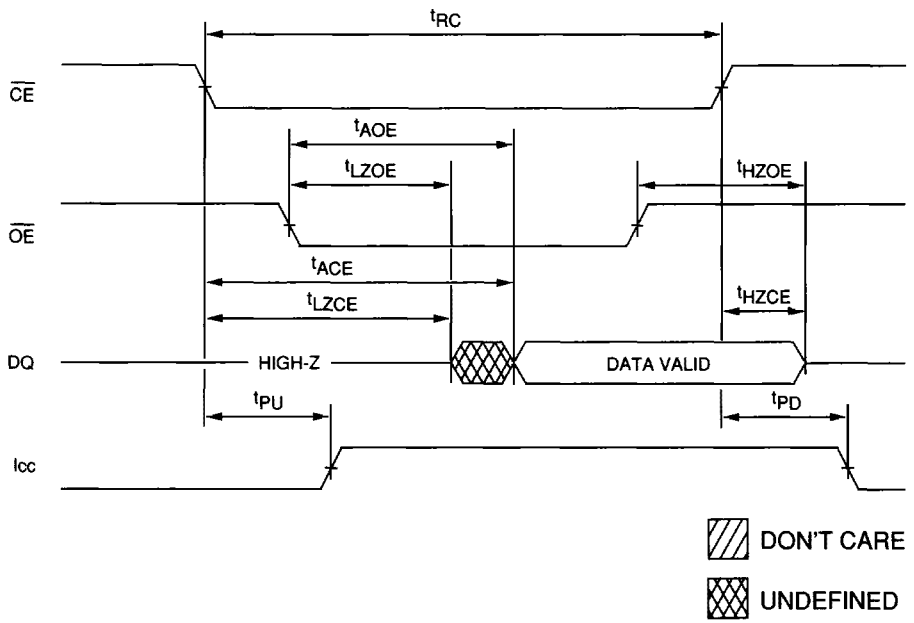
LOW Vcc DATA RETENTION WAVEFORM



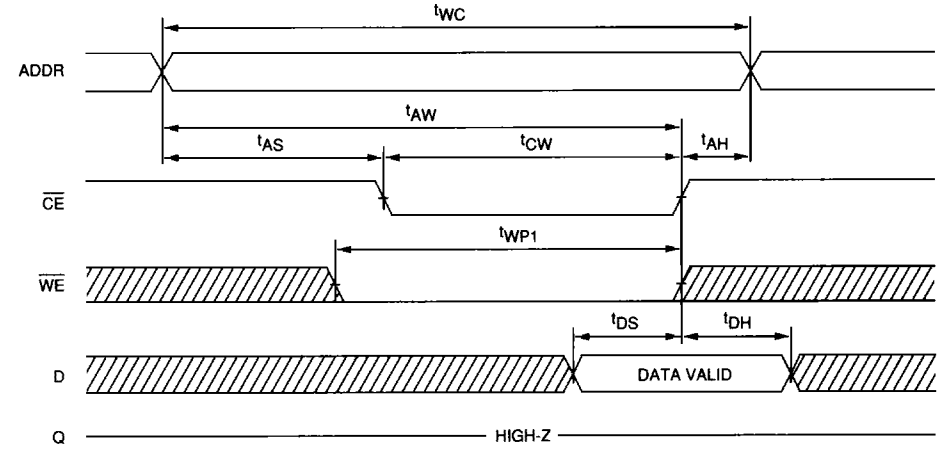
READ CYCLE NO. 1 [8, 9]



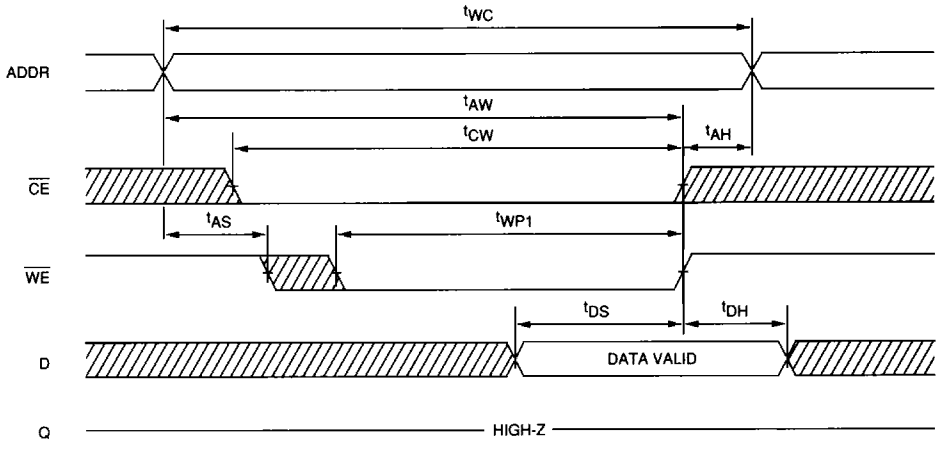
READ CYCLE NO. 2 [7, 8, 10, 12]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)

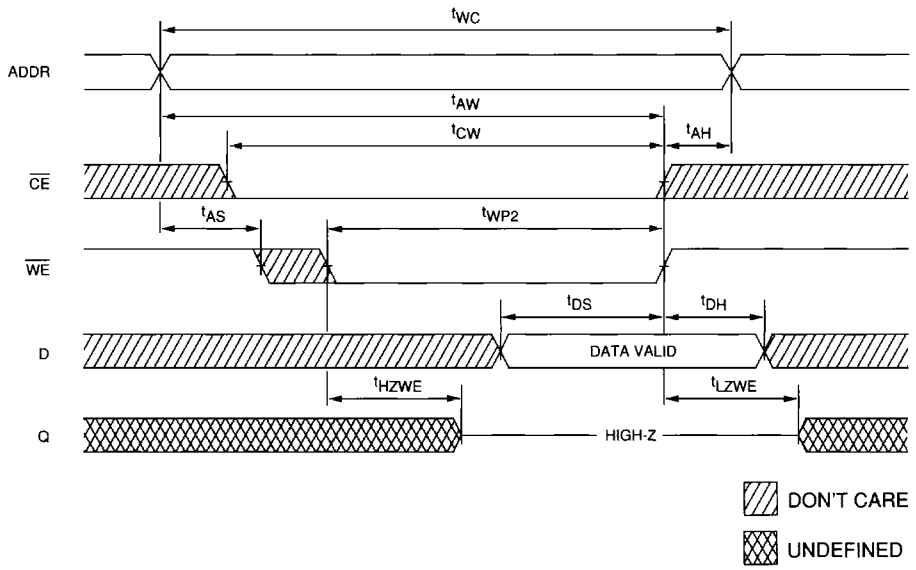


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).