M2N1G64TU8HA2B (Green)   **Preliminary Edition**
1GB : 128M x 64
PC2-3200 / PC2-4200 / PC2-5300 Unbuffered DDR2 SO-DIMM

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200 pin Unbuffered DDR2 SO-DIMM
Based on 64Mx8 DDR2 SDRAM

Features

- 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 128Mx64 Unbuffered DDR2 SO-DIMM based on 64Mx8 DDR2 SDRAM devices.
- Performance:

		PC2-3200	PC2-4200	PC2-5300	Unit
	Speed Sort	5A	37B	3C	
	DIMM $\overline{CAS}$ Latency	3	4	5	
f_{CK}	Clock Frequency	200	266	333	MHz
t_{CK}	Clock Cycle	5	3.75	3	ns
f_{DQ}	DQ Burst Frequency	400	533	667	MHz

- Intended for 200 MHz, 266MHz, and 333MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- SDRAMs have 4 internal banks for concurrent operation
- Module has one physical bank
- Differential clock inputs
- Data is read or written on both clock edges

- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/2 Addressing
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 60-ball FBGA Package
- RoHs Compliant products

Description

M2N1G64TU8HA2B is unbuffered 200-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as two ranks of 128Mx64 high-speed memory array. Modules use sixteen 64Mx8 60-ball FBGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 2.66" long space-saving footprint.

The DIMM is intended for use in applications operating up to 200 MHz (266MHz, 333MHz) clock speeds and achieves high-speed data transfer rates of up to 400 MHz (533MHz, 667MHz). Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
M2N1G64TU8HA2B –5A	DDR2-400	PC2-3200	200MHz (5ns @ CL = 3)	128Mx64	1.8V	Gold	Green
M2N1G64TU8HA2B –37B	DDR2-533	PC2-4200	266MHz (3.7ns @ CL = 4)				
M2N1G64TU8HA2B –3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				

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Pin Description

CK0, $\overline{CK0}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	$\overline{DQS0}$-$\overline{DQS7}$	Differential data strobes
$\overline{CAS}$	Column Address Strobe	DM0-DM7	Input Data Masks
$\overline{WE}$	Write Enable	V_{DD}	Power (1.8V)
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	V_{REF}	Ref. Voltage for SSTL_18 inputs
A0-A12	Row Address Inputs	V_{DDSPD}	Serial EEPROM positive power supply
A0-A9	Column Address Inputs	V_{SS}	Ground
A10/AP	Column Address Input/Auto-precharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	Active termination control lines	SA0, SA1	Serial Presence Detect Address Inputs
NC	No Connect		

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	$\overline{WE}$	110	$\overline{CS0}$	159	DQ49	160	DQ53
11	$\overline{DQS0}$	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	$\overline{CS1}$	116	(A13)	165	V_{SS}	166	$\overline{CK1}$
17	DQ2	18	V_{SS}	67	DM3	68	$\overline{DQS3}$	117	V_{DD}	118	V_{DD}	167	$\overline{DQS6}$	168	V_{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	$\overline{DQS1}$	30	CK0	79	CKE0	80	CKE1	129	$\overline{DQS4}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK0}$	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	NC	84	(A15)	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	(BA2)	86	(A14)	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS7}$
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	$\overline{DQS5}$	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS2}$	50	NC	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DDSPD}	200	SA1

Note: All pin assignments are consistent for all 8-byte unbuffered versions.

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Input/Output Functional Description

| Symbol	Type	Polarity	Function
CK0 – CK2, $\overline{CK0}$ - $\overline{CK2}$	(SSTL)	Cross Point	The system clock inputs. All the DDR2 SDRAM address and control inputs are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V$_{REF}$	Supply		Reference voltage for SSTL-18 inputs
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 – A13 defines the column address when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63 CB0 – CB7	(SSTL)	Active High	Data and Check Bit Input/Output pins. Check bits are only applicable on the x64 DIMM configurations.
V$_{DD}$, V$_{SS}$	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS7 $\overline{DQS0}$ – $\overline{DQS7}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V$_{DD}$ or V$_{SS}$ on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V$_{DD}$ to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V$_{DD}$ to act as a pull-up.
V$_{DDSPD}$	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

(1GB, 2Ranks, 64Mx8 DDR2 SDRAMs)
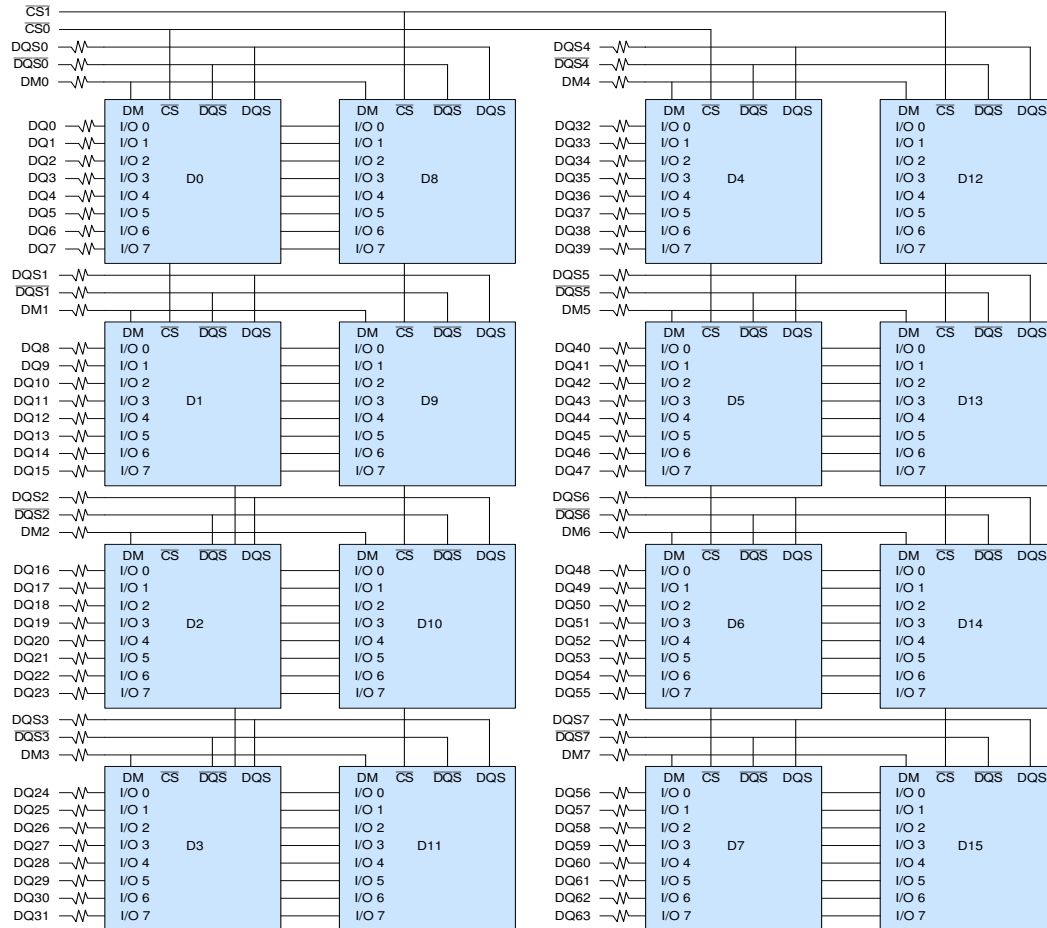
BA0-BA1 — BA0-BA1 : SDRAMs D0-D17
A0-A13 — A0-A13 : SDRAMs D0-D17
$\overline{RAS}$ — $\overline{RAS}$: SDRAMs D0-D17
$\overline{CAS}$ — $\overline{CAS}$: SDRAMs D0-D17
$\overline{WE}$ — $\overline{WE}$: SDRAMs D0-D17
CKE0 — CKE : SDRAMs D0-D8
CKE1 — CKE : SDRAMs D9-D17
ODT0 — ODT : SDRAMs D0-D8
ODT1 — ODT : SDRAMs D9-D17

VDDSPD — Serial PD
VDDQ — D0-D8
VDD — D0-D8
VREF — D0-D8
VSS — D0-D8
VDDID — Strap : see Note 4
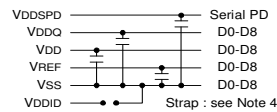
Notes : 1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/$\overline{DQS}$ resistors are 22 Ohms +/- 5%
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%

Serial PD
SCL
WP A0 A1 A2 SDA
SA0 SA1 SA2
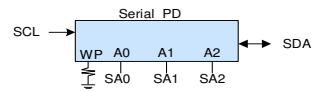
Serial Presence Detect

(Part 1 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-400	DDR2-533	DDR2-667	DDR2-400	DDR2-533	DDR2-667	
		-5A	-37B	-3C	-5A	-37B	-3C	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	14			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Ranks	2 rank, Height = 30mm			61			
6	Data Width of Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8			05			
9	DDR2 SDRAM Device Cycle Time at CL=5	5ns	3.75ns	3ns	50	3D	30	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.6ns	0.5ns	0.45ns	60	50	45	
11	DIMM Configuration Type	Non-Parity			00			
12	Refresh Rate/Type	SR/1x(7.8us)			82			
13	Primary DDR2 SDRAM Width	X8			08			
14	Error Checking DDR2 SDRAM Device Width	NA			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3/4/5			38			
19	DIMM Mechanical Characteristics	Undefined		<3.80mm	00		01	
20	DDR2 SDRAM DIMM Type Information	SODIMM			04			
21	DDR2 SDRAM Module Attributes:	Regular SODIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver			01		03	
23	Minimum Clock Cycle at CL=4	5ns	3.75ns	3.75ns	50	3D	3D	
24	Maximum Data Access Time from Clock at CL=4	±0.6ns	±0.5ns	±0.5ns	60	50	50	
25	Minimum Clock Cycle Time at CL=3	5ns			50			
26	Maximum Data Access Time from Clock at CL=3	0.6ns			60			
27	Minimum Row Precharge Time (t_{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns			1E			
29	Minimum RAS to CAS delay (t_{RCD})	15ns			3C			
30	Minimum RAS Pulse Width (t_{RAS})	45ns			2D			
31	Module Bank Density	512MB			80			
32	Address and Command Setup Time Before Clock (t_{IS})	0.35ns	0.25 ns	0.2ns	35	25	20	
33	Address and Command Hold Time After Clock (t_{IH})	0.475 ns	0.375 ns	0.325ns	47	37	27	
34	Data Input Setup Time Before Clock (t_{DS})	0.15 ns	0.10 ns	0.05ns	15	10	10	
35	Data Input Hold Time After Clock (t_{DH})	0.275ns	0.225ns	0.175ns	27	22	17	
36	Write Recovery Time (t_{WR})	15ns			3C			
37	Internal Write to Read Command delay (t_{WTR})	10ns	7.5 ns	7.5ns	28	1E	1E	
38	Internal Read to Precharge delay (t_{RTP})	7.5ns			1E			
39	Reserved	Undefined			00			
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns			00			
41	Minimum Core Cycle Time (t_{RC})	60ns			3C			

Serial Presence Detect

(Part 2 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2-400	DDR2-533	DDR2-667	DDR2-400	DDR2-533	DDR2-667	
		-5A	-37B	-3C	-5A	-37B	-3C	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns			69			
43	Maximum Clock Cycle Time (t_{CK})	8ns			80			
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.35ns	0.30ns	0.25ns	23	1E	18	
45	Read Data Hold Skew Factor (t_{QHS})	0.45ns	0.40ns	0.35ns	2D	28	22	
46-61	Reserved	Undefined			00			
62	SPD Revision	1.0			10			
63	Checksum for Byte 0-62	Checksum Data			37	B3	72	
64-255	Reserved	Undefined			--			

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to +2.3	V
V_{DD}	Voltage on VDD pins relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.5 to +2.3	V
V_{DDL}	Voltage on VDDL pins relative to Vss	-0.5 to +2.3	V
T_{STG}	Storage Temperature (Plastic)	-55 to +100	℃

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	℃	1

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. $t_{CASE} > 85℃$ ➔ $t_{REFI} = 3.9$ µs

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDL}	DLL Supply Voltage	1.7	1.9	V	1
V_{DDQ}	Output Supply Voltage	1.7	1.9	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	Input Reference Voltage	$0.49V_{DDQ}$	$0.51V_{DDQ}$	V	1, 2
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF} + 0.04	V	3

Note:
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V $_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.

Input AC/DC logic level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH (AC)}$	Input High (Logic1) Voltage	V_{REF} + 0.250	-	V	1
$V_{IL (AC)}$	Input Low (Logic0) Voltage	-	V_{REF} - 0.250	V	1
$V_{IH (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
$V_{IL (DC)}$	Input Low (Logic0) Voltage	-0.3	V_{REF} - 0.125	V	1

On Die Termination (ODT) Current

Symbol	Parameter	Min	Max	Units	EMRS(1) State
IODTO	Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	5	7.5	mA/DQ	A6=0, A2=1
		2.5	3.75	mA/DQ	A6=1, A2=0
IODTT	Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING	10	15	mA/DQ	A6=0, A2=1
		5	7.5	mA/DQ	A6=1, A2=0

Operating, Standby, and Refresh Currents

T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-3200 (5A)	PC2-4200 (37B)	PC2-5300 (3C)	Unit	Notes
IDD0	Operating Current: one bank; active/precharge; t_{RC} = $t_{RC\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	776	800	1000	mA	1
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; t_{RC} = $t_{RC\ (MIN)}$; CL= 4; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	816	880	1120	mA	1
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	80	80	80	mA	1
IDD2Q	Precharge Quiet Stand by Current	400	640	640	mA	1
IDD2N	Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle	512	480	800	mA	1
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; Fast PDN Exit MRS(12) = 0mA	208	256	304	mA	1
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; Slow PDN Exit MRS(12) = 1mA	80	80	96	mA	1
IDD3N	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; t_{RC} = $t_{RAS\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	280	336	400	mA	1
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 4; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA	896	960	1440	mA	1
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL= 4; t_{CK} = $t_{CK\ (MIN)}$	856	1000	1520	mA	1
IDD5	Auto-Refresh Current: t_{RC} = $t_{RFC\ (MIN)}$	1296	1520	1680	mA	1
IDD6	Self-Refresh Current: CKE ≤ 0.2V	80	80	80	mA	1
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = $t_{RC\ (min)}$; I_{OUT} = 0mA.	1456	1520	1760	mA	1

Note:

1. Module IDD was calculated from component IDD. It may different from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T$_{CASE}$ = 0 ℃ ~ 85 ℃; V$_{DDQ}$ = 1.8V ± 0.1V; V$_{DD}$ = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-5A		-37B		-3C		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t$_{AC}$	DQ output access time from CK/$\overline{CK}$	-0.6	+0.6	-0.5	+0.5	-0.45	+0.45	ns	
t$_{DQSCK}$	DQS output access time from CK/$\overline{CK}$	-0.5	+0.5	-0.45	+0.45	-0.4	+0.4	ns	
t$_{CH}$	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	t$_{CK}$	
t$_{CL}$	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	t$_{CK}$	
t$_{HP}$	Minimum half clk period for any given cycle; defined by clk high (t$_{CH}$) or clk low (t$_{CL}$) time	t$_{CH}$ or t$_{CL}$	-	t$_{CH}$ or t$_{CL}$	-	t$_{CH}$ or t$_{CL}$	-	t$_{CK}$	
t$_{CK}$	Clock Cycle Time	5	8	3.75	8	3	8	ns	
t$_{DH}$	DQ and DM input hold time	275	-	225	-	175	-	ps	
t$_{DS}$	DQ and DM input setup time	150	-	100	-	100	-	ps	
t$_{IPW}$	Input pulse width	0.6	-	0.6	-	0.6	-	t$_{CK}$	
t$_{DIPW}$	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	t$_{CK}$	
t$_{HZ}$	Data-out high-impedance time from CK/$\overline{CK}$	-	t$_{AC\ max}$	-	t$_{AC\ max}$	-	t$_{AC\ max}$	ns	
t$_{LZ(DQ)}$	Data-out low-impedance time from CK/$\overline{CK}$	2t$_{AC\ min}$	t$_{AC\ max}$	2t$_{AC\ min}$	t$_{AC\ max}$	2t$_{AC\ min}$	t$_{AC\ max}$	ns	
t$_{LZ(DQS)}$	DQS low-impedance time from CK/$\overline{CK}$	t$_{AC\ min}$	t$_{AC\ max}$	t$_{AC\ min}$	t$_{AC\ max}$	t$_{AC\ min}$	t$_{AC\ max}$	ns	
t$_{DQSQ}$	DQS-DQ skew (DQS & associated DQ signals)	-	0.35	-	0.30	-	0.24	ns	
t$_{QHS}$	Data hold Skew Factor	-	0.45	-	0.4	-	0.34	ns	
t$_{QH}$	Data output hold time from DQS	t$_{HP}$ - t$_{QHS}$	-	t$_{HP}$ - t$_{QHS}$	-	t$_{HP}$ - t$_{QHS}$	-	ns	
t$_{DQSS}$	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	0.25	-0.25	0.25	t$_{CK}$	
t$_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	t$_{CK}$	
t$_{DSS}$	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	t$_{CK}$	
t$_{DSH}$	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	t$_{CK}$	
t$_{MRD}$	Mode register set command cycle time	2	-	2	-	2	-	t$_{CK}$	
t$_{WPST}$	Write postamble	0.40	0.60	0.40	0.60	0.40	0.60	t$_{CK}$	
t$_{WPRE}$	Write preamble	0.35	-	0.35	-	0.35	-	t$_{CK}$	
t$_{IH}$	Address and control input hold time	475	-	375	-	275	-	ps	
t$_{IS}$	Address and control input setup time	0.35	-	0.25	-	0.2	-	ns	
t$_{RPRE}$	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	t$_{CK}$	
t$_{RPST}$	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	t$_{CK}$	
t$_{Delay}$	Minimum time clocks remains ON after CKE asynchronously drops Low	t$_{IS}$ + t$_{CK}$ + t$_{IH}$	-	t$_{IS}$ + t$_{CK}$ + t$_{IH}$	-	t$_{IS}$ + t$_{CK}$ + t$_{IH}$	-	ns	
t$_{RFC}$	Refresh to active/Refresh command time	105		105		105		ns	
t$_{REFI}$	Average Periodic Refresh Interval (85ºC < T$_{CASE}$ ≤ 95ºC)	3.9		3.9		3.9		µs	
	Average Periodic Refresh Interval (0ºC ≤ T$_{CASE}$ ≤ 85ºC)	7.8		7.8		7.8		µs	
t$_{RRD}$	Active bank A to Active bank B command	7.5	-	7.5	-	7.5	-	ns	

M2N1G64TU8HA2B (Green)   **Preliminary Edition**
1GB : 128M x 64
PC2-3200 / PC2-4200 / PC2-5300 Unbuffered DDR2 SO-DIMM

elixir

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-5A Min.	-5A Max.	-37B Min.	-37B Max.	-3C Min.	-3C Max.	Unit	Notes
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$	2	-	2	-	2	-	t_{CK}	
t_{WR}	Write recovery time	15	-	15	-	15	-	ns	
WR	Write recovery time with Auto-Precharge	t_{WR}/t_{CK}		t_{WR}/t_{CK}		t_{WR}/t_{CK}		ns	
t_{DAL}	Auto precharge write recovery + precharge time	WR +t_{RP}	-	WR +t_{RP}	-	WR +t_{RP}	-	t_{CK}	
t_{WTR}	Internal write to read command delay	10	-	7.5	-	7.5	-	ns	
t_{RTP}	Internal read to precharge command delay	7.5	-	7.5	-	7.5	-	ns	
t_{XSNR}	Exit self refresh to a Non-read command	t_{RFC} +10	-	t_{RFC} +10	-	t_{RFC} +10	-	ns	
t_{XSRD}	Exit self refresh to a Read command	200	-	200	-	200	-	t_{CK}	
t_{XP}	Exit precharge power down to any Non- read command	2	-	2	-	2	-	t_{CK}	
t_{XARD}	Exit active power down to read command	2	-	2	-	2	-	t_{CK}	
t_{XARDS}	Exit active power down to read command	6-AL	-	6-AL	-	7-AL	-	t_{CK}	
t_{CKE}	CKE minimum pulse width	3	-	3	-	3	-	t_{CK}	
t_{OIT}	OCD drive mode output delay	0	12	0	12	0	12	ns	
ODT									
t_{AOND}	ODT turn-on delay	2	2	2	2	2	2	t_{CK}	
t_{AON}	ODT turn-on	t_{AC} (min)	t_{AC} (max) +1	t_{AC} (min)	t_{AC} (max) +1	$t_{AC(min)}$	$t_{AC(max)}$ +0.7	ns	
t_{AONPD}	ODT turn-on (Power down mode)	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	ns	
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$ +1	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$ +1	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{ANPD}	ODT to power down entry latency	3	-	3	-	3	-	t_{CK}	
t_{AXPD}	ODT power down exit latency	8	-	8	-	8	-	t_{CK}	
Speed Grade Definition									
t_{RAS}	Row Active Time	40	70000	45	70000	45	70000	ns	
t_{RCD}	RAS to CAS delay	15	-	15	-	15	-	ns	
t_{RC}	Row Cycle Time	55	-	60	-	60	-	ns	
t_{RP}	Row Precharge Time	15	-	15	-	15	-	ns	

06/2006

Package Dimensions

(1GB, 2Ranks, 64Mx8 DDR2 SDRAMs)

FRONT

BACK

SIDE

Detail A

Detail B
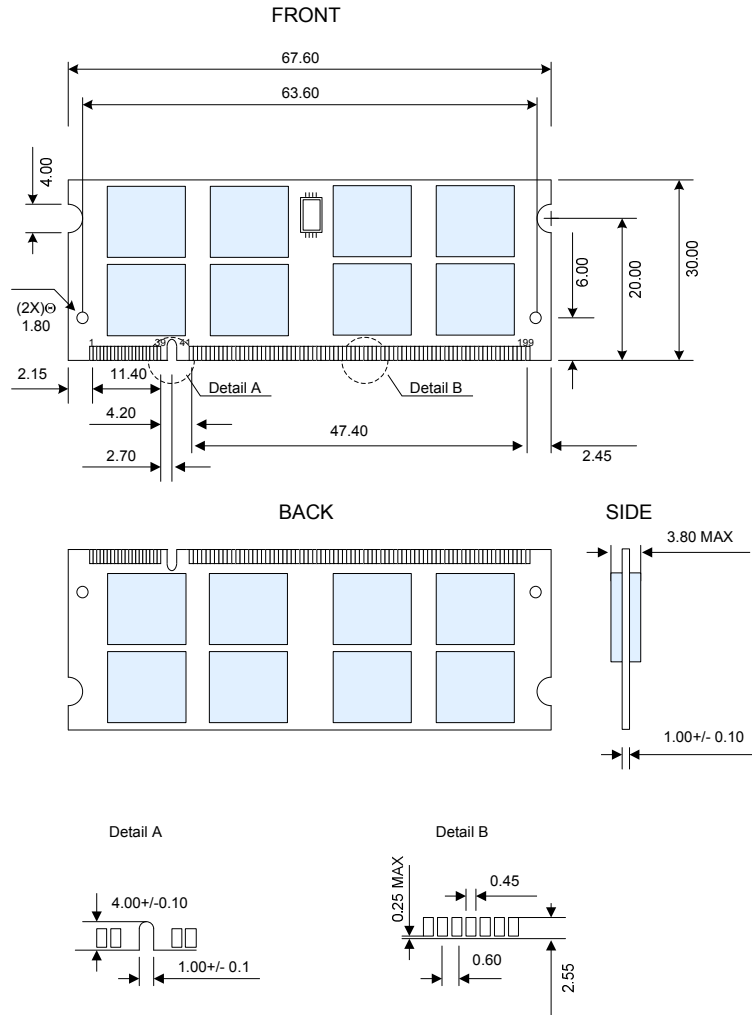
Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
0.1	06/2006	Preliminary Edition

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