
DATA SHEET

HM 65798

64 K x 4 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
COMMERCIAL/INDUSTRIAL :
20/25/35/45/55 ns (max)
MILITARY : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
ACTIVE : 770 mW
STANDBY : 220 mW
- **WIDE TEMPERATURE RANGE :**
- 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000V ELECTROSTATIC DISCHARGE SINGLE 5 VOLT SUPPLY**

INTRODUCTION

The HM 65798 is a high speed CMOS static RAM organized as 65,536 x 4 bit. It is manufactured using MHS high performance CMOS technology.

Access times as fast 20 ns are available with maximum power consumption of only 770 mW.

The HM 65798 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 71 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and three state drivers.

All inputs and outputs of the HM 65798 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 65798 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCL 9000, making ideally suitable for military/space applications that demand superior levels of performance and reliability.

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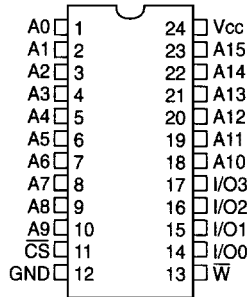
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INTERFACE

PIN CONFIGURATION

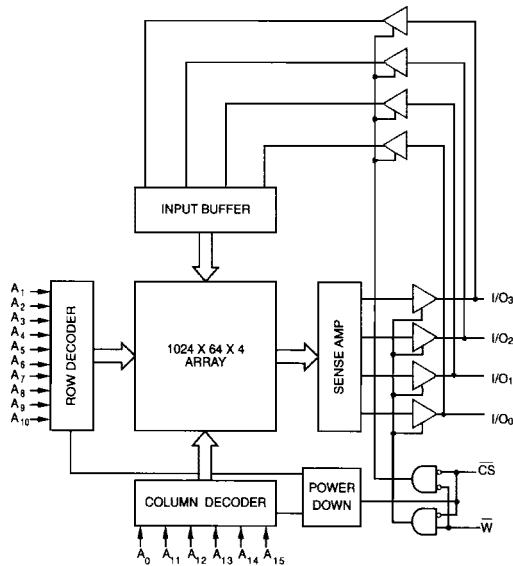
Plastic 300 mils, 24 pins, DIL
Ceramic 300 mils, 24 pins, DIL

SO/SOJ 300 mils, 24 pins.



Pinout DIL/SO 24 pins (top view)

BLOCK DIAGRAM



PIN NAMES

A0-A15	: Address inputs	$\bar{W}$	: Write enable
I/O0-I/O3	: Input/Output	Vcc	: Power
CS	: Chip select	GND	: Ground

TRUTH TABLE

CS	W	INPUT/OUTPUTS	MODE
H	X	High Z	Deselect/Power Down
L	H	Data Out	Read
L	L	Data In	Write

L = low, H = high, X = H or L, Z = High impedance

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential - 0.5 V to + 7.0 V
 DC input voltage - 3.0 V to + 7.0 V
 DC output voltage in high Z state - 0.5 V to + 7.0 V
 Storage temperature - 65°C to + 150°C
 Output current into outputs (low) 20 mA
 Electro static discharge voltage > 2000 V (MIL STD 883C method 3015.5)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(- 2)	5 V $\pm$ 10 %	- 55°C to + 125°C
Industrial	(- 9)	5 V $\pm$ 10 %	- 40°C to + 85°C
Commercial	(- 5)	5 V $\pm$ 10 %	- 0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	- 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	-	VCC	V

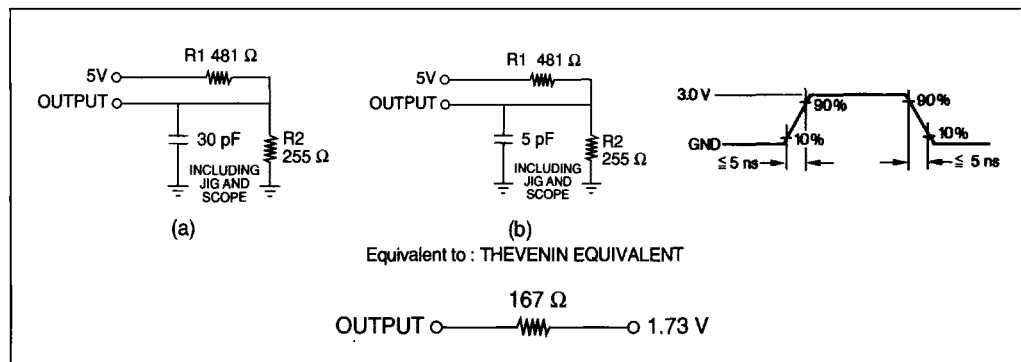
CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1) Input capacitance	-	-	5	pF
Cout	(1) Output capacitance	-	-	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

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AC TEST LOADS AND WAVEFORMS



DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	- 10	-	10	μ A
IOZ	(2)	Output leakage current	- 10	-	10	μ A
IOS	(3)	Output short circuit current	-	-	- 350	mA
VOL	(4)	Output low voltage	-	-	0.4	V
VOH	(5)	Output high voltage	2.4	-	-	V

- Notes :**
2. $Gnd < V_{in} < V_{oc}$, $Gnd < V_{out} < V_{oc}$ output disabled.
 3. $V_{oc} = \max$, $V_{out} = Gnd$, duration of the short circuit not exceed 30 seconds.
Not more than 1 output should be shorted at one time.
 4. $V_{oc} \min$, $I_{OL} = 8.0 \text{ mA}$
 5. $V_{oc} \min$, $I_{OH} = - 4.0 \text{ mA}$.

CONSUMPTION FOR COMMERCIAL (- 5) SPECIFICATION

SYMBOL		PARAMETER	65798 F-5	65798 H-5	65798 K-5	65798 M-5	65798 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	35	35	35	35	mA	max
ICCSB1	(8)	Standby supply current	20	20	20	20	20	mA	max
ICCOP	(7)	Operating supply current	140	120	120	120	120	mA	max

CONSUMPTION FOR INDUSTRIAL (- 9) AND MILITARY (- 2) SPECIFICATION

SYMBOL		PARAMETER	65798 F-9	65798 H-9/-2	65798 K-9/-2	65798 M-9/-2	65798 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	35	35	35	35	mA	max
ICCSB1	(8)	Standby supply current	20	20	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	150	130	130	130	130	mA	max

- Notes :**
6. $CS \geq V_{IH}$, a pull-up resistor to V_{oc} on the CS is required to keep the devices unselected during the V_{oc} power-up. Otherwise ICCSB will exceed the above values. Min duty cycle = 100 %.
 7. $V_{oc} \max$, Output current = 0 mA, $f = \max$, $V_{in} = V_{oc}$ or Gnd.
 8. $CS \geq V_{oc} - 0.3V$ $I_{out} = 0 \text{ mA}$.

AC PARAMETERS

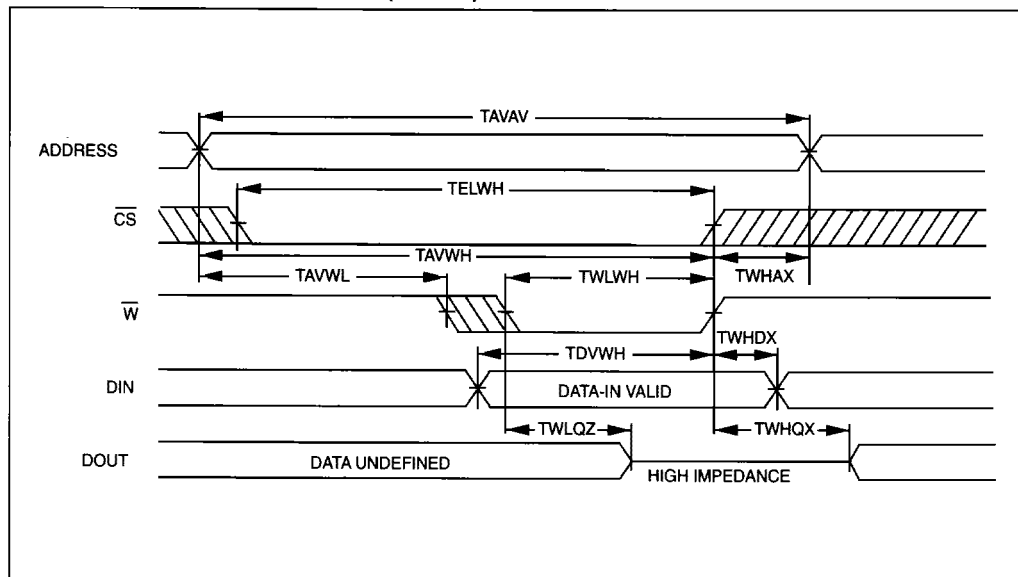
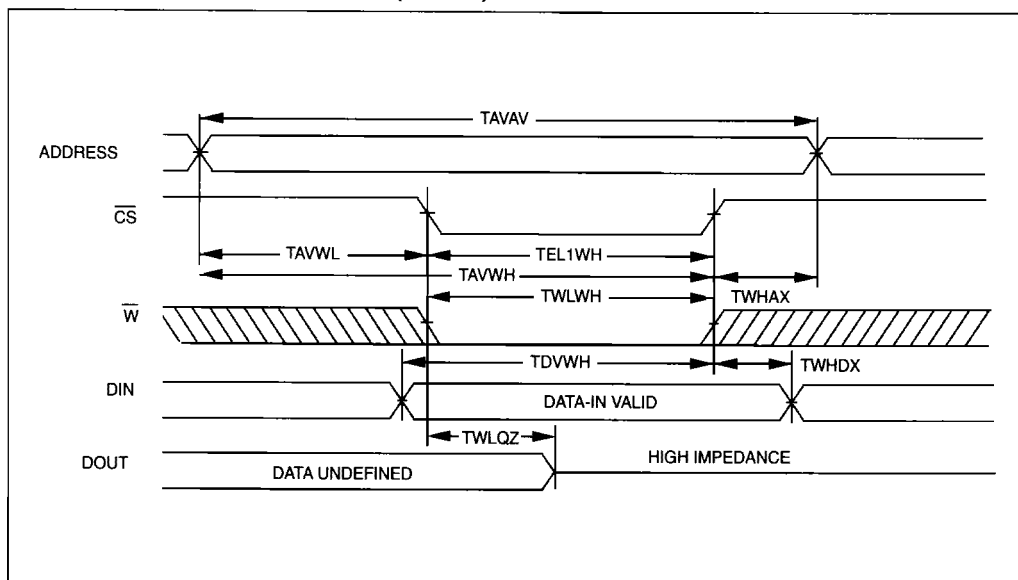
Input pulse levels : Gnd to 3.0 V
 Input rise : 5 ns

Input timing reference levels : 1.5 V
 Output loading IOL/IOH (see figure 1a and 1b) : +30 pF

WRITE CYCLE : COMMERCIAL (-5), INDUSTRIAL (-9) AND MILITARY (-2) SPECIFICATION

SYMBOL	PARAMETER	65798 F-5/-9	65798 H-5/-9/-2	65798 K-5/-9/-2	65798 M-5/-9/-2	65798 N-5/-9/-2	UNIT	VALUE
TAVAV	Write cycle time	20	20	30	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to write end	15	20	25	35	40	ns	min
TDVWH	Data set-up time	10	15	17	20	25	ns	min
TELWH	CS low to write end	15	20	30	40	50	ns	min
TWLQZ (9)	Write low to high Z	10	13	15	20	25	ns	max
TWLWH	Write pulse width	15	20	25	30	35	ns	min
TWHAX	Address hold from write end	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	0	ns	min
TWHQX (9)	Write high to low Z	3	3	3	3	3	ns	min

Note : 9. The data input set-up and hold timing should be referenced to rising edge of the signal that terminates the write.

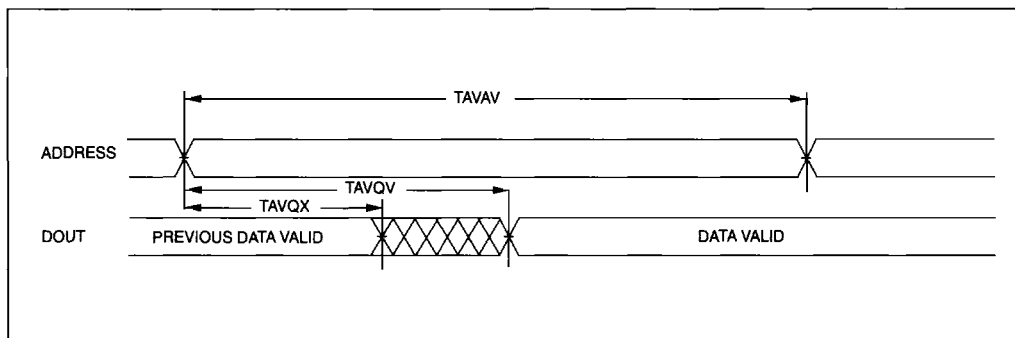
WRITE CYCLE 1 : $\overline{W}$ CONTROLLED (note 10)WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED (note 10)

Note : 10. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.

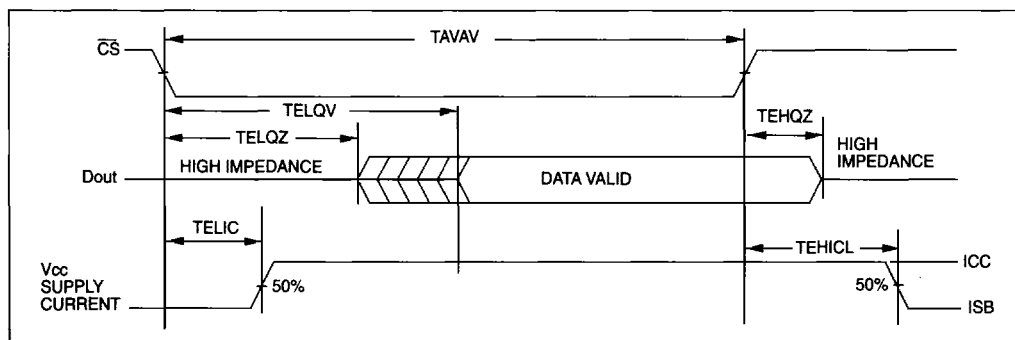
READ CYCLE : COMMERCIAL (-5), INDUSTRIAL (-9) AND MILITARY (-2) SPECIFICATION

SYMBOL	PARAMETER	65798 F-5/-9	65798 H-5/-9/-2	65798 K-5/-9/-2	65798 M-5/-9/-2	65798 N-5/-9/-2	UNIT	VALUE
TAVAV	READ cycle time	20	25	35	45	55	ns	min
TAVQV	Address access time	20	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	3	ns	min
TELQV	Chip-select access time	20	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	13	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power up	20	25	35	45	55	ns	max

READ CYCLE 1 : (note 11, 12, 13)



READ CYCLE 2 : (note 11, 13)



- Notes : 11. W is high for read cycle.
 12. Device is continuously selected, $\overline{CS} = V_{IL}$.
 13. Address valid prior or coincident with CS transition low.

ORDERING INFORMATION

HM	PACKAGE	DEVICE TYPE	GRADE	LEVEL
<u>HM</u>	<u>3</u>	<u>65798</u>	<u>H</u>	<u>-5 : R</u>
		64 K x 4 high speed static RAM		
	0 - Chip form		F = 20 ns	-2 : Military
	1 - Ceramic 24 pins 300 mils		H = 25 ns	-5 : Commercial
	3 - Plastic 24 pins 300 mils		K = 35 ns	-6 : 100% 25°C Probe
	T - SOIC 24 pins 300 mils		M = 45 ns	-9 : Industrial
	U - SOJ 24 pins		N = 55 ns	/883 : MIL STD 883 Class B or S
				DB : Dice Military program
				R : Tape & Reel option
				RD : Tape & Reel / Dry pack option
				D : Dry pack option