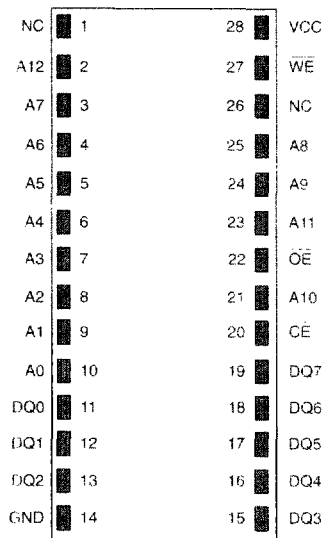


## FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 28-pin DIP package
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full  $\pm 10\%$   $V_{CC}$  operating range (DS1225AD)
- Optional  $\pm 5\%$   $V_{CC}$  operating range (DS1225AB)
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND

## PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE  
720 MIL EXTENDED

## PIN DESCRIPTION

A0–A12	– Address Inputs
DQ0–DQ7	– Data In/Data Out
$\overline{\text{CE}}$	– Chip Enable
$\overline{\text{WE}}$	– Write Enable
$\overline{\text{OE}}$	– Output Enable
$V_{CC}$	– Power (+5V)
GND	– Ground
NC	– No Connect

## DESCRIPTION

The DS1225AB and DS1225AD are 65,536-bit, fully static, nonvolatile SRAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV

SRAMs can be used in place of existing 8K x 8 SRAMs directly conforming to the popular byte-wide 28-pin DIP standard. The devices also match the pinout of the 2764 EPROM and the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.