VLSI Technology, Inc.

VES1777
Single-Chip DSS®/DVB Satellite Channel Receiver

Overview The VES1777 is the latest addition to VLSI's industry-leading set-top front-end solutions. In order to provide world-wide multi-standard support, the VES1777 is a universal digital satellite receiver compliant with both the DVB and DSS® standards. Based on the VES1789 architecture, the VES1777 integrates VLSI's true variable rate BPSK/QPSK demodulation and forward error correction (FEC) functions. Moreover, the VES1777 is pin-compatible to the VES1789.

Description

The VES1777 universal single chip satellite channel receiver provides true variable rate performance between 1 Mhz and 62Mhz (500 Kbaud to 30 Mbaud) for both DVB and DSS. The device interfaces directly with I and Q digital baseband signals which are filtered with a half-Nyquist filter. Coherent demodulation is achieved without any feedback to the local oscillator, which negates the need for an external voltage controlled crystal oscillator (VCXO).

The VES1777 Forward Error Correction (FEC) decodes two concatenated codes with the Reed-Solomon used as the outer code, and a Viterbi decoder used as the inner code. The Reed-Solomon decoder corrects up to 8 erroneous bytes among the N bytes of one data packet. A convolutional deinterleaver with a depth of 12 or 13 blocks, is located between the Viterbi output and Reed-Solomon decoder input. The deinterleaver and Reed-Solomon decoder are automatically synchronized by a frame synchronization algorithm which uses timing information from the packet header.

The VES1777 is controlled via an I²C or 8-bit bus interface. Through this interface the VES1777 offers the following DSS or DVB programmable features: Half-Nyquist filter roll-off factor; deinterleaver; packet length; and Reed-Solomon decoder. The device also has the ability to disable the energy dispersion descrambler (a feature used only for DVB).

The device is offered in both a 68-pin PLCC and a 100-pin MQFP package. Designed in 0.5µm CMOS technology, the VES1777 operates over the commercial temperature range.

Features

- DSS and DVB-S compatible single chip demodulator and forward error correction
- Variable rate BPSK/QPSK coherent demodulator
- Modulation rates up to 30 Mbaud
- Analog power estimation for AGC
- Symbol timing recovery:
  Programmable second-order loop filter
  -Acquisition Range:
  ± 100 ppm typical
- Carrier recovery:
  -Programmable second-order loop filter
  -AFC output provision
  -Acquisition range:
  Up to ± D/2 where D= modulation rate
  -Carrier lock detection provided
- Half-Nyquist baseband filters on chip
  -2 selectable roll-off factors
- Viterbi decoder:
  -Supported rates:
  from 1/2 to 8/9
  -Constraint length K=7 with $G1=171_8$ and $G2=133_8$
  -Automatic depuncturing and bit synchronization for all rates including spectral inversion resolution
  -Coding gain of 5.4 dB at BER of 10^{-5}, rate of 1/2
  -BER measurements provided
- Reed-Solomon decoder:
  -Programmable block length
  -Fixed power correction of t=8
- Convolutional deinterleaving of depth 12 or 13
- Automatic frame synchronization
- Selectable DVB descrambling
- I²C or 8-bit bus interface
- 68-pin PLCC or 100-pin MQFP package
- CMOS technology (0.5 µm)

Applications

- Dual-Mode DSS/DVB-S Receivers
- Direct Broadcast Satellite (DBS)

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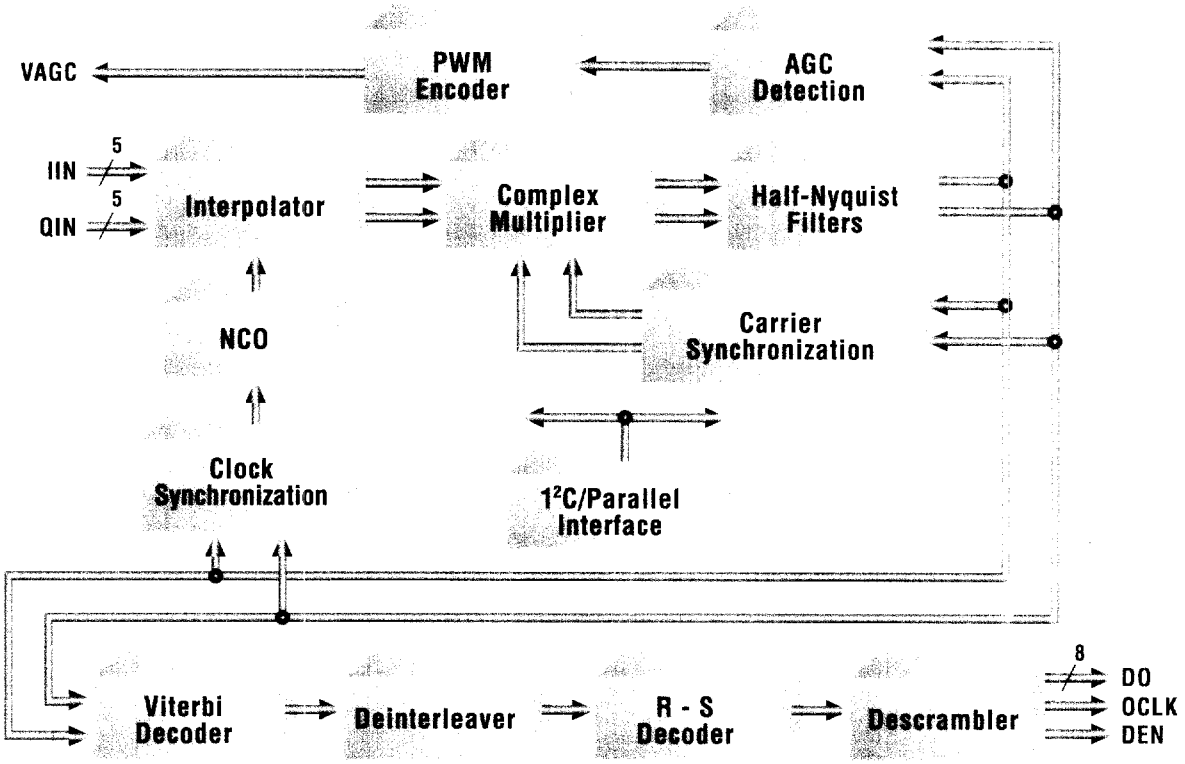
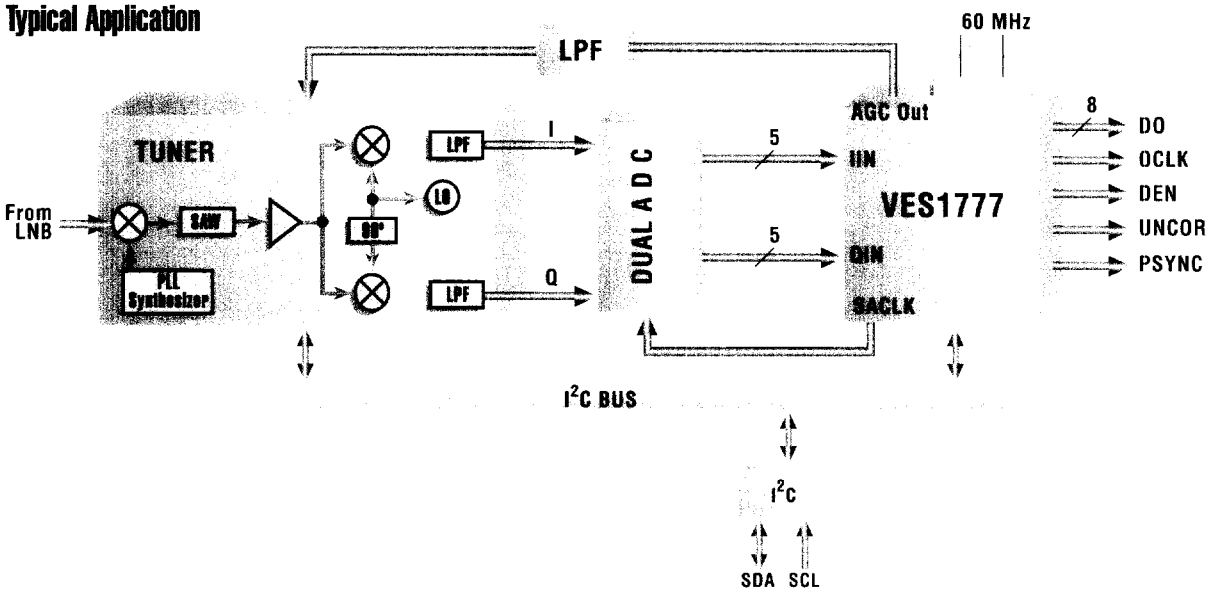
VES1777 Block Diagram



Typical Application



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