SPICoder® 06 UR5HCSPI-06

Extremely Low-Power Keyboard Encoder & Power Management IC for H/PCs

HID & SYSTEM MANAGEMENT PRODUCTS, KEYCODER® FAMILY **PRELIMINARY**

DESCRIPTION

The SPICoder® 06 UR5HCSPI-06 keyboard encoder and power management IC is designed specifically for handheld PCs (H/PCs). The off-the-shelf SPICoder® 06 works readily with CPUs designed for Windows® CE, saving OEMs significant development time and money as well as minimizing time-to-market for the new generations of handheld products.

Three main design features of the SPICoder® 06 make it the ideal companion for the new generation of Windows® CE-compatible, single-chip computers: low-power consumption; real estate-saving size; and special keyboard modes.

Extremely low power consumption (less than 2 µA at 3V), a must for H/PCs, provides the host system with both power management and I/O flexibility, with almost no battery drainage.

Finally, special keyboard modes and built-in power management features allow the SPICoder® 06 to operate in harmony with the power management modes of Windows® CE, resulting in more user flexibility and longer battery life.

The SPICoder® 06 also offers programmable features for wake-up keys and general purpose I/O pins.

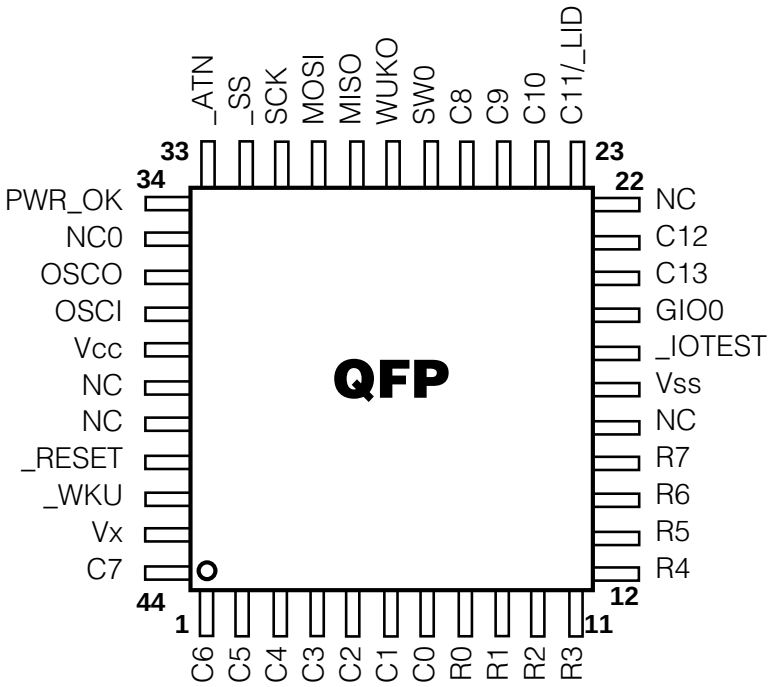
FEATURES

- SPI-compatible keyboard encoder and power management IC
- Compatible with Windows® CE keyboard specification
- Extremely low power consumption — typically less than 2 µA, between 3-5V
- Offers overall system power management capabilities
- Compatible with “system-on silicon” CPUs for H/PCs
- Special keyboard and power management modes for H/PCs, including programmable “wake-up” keys
- Scans, debounces, and encodes an 8 x 14 matrix
- Provides GPIO pins and controls discrete switches
- Available in a small 44-pin QFP package

APPLICATIONS

- StrongARM™ handheld PCs
- Windows® CE platforms
- Web phones
- Personal digital assistants (PDAs)
- Wearable computers
- Internet appliances

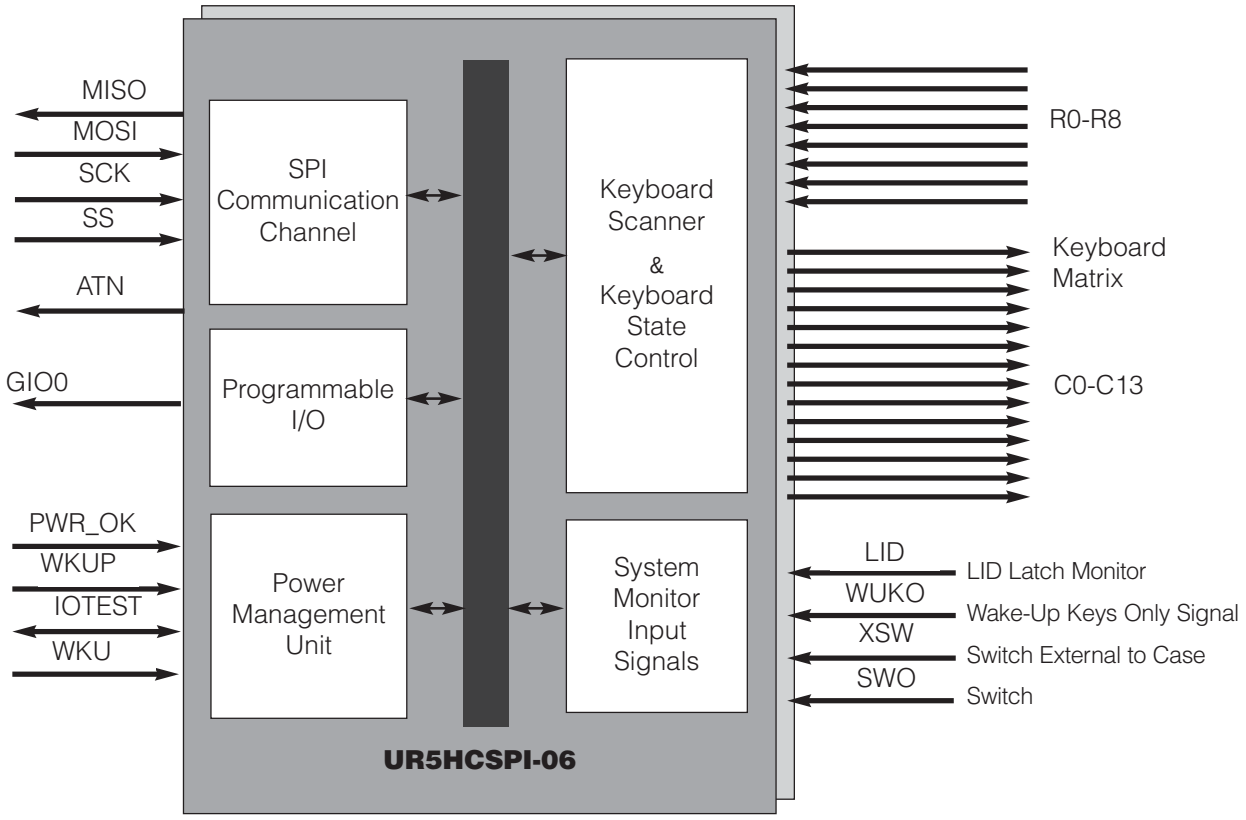
PIN ASSIGNMENTS



ORDERING CODE

Package Options	Pitch	TA = -20° C to +85° C
44-pin plastic QFP	0.8 mm	UR5HCSPI-06-FB

BLOCK DIAGRAM



SEMTECH

FUNCTIONAL DESCRIPTION

The SPICoder® 06 consists functionally of five major sections as shown in the the block diagram. These are the Keyboard Scanner and State control, the Programmable I/O, the SPI Communication Channel, the System Monitor and the Power Management unit. All sections communicate with each other and operate concurrently.

PIN DEFINITIONS

Mnemonic	Pin #	Type	Name and Function
VCC	38	I	**Power supply:** 3-5V
VSS	17	I	**Ground**
VX	43	I	Tie to VCC
OSCI	37	I	**Oscillator input**
OSCO	36	O	**Oscillator output**
_RESET	41	I	**Reset:** apply 0V for orderly start up
			SPI interface signals:
MISO	29	O	Master In, Slave Out
MOSI	30	I	Master Out, Slave In
SCK	31	I	SPI clock
_SS	32	I	Slave Select: If not used tie to VSS
_IOTEST	18	O	**Wake-up control signals**
_WKU	42	I	
R0-R4	8-12	I	**Row data inputs**
R5-R7	13-15	I	Port provides internal pull-up resistors
C0-C5	7-2	O	**Column select outputs**
C6-C7	1,44	O	
C8-C9	26-25	O	
			Multi-function pins:
C10	24	I/O	C10 & “Wake-Up Keys Only” imput
C11/_LID	23	I/O	C11 & Lid latch detect input
			Column select outputs
C12	21	I/O	C12
C13	20	I/O	C13
			Miscellaneous functions:
GIO0	19	I/O	Programmable I/O
WUKO	28	I	External discrete switch
SWO	27	I	Discrete switch
			Power Management Pins:
_ATN	33	O	CPU Attention Output
_PWR_OK	34	I	Power OK Input
NC	16, 22 ,39, 40		**No Connects**: these pins are unused
NC0	35		NC0 should be tied to VSS or GND

Note: An underscore before a pin mnemonic denotes an active low signal.

PIN DESCRIPTIONS

VCC and VSS

VCC and VSS are the power supply and ground pins. The SPICoder® 06 operates from a 3-5 Volt power supply. To prevent noise problems, provide bypass capacitors and place them as close as possible to the IC with the power supply. VX, where available, should be tied to Vcc.

OSCI and OSCO

OSCI and OSCO provide the input and output connections for the on-chip oscillator. The oscillator can be driven by any of the following circuits:

- Crystal
- Ceramic resonator
- External clock signal

The frequency of the on-chip oscillator is 2.00 MHz.

_RESET

A logic zero on the _RESET pin forces the SPICoder® 06 into a known start-up state. The reset signal can be supplied by any of the following circuits:

- RC
- Voltage monitor
- Master system reset

MOSI, MISO, SCK, _SS, _ATN

These five signals implement the SPI interface. The device acts as a slave on the SPI bus. The _SS (Slave Select) pin should be tied to ground if not used by the SPI master. The _ATN pin is asserted low each time the UR5HCSPI-06 has a packet ready for delivery. For a more detailed description, refer to the SPI Communication Channel section of this document.

_IOTEST and _WKU

"Input Output Test" and "Wake Up" pins control the stop mode exit of the device. The designer can connect any number of active low signals to these two pins through a 17KΩ resistor, in order to force the device to exit the stop mode. A sample circuit is shown in this document.

All the signals are "wire-anded." When any one of these signals is not active, it should be floating (i.e., these signals should be driven from "open-collector" or "open-drain" outputs).

R0 - R7

The R0-R7 pins are connected to the rows of the scanned matrix. Each pin provides an internal pull-up resistor, eliminating the need for external components.

C0 - C9

C0 to C9 are bi-directional pins connected to the columns of the scanned matrix. When a column is selected, the pin outputs an active low signal. When the column is de-selected, the pin turns into high-impedance.

C10 / WUKO

The C10 / WUKO pin acts alternatively as column scan output and as an input. As an input, the pin detects the "Wake-Up Keys Only" signal, typically provided by the host CPU to indicate that the user has turned the unit off. When the device detects an active high state on this pin, it feeds this information into the "Keyboard State Control" unit, in order to disable the keyboard and enable the programmed wake-up keys.

C11 / _LID

The C11 / _LID pin acts in a similar manner to the C10 / WUKO. This pin is typically connected to the LID latch through a 150KΩ resistor, in order to detect physical closing of the device cover. When the pin detects an active low state in this input, it feeds this information into the "Keyboard State Control" unit, in order to disable keys inside the case and enable only switches located physically on the outer body of the H/PC unit.

PIN DESCRIPTIONS (CONT'D)

The SPICoder® 06 offers pins C12, C13 and GIO0.

C12 and C13

C12 and C13 are used as additional column pins in order to accommodate larger-size keyboards, such as the Fujitsu FKB1406 palmtop keyboard.

GIO0

GIO0 is a programmable general-purpose input/output switch; it can also be used as a wake-up signal. The General-Purpose I/O Pin section of this document explains the use of GIO0.

XSW

The XSW pin is dedicated to an external switch. This pin is handled differently than the rest of the switch matrix and is intended to be connected to a switch physically located on the outside of the unit.

SW0

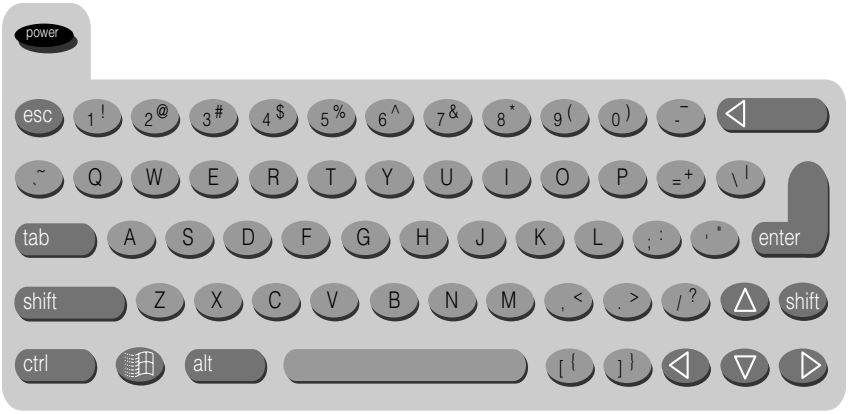
The SW0 pin is a dedicated input pin for a switch.

PWR_OK

The PWR_OK pin is an active low pin that monitors the battery status of the unit. When the SPICoder® 06 detects a transition from high to low on this pin, it immediately enters the STOP mode and remains in that state until the batteries are replaced and the signal is deasserted.

WINDOWS® CE KEYBOARD

The following illustration shows a typical implementation of a Windows® CE keyboard.



Windows® CE does not support the following keyboard keys typically found on desktop and laptop keyboards:

- INSERT
- SCROLL LOCK
- PAUSE
- NUM LOCK
- Function Keys (F1-F12)
- PRINT SCREEN

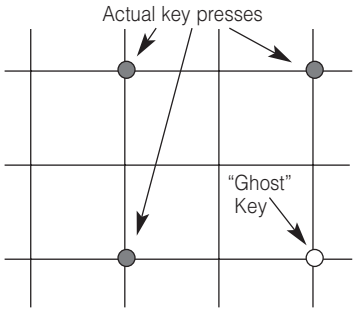
If the keyboard implements the Windows key, the following key combinations are supported in the Windows® CE environment:

Key Combination	Result
Windows	Open Start Menu
Windows+K	Open Keyboard Tool
Windows+I	Open Stylus Tool
Windows+C	Open Control Panel
Windows+E	Explore the H/PC
Windows+R	Display the Run Dialog Box
Windows+H	Open Windows® CE Help
Ctrl+Windows+A	Select all on desktop

"GHOST" KEYS

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is sensed as being pressed. This is known as the "ghost" or "phantom" key problem.

Figure 1: "Ghost" or "Phantom" Key Problem



Although the problem cannot be totally eliminated without using external hardware, there are methods to neutralize its negative effects for most practical applications. Keys that are intended to be used in combinations should be placed in the same row or column of the matrix, whenever possible. Shift keys (Shift, Alt, Ctrl, Window) should not reside in the same row (or column) as any other keys. The SPICoder®06 has built-in mechanisms to detect the presence of "ghost" keys.

KEYBOARD SCANNER

The encoder scans a keyboard organized as an 8 row by 14 column matrix for a maximum of 112 keys. Smaller size matrixes can also be accommodated by simply leaving unused pins open. The SPICoder®06 provides internal pull-ups for the row input pins. When active, the encoder selects one of the column lines (C0-C13) every 512 µS and then reads the row data lines (R0-R7). A key closure is detected as a zero in the corresponding position of the matrix.

A complete scan cycle for the entire keyboard takes approximately 9.2 ms. Each key found pressed is debounced for a period of 20 ms. Once the key is verified, the corresponding key code(s) are loaded into the transmit buffer of the SPI communication channel.

N-Key Rollover

In this mode, the code(s) corresponding to each key press are transmitted to the host system as soon as that key is debounced, independent of the release of other keys.

When a key is released, the corresponding break code is transmitted to the host system. Several keys that can be held pressed at the same time. However, if two or more key closures occur within a time interval of less than 5 ms, an error flag is set and those key presses are not processed. This feature protects against the effects of accidental key presses.

Data Command Buffer

The SPICoder®06 implements a data buffer, which contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer is cleared and an "Initialize" command is sent to the host. At the same time, the keyboard is disabled until the "Initialize" or "Initialize Complete" command from the host is received.

Power Management Unit

Power management is covered in the next section, Keyboard States.

In most keyboard subsystems, the power consumption is largely determined by the use of the LEDs. However, the SPICoder®06 does not provide LED ouput.

A related IC, the SPICoder®SA01 UR5HCSPI-SA01, does provide LED output and uses two modes of operation to minimize power drain; for more information, see the data sheets for that IC.

KEYBOARD STATES

These states of operation refer only to the keyboard functionality and, although they are related to power states, they are also independent of them.

"Send All Keys"

Entry Conditions: Power on reset, soft reset, PWR_OK =1, {(LID=1) AND (WUKO=0)}

Exit Conditions: PWR_OK = 0 -> "Send No Keys"(WUKO=1) AND (Key Press) -> "Send Wake-Up Keys Only"(LID = 0) AND (WUKO=0) AND (Key Press) -> "Send XSW Key Only"

Description: This is the SPICoder®06's normal state of operation, accepting and transmitting every key press to the system. This state is entered after the power-on and is sustained while the unit is being used.

"Send Wake-Up Keys Only"

Entry Conditions: (WUKO=1) AND (Key or Switch press)

Exit Conditions: Soft Reset -> "Send All Keys"PWR_OK = 0 -> "Send No Keys"

Description: This state is entered when the user turns the unit off. A signal line driven by the host notifies the SPICoder®06 about this state transition. While in this state, the SPICoder®06 transmits only keys programmed to be wake-up keys to the system. It is not necessary for the SPICoder®06 to detect this transition in real time, since it does not affect any operation besides buffering keystrokes.

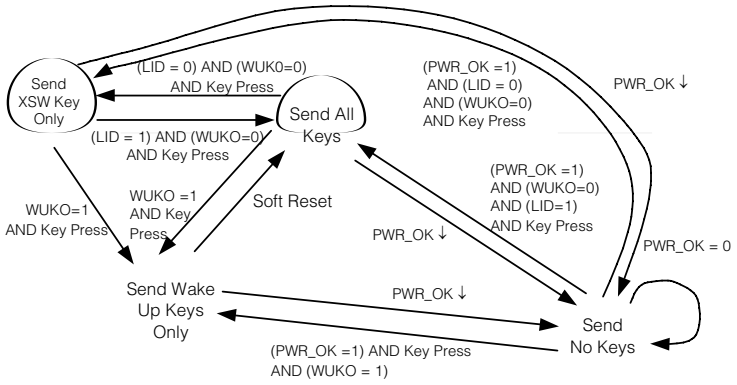


Figure 2: The UR5HCSPI-06 implements four modes of keyboard and switch operation.

"Send No Keys"

Entry Conditions: PWR_OK transition from high to low

Exit Conditions: (PWR_OK = 1) AND (Matrix key pressed OR Switch OR _WKUP)

Description: This state is entered when a PWR_OK signal is asserted (transition high to low), indicating a critically low level of battery voltage. The PWR_OK signal causes an interrupt to the SPICoder®06, which guarantees that the transition is performed in real time. While in this state, the SPICoder®06 performs as follows:

1. The SPICoder®06 enters the STOP mode for maximum energy conservation.

2. Stop mode time-out entry is shortened to further conserve energy.

3. While in this state all interrupts are disabled. The SPICoder®06 exits this state on the next interrupt event that detects the PWR_OK line has been de-asserted.

"Send XSW Key Only"

Entry Condition: (LID=0) AND (WUKO=0) AND (Key Press)

Exit Condition: (LID=1) AND (WUKO=0) AND (Key Press) -> "Send All Keys"PWR_OK = 0 -> "Send No Keys"
(WUKO = 1) AND (Key Press) -> "Send Wake Up Keys Only"

Description: This state is entered upon closing the lid of the device. While in this state, the SPICoder®06 transmits only the XSW key, which is located outside the unit. This feature is designed to accommodate buttons on the outside of the box, such as a microphone button, that need to be used while the lid is closed.

KEY CODES

Key codes range from 0x01 to 0x73 and are arranged as follows:

Make code = column_number * 8 + row_number + 1

Break code = Make code OR 0x80

Discrete Switches transmit the following codes:

XSW = 0x71

SW0 = 0x72

GIO0 = 0x73

Pin Configurations

When prototyping, caution should be taken to ensure that programming of the GIO0 pin does not conflict with the circuit implemented. A series protection resistor is recommended to be used for protection over improper programming of the pin.

After a power-on or soft reset, GIO0 defaults to the Input state.

The drawing to the right illustrates the suggested interface to the general purpose input/output pin.

GENERAL PURPOSE I/O PIN

The SPICoder® 06 has a general purpose I/O pin, GIO0, that can be programmed as input, output, or debounced switch input. The programmable I/O pin can be configured to the desired mode through a command from the system. After the I/O pin is configured, the host system can read data from it or write data to it. If the pin is configured as a debounced switch input, it returns scan codes.

Input Mode

While in the Input Mode, the GIO0 pin detects input signals and reports the input status to the system as required.

Output Mode

In the Output Mode, the SPICoder® 06 controls the output signal level according to the system command. When the pin is set at Output Mode, the default output is low.

Debounced Switch Input Mode

In Switch Input Mode, the SPICoder® 06 generates an individual make key code when the switch closes (pin goes low), and a break key code when the switch returns to open (pin goes to high). The switches generate key codes outside of those generated by the keyboard matrix, from 0x71 - 0x73. When the switch is closed, the SPICoder® 06 does not fall asleep.

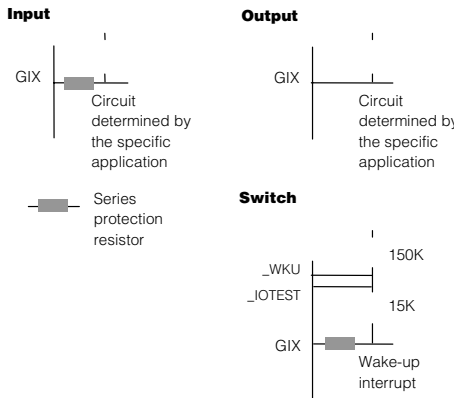


Figure 3: Suggested interface to the general purpose input/output pin

SPI COMMUNICATION CHANNEL

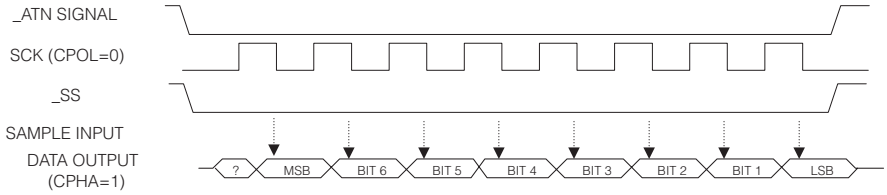
SPI data transfers can be performed at a maximum clock rate of 500 KHz. When the SPICoder® 06 asserts the _ATN signal to the host master, the data has already been loaded into the data register waiting for the clocks from the master. The Slave Select (SS) line can be tied permanently to ground if the SPICoder® 06 is the only slave device on the SPI bus. One _ATN signal is used per each byte transfer. If the host fails to provide clock signals for successive bytes in the data packet within 120 ms, the transmission is aborted and a new session is initiated by asserting a new ATN signal. In this case, the whole packet is re-transmitted.

If the SPI transmission fails 20 times consecutively, the synchronization between the master and slave may be lost. In this case, the SPICoder® 06 enters the reset state.

The SPICoder® 06 implements the SPI communication protocol according to the following diagram:

CPOL = 0 ---------- SCK line idles in low state

CPHA = 1 ---------- SS line is an output enable control



When the host sends commands to the keyboard, the SPICoder™ 06 requires that the minimum and maximum intervals between two successive bytes be 200 µs and 5 ms respectively.

Figure 4: SPI Communication Protocol

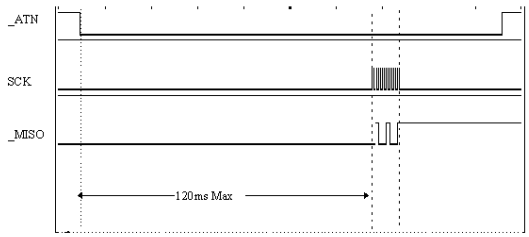


Figure 5: Transmitting Data Waveforms

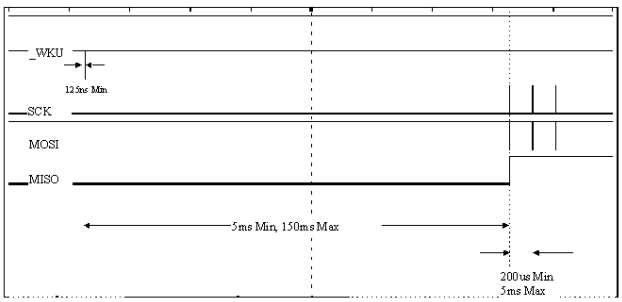


Figure 6: Receiving Data Waveforms

DATA/COMMAND BUFFER

The SPICoder® 06 implements a data buffer that contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer is cleared and an "Initialize" command is sent to the host. At the same time, the keyboard is disabled until the "Initialize" or "Initialize Complete" command from the host is received.

POWER MANAGEMENT UNIT

The SPICoder® 06 supports two modes of operation. The following table lists the typical and maximum supply current (no DC loads) for each mode at 3.3 Volts (+/- 10%).

Current	Typical	Max	Unit	Description
RUN	1.5 1	3.0	mA	Entered only while data/commands are in process
STOP	2.0	20	µA	Entered after 125 ms of inactivity

While the SPICoder® 06 is in the STOP mode, an active low Wake-Up Output from the Master must be connected to the edge-sensitive _WKU pin of the SPICoder® 06. This signal is used to wake up the SPICoder® 06 in order to receive data from the master host. The master host must wait a minimum of 5 ms prior to providing clocks to the SPICoder® 06. The SPICoder® 06 enters the STOP mode after a 125 ms period of keypad and/or host communications inactivity, or any time the PWR_OK line is asserted low by the host. Note that while one or more keys are held pressed, the SPICoder® 06 does not enter the STOP mode until every key is released.

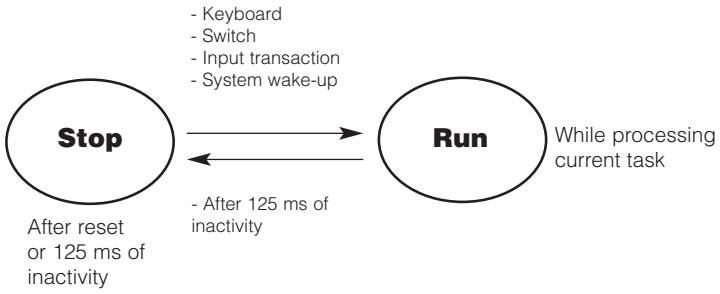


Figure 7: The Power States of the SPICoder® 06

LRC CALCULATION

The following C language function is an example of an LRC calculation program. It accepts two arguments: a pointer to a buffer and a buffer length. Its return value is the LRC value for the specified buffer.

```
char Calculate LRC (char  buffer,
size  buffer)
{
char LRC;
size_t index;
/*
* Init the LRC using the first two
message bytes.
*/
LRC = buffer [0] ^ buffer [1];
/*
* Update the LRC using the
remainder of the buffer.
*/
for (index = 2; index < buffer; index
++)
  LRC ^ = buffer[index];
/*
* If the MSB is set then clear the
MSB and change the next most
significant bit
*/
if (LRC & 0x80)
LRC ^ = 0xC0;
/* * Return the LRC value for the
buffer.*/}
```

COMMANDS FROM THE SPICODER® 06 TO THE HOST

Resend Request

<CONTROL>	0x80
<RESEND>	0xA5
<LRC>	0x25

The SPICoder® 06 sends this Resend Request Command to the host when its command buffer is full, or if it detects either a parity error or an unknown command during a system command transmission.

Input/Output Mode Status Report

<CONTROL>	0x80H	
<MODIO>	0xA7H	
<IO NUMBER>	0xnn	IO number, 0
<IO MODE>	0xnn	IO mode: (0=input; 1=output; 2=switch)
<LRC>	0xnn	

The SPICoder® 06 sends the I/O Mode Status Report to the host when it receives the I/O Mode Status Request Command from the host, in order to report the status of the GIO0 pin.

Input/Output Data Report

<CONTROL>	0x80	
<MODIO>	0xA8	
<IO NUMBER>	0xnn	IO number, 0
<IO DATA>	0xnn	IO data: (0=low, 1=high)
<LRC>	0xnn	

The SPICoder® 06 sends the I/O Data Report to the host when it receives the I/O Data Request Command from the host.

COMMANDS FROM THE HOST TO THE SPICODER® 06

Commands from the Host - Summary

Command Name	Code	Description
Initialize	0xAO	Causes the SPICoder® 06 to enter the power-on state
Initialization Complete	0xA1	Issued as a response to the “Initialize Request”
Heartbeat Request	0xA2	The SPICoder® 06 responds with “Heartbeat Response”
Identification Request	0xF2	The SPICoder® 06 responds with “Identification Response”
Resend Request	0xA5	Issued upon error during the reception of a packet
Input/Output Mode Modify	0xA7	The SPICoder® 06 modifies or reports the status of the GIO0 pin
Output Data to I/O pin	0xA8	The SPICoder® 06 outputs a signal to the GIO0 pin
Set Wake-Up Keys	0xA9	Defines which keys are “wake-up” keys

Each command to SPICoder® 06 is composed of a sequence of codes. All commands start with <ESC> code (0x1B) and end with the LRC code (bitwise exclusive OR of all bytes).

COMMANDS FROM THE HOST TO THE SPICODER® 06 ANALYTICALLY

Initialize

<ESC>	0x1B
<INIT>	0xA0
<LRC>	0x7B

When the SPICoder® 06 receives this command, it clears all buffers and return to the power-on state.

Initialization Complete

<ESC>	0x1B
<INIT COMPLETE>	0xA1
<LRC>	0x7A

When the SPICoder® 06 receives this command, it enables transmission of keyboard data. Keyboard data transmission is disabled if the TX output buffer is full (32 bytes). Note that if the transmit data buffer gets full the encoder issues an "Initialize Request" to the host.

Heartbeat Request

<ESC>	0x1B
<ONLINE>	0xA2
<LRC>	0x79

When the SPICoder® 06 receives this command, it replies with the Heartbeat Response Report.

Identification Request

<ESC>	0x1B
<ID>	0xF2
<LRC>	0x29

The SPICoder® 06 replies to this command with the Identification Response Report.

COMMANDS FROM THE HOST TO THE SPICODER® 06 (CONT'D)

Set Wake-Up Keys

<ESC>	0x1B	
<SETMATRIX>	0xA9	
<COL0>	0xnn	(R7 R6 R5 R4 R3 R2 R1 R0 Bitmap: 0-enabled, 1-disabled)
<COL1>	0xnn	
<COL2>	0xnn	
<COL3>	0xnn	
<COL4>	0xnn	
<COL5>	0xnn	
<COL6>	0xnn	
<COL7>	0xnn	
<COL8>	0xnn	
<COL9>	0xnn	
<COL10>	0xnn	
<COL11>	0xnn	
<COL12>*	0xnn	(*UR5HCSPI-06-06-XX only)
<COL13>*	0xnn	(*UR5HCSPI-06-06-XX only)
<SWITCHES>	0xnn	(where SWITCHES bit assignments are = x x x x x GIO0 SW0 XSW)
<LRC>	0xnn	

The "Set Wake-Up Keys" command is used to disable specific keys from waking up the host. Using this command, the host can set only a group of keys. For the SPICoder® 06, data in bytes <COL12> and <COL 13> is not relevant, but these two bytes must be present in the packet in order to preserve the packet structure.

I/O Mode Modify

<ESC>	0x1B	
<MODIO>	0xA7	
<IO NUMBER>	0xnn	IO number: 0
<IO MODE>	0xnn	IO mode: (0=input, 1=output, 2=switch, 4=current mode state request)
<LRC>	0xnn	

When the SPICoder® 06 receives this command, it changes the I/O pin's mode accordingly. If the <IO MODE> =4, the SPICoder® 06 sends the I/O Mode Status Report to the host.

Output Data to I/O Pin

<ESC>	0x1B	
<MODIO>	0xA8	
<IO NUMBER>	0xnn	IO number: 0
<IO DATA>	0xnn	IO data: (0=low, 1=high, 2=current I/O data request)
<LRC>	0xnn	

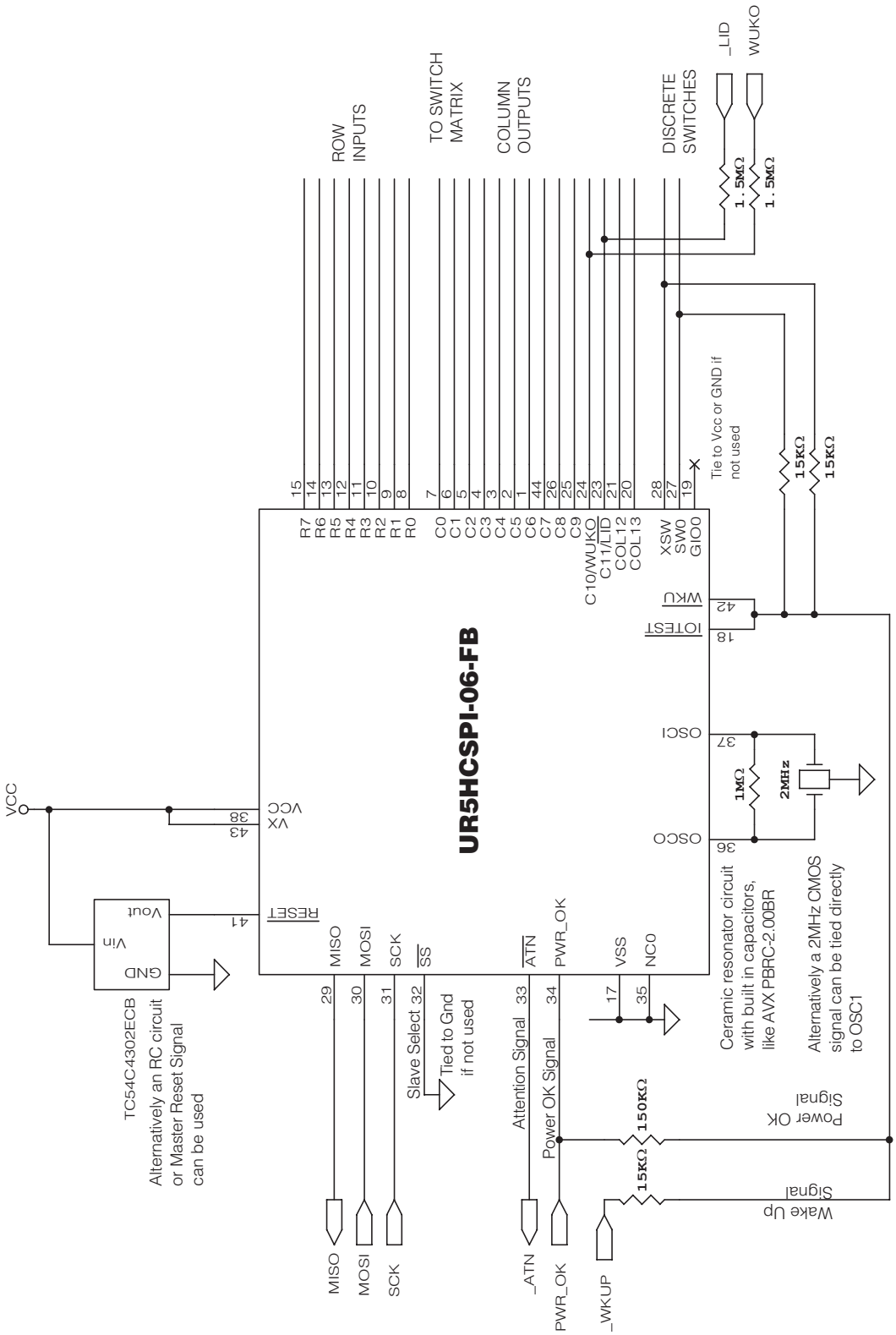
When the SPICoder® 06 receives this command, it changes the value of the output pin accordingly. If the addressed pin is not configured as an output pin, the command is ignored. If <IO DATA> =2, the SPICoder® 06 responds by issuing the I/O Data Status Report to the host.

KEY MAP FOR THE FUJITSU FKB1406

Rows (R0–R6) \ Columns (C0–C13)	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0	LAlt	`		LCtrl	FN	Esc	1 F1	2 F2	9 F9	0 F10	- NmLk	+ Bk		BkSp
1		\	LSft			Del		T	Y	U Pad 4	I Pad 5	Enter	RShift	↓ PgDn
2		TAB				Q	W	E	R	O Pad 6	P Ins	[Pause		] ScrLk
3		Z				CapLk			K Pad 2	L Pad 3	; PrtScr	‘ SysReq		↑ PgUp
4		A				S	D	F	G	H	J Pad 1	/ /		← Home
5		X				C	V	B	N Pad 0	M	,	.		Spc
6						3 F3	4 F4	5 F5	6 F6	7 F7	8 F8	Prog		→ End

KEYBOARD LAYOUT FOR FUJITSU FKB1406

SAMPLE CONFIGURATION UR5HCSPI-06-FB



SEMTECH

SPICODER® 06 BILL OF MATERIALS

UR5HCSPI-06-FB

Quantity	Manufacture	Part#	Description
3	Generic	15KΩ	15 KΩ resistor
1	Generic	150KΩ	150 KΩ resistor
1	Generic	1MΩ	1 MΩ resistor
2	Generic	1.5KΩ	1.5 KΩ resistors
1	Microchip	TC54VC4302ECB713	IC volt detector CMOS 4.3V SOT23, for 5V operation
		TC54VC2702ECB713	IC volt detector CMOS 2.7V SOT23, for 3.3V operation
1	AVX	PBRC-2.00BR	2.00 MHZ ceramic resonator with built in load capacitors, SMT

IMPLEMENTATION NOTES FOR THE SPICODER® 06

The following notes pertain to the suggested schematic found on a previous page.

The built-in oscillator on the SPICoder® 06 requires the attachment of a 2.00 MHz ceramic resonator with built-in load capacitors. You can use either an AVX, part number PBRC-2.00 BR; or a Murata part number CSTCC2.00MG ceramic resonator.

It may also be possible to operate with the 2.00 MHz crystal, albeit with reduced performance. Due to their high Q, the crystal oscillator circuits start up slowly. Since the SPICoder® 06 constantly switches the clock on and off, the ceramic resonator is better (it starts up much quicker than the crystal). Resonators are also less expensive than crystals.

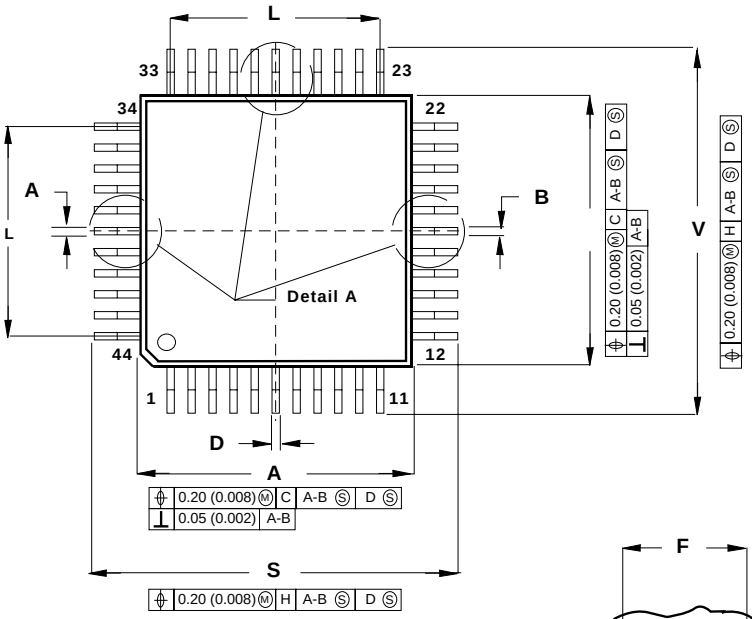
Also, if a crystal is used, two load capacitors (33pF to 47pF) should be added, a capacitor between each side of the crystal and ground.

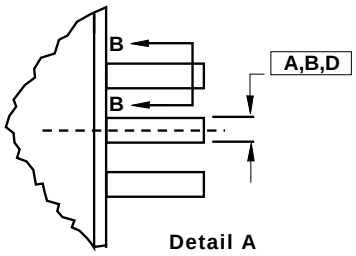
In both cases, using ceramic resonator with built-in load capacitors, or crystal with external load capacitors, a feedback resistor of 1 MegaOhm should be connected between OSCI and OSCO.

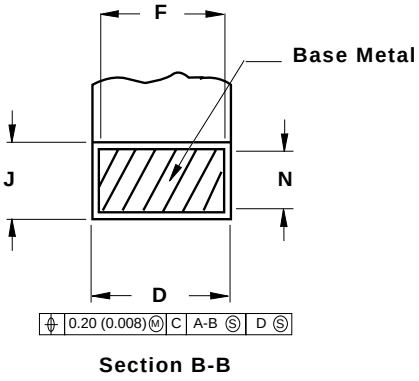
Troubleshoot the circuit by looking at the output pin of the oscillator. If the voltage is half-way between supply and ground (while the oscillator should be running) --- the problem is with the load caps / crystal. If the voltage is all the way at supply or ground (while the oscillator should be running) --- there are shorts on the PCB.

Note: When the oscillator is intentionally turned OFF, the voltage on the output pin of the oscillator is high (at the supply rail).

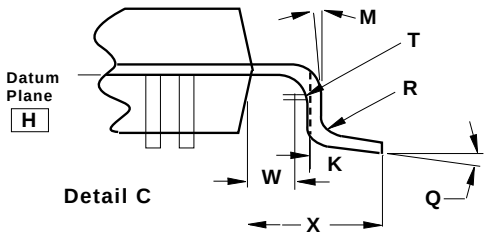
MECHANICALS FOR THE UR5HCSPI-06-FB

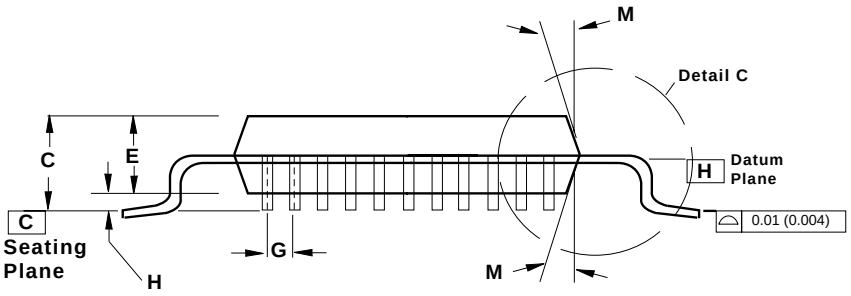






Section B-B





Notes

1. Dimensioning and tolerancing per Ansi Y14.5-M, 1982
2. Controlling dimension: Millimeter
3. Datum Plane "H" is located at the bottom of the lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -A-, -B-, and -D- to be determined at Datum Plane -H-.
5. Dimensions S and V to be determined at seating plane -C-.
6. Dimensions A and B do not include Mold protusion. Allowable protusion is 0.25 (0.010) per side. Dimensions A and B do include mold mismatch and are determined at Datum Plane -H-.
7. Dimension D does not include Danbar protrusion. Allowable Danbar protrusion is 0.08 (0.003) total in excess of the D dimension at Maximum Material Condition. Danbar cannot be located on the lower radius or the foot.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	-	0.25	-	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	-	0.005	-
U	0°	-	0°	-
V	12.95	13.45	0.510	0.530
W	0.40	-	0.016	-
X	1.6 REF		0.063 REF	

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ratings	Symbol		Value	Unit
Supply voltage	Vdd		-0.3 to +7.0	V
Input voltage	Vin		Vss -0.3 to Vdd +0.3	V
Current drain per pin (not including Vss or Vdd)	I		25	mA
Operating temperature UR5HCSPI-06	Ta		T low to T high -40 to +85	° C
Storage temperature range	Tstg -		-65 to +150	° C
ESD rating (human body model)	VESD		TBD	KV

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance	Tja		°C per W
■ Plastic		60	

DC Electrical Characteristics (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output voltage (I load<10µA)	Vol			0.1	V
	Voh	Vdd–0.1			
Output high voltage (I load=0.8mA)	Voh	Vdd–0.8			V
Output low voltage (I load=1.6mA) Vo			0.4	V	
Input high voltage	Vih	0.7xVdd		Vdd	V
Input low voltage	Vil	Vss		0.2xVdd	V
User mode current	Ipp		5	10	mA
Data retention mode (0 to 70°C)	Vrm	2.0			V
Supply current (Run)	Idd		1.53	3.0	mA
(Wait)			0.711	1.0	mA
(Stop)			2.0	20	µA
I/O Ports Hi-Z leakage current	Iil			+/-10	µA
Input current	Iin			+/- 1	µA
I/O port capacitance	Cio		8	12	pF

Control Timing (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
■ Crystal option	fosc		2.0	MHz
■ External clock option	fosc		2.0	MHz
Cycle time	tcyc	1000		ns
Crystal oscillator startup time	toxov		100	ms
Stop recovery startup time	tilch		100	ms
RESET pulse width	trl	8		tcyc
Interrupt pulse width low	tlih	250		ns
Interrupt pulse period	tilil	*		tcyc
OSCI pulse width	toh, tol	200		ns

*The minimum period tlil should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 tcyc.

SEMTECH

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