PaceMips™ PR3000A CPU
32-BIT RISC PROCESSOR WITH INTEGRATED MEMORY MANAGEMENT

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FEATURES

- 32-BIT RISC Processor:
  - Contains thirty-two general purpose 32-bit registers
  - All instructions and addresses are 32-bits
- On-Chip Memory Management Unit provides fast address translation for virtual-to-physical memory mapping of the 4 GByte virtual address space
- On-Chip Cache Control for Separate External Instruction and Data Caches of up to 256KBytes each
- Co-Processors can be used, including the PaceMips PR3010A (FPA)
- Five stage pipeline approaches execution rate of one instruction per cycle
- Produced with PACE III Technology™
- Very High Sustained System Performance
  - 17 VAX-MIPS @ 20 MHz
  - 21 VAX-MIPS @ 25 MHz
  - 28 VAX-MIPS @ 33 MHz
  - 34 VAX-MIPS @ 40 MHz
- Comprehensive System Development Support
- Available Packages:
  - 160-lead Metal Quad Flat Pack
  - 172-lead Ceramic Quad Flat Pack
  - 175-pin Ceramic Pin Grid Array
- Military Product Compliant to MIL-STD-883C, Class B
- Fully PR3000 Compatible

DESCRIPTION

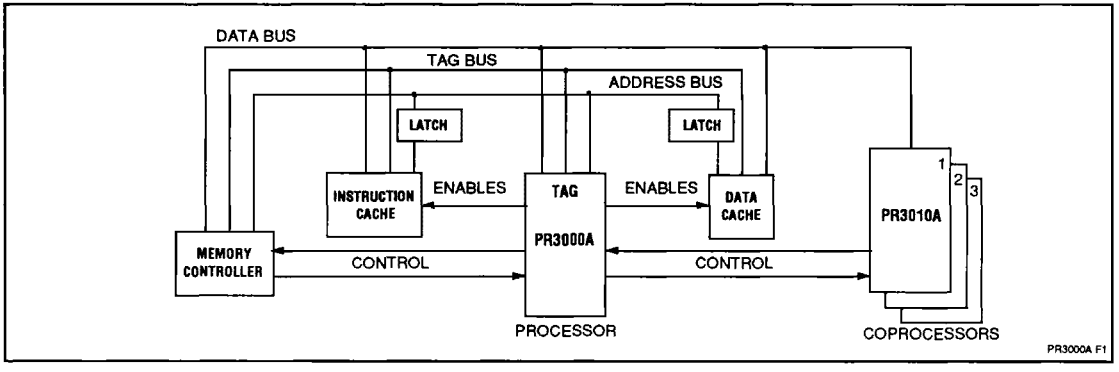
The PaceMips PR3000A Processor is an advanced 32-bit RISC processor designed for very high performance applications. The 32-bit architecture is based on "Reduced Instruction Set Computer" technology to achieve the highest performance possible from the PACE Technology. The PaceMips PR3000A approaches an execution rate of one instruction per cycle by using a LOAD/STORE architecture and a five stage pipeline. In a LOAD/STORE architecture all operations are carried out on operands contained in the processor registers, and only the load and store instructions can access the main memory system. The integrated memory management unit supports fast address translation for virtual-to-physical memory mapping.

The PaceMips PR3000A Processor is manufactured using PACE III Technology which is Performance Advanced CMOS Engineered to use 0.6 micron effective channel lengths resulting in 250 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

The PaceMips PR3000A Processor is available in a 160-lead Metal Quad Flat Pack, 172-lead Ceramic Quad Flat Pack and a 175-pin Ceramic Pin Grid Array.

* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply.

PROCESSOR SYSTEM BLOCK DIAGRAM



1.0 PR3000A vs. PR3000 DIFFERENCES

The PR3000A corrects the following errata found in Rev. 2 of PR3000:

1. If the processor is running in mapped space, data memory reads that are terminated by a bus error may modify the destination of the load instruction.

2. The isolate cache mode will not prevent the assertion of $\overline{\text{MemWr}}$ if the $\overline{\text{WrBusy}}$ signal is asserted during a store instruction.

3. When in the StorePartial Mode data parity driven to the system during a write buffer stall fixup cycle of partial word store will be incorrect.

4. When in the StorePartial Mode, if $\overline{\text{WrBusy}}$ is asserted during the Run cycle of a store partial instruction and is deasserted during the Fixup cycle, when $\overline{\text{MemWr}}$ is asserted, a write busy stall will be entered, which will cause another assertion of $\overline{\text{MemWr}}$ with the same data and address.

1.1 In addition, the following new functions have been added to the PR3000A:

1. Optionally drive AddrLo Bus high impedance during MP Stalls

   This is enabled by a mode bit [$\overline{\text{Int}}$(1)-Y cycle: LOW = hi-Z in MP stalls].

2. In $\overline{\text{PR3000}}$ Mode, allows Processor to display Parity Errors by asserting AccTyp(1) Pin during Cache Miss Stalls.

   This is enabled via a mode bit [$\overline{\text{Int}}$(2) – W cycle: HIGH = no signalling, LOW = signalling]. The state of this pin is undefined in the PR3000 .

3. Endianess Reversal in User Mode

   The RE bit has been added to bit 25 of the status register. When this bit is "1", all partial word/ unaligned data references in user mode will have the opposite byte ordering from the Endianess chosen at Reset provided the Display Parity option is selected as described above.

4. Provide Mode Bit to Allow Parity to be Ignored

   Controlled by a mode bit [$\overline{\text{Int}}$(2) – Y cycle: HIGH = normal parity checking, LOW = ignore parity errors]. If this option is chosen and no RAMs are provided to hold the cache parity bits, the unused parity lines must be pulled high or low with resistors so as to not allow inputs to the processor to float. Note that the parity outputs are still driven by the processor.

PR3000A User Selectable Modes

Interrupt Input	W Cycle	X Cycle	Y Cycle	Z Cycle
$\overline{\text{Int}}$(0)	$\overline{\text{DBlkSize0}}$	$\overline{\text{DBlkSize1}}$	ExCache	$\overline{\text{Big-Endian}}$
$\overline{\text{Int}}$(1)	$\overline{\text{IBlkSize0}}$	$\overline{\text{IBlkSize1}}$	$\overline{\text{MPAdrDisable}}$	$\overline{\text{Three-State}}$
$\overline{\text{Int}}$(2)	$\overline{\text{DispParRevEnd}}$	IStream	$\overline{\text{IgnoreParity}}$	$\overline{\text{NoCache}}$
$\overline{\text{Int}}$(3)	Reserved	StorePartial	MPS	BusDriveOn
$\overline{\text{Int}}$(4)	$\overline{\text{PhaseDelayOn}}$	$\overline{\text{PhaseDelayOn}}$	$\overline{\text{PhaseDelayOn}}$	$\overline{\text{PhaseDelayOn}}$
$\overline{\text{Int}}$(5)	$\overline{\text{PR3000}}$	$\overline{\text{PR3000}}$	$\overline{\text{PR3000}}$	$\overline{\text{PR3000}}$

For detailed operation and timing information, see the R3000A Processor Interface, March 9, 1990.

2.0 SIGNAL DESCRIPTIONS

Data(31:0)	I/O	A 32-bit bus used for all instruction & data transmission among processor, caches, memory interface, & coprocessors.
DataP(3:0)	I/O	A 4-bit bus containing even parity over the data bus.
Tag(31:12)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
TagP(2:0)	I/O	A 3-bit bus containing even parity over the catenation of TagV and Tag(31:12).
AdrLo(17:0)	O	A 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface.
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instruction cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp(2:0)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occuring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write.
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the run or stall state.
$\overline{\text{Exception}}$	O	Indicates instructions about to commit state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A reflection of the internal processor clock used to generate the system clock.
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by coprocessors for timing synchronization with the CPU.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
CpBusy	I	The coprocessor busy stall initiation/termination signal.
CpCond(1:0)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
$\overline{\text{Int}}$(5:0)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor.
Clk2xSys	I	The master double frequency input clock used for generating $\overline{\text{SysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine sample point for data coming into processor & coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{\text{Reset}}$ must be deasserted synchronously but asserted asynchronously. The deassertion of $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$.
CpCond(2:3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo(16:17) pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor to stall cache accesses. Multiplexed on CpCond(3).
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor to invalidate cache entries. Multiplexed on CpCond(2).

3.0 ELECTRICAL SPECIFICATIONS, COMMERCIAL TEMPERATURE RANGE (T = 0°C TO 70°C, V = 5V ±5%)

3.1 MAXIMUM RATINGS [3]

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	Input Voltage[1,2]		-0.5	+7.0	V

Notes:
1. V_{IN} Min. = -3.0V for pulse width less than 15ns.
2. $V_{in} \leq V_{CC} + 0.5$
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

3.2 RECOMMENDED OPERATING CONDITIONS [1, 2, & 3]

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 5%

Notes:
1. The case temperature must be limited by using adequate air flow and/or an appropriate heat sink or other thermal management design.
2. The maximum operating junction temperature should be limited to 125°C.
3. For optimum performance and improved reliability, it is recommended that the operating junction temperature should be kept below 85°C.

3.3 CAPACITIVE LOAD DERATING FACTOR

Sym.	Parameter	Conditions	20MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
C_{LD}	Load Derate		0.5	1	0.5	1	0.5	1	0.5	1	ns/25pF

3.4 DC ELECTRICAL CHARACTERISTICS

Sym.	Parameter	Conditions	20MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5		3.5		3.5		3.5		V
V_{OHC}	Output HIGH Voltage[3]	V_{CC} = Min., I_{OH} = -4mA	4.0		4.0		4.0		4.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC}+0.5	2	V_{CC}+0.5	2	V_{CC}+0.5	2	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V_{IHS}	Input HIGH Voltage[2]		3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	V
V_{ILS}	Input LOW Voltage[2]		-0.5	0.4	-0.5	0.4	-0.5	0.4	-0.5	0.4	V
C_{IN}	Input Capacitance			10		10		10		10	pF
C_{OUT}	Output Capacitance			10		10		10		10	pF
I_{CC}	Operating Current	V_{CC} = Max.		500		600		700		800	mA
C_{Ld}	Load Capacitance			25		25		25		25	pF
I_{IL}	Input LOW Current	V_{IN} = Gnd., V_{CC} = Max.		–10		–10		–30		–50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{CC}, V_{CC} = Max.	10		10		30		50		µA
I_{OZL}	Output 3-State Current LOW	V_{OUT} = 0.5V, V_{CC} = Max.		–40		–60		–80		–100	µA
I_{OZH}	Output 3-State Current HIGH	V_{OUT} = 2.4V, V_{CC} = Max.	40		60		80		100		µA

Notes:
1. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively are permissible for pulse widths up to 15ns.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2Phi, CpBusy and $\overline{\text{Reset}}$.
3. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.

3.5 AC ELECTRICAL CHARACTERISTICS, COMMERCIAL TEMPERATURE RANGE[1,2,3] (T = 0°C to 70°C, V = 5V ±5%)

Sym.	Parameter[1,2,3]	Conditions	20MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
T_{CkHigh}	Input Clock HIGH	Transition≤5ns	10		8		6		5		ns
T_{CkLow}	Input Clock LOW	Transition≤5ns	10		8		6		5		ns
T_{CkP}	Input Clock Period		25	125	20	100	15	75	12.5	60	ns
	Clk2xSys to Clk2xSmp		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xRd		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xPhi		7	$t_{Cyc/4}$	5	$t_{Cyc/4}$	4.0	$t_{Cyc/4}$	3.0	$t_{Cyc/4}$	ns
T_{DEn}	Data Enable	Run	-1	-2	-0.5	-1.5		-1		-1	ns
T_{DDis}	Data Disable	Run	0	-1	0	-0.5		-0.5		-0.5	ns
T_{DVal}	Data Valid	Run	2	3	1	2		2		1.5	ns
T_{WrDly}	Write Delay	Run	0	4	0	3		2		1.5	ns
T_{DS}	Data Setup	Run	8		6		4.5		4		ns
T_{DH}	Data Hold	Run	-2.5		-2.5		-1.5		-1.5		ns
T_{CBS}	CpBusy Setup	Run	11		9		7		6		ns
T_{CBH}	CpBusy Hold	Run	-2.5		-2.5		-1.5		-1.5		ns
T_{AcTy}	Access Type (1:0)	Run	1	6	1	5		4		3	ns
T_{AT2}	Access Type (2)	Run	1	15	1	12		8.5		7	ns
T_{MWr}	Memory Write	Run	1	23	1	18	0	8.5	0	7	ns
T_{Exc}	Exception	Run	1	6	1	5		3.5		3	ns
T_{AVal}	Address Valid	Run		2.5		2		1.5		1	ns
T_{IntS}	Int Setup	Run	7.5		6		5		4		ns
T_{IntH}	Int Hold	Run	-3.0		–2.5		-1.5		-1.0		ns
T_{SAVal}	Address Valid	Stall		25		20		15		12.5	ns
T_{SAcTY}	Access Type	Stall		23		18		9.5		8	ns
T_{MRdI}	Memory Read Initiate	Stall	1	23	1	18	1	9.5	1	8	ns
T_{MRdT}	Mem. Read Terminate	Stall	1	6	1	5		3.5		3	ns
T_{Sd}	Run Terminate	Stall	3	15	3	11	2	8	2	7	ns
T_{Run}	Run Initiate	Stall	1	6	1	4		3		2.5	ns
T_{SMWr}	Memory Write	Stall	3	23	3	18	1	9.5	1	8	ns
T_{SExc}	Exception Valid	Stall	3	18	3	15		9		7.5	ns

Notes: 1.All output times are given assuming 25pF of capacitive load.
2.All timings referenced to 1.5V.
3.The clock parameters apply to all four 2x Clocks.

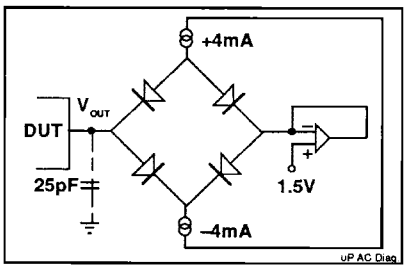


Figure 3.5.1 OUTPUT LOADING FOR AC TESTING

4.0 ELECTRICAL SPECIFICATIONS, MILITARY TEMPERATURE RANGE (T = –55°C TO 125°C, V = 5V ±10%)

4.1 MAXIMUM RATINGS [3]

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	Input Voltage[1,2]		-0.5	+7.0	V

Notes:
1. V_{IN} Min. = -3.0V for pulse width less than 15ns.
2. $V_{in} \leq V_{CC} + 0.5$
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

4.2 RECOMMENDED OPERATING CONDITIONS [1, 2, & 3]

Grade	Case Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0V ± 10%

Notes:
1. The case temperature must be limited by using adequate air flow and/or an appropriate heat sink or other thermal management design.
2. The maximum operating junction temperature should be limited to 125°C.
3. For optimum performance and improved reliability, it is recommended that the operating junction temperature should be kept below 85°C.

4.3 CAPACITIVE LOAD DERATING FACTOR

Sym.	Parameter	Conditions	20MHz		25MHz		28MHz		33MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
C_{LD}	Load Derate		0.5	1	0.5	1	0.5	1	0.5	1	ns/25pF

4.4 DC ELECTRICAL CHARACTERISTICS

Sym.	Parameter	Conditions	20MHz		25MHz		28MHz		33MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5		3.5		3.5		3.5		V
V_{OHC}	Output HIGH Voltage[3]	V_{CC} = Min., I_{OH} = -4mA	4.0		4.0		4.0		4.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC}+0.5	2	V_{CC}+0.5	2	V_{CC}+0.5	2	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	-0.5	0.8	–0.5	0.8	-0.5	0.8	V
V_{IHS}	Input HIGH Voltage[2]		3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	V
V_{ILS}	Input LOW Voltage[2]		-0.5	0.4	-0.5	0.4	–0.5	0.4	-0.5	0.4	V
C_{IN}	Input Capacitance			10		10		10		10	pF
C_{OUT}	Output Capacitance			10		10		10		10	pF
I_{CC}	Operating Current	V_{CC} = Max.		500		600		650		700	mA
C_{Ld}	Load Capacitance			25		25		25		25	pF
I_{IL}	Input LOW Current	V_{IN} = Gnd., V_{CC} = Max.		–10		–10		–20		–30	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{CC}, V_{CC} = Max.	10		10		20		30		µA
I_{OZL}	Output 3-State Current LOW	V_{OUT} = 0.5V, V_{CC} = Max.		–40		–60		–70		–80	µA
I_{OZH}	Output 3-State Current HIGH	V_{OUT} = 2.4V, V_{CC} = Max.	40		60		70		80		µA

Notes:
1. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively are permissible for pulse widths up to 15ns.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2Phi, CpBusy and $\overline{\text{Reset}}$.
3. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.

4.5 AC ELECTRICAL CHARACTERISTICS, MILITARY TEMPERATURE RANGE[1,2,3] (T = –55° to 125°C, V = 5V±10%)

Sym.	Parameter	Conditions	20MHz		25MHz		28MHz		33MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
T_{CkHigh}	Input Clock HIGH	Transition≤5ns	10		8		7		6		ns
T_{CkLow}	Input Clock LOW	Transition≤5ns	10		8		7		6		ns
T_{CkP}	Input Clock Period		25	125	20	100	17.5	75	15	60	ns
	Clk2xSys to Clk2xSmp		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xRd		0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	0	$t_{Cyc/4}$	ns
	Clk2xSmp to Clk2xPhi		7	$t_{Cyc/4}$	5	$t_{Cyc/4}$	4.5	$t_{Cyc/4}$	4.0	$t_{Cyc/4}$	ns
T_{DEn}	Data Enable	Run	-1	-2	-0.5	-1.5		–1		-1	ns
T_{DDis}	Data Disable	Run	0	-1	0	-0.5		–0.5		-0.5	ns
T_{DVal}	Data Valid	Run	2	3	1	2		2		2	ns
T_{WrDly}	Write Delay	Run	0	4	0	3		2.5		2	ns
T_{DS}	Data Setup	Run	8		6		4.5		4.5		ns
T_{DH}	Data Hold	Run	-2.5		-2.5		–1.5		-1.5		ns
T_{CBS}	CpBusy Setup	Run	11		9		8		7		ns
T_{CBH}	CpBusy Hold	Run	-2.5		-2.5		–1.5		-1.5		ns
T_{AcTy}	Access Type (1:0)	Run	1	6	1	5		4.5		4	ns
T_{AT2}	Access Type (2)	Run	1	15	1	12		10		8.5	ns
T_{MWr}	Memory Write	Run	1	23	1	18		11	0	8.5	ns
T_{Exc}	Exception	Run	1	6	1	5		4.5		3.5	ns
T_{AVal}	Address Valid	Run		2.5		2		1.5		1	ns
T_{IntS}	Int Setup	Run	7.5		6		5.5		5		ns
T_{IntH}	Int Hold	Run	–3.0		–2.5		–2.0		-1		ns
T_{SAVal}	Address Valid	Stall		25		20		18		15	ns
T_{SAcTY}	Access Type	Stall		23		18		13		9.5	ns
T_{MRdI}	Memory Read Initiate	Stall	1	23	1	18		13	1	9.5	ns
T_{MRdT}	Mem. Read Terminate	Stall	1	6	1	5		4.5		3.5	ns
T_{Sd}	Run Terminate	Stall	3	15	3	11		10	2	8	ns
T_{Run}	Run Initiate	Stall	1	6	1	4		3.5		3	ns
T_{SMWr}	Memory Write	Stall	3	23	3	18		13	1	9.5	ns
T_{SExc}	Exception Valid	Stall	3	18	3	15		12		9	ns

Notes: 1. All output times are given assuming 25pF of capacitive load.
2. All timings referenced to 1.5V.
3. The clock parameters apply to all four 2x Clocks.

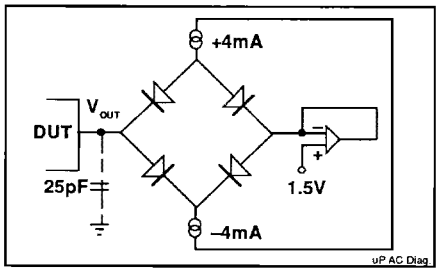


Figure 4.5.1 OUTPUT LOADING FOR AC TESTING

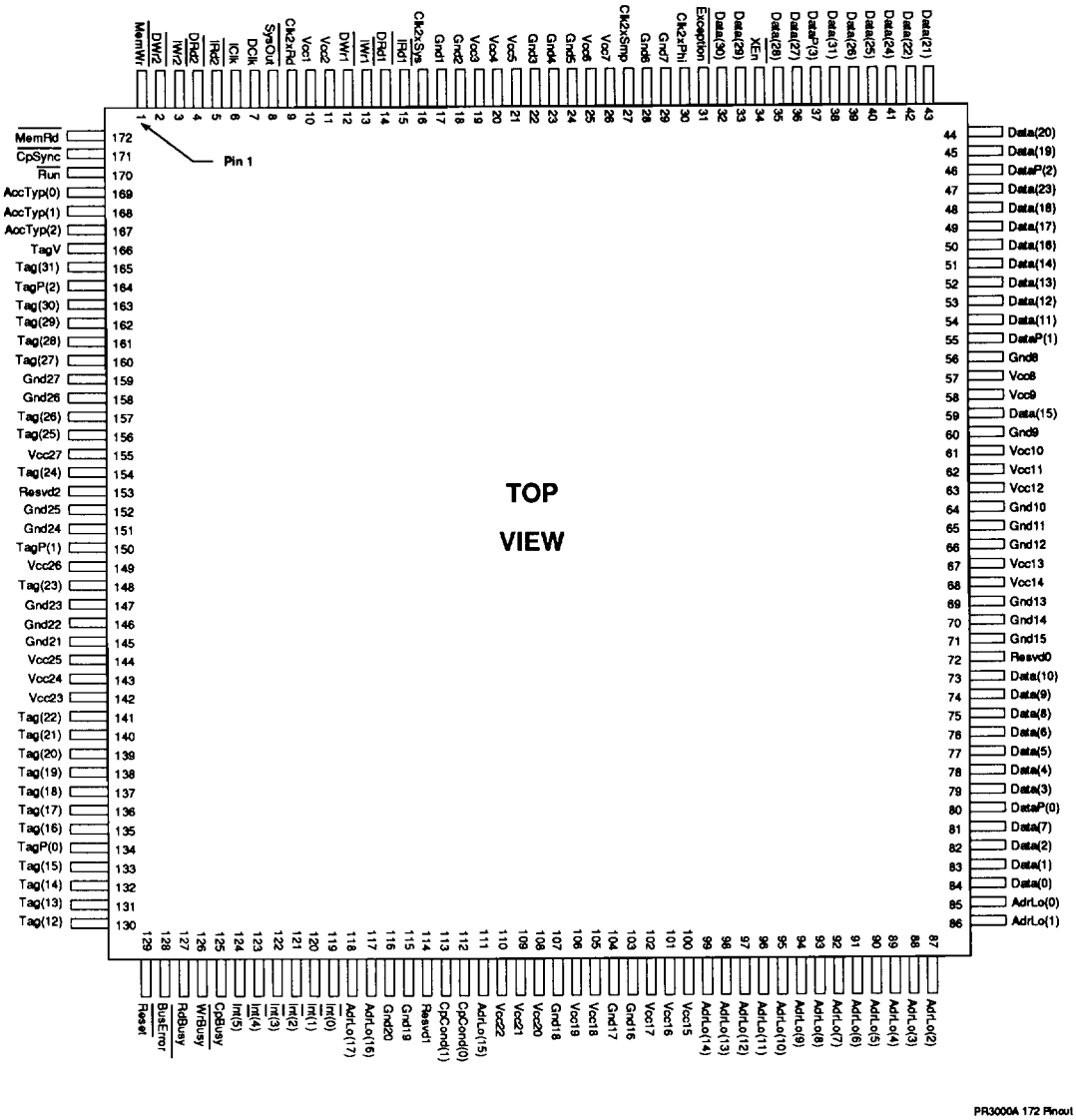
5.0 MECHANICAL DATA – PIN ASSIGNMENTS and PACKAGE DIMENSIONS

5.1 172-Lead Ceramic Quad Flat Pack

Table 5.1 PR3000A Pinout—172-Lead Ceramic Quad Flat Pack, Straight Lead, Cavity Down

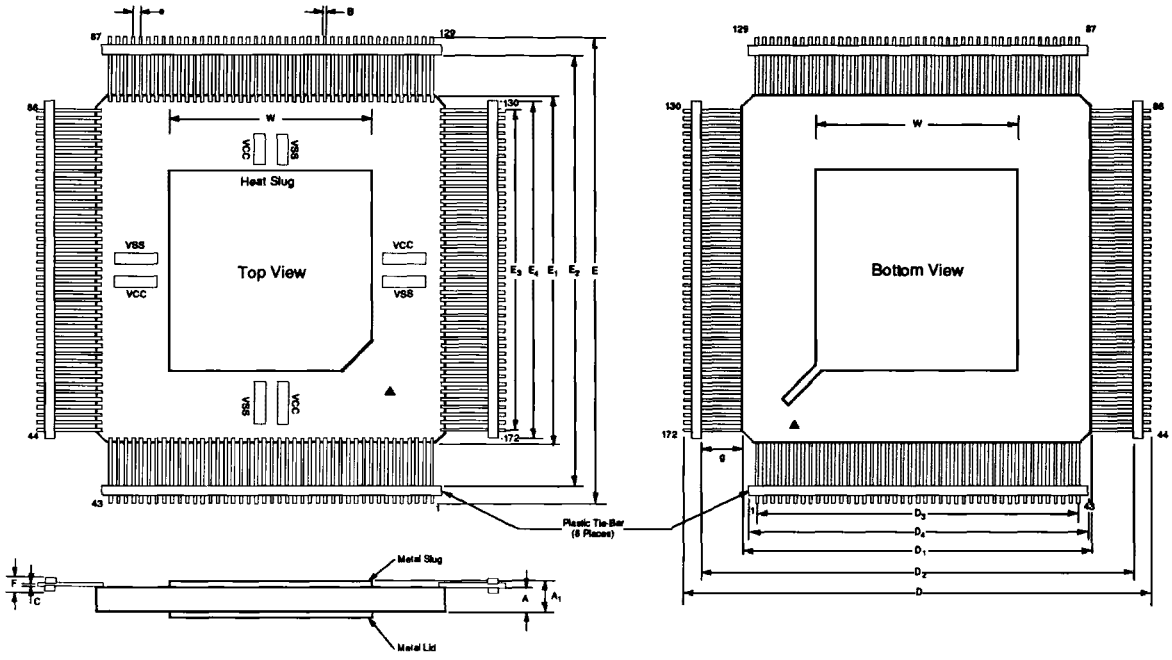
Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	84	Tag(12)	130	AdrLo(0)	85	Gnd1	17
Data(1)	83	Tag(13)	131	AdrLo(1)	86	Gnd2	18
Data(2)	82	Tag(14)	132	AdrLo(2)	87	Gnd3	22
Data(3)	79	Tag(15)	133	AdrLo(3)	88	Gnd4	23
Data(4)	78	Tag(16)	135	AdrLo(4)	89	Gnd5	24
Data(5)	77	Tag(17)	136	AdrLo(5)	90	Gnd6	28
Data(6)	76	Tag(18)	137	AdrLo(6)	91	Gnd7	29
Data(7)	81	Tag(19)	138	AdrLo(7)	92	Gnd8	56
Data(8)	75	Tag(20)	139	AdrLo(8)	93	Gnd9	60
Data(9)	74	Tag(21)	140	AdrLo(9)	94	Gnd10	64
Data(10)	73	Tag(22)	141	AdrLo(10)	95	Gnd11	65
Data(11)	54	Tag(23)	148	AdrLo(11)	96	Gnd12	66
Data(12)	53	Tag(24)	154	AdrLo(12)	97	Gnd13	69
Data(13)	52	Tag(25)	156	AdrLo(13)	98	Gnd14	70
Data(14)	51	Tag(26)	157	AdrLo(14)	99	Gnd15	71
Data(15)	59	Tag(27)	160	AdrLo(15)	111	Gnd16	103
Data(16)	50	Tag(28)	161	AdrLo(16)	117	Vcc1	10
Data(17)	49	Tag(29)	162	AdrLo(17)	118	Vcc2	11
Data(18)	48	Tag(30)	163	$\overline{\text{XEn}}$	34	Vcc3	19
Data(19)	45	Tag(31)	165	$\overline{\text{IRd1}}$	15	Vcc4	20
Data(20)	44	TagP(0)	134	$\overline{\text{IRd2}}$	5	Vcc5	21
Data(21)	43	TagP(1)	150	$\overline{\text{IWr1}}$	13	Vcc6	25
Data(22)	42	TagP(2)	164	$\overline{\text{IWr2}}$	3	Vcc7	26
Data(23)	47	TagV	166	$\overline{\text{DRd1}}$	14	Vcc8	57
Data(24)	41	$\overline{\text{Int}}$(0)	119	$\overline{\text{DRd2}}$	4	Vcc9	58
Data(25)	40	$\overline{\text{Int}}$(1)	120	$\overline{\text{DWr1}}$	12	Vcc10	61
Data(26)	39	$\overline{\text{Int}}$(2)	121	$\overline{\text{DWr2}}$	2	Vcc11	62
Data(27)	36	$\overline{\text{Int}}$(3)	122	IClk	6	Vcc12	63
Data(28)	35	$\overline{\text{Int}}$(4)	123	DClk	7	Vcc13	67
Data(29)	33	$\overline{\text{Int}}$(5)	124	Resvd0	72	Vcc14	68
Data(30)	32	CpCond(0)	112	Resvd1	114	Vcc15	100
Data(31)	38	CpCond(1)	113	Resvd2	153	Vcc16	101
DataP(0)	80	AccTyp(0)	169	Gnd17	104	Vcc17	102
DataP(1)	55	AccTyp(1)	168	Gnd18	107	Vcc18	105
DataP(2)	46	AccTyp(2)	167	Gnd19	115	Vcc19	106
DataP(3)	37	$\overline{\text{MemWr}}$	1	Gnd20	116	Vcc20	108
Clk2xSys	16	$\overline{\text{MemRd}}$	172	Gnd21	145	Vcc21	109
Clk2xSmp	27	$\overline{\text{Run}}$	170	Gnd22	146	Vcc22	110
Clk2xRd	9	$\overline{\text{Exception}}$	31	Gnd23	147	Vcc23	142
Clk2xPhi	30	$\overline{\text{BusError}}$	128	Gnd24	151	Vcc24	143
$\overline{\text{RdBusy}}$	127	$\overline{\text{Reset}}$	129	Gnd25	152	Vcc25	144
$\overline{\text{WrBusy}}$	126	$\overline{\text{SysOut}}$	8	Gnd26	158	Vcc26	149
CpBusy	125	$\overline{\text{CpSync}}$	171	Gnd27	159	Vcc27	155

Figure 5.1 PR3000A Pin Diagram — 172-Lead Ceramic Quad Flat Pack, Straight Lead, Cavity Down



PR3000A 172 Pinout

Figure 5.2 PR3000A Package Dimensions — 172-Lead Ceramic Quad Flat Pack, Straight Lead, Cavity Down



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.085	2,15	0.105	2,67
A_1	0.108	2,75	0.122	3,10
B	0.008	0,20	0.012	0,30
C	0.004	0,10	0.008	0,20
D/E	1.850	47,0	1.890	48,0
D_1/E_1	1.145	29,03	1.155	29,33
D_2/E_2	1.670	42,41	1.710	43,43
D_3/E_3	1.050	26,67	1.050	26,67
D_4/E_4	1.100	27,94	1.120	28,44
e	0.025 BSC	0,64 BSC	0.025 BSC	0,64 BSC
g	0.214	5,43	N/A	N/A
W	0.785	20,0	0.860	22,0

5.2 175-Pin Pin Grid Array

Table 5.2 PR3000A Pinout—175-Pin Ceramic Pin Grid Array, Cavity Down

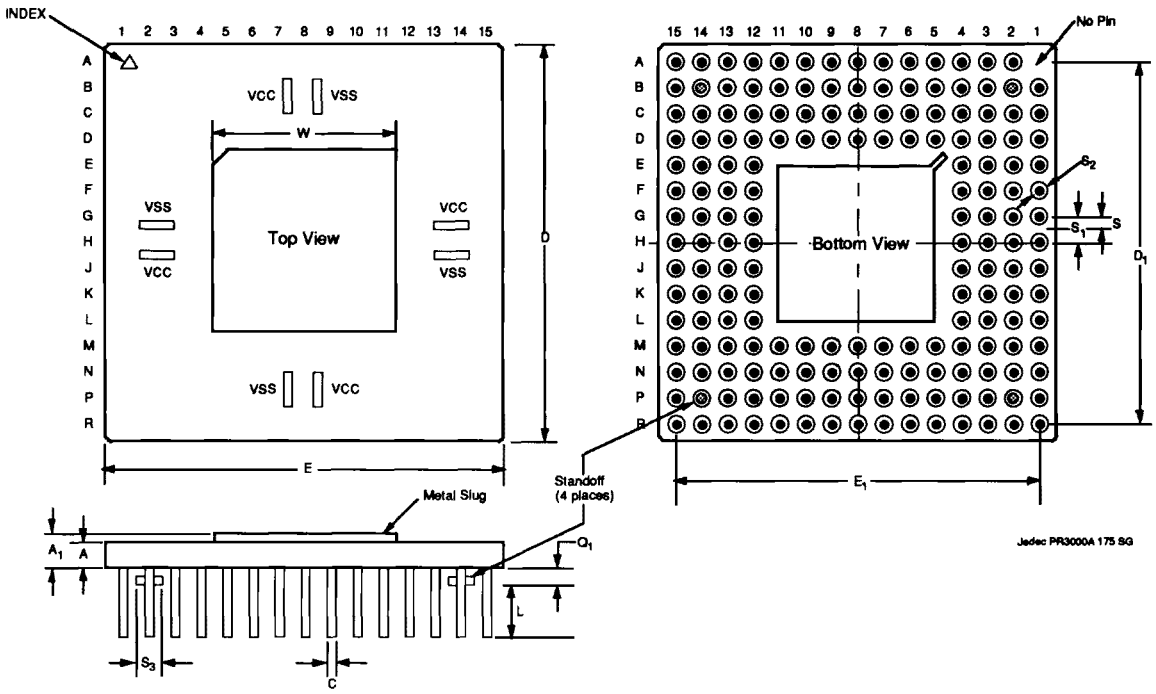
Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	E2	Tag(12)	B14	AdrLo(0)	C1	Vcc17	M11
Data(1)	D1	Tag(13)	C13	AdrLo(1)	E3	Vcc18	L4
Data(2)	F3	Tag(14)	D13	AdrLo(2)	D2	Vcc19	L12
Data(3)	G2	Tag(15)	B15	AdrLo(3)	B1	Vcc20	J4
Data(4)	G1	Tag(16)	E13	AdrLo(4)	C2	Vcc21	J12
Data(5)	H2	Tag(17)	D14	AdrLo(5)	C4	Vcc22	G4
Data(6)	H1	Tag(18)	C15	AdrLo(6)	A2	Vcc23	G12
Data(7)	F2	Tag(19)	D15	AdrLo(7)	B3	Vcc24	E4
Data(8)	H3	Tag(20)	E14	AdrLo(8)	C5	Vcc25	E12
Data(9)	J3	Tag(21)	F14	AdrLo(9)	B4	Vcc26	D5
Data(10)	J1	Tag(22)	G14	AdrLo(10)	A3	Vcc27	D7
Data(11)	K2	Tag(23)	F15	AdrLo(11)	A4	Vcc28	D9
Data(12)	L2	Tag(24)	H15	AdrLo(12)	B5	Vcc29	D11
Data(13)	M1	Tag(25)	H14	AdrLo(13)	B7		
Data(14)	N1	Tag(26)	J15	AdrLo(14)	A6	Gnd0	D3
Data(15)	K1	Tag(27)	K15	AdrLo(15)	A7	Gnd1	G3
Data(16)	M2	Tag(28)	J13	$\overline{\text{SysOut}}$	R11	Gnd2	K3
Data(17)	L3	Tag(29)	J14	$\overline{\text{CpSync}}$	P14	Gnd3	N4
Data(18)	N2	Tag(30)	L15	$\overline{\text{Reset}}$	A14	Gnd4	R6
Data(19)	N3	Tag(31)	L14	$\overline{\text{Exception}}$	R8	Gnd5	N9
Data(20)	P2	TagP(0)	C14	IClk	R13	Gnd6	N10
Data(21)	R2	TagP(1)	G15	DClk	P11	Gnd7	M13
Data(22)	P4	TagP(2)	K14	$\overline{\text{XEn}}$	P7	Gnd8	K13
Data(23)	P1	TagV	N15	$\overline{\text{IRd2}}$	B6	Gnd9	G13
Data(24)	N5	$\overline{\text{Int}}$(0)	C9	$\overline{\text{IWr2}}$	P3	Gnd10	F13
Data(25)	R3	$\overline{\text{Int}}$(1)	B9	$\overline{\text{DRd2}}$	B2	Gnd11	C12
Data(26)	P5	$\overline{\text{Int}}$(2)	A11	$\overline{\text{DWr2}}$	B13	Gnd12	C7
Data(27)	P6	$\overline{\text{Int}}$(3)	B10	Vcc0	F1	Gnd13	C6
Data(28)	R5	$\overline{\text{Int}}$(4)	C10	Vcc1	L1	Gnd14	M4
Data(29)	R7	$\overline{\text{Int}}$(5)	A12	Vcc2	R1	Gnd15	M6
Data(30)	P8	CpCond(0)	A8	Vcc3	N7	Gnd16	M8
Data(31)	R4	CpCond(1)	B8	Vcc4	N8	Gnd17	M10
DataP(0)	E1	AdrLo(16)	A9	Vcc5	R12	Gnd18	M12
DataP(1)	J2	AdrLo(17)	A10	Vcc6	R15	Gnd19	K4
DataP(2)	M3	AccTyp(0)	P15	Vcc7	M15	Gnd20	K12
DataP(3)	N6	AccTyp(1)	M14	Vcc8	H13	Gnd21	H4
Clk2xSys	P9	AccTyp(2)	L13	Vcc9	E15	Gnd22	H12
Clk2xSmp	R10	$\overline{\text{MemWr}}$	N12	Vcc10	A15	Gnd23	F4
Clk2xRd	P10	$\overline{\text{MemRd}}$	N13	Vcc11	C8	Gnd24	F12
Clk2xPhi	R9	$\overline{\text{Run}}$	N14	Vcc12	A5	Gnd25	D4
$\overline{\text{RdBusy}}$	C11	$\overline{\text{IRd1}}$	P12	Vcc13	C3	Gnd26	D6
$\overline{\text{WrBusy}}$	A13	$\overline{\text{IWr1}}$	P13	Vcc14	M5	Gnd27	D8
$\overline{\text{CpBusy}}$	B11	$\overline{\text{DRd1}}$	N11	Vcc15	M7	Gnd28	D10
$\overline{\text{BusError}}$	B12	$\overline{\text{DWr1}}$	R14	Vcc16	M9	Gnd29	D12

Figure 5.3 PR3000A Pin Diagram — 175-Pin Ceramic Pin Grid Array, Cavity Down

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	Vcc 2	DATA (21)	DATA (25)	DATA (31)	DATA (28)	Gnd 4	DATA (29)	EXCEPTION	CLK2X PHI	CLK2X SMP	SYSOUT	Vcc 5	ICLK	DWR1	Vcc 6
P	DATA (23)	DATA (20)	IWR2	DATA (22)	DATA (26)	DATA (27)	XEN	DATA (30)	CLK2X SYS	CLK2X RD	DCLK	IRD1	IWR1	CP SYNC	ACC TYP(0)
N	DATA (14)	DATA (18)	DATA (19)	Gnd 3	DATA (24)	DATA P(3)	Vcc 3	Vcc 4	Gnd 5	Gnd 6	DRD1	MEM WR	MEM RD	RUN	TAG V
M	DATA (13)	DATA (16)	DATA P(2)	Gnd 14	Vcc 14	Gnd 15	Vcc 15	Gnd 16	Vcc 16	Gnd 17	Vcc 17	Gnd 18	Gnd 7	ACC TYP(1)	Vcc 7
L	Vcc 1	DATA (12)	DATA (17)	Vcc 18								Vcc 19	ACC TYP(2)	TAG (31)	TAG (30)
K	DATA (15)	DATA (11)	Gnd 2	Gnd 19								Gnd 20	Gnd 8	TAG P(2)	TAG (27)
J	DATA (10)	DATA P(1)	DATA (9)	Vcc 20								Vcc 21	TAG (28)	TAG (29)	TAG (26)
H	DATA (6)	DATA (5)	DATA (8)	Gnd 21				**175-Pin PGA (Bottom View)**				Gnd 22	Vcc 8	TAG (25)	TAG (24)
G	DATA (4)	DATA (3)	Gnd 1	Vcc 22								Vcc 23	Gnd 9	TAG (22)	TAG P(1)
F	Vcc 0	DATA (7)	DATA (2)	Gnd 23								Gnd 24	Gnd 10	TAG (21)	TAG (23)
E	DATA P(0)	DATA (0)	ADRLO (1)	Vcc 24								Vcc 25	TAG (16)	TAG (20)	Vcc 9
D	DATA (1)	ADRLO (2)	Gnd 0	Gnd 25	Vcc 26	Gnd 26	Vcc 27	Gnd 27	Vcc 28	Gnd 28	Vcc 29	Gnd 29	TAG (14)	TAG (17)	TAG (19)
C	ADRLO (0)	ADRLO (4)	Vcc 13	ADRLO (5)	ADRLO (8)	Gnd 13	Gnd 12	Vcc 11	INT0	INT4	RD BUSY	Gnd 11	TAG (13)	TAG P(0)	TAG (18)
B	ADRLO (3)	DRD2	ADRLO (7)	ADRLO (9)	ADRLO (12)	IRD2	ADRLO (13)	CP COND (1)	INT1	INT3	CP BUSY	BUS ERROR	DWR2	TAG (12)	TAG (15)
A	NO PIN	ADRLO (6)	ADRLO (10)	ADRLO (11)	Vcc 12	ADRLO (14)	ADRLO (15)	CP COND (0)	ADRLO (16)	ADRLO (17)	INT2	INT5	WR BUSY	RESET	Vcc 10

PR3000A 175 Pinout

Figure 5.4 PR3000A Package Dimensions — 175-Pin Ceramic Pin Grid Array, Cavity Down



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.075	1,93	0.110	2,79
A_1	0.110	2,80	0.130	3,30
C	0.013	0,33	0.023	0,58
D/E	1.559	39,59	1.590	40,4
D_1/E_1	1.388	35,36	1.412	35,76
L	0.120	3,05	0.140	3,55
M*	15	15	15	15
N**	175	175	175	175
Q_1	0.050	1,27	0.050	1,27
S	0.050	1,27	0.050	1,27
S_1	0.100 BSC	2,54 BSC	0.100 BSC	2,54 BSC
S_2	0.055	1,40	0.075	1,90
S_3	0.050	1,27 TYP	0.050	1,27 TYP
W	0.670	17,02	0.690	17,52

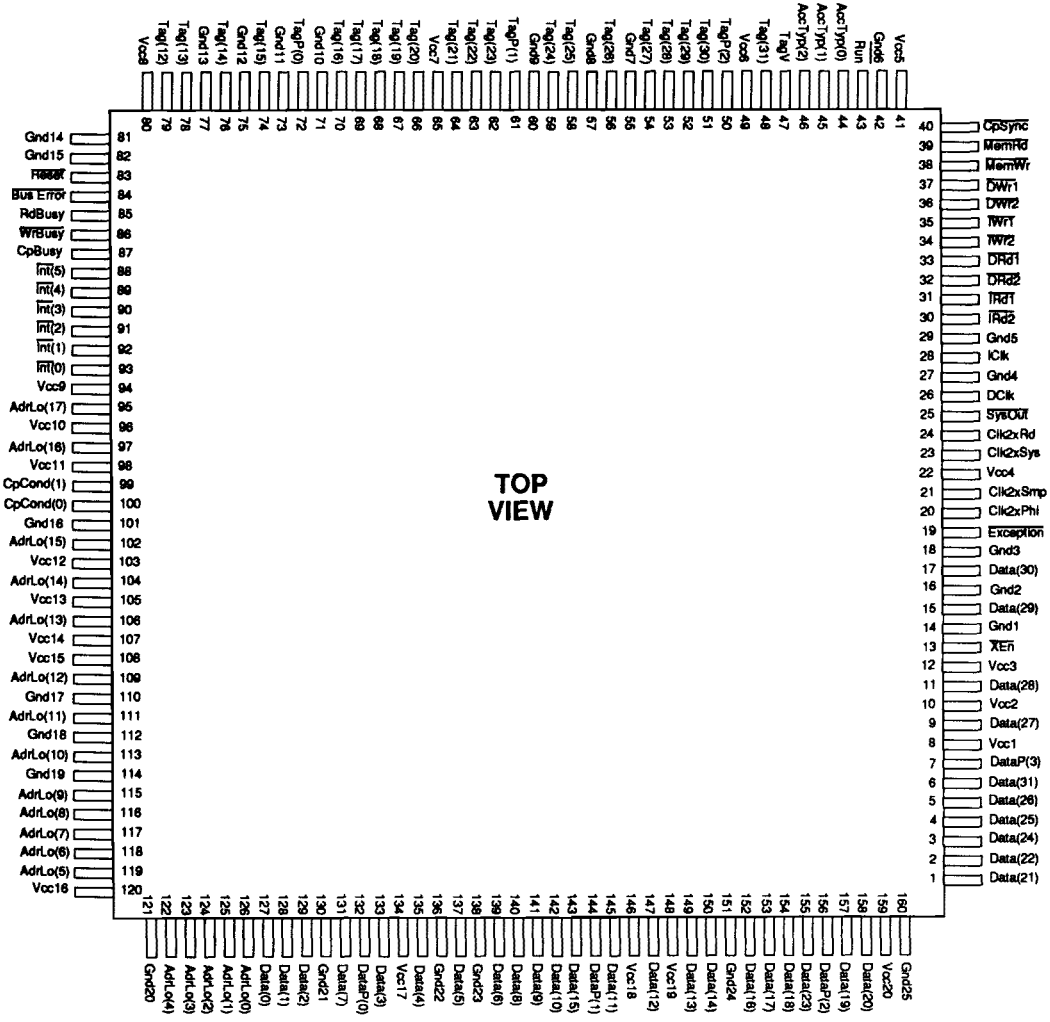
* Typical number of pins per row
** Total number of pins per package
BSC = Basic Spacing between Centers

5.3 160 -Lead Metal Quad Flat Pack

Table 5.3 Pinout —160-lead Metal Quad Flat Pack, Gull Wing, Cavity Down, EIAJ Standard

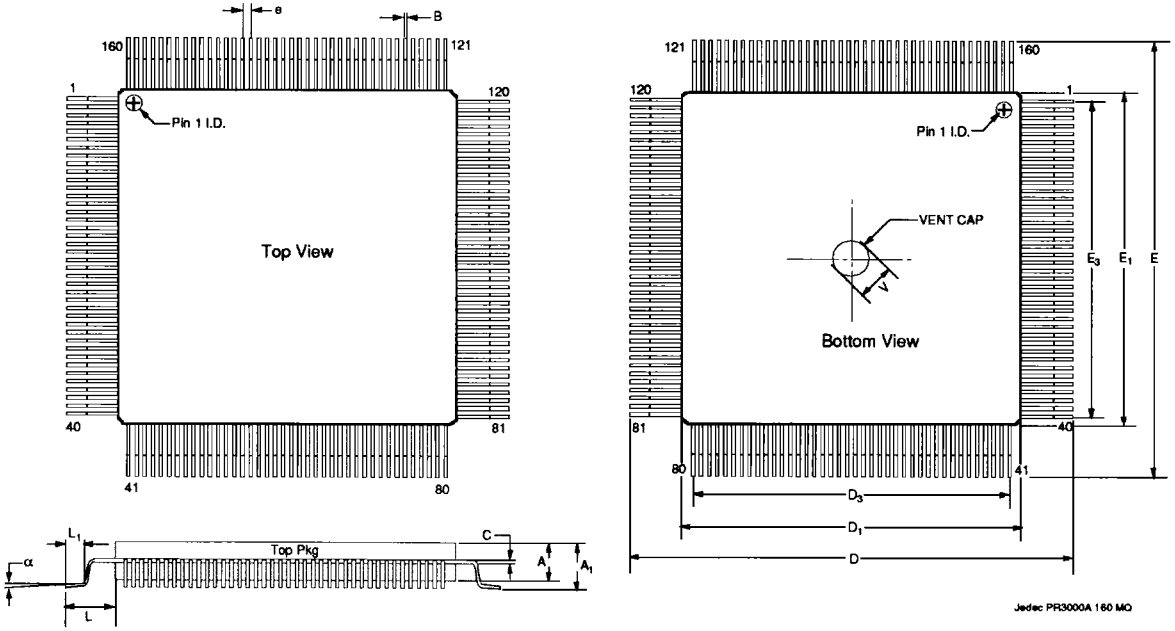
Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	127	Tag(12)	79	AdrLo(0)	126	Gnd10	71
Data(1)	128	Tag(13)	78	AdrLo(1)	125	Gnd11	73
Data(2)	129	Tag(14)	76	AdrLo(2)	124	Gnd12	75
Data(3)	133	Tag(15)	74	AdrLo(3)	123	Gnd13	77
Data(4)	135	Tag(16)	70	AdrLo(4)	122	Gnd14	81
Data(5)	137	Tag(17)	69	AdrLo(5)	119	Gnd15	82
Data(6)	139	Tag(18)	68	AdrLo(6)	118	Gnd16	101
Data(7)	131	Tag(19)	67	AdrLo(7)	117	Gnd17	110
Data(8)	140	Tag(20)	66	AdrLo(8)	116	Gnd18	112
Data(9)	141	Tag(21)	64	AdrLo(9)	115	Gnd19	114
Data(10)	142	Tag(22)	63	AdrLo(10)	113	Gnd20	121
Data(11)	145	Tag(23)	62	AdrLo(11)	111	Gnd21	130
Data(12)	147	Tag(24)	59	AdrLo(12)	109	Gnd22	136
Data(13)	149	Tag(25)	58	AdrLo(13)	106	Gnd23	138
Data(14)	150	Tag(26)	56	AdrLo(14)	104	Gnd24	151
Data(15)	143	Tag(27)	54	AdrLo(15)	102	Gnd25	160
Data(16)	152	Tag(28)	53	Exception	19		
Data(17)	153	Tag(29)	52	XEn	13		
Data(18)	154	Tag(30)	51	Run	43		
Data(19)	157	Tag(31)	48	Vcc1	8		
Data(20)	158	TagP(0)	72	Vcc2	10		
Data(21)	1	TagP(1)	61	Vcc3	12		
Data(22)	2	TagP(2)	50	Vcc4	22		
Data(23)	155	TagV	47	Vcc5	41		
Data(24)	3	Int(0)	93	Vcc6	49		
Data(25)	4	Int(1)	92	Vcc7	65		
Data(26)	5	Int(2)	91	Vcc8	80		
Data(27)	9	Int(3)	90	Vcc9	94		
Data(28)	11	Int(4)	89	Vcc10	96		
Data(29)	15	Int(5)	88	Vcc11	98		
Data(30)	17	CpCond(0)	100	Vcc12	103		
Data(31)	6	CpCond(1)	99	Vcc13	105		
DataP(0)	132	AdrLo(16)	97	Vcc14	107		
DataP(1)	144	AdrLo(17)	95	Vcc15	108		
DataP(2)	156	AccTyp(0)	44	Vcc16	120		
DataP(3)	7	AccTyp(1)	45	Vcc17	134		
Clk2xSys	23	AccTyp(2)	46	Vcc18	146		
Clk2xSmp	21	MemWr	38	Vcc19	148		
Clk2xRd	24	MemRd	39	Vcc20	159		
Clk2xPhi	20	DWr2	36	Gnd1	14		
RdBusy	85	IRd1	31	Gnd2	16		
WrBusy	86	IWr1	35	Gnd3	18		
CpBusy	87	DRd1	33	Gnd4	27		
BusError	84	DWr1	37	Gnd5	29		
Reset	83	IClk	28	Gnd6	42		
SysOut	25	DClk	26	Gnd7	55		
CpSync	40	IWr2	34	Gnd8	57		
DRd2	32	IRd2	30	Gnd9	60		

Figure 5.5 PR3000A Pin Diagram–160-Lead Metal Quad Flat Pack, Gull Wing, Cavity Down, EIAJ Standard



PR3000A 160 Pinout

Figure 5.6 PR3000A Package Dimensions–160-Lead Metal Quad Flat Pack, Gull Wing, Cavity Down, EIAJ Standard



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.125	3,15	0.135	3,45
A_1	0.135	3,50	0.150	3,85
C	0.004	0,10	0.008	0,20
B	0.010	0,25	0.012	0,30
D/E	1.240	31,50	1,260	32,0
D_1/E_1	1.085	27,55	1.100	27,75
D_3/E_3	1.000	25,4	1.000	25,4
e	0.025 BSC	0,64 BSC	0.25 BSC	0,64 BSC
L	0.040	1,00	0.080	2,00
L_1	0.025	0,65	0.040	0,95
V	0.120	3,10	0.125	3,20
α	0°–5°	0°–5°	0°–5°	0°–5°

BSC = Basic Spacing between Centers

6.0 MOUNTING

A variety of sockets allow low insertion force or zero insertion force mountings, and a choice of terminals such as soldertail, surface mount or wire wrap. Several sockets are available from the following sample list of socket manufacturers. Contact the manufacturer directly for the latest socket specifications.

- AMP Incorporated
  P.O.Box 3608
  Harrisburg, PA 17105-3608
  (800) 522-6752
- Burndy Corporation
  Richards Avenue
  Norwalk, CT 06856
  (203) 838-4444
- Yamaichi Electronics Inc.
  1425 Koll Circle, Suite 106
  San Jose, CA 95112
  (408) 452-0797
- Textool/3M Test
  and Interconnect Products Department
  3M Austin Center
  P.O.Box 2963
  Austin, TX 78769-2963
  (800) 225-5373

7.0 ORDERING INFORMATION

PACEMIPS Microprocessor Products

PR3000A – xx x x xxx x

Temperature/Qualification
C = Commercial Temperature Range, 0° to 70°C
M = Military Temperature Range, –55° to +125°C
B = Military Qual to MIL-STD-883C, Class B

Number of Pins: 160, 172 &175

Package Code
F = Quad Flat Pack/Straight Lead
G = Pin Grid Array
Q = Quad Flat Pack/Gull Wing

Package Type
M = Metal
S = Hermetic Solder Seal

Speeds (MHz):
Commercial = 20, 25, 33 & 40
Military = 20, 25, 28 & 33