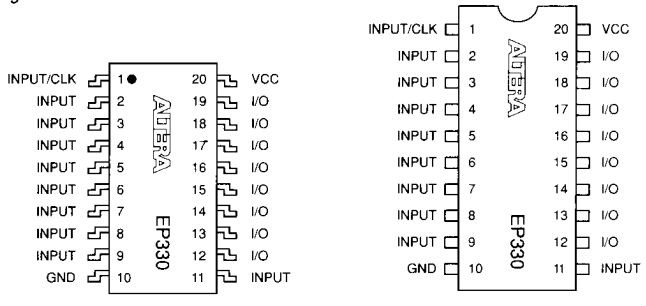
Features

- High-performance, 8-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 125 MHz
- Low power; I_{CC} = 45 mA (typical)
- Macrocell flipflops can be individually programmed for registered or combinatorial operation
- Available in 20-pin, one-time-programmable (OTP) plastic packages (see Figure 7):
  - Small-outline integrated circuit (SOIC)
  - Dual in-line package (PDIP)
- Direct replacement for 20-pin PAL/GAL devices

Figure 7. EP330 Package Pin-Out Diagrams

Package outlines not drawn to scale.



General Description

The Altera EP330 EPLD is a high-speed, low-power device that is a direct replacement for GAL 16V8 and most 20-pin PAL programmable logic devices. The EP330 has 8 macrocells, 10 dedicated input pins, and 8 I/O pins (see Figure 8). Each macrocell can access signals from the global bus. The global bus consists of the true and complement forms of the device inputs and the macrocell outputs. Pin 1 can be used as the global Clock for registers in the device or as a dedicated input for combinatorial logic.

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Figure 8. EP330 Block Diagram

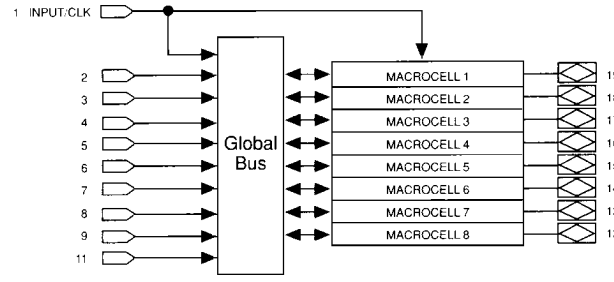
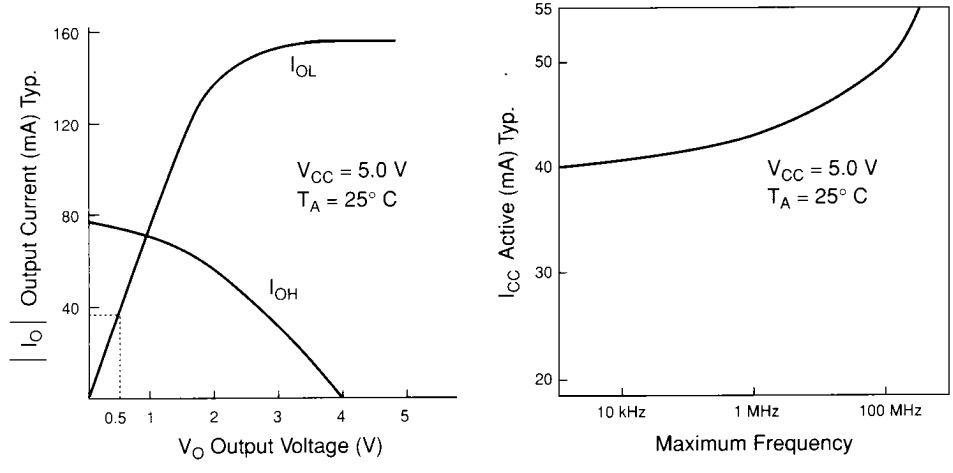


Figure 9 shows the maximum output drive characteristics of EP330 I/O pins and typical supply current (I_{CC}) versus frequency for the EP330 EPLD.

Figure 9. EP330 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



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Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–160	160	mA
I_{OUT}	DC output current, per pin		–50	50	mA
P_D	Power dissipation			800	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*Note (2)*		20	ns
t_F	Input fall time	*Note (2)*		20	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load, *Note (5)*		40	75	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Note (5)*		45	75	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF

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AC Operating Conditions *Note (4)*

			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15	ns
t_{PD2}	I/O input to non-registered output			13		16	ns
t_{PZX}	Input to output enable			12		15	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		12		15	ns
t_{IO}	I/O input pad and buffer delay			1		1	ns

Global Clock Mode			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	125		100		MHz
t_{SU}	Setup time		6		8		ns
t_H	Hold time		0		0		ns
t_{CH}	Clock high time		4		5		ns
t_{CL}	Clock low time		4		5		ns
t_{CO1}	Clock to output delay			8		10	ns
t_{CNT}	Minimum clock period			10		12	ns
f_{CNT}	Internal maximum frequency	*Note (5)*	100		83.3		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.

(2) For all Clocks: t_R and t_F = 20 ns.

(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.

(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.

(5) Measured with a device programmed as an 8-bit counter. I_{CC} measured at 0° C.

(6) Capacitance measured at 25° C. Sample-tested only. Pin 11 (high-voltage pin during programming) has maximum capacitance of 20 pF.

(7) Sample-tested only for an output change of 500 mV.

(8) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP330-12, EP330-15
Industrial Temp.	(–40° C to 85° C)	EP330-15

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