4-Bit Microcontroller

TMP47C241N
TMP47C241M

CMOS 4-Bit Microcontroller

TMP47C241N, TMP47C241M

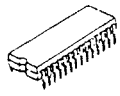
The 47C241 has 8-bit A/D converter, watchdog timer serial interface based on the TLCS-47E series.

Part No.	ROM	RAM	Package	OTP	Piggyback + Adapter
TMP47C241N	2048 x 8-bit	128 x 4-bit	SDIP28	TMP47P241VN	TMP47P940AE + BM1152 (SDIP)
TMP47C241M			SOP28	TMP47P241VM	

Features

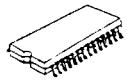
- 4-bit single chip microcomputer
- Instruction execution time:
  - 1.3μs (at 6MHz)
- Low voltage operation:
  - 2.7V (at 4.2MHz RC)
- 90 basic instructions
- Table look-up instructions
- Subroutine nesting:
  - 15 levels max.
- 6 interrupt sources (External: 2, Internal: 4)
  - All sources have independent latches each, and multiple interrupt control is available.
- I/O port (21 pins)
  - Input 2 ports 5 pins
  - Output 2 ports 5 pins
  - I/O 4 ports 11 pins
- Two 12-bit Timer/Counters
  - Timer, event counter, and pulse width measurement mode
- Interval Timer
- Watchdog Timer
- Serial Interface with 4-bit buffer
  - External/internal clock, and leading/trailing edge shift mode
- 8-bit successive approximate type A/D converter
  - With sample and hold
  - 4 analog inputs
  - Converting time: 48μs (4MHz)
- High current outputs
  - LED direct drive capability: typ. 20mA x 5 bits (Ports P1, P2)
    typ. 7mA x 3 bits (Port R9)
- Hold function
  - Battery/Capacitor back-up
- Real Time Emulator:
  - BM47214A + BM1152 (SDIP)

SDIP28-P-400



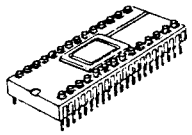
TMP47C241N
TMP47C241VN

SOP28-P-450



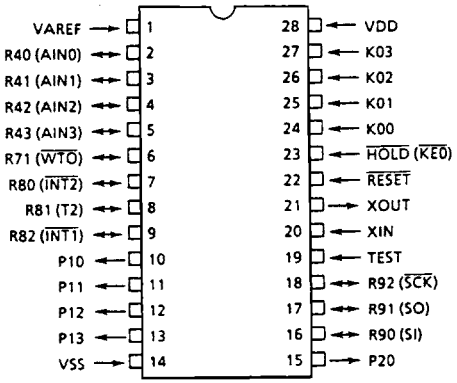
TMP47C241M
TMP47C241VM

SDIC42

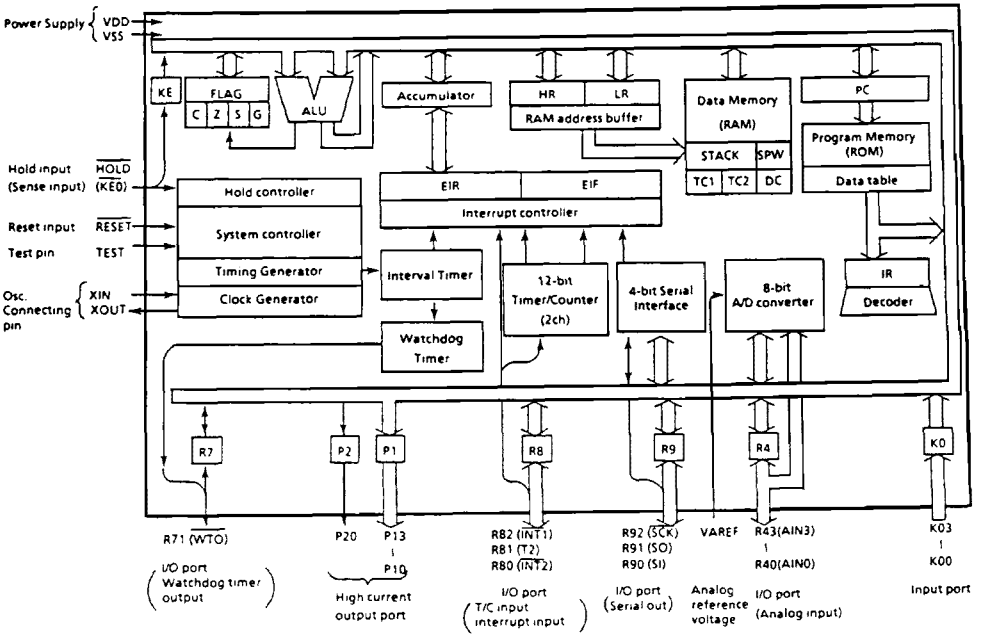


TMP47C940AE

Pin Assignment (Top View)



Block Diagram



Pin Function

Pin Name	Input/Output	Functions	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch.	
P20		1-bit output port with latch.	
R43 (AIN3) R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	A/D converter analog input
R71 ($\overline{WT0}$)	I/O (Output)	1-bit I/O port with latch. When using as input port or watchdog timer output, the latch must be set to "1".	Watchdog timer output
R82 ($\overline{INT1}$) R81 (T2) R80 ($\overline{INT2}$)	I/O (Input)	3-bit I/O port with latch. When using as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	External interrupt 1 input Timer/Counter 2 external input External interrupt 2 input
R92 ($\overline{SCK}$) R91 (SO) R90 (SI)	I/O (I/O) I/O (Output) I/O (Input)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O Serial data output Serial data input
XIN XOUT	Input Output	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{RE0}$)	Input (I/O)	Hold request/release signal input	Sense input
VDD VSS	Power Supply	+5V, 0V (GND)	
VAREF		A/D converter analog reference	

Operational Description

Concerning the 47C241, the hardware configuration and operation are described.

As the description is provided with priority on those parts differing from the 47C200B, the technical data sheets for the 47C200B shall also be reffered to.

The 47C940A can be used by piggyback. Therefore, caution is required, the technical data sheets for 47C940A shall also referred to. Notes for use of the piggyback are the same as the 47C242B.

1. System Configuration

(1) I/O Ports
(2) A/D Converter
(3) Watchdog Timer

2. Peripheral Hardware Function

2.1 Ports

The 47C241 has 8 I/O ports (21 pins) each as follows:

1) K0 ; 4-bit input
2) P1 ; 4-bit output
3) P2 ; 1-bit output
4) R4 ; 4-bit input/output (shared by A/D converter analog inputs)
5) R7 ; 1-bit input/output (shared by the watchdog timer output)
6) R8 ; 3-bit input/output (shared by external interrupt request input and timer/counter output)
7) R9 ; 3-bit input (shared bt serial port)
8) KE ; 1-bit sense input (shared by hold request/release signal input)

This section describes ports of 3~6 which are changed from the 47C200B. Table 2-1 lists the port address assignments and the I/O instructions that can access the ports. The 5-bit to 8-bit data conversion instruction [OUTB @HL] is invalid.

(1) Port P2 (P20)

Port P2 is 1-bit output port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset. P21, P22 and P23 pins do not exist actually but these pins have the latches.

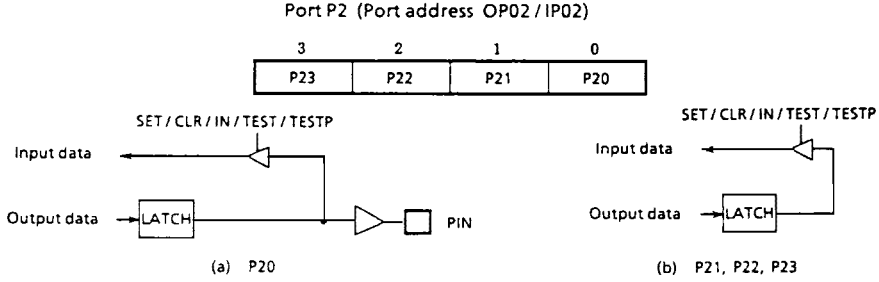


Figure 2-1. Port P2

(2) Ports R4 (R43-R40)

Ports R4 is 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion.

The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

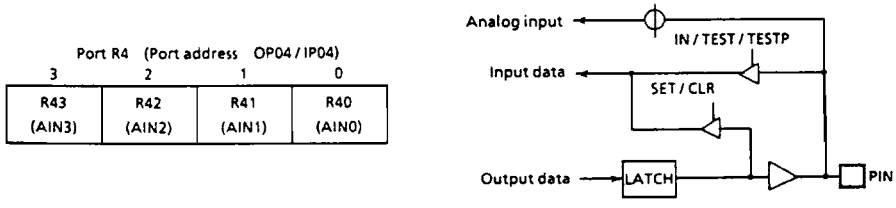


Figure 2-2. Port R4

3) Port R7 (R71)

1-bit I/O pin with latch. R71 pin is shared by the watchdog timer output. To use R71 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R70, R72, R73 pins do not exist actually but R70 has the latch. In R72 and R73, "1 " is read when an input instruction is executed.

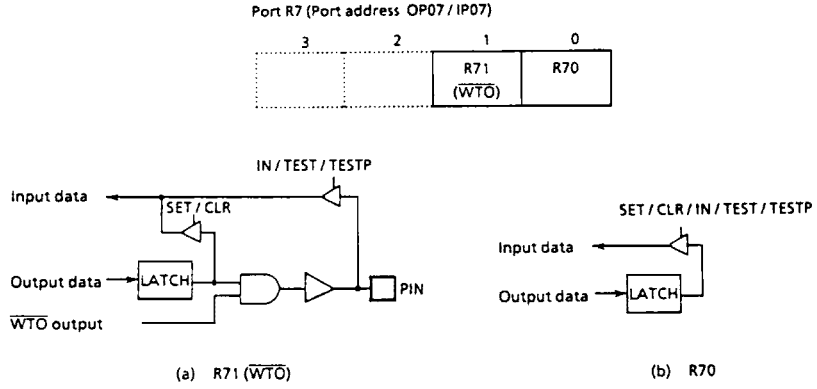


Figure 2-3. Port R7

(4) Port R8 (R82-R80)

3-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset. R83 pins does not exist actually but R83 has the latch. There is no timer/counter 1 external input pin (T1).

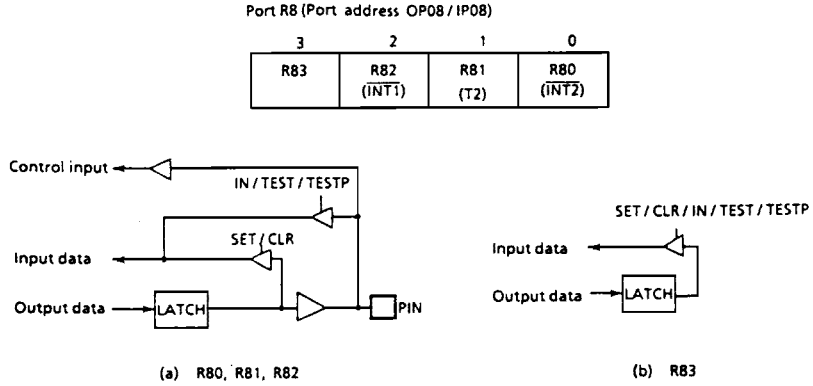


Figure 2-4. Port R8

2.2 Timer/Counter (TC1, TC2)

The 47C241 does not have timer/counter 1 external input. Therefore, timer/counter 1 can be used as internal timer mode only. Other function are equivalent to the 47C200B.

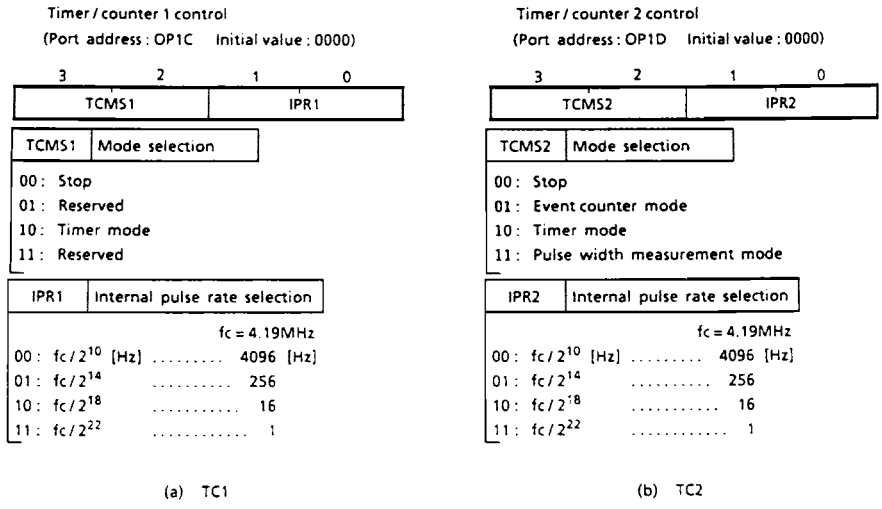


Figure 2-5. Timer/Counter Control Command Registers

Table 2-1. Port Address Assignments and Available I/O Instructions

Port Address (**)	Port		Input/Output Instructions						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB@HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	-	O	-	-	-	-	O	-
01	P1 output latch	P1 output port	O	O	O	-	O	O	-
02	P2 output latch	P2 output port	O	O	O	-	O	O	-
03	-	-	-	-	-	-	-	-	-
04	R4 input port	R4 output port	O	O	O	-	O	O	O
05	-	-	-	-	-	-	-	-	-
06	R6 input port	R6 output port	-	-	-	-	-	-	-
07	-	-	O	O	O	-	O	O	O
08	R8 input port	R8 output port	O	O	O	-	O	O	
09	R9 input port	R9 output port	O	O	O	-	O	O	
0A			-	-	-	-	-	-	-
0B			-	-	-	-	-	-	-
0C	A/D Status input		O	-	-	-	-	-	-
0D	A/D converted value		O	-	-	-	-	-	-
0E	SIO Hold Status	-	O	-	-	-	-	-	-
0F	Serial receive buffer	Serial transmit buffer	O	O	O	-	-	-	-
10_H	Undefined	Hold operating mode control	-	O	-	-	-	-	-
11	Undefined	-	-	-	-	-	-	-	-
12	Undefined	A/D analog input selector	-	O	-	-	-	-	-
13	Undefined	A/D analog input selector	-	O	-	-	-	-	-
14	Undefined	-	-	-	-	-	-	-	-
15	Undefined	Watchdog timer control	-	O	-	-	-	-	-
16	Undefined	-	-	-	-	-	-	-	-
17	Undefined	-	-	-	-	-	-	-	-
18	Undefined	-	-	-	-	-	-	-	-
19	Undefined	Interval Timer interrupt control	-	O	-	-	-	-	-
1A	Undefined	-	-	-	-	-	-	-	-
1B	Undefined	-	-	-	-	-	-	-	-
1C	Undefined	Timer/Counter 1 control	-	-	-	-	-	-	-
1D	Undefined	Timer/Counter 2 control	-	O	-	-	-	-	-
1E	Undefined	Serial Interface Control	-	-	-	-	-	-	-
1F	Undefined	SIO control 2	-	O	-	-	-	-	-

Note 1. "-" means the reserved state. Unavailable for the user programs.

2.3 A/D Converter

The 47C241 has a 8-bit successive approximate type A/D converter and is capable of processing 4 analog inputs.

2.3.1 Circuit Configuration

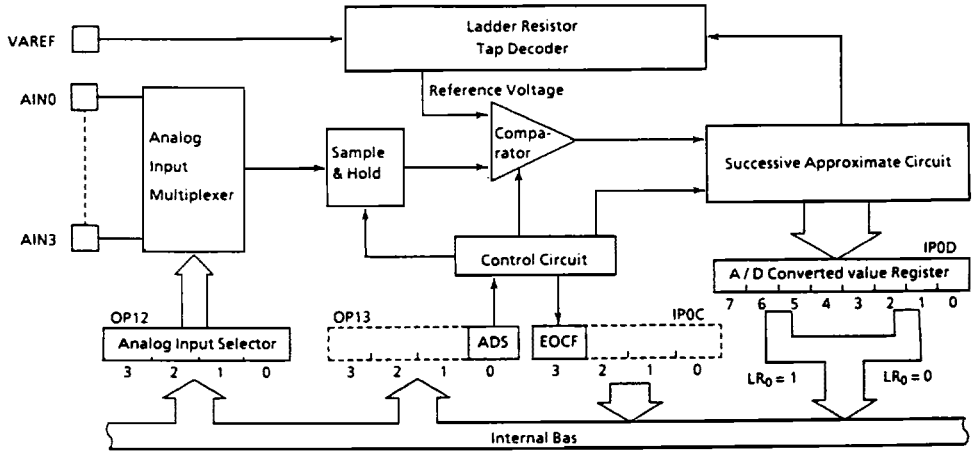


Figure 2-6. Block Diagram of A/D Converter

2.3.2 Control of A/D Converter

The operation of A/D converter is controlled by a command. The command register is accessed as port addresses OP12 and OP13. A/D converted value and end of conversion flag (EOCF) can be known by accessing port addresses IPOD and IPOC.

(1) Analog input selector

Analog inputs (AIN0 through AIN3) are selected by values of this register.

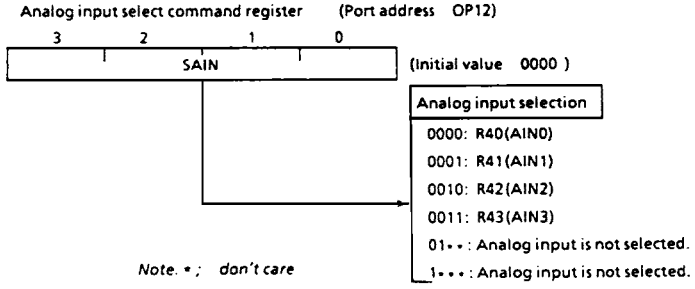


Figure 2-7. Analog Input Selector

(2) Start of AID conversion

A/D conversion is started when ADS is set to "1". After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time.

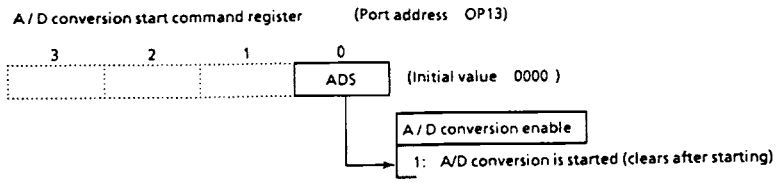


Figure 2-8. A/D Conversion Start Register

(3) A/D converted value register

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L-registers).

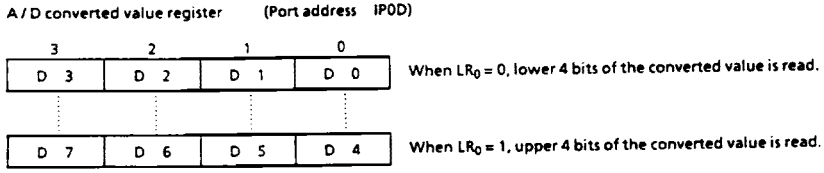


Figure 2-9. A/D Converted Value Register

(4) A/D converter status register

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

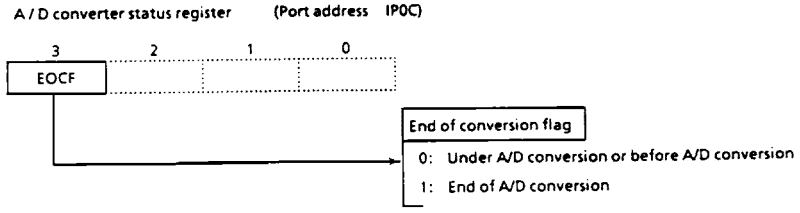


Figure 2-10. A/D Converter Status Register

2.3.3 How to use A/D Converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VSS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VSS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

Analog supply current (I_{REF}) is typically 500µ1A at VAREF = 5V.

Note that this ladder resistor is connected to VAREF and VSS even in the HOLD mode. Therefore to reduce the power consumption, VAREF should be disconnected from the analog reference voltage supply.

(1) Start of A/D conversion

Prior to conversion, select one of the analog input AIN0 through AIN3 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

Analog input voltage is sampled during the following 2 instruction cycles after setting ADS.

Note: The sample and hold circuit has capacitor (C_A = 12pF typ.) with resistor (R_A = 5KΩtyp.). See I/O circuitry table. This capacitor should be charged within 2 instruction cycles.

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value

is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).

Lower 4 bits of the A/D converted value can be read when LR_0 = 0 and upper 4 bits when LR_0 = 1. Usually an A/D converted value is stored in RAM by an instruction [IN % p, @HL]. Further, if an A/D converted value ; 5 read during the conversion, it becomes an indefinite value.

(3) A/D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of A/D conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

Example: Selecting analog input (AIN3), starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
        LD OUT A,       #3      ; Selects analog input
                                  (AIN3)
        OUT     A,      %OP12
        LD      A,      #1      ; Start of A/D conversion
        OUT     A,      %OP13
SLOOP:  TEST    %IP0C,  3       ;To wait until EOCF goes
                                  to "1"
        B       SLOOP
        LD      HL,     #10H    ; HL←10H
        IN      %IP0D,  @HL     ; RAM [10H]←Lower
                                  4-bits
        INC     L               ; Increment of L registers
        IN      %IP0D,  @HL     ; RAM [11H]←Upper
                                  4-bits
```

2.4 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (runaway) of the external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.

The intialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.4.1 Watchdog Timer (WDT)

The watchdog timer consists of a 3-stage counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

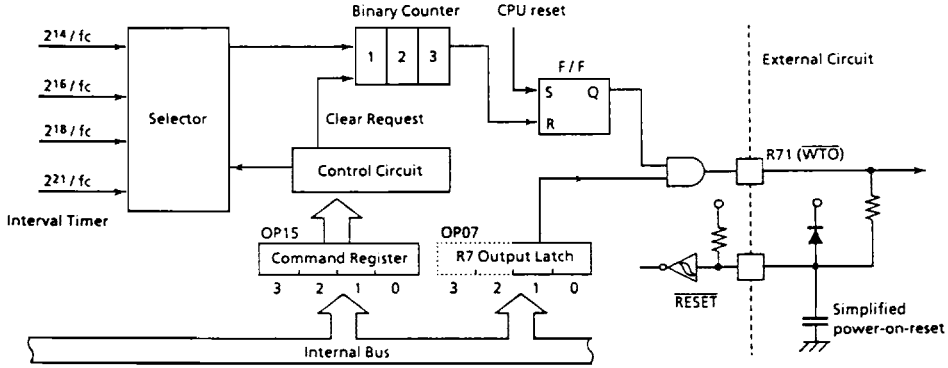


Figure 2-11. Watchdog Timer

2.4.2 Control of watchdog timer

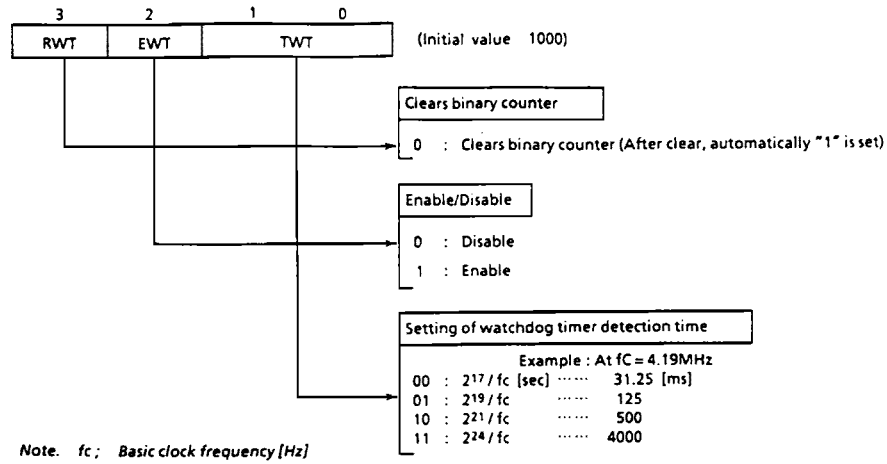
The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000_B" during reset. The following are the procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

1) At first, detection time of the watchdog timer should be set and binary counter should be cleared.

2) The watchdog timer should become enable.

3) Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken palce for some reason and binary counter is not cleared, the F/F is cleared to "0" at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

Watchdog Timer control command register (Port address OP15)



Note. fc ; Basic clock frequency [Hz]

Example: To set the watchdog detection time (2^{21}/fc[sec]). And to enable the watchdog timer.

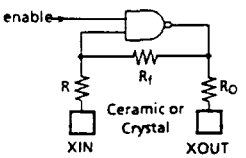
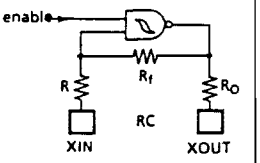
```
    LD      A,      #0010B      ; OP15←0010B
                                (Sets WDT detection time. Clears binary counter)
    OUT     A, %OP15
    LD      A, #1110B           ; OP15←0010B (Enables interrupt)
    OUT     A, %OP15
Within WDT detection time
    LD      A, #1110B           ; OP15←0010B (Clears binary counter)
    OUT     A, %OP15
```

Note: It is not necessary to set RWT to "1". Note that both EWT (enable Watchdog Timer) and RWT should not be set to "1" at the same time.

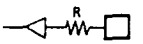
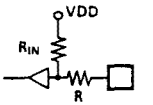
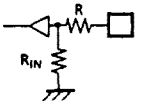
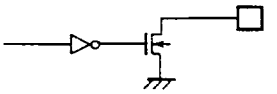
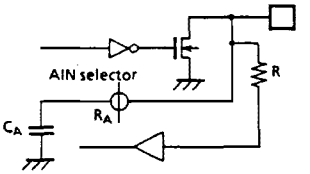
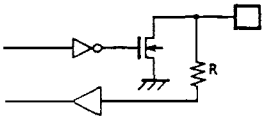
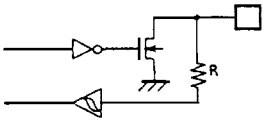
Input/Output Circuitry

The input/output circuitries of the 47C241 control pins except XIN and XOUT pins are similar to that of the 47C200A.

(1) Control pins

Control Pin	I/O	Circuitry and Code		Remarks
		SA, SB, SC	SG	
XIN XOUT	Input Output			Resonator connecting pins R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)

(2) I/O ports

Port	I/O	Input/Output Circuitry and Code			Remarks
		SA, SG	SB	SC	
K0	Input				Push-up/Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 20mA (typ.)
R4	I/O				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.) Analog input R_A = 5KΩ (typ.) C_A = 12pF (typ.)
R7	I/O				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" High current (R9) I_{OL} = 7mA (typ.) Hysteresis input R = 1KΩ (typ.)

Absolute Maximum Ratings (V_{SS} = 0V)

Symbol	Item	Pins	Rating	Unit
V_{DD}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to V_{DD} + 0.3	V
I_{OUT1}	Output Current	Except sink open drain pin	-0.3 to V_{DD} + 0.3	V
I_{OUT2}		Ports P1, P2, R7 - R9	-0.3 to 10	
I_{OUT3}		Analog inputs	-0.3 to V_{DD} + 0.3	
I_{OUT1}	Output Current (Per 1 pin)	Ports P1, P2	30	mA
I_{OUT2}		Ports R9	15	
I_{OUT3}		Port R4, R7, R8	3.2	
ΣI_{OUT1}	Output Current (Total)	Port P1, P2, R9	120	mA
PD	Power Dissipation [Topr = 70°C]		600	mW
T_{sld}	Soldering Temperature (time)		260 (10sec)	°C
T_{stg}	Storage Temperature		-55 to 125	°C
T_{opr}	Operating Temperature		-30 to 70	°C

Recommended Operating Conditions (T_{opr} = -30 to 70°C, V_{SS} = 0V)

Symbol	Parameter	Pins	Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		fc = 6.0MHz	4.5	6.0	V
			fc = 4.2MHz	2.7		
			In the HOLD mode	2.0		
V_{IH1}	Input High Voltage	Except Hysteresis Input	$V_{DD} \geq 4.5V$	V_{DD} x 0.3	V_{DD}	V
V_{IH2}		Hysteresis Input		V_{DD} x 0.75		
V_{IH3}			$V_{DD} < 4.5V$	V_{DD} x 0.9		
V_{IL1}	Input Low Voltage	Except Hysteresis Input	$V_{DD} \geq 4.5V$	0	V_{DD} x 0.7	V
V_{IL2}		Hysteresis Input			V_{DD} x 0.25	
V_{IL3}			$V_{DD} < 4.5V$		V_{DD} x 0.1	
fc	Clock Frequency		V_{DD} = 4.5 ~ 6.0V	0.4	6.0	MHz
			V_{DD} = 2.7 ~ 6.0V		4.2	
			V_{DD} = 2.2 ~ 5.5V(RC)		2.5	

Note: Input Voltage V_{IH3}, V_{IL3}: in the HOLD operating mode.

D.C. Characteristics (T_{opr} = -30 to 70°C, V_{SS} = 0V)

Symbol	Parameter	Pins	Conditions	Min.	Typ.	Max.	Unit
V_{HS}	Hysteresis Voltage	Hysteresis Input		-	0.7	-	V
I_{IN1}	Input Current	Port K0, TEST, RESET, HOLD	V_{DD} = 5.5V, V_{IN} = 5.5V/0V	-	-	±2	μA
I_{IN2}		Ports R (open drain)					
R_{IN1}	Input Resistance	Ports K0 with push-up/pull-down		30	70	150	KΩ
R_{IN2}		RESET		100	220	450	
I_{LO}	Output Leakage Current	Ports R, P (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	-	-	2	μA
V_{OL2}	Output Low Voltage	Except XOUT, ports P	V_{DD} = 4.5V, I_{OL} = 1.6mA	-	-	0.4	V
I_{OL1}	Low Output Current	Ports P1, P2	V_{DD} = 4.5V, I_{OL} = 1.0V	-	20	-	mA
I_{OL2}		Port R9			7		
I_{DD}	Supply Current (in the Normal operating mode)		V_{DD} = 5.5V, fc = 4MHz	-	3	6	mA
I_{DDH}	Supply Current (in the HOLD operating mode)		V_{DD} = 5.5V	-	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1}: The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current: I_{DD}, I_{DDH} ; V_{IN}5.3V/0.2V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the vaild range.

A/D Conversion Characteristics (T_{opr} = -30 to 70°C)

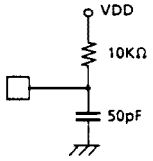
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{AREF}	Analog Reference Voltage	V_{AREF} - V_{SS}	V_{DD} - 1.5	-	V_{DD}	V
ΔV_{AREF}	Analog Reference Voltage Range		2.7	-	-	V
V_{AIN}	Analog Input Voltage		V_{SS}	-	V_{AREF}	V
I_{REF}	Analog Supply Current		-	0.5	1.0	mA
	Nonlinearity Error	V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = 5.000V V_{ASS} = 0.000V	-	-	±1	LB
	Zero Point Error		-	-	±1	
	Full Scale Error		-	-	±1	
	Total Error		-	-	±1	

A.C. Characteristics (T_{opr} = -30 to 70°C, V_{SS} = 0V)

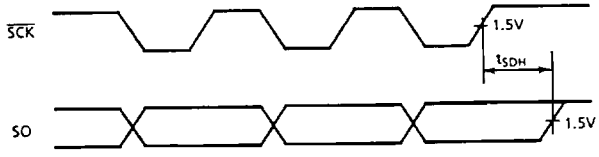
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Instruction Cycle Time	V_{DD} = 4.5 ~ 6.0V	1.3	-	20	μs
		V_{DD} = 2.7 ~ 6.0V	1.9			
t_{WCH}	High level Clock pulse Width	For external clock mode	80	-	-	ns
t_{WCL}	Low level Clock pulse Width					
t_{AIN}	A/D Sampling Time		-	4	-	μs
t_{SDH}	Shift Data Hold Time		$0.5t_{cy}$ - 300	-	-	ns

Note. Shift data Hold Time:

External circuit for pins $\overline{SCK}$ and SO



Serial port (completed of transmission)



Recommended Oscillating Conditions

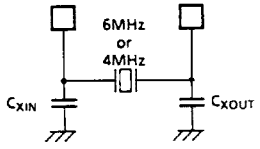
(T_{opr} = -30 to 70°C, V_{DD} = 4.5 to 6.0V, V_{SS} = 0V)

(1) 6MHz

Ceramic Resonator

CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF



(2) 4MHz

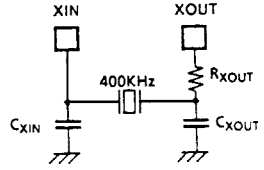
Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF



(3) 400KHz

Ceramic Resonator

CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ

KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

(4) RC Oscillation

2MHz (Typ.) C_{XIN} = 33pF, Rx = 10KΩ

400KHz (Typ.) C_{XIN} =100pF, Rx = 26KΩ