ExpressLane PEX 8524VAA/BB/BC and PEX 8524BB/BC

6-Port/24-Lane Versatile PCI Express Switch

Data Book

Version 1.5

February 2007

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Revision History

Version	Date	Description of Changes
1.0	January, 2006	Production Release, Silicon Revision BB. Includes JTAG, power, and ordering information for Silicon Revision AA. Includes two package types: • 35 x 35 mm 680-ball EHBGA (AA/BB) • 31 x 31 mm 644-ball PBGA (BB) All information pertains to AA and BB devices, unless indicated otherwise as PEX 8524AA or PEX 8524BB.
1.1	March, 2006	• Changed EHBGA to Plastic BGA / PBGA • Section 12.1.2.2, "Intelligent Adapter Mode NT Port Reset" – Changed "1 ms" to "1 µs" in second paragraph • Register 11-8, offset 1Ch[31] – Corrected cross-reference to indicate the *Parity Error Response Enable* bit • Register 11-49, offset 1CCh[13] – Corrected value of 1 to indicate ≥ 8 • Corrected Table 17-1 title to indicate field value of 10b • Miscellaneous changes for readability
1.2	June, 2006	• Changed Data Book title to include reference to both devices, PEX 8524V and PEX 8524, and clarified differences between the two, and added missing data related to one or the other, as appropriate, particularly in Chapter 17, "Testability and Debug," and Chapter 18, "Electrical Specifications" • Removed references to PEX 8524AA (Silicon Revision AA exists only for PEX 8524V) • Removed references to Silicon Revision BA for PEX 8524V and PEX 8524 • Device ID – Corrected 35 x 35 (680-ball) package Device ID to be 8532h • Chapter 2 – Replaced illustrations • Figure 3-1 and 3-2 – Clarified view as "See-Through Top View" • Table 3-11 – Corrected locations for 644-ball package (PEX_PETp29 is at B28, PEX_PERp27 is at D24, and PEX_PERn27 is at E24) • Figure 4-7 – Replaced illustration • Tables 4-1 and 5-3 – Updated to indicate that Ports 8 and 9 (value of 1h) can be combined to create a x16 port • Section 5.1.3.1 – Changed "upstream and downstream stations" to "upstream and downstream ports" • Section 5.2.5, "Reset and Clock Initialization Timing" – Created new heading, to include table and figure • Table 8-1 – Moved to "RAM and Queue Size" section • Figure 9-3 – Corrected HP_PERST# signal to be high • Chapter 11, register offset 1D0h – Changed "***Reserved***" reference to "***Factory Test Only***" • Section 12.4 – Changed "upstream port" reference to "downstream ports" • Chapters 15 and 16 – Changed "corresponding port" references to appropriate NT Port interface • Section 17.1.7 – Removed reference to reserved registers for Station 1 • Tables 17-3, 17-4, and 17-5 – Merged JTAG IDCODE content into a single table, Table 17-3 • Tables 17-3 – Added PEX 8524V content; added missing PEX 8524 JTAG IDCODE binary part number and changed hex part number • Figure 19-2 – Rearranged drawing so it can be viewed without turning page • Appendix B – Updated Product Ordering tables • Miscellaneous changes for readability
1.3	August, 2006	Miscellaneous changes, corrections, and enhancements throughout the data book.

Version	Date	Description of Changes
1.4	January, 2007	Rewrote Chapter 18, “Electrical Specifications.” Updated RDK ordering information in Appendix B, “General Information.”
1.5	February, 2007	Production Release, Silicon Revision BC. Miscellaneous changes, corrections, and enhancements throughout the data book. Moved Table A-2 content into Table A-1.

Preface

The information contained in this data book is subject to change without notice. This PLX data book is updated periodically as new information is made available.

This data book documents information for the PEX 8524V, Silicon Revisions AA, BB, and BC, and PEX 8524, Silicon Revisions BB and BC. The information provided pertains to all silicon revisions, unless specified otherwise.

Note: Throughout this data book, unless specified otherwise, "PEX 8524" is used to indicate PEX 8524V and PEX 8524.

Audience

This data book provides the functional details of PLX Technology's ExpressLane PEX 8524VAA/BB/BC and PEX 8524BB/BC 6-Port/24-Lane Versatile PCI Express Switches, for hardware designers and software/firmware engineers.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc. (PLX)

  870 W Maude Avenue, Sunnyvale, CA 94085

  Tel: 800 759-3735 (domestic only) or 408 774-9060, Fax: 408 774-2169, www.plxtech.com

  - *PEX 85XX EEPROM – PEX 8532/8524/8516 Design Note*
  - *PEX 8524 Errata*

  The PLX PEX 8524 Toolbox includes other PEX 8524 documentation as well.

- PCI Special Interest Group (PCI-SIG)

  3855 SW 153rd Drive, Beaverton, OR 97006 USA

  Tel: 503 619-0569, Fax: 503 644-6708, www.pcisig.com

  - *PCI Local Bus Specification, Revision 2.3*
  - *PCI Bus Power Management Interface Specification, Revision 1.1*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1*
  - *PCI Hot Plug Specification, Revision 1.1*
  - *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
  - *PCI Express Base Specification, Revision 1.0a*
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
  - *PCI Express Architecture PCI Express Jitter and BER White Paper, Revision 1.0*

- The Institute of Electrical and Electronics Engineers, Inc.

  445 Hoes Lane, Piscataway, NJ 08854-4141 USA

  Tel: 800 701-4333 (domestic only) or 732 981-0060, Fax: 732 981-9667, www.ieee.org

  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*

Note: *In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r2.3	*PCI Local Bus Specification, Revision 2.3*
PCI Power Mgmt. r1.1	*PCI Bus Power Management Interface Specification, Revision 1.1*
PCI-to-PCI Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
Hot Plug r1.1	*PCI Hot Plug Specification, Revision 1.1*
PCI Standard Hot Plug Controller and Subsystem r1.0	*PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
PCI Express Base r1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express CEM r1.0a	*PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*
IEEE Standard 1149.6-2003	*IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*

Terms and Abbreviations

The following table lists common terms and abbreviations used in this data book. Terms and abbreviations defined in the *PCI Express Base r1.0a* are not included in this table.

Terms and Abbreviations	Definitions
AMCAM	Address mapping CAM that determines a memory request route. Contains mirror copies of the PCI-to-PCI Bridges Memory Base and Limit registers in the switch.
BusNoCAM	Bus Number mapping CAM that determines the completion route. Contains mirror copies of the PCI-to-PCI Bridges Secondary Bus-Number and Subordinate Bus-Number registers in the switch.
CAM	Content Addressable Memory.
CSRs	Configuration Space registers.
Downstream Station	A station that contains only downstream ports.
Egress queue	• Egress – Outgoing traffic from chip • Egress queue – Egress queuing/scheduling mechanism
GPIO	General-Purpose Input/Output.
Ingress queue	• Ingress – Incoming traffic to chip • Ingress queue – Ingress queuing/scheduling mechanism
IOAMCAM	I/O Address mapping CAM that determines an I/O request route. Contains mirror copies of the PCI-to-PCI Bridges I/O Base and Limit registers in the switch.
Lane	Lanes are comprised of a bi-directional pair of differential PCI Express I/O signals.
Link Interface	Primary side of the NT port, connects to external device pins. The secondary side of the NT port is referred to as the *NT Port Virtual Interface*, and connects to the internal virtual PCI Express interface.
Local	Reference to PCI Express attributes (*such as*, credits) that belong to the PCI Express station.
Non-Transparent	A bridging technique used in the PCI Express Switch to isolate memory spaces by presenting the processor as an endpoint rather than another memory system.

Terms and Abbreviations	Definitions
PCI Express Station	A functional unit that provides the PCI Express conforming system interface. Includes the Serializer and De-serializer (SerDes) hardware interface modules and PCI Express Interface, which provides the Physical Layer, Data Link Layer, and Transaction Layer logic.
PHY	Physical Layer.
Port	Ports are a collection of lanes configured at startup which contain the functional logic and memory resources to communicate with like resources in other PCI Express devices.
PRBS	Pseudo-Random Bit Sequence.
QoS	Quality of Service.
RAS	Reliability, Availability, and Serviceability.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RR	Round-Robin scheduling.
SerDes	Serializer/De-serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to lane pads.
TC	Traffic Class.
TDM	Time Division Multiplexing.
TLC	Transaction Layer Control. The module performing PCI Express Transaction Layer functions.
TLP	Transaction Layer Packet. PCI-Express packet formation and organization.
Transparent	Refers to standard PCI Express upstream-to-downstream routing protocol.
Upstream station	Upstream station. Contains the component's upstream port. An upstream station can contain downstream ports.
VC	Virtual Channel.
Virtual Interface	Secondary side of the NT port, connects to the internal virtual PCI Express interface.
WRR	Weighted Round-Robin scheduling.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXp[15:0]	When the signal name appears in all CAPS, with the primary port description listed first, field [15:0] indicates the number of signal balls/pads assigned to that port. The lowercase "p = positive" or "n = negative" suffix indicates the differential pair of signal, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PEX_PERST#).
`Program/code samples`	`Monospace font` (*`program or code samples`*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
`command_done`	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response. K = 1,024 (2^{10}) is used for memory size references. KB = 1,024 bytes. M = meg. = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to memory sizes (binary notation)
1Fh	h = suffix which identifies hex values. Each prefix term is equivalent to a 4-bit binary value (nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 or 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes)
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord	DWord (32 bits) is the primary register size in these devices.
Reserved	Do not modify ***reserved*** bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.

Contents

Registers

Chapter 1 Introduction

1.1 Features

Note: Throughout this data book, unless specified otherwise, "PEX 8524" is used to indicate PEX 8524V and PEX 8524.

PLX Technology's ExpressLane™ PEX 8524 PCI Express Switch device supports the following features:

- High Performance
  - PEX 8524 = 24 PCI Express lanes provide 120 Gbps aggregate bandwidth [2.5 Gbps/lane x 24 lanes x 2 (full duplex)]
  - Non-blocking internal crossbar architecture supports TLP bandwidth capacity of each x8 (Station 0) and x16 (Station 1) link
  - Maximum Packet Payload Size of 256 bytes
  - Performance tuning
- Flexible Configuration
  - PEX 8524 = 24 PCI Express lanes, up to 6 ports
  - Up to 40 possible port configurations
  - Choice of width (number of lanes) per unique port/link – x1, x2, x4, or x8 (Station 0) or x1, x2, x4, x8, or x16 (Station 1)
  - Designate any port as the *upstream port*
  - Configure with Strapping balls and/or serial EEPROM
  - Lane reversal support
- PCI Express Power Management
  - Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3
  - Device Power Management states – D0 and D3hot
- Quality of Service (QoS)
  - All ports support two, full-featured Virtual Channels (VC0 and VC1)
  - All ports support eight Traffic Class (TC) mapping, independent of other ports
  - Port arbitration – Hardware-fixed arbitration scheme
  - Virtual Channel arbitration – Weighted Round-Robin (WRR) or Hardware-fixed arbitration scheme
- Non-Transparent Bridging
  - Program any one port as *Non-Transparent*
  - Enables Dual-Host, Dual-Fabric, Host-Failover applications
- Transaction Forwarding with Address Translation
- Reliability, Availability, and Serviceability (RAS) features
  - Each downstream port includes a PCI Express Hot Plug Controller
  - Upstream port supports Hot Plug as a client
  - Transaction Layer Packet Digest support
    - Poison bit
    - End-to-end Cyclic Redundancy Check (ECRC)

  - Advanced Error Reporting capability
  - Per-port diagnostics
    - TLP errors
    - CRC errors
  - All on-chip RAM are ECC-protected
  - Serial EEPROM content is CRC-protected
- Testability – JTAG support for DC
- Package types
  - PEX 8524VAA/BB/BC – 35-mm square, 680-ball PBGA (Plastic BGA) package
  - PEX 8524BB/BC – 31-mm square, 644-ball PBGA (Plastic BGA) package
- Compliant to the following standards
  - *PCI Local Bus Specification, Revision 2.3 (PCI r2.3*)
  - *PCI Bus Power Management Interface Specification, Revision 1.1 (PCI Power Mgmt. r1.1*)
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1 (PCI-to-PCI Bridge r1.1)*
  - *PCI Hot Plug Specification, Revision 1.1 (PCI Hot Plug r1.1)*
  - *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0 (PCI Standard Hot Plug Controller and Subsystem r1.0)*
  - *PCI Express Base Specification, Revision 1.0a (PCI Express Base r1.0a*)
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a (PCI Express CEM r1.0a*)
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990 (IEEE Standard 1149.1-1990*)
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*

1.2 Overview

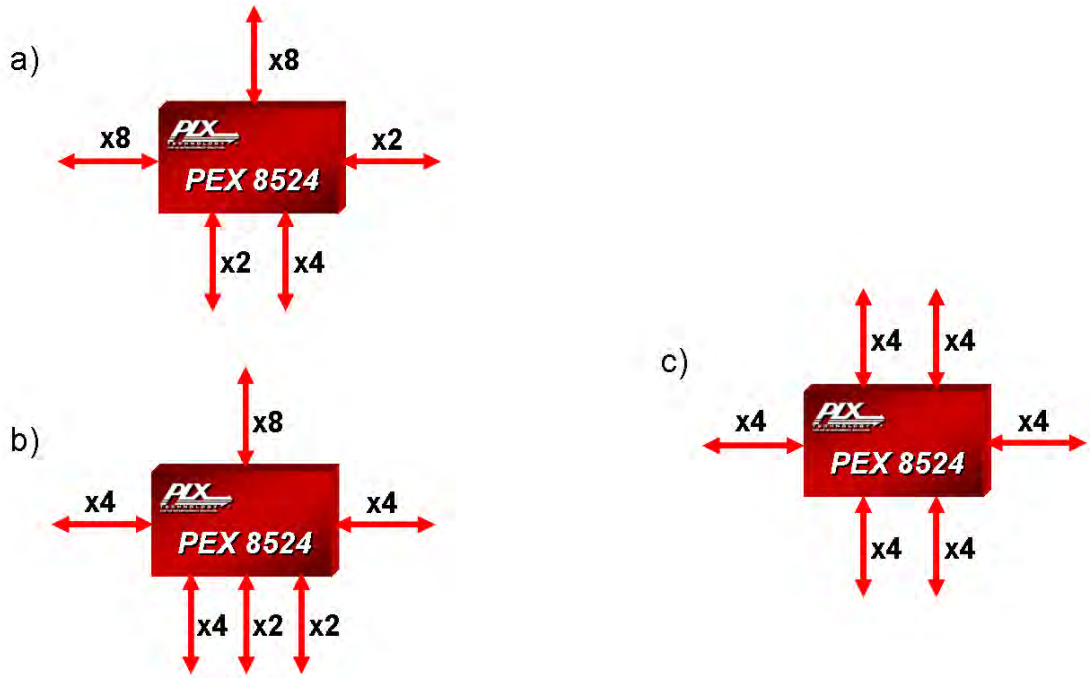
This data book describes the PEX 8524, a fully non-blocking, low-latency, low-cost, and low-power 6-port, 24-lane PCI Express switch. Conforming to the *PCI Express Base r1.0a*, the PEX 8524 enables users to add scalable, high-bandwidth I/O to a wide variety of products, including servers, communication products, storage systems, routers, blade servers, and other embedded products. The PEX 8524's flexible hardware configuration and software programmability allow the switch to be tailored to suit a wide variety of applications.

1.3 Lane Configuration

The PEX 8524 switch is suitable for host-centric and peer-to-peer communication. The PEX 8524 contains 24 PCI Express lanes and up to six ports.

Figure 1-1 illustrates the way in which the PEX 8524 flexible-lane configuration feature supports a variety of switch applications. Figure 1-1 (a) illustrates a host-centric port configuration, where a wide PCI Express link is fanned out into smaller ports with different bandwidth requirements. Figure 1-1 (b) illustrates backplane port configuration, where the wide PCI Express port provides a high-bandwidth path to a host or a switch fabric from a large number of line cards with smaller ports. Figure 1-1 (c) illustrates a 6-slot symmetric backplane, with x4 links traveling to each slot for peer-to-peer applications.

Figure 1-1. PEX 8524 Flexible-Lane Configuration



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Chapter 2 PEX 8524 Applications

2.1 Multi-Purpose and Feature-Rich PCI Express Switch

The ExpressLane PEX 8524 device offers PCI Express switching capability, conforming to the *PCI Express Base r1.0a*, enabling users to add scalable, high-bandwidth, non-blocking interconnection to a wide variety of applications including servers, storage systems, communications platforms, blade servers, and embedded-control products. The PEX 8524 switch can be used as fan-out, aggregation, dual graphics, or peer-to-peer switching, and is equally well-suited for intelligent I/O module applications.

2.1.1 End-to-End Packet Integrity

The PEX 8524 provides End-to-end CRC (ECRC) protection and Poison-Bit support to enable designs that require guaranteed error-free packets. These features are optional in the *PCI Express Base r1.0a*; however, PLX provides them across its entire ExpressLane switch product line.

2.1.2 PCI Express Switch Non-Transparent Bridging (NTB)

The PEX 8524 supports full Non-Transparent bridging (NTB) functionality to allow implementation of multi-host systems and intelligent I/O modules in applications *such as* communications, storage, and graphics fan-out. To ensure prompt product migration, non-transparency features are implemented in the same manner as Conventional PCI applications.

Non-transparent bridges allow systems to isolate memory domains by presenting the processor subsystem as an endpoint, rather than another memory system:

- **Base Address** registers (BARs) are used to translate addresses
- **Doorbell** registers are used to transmit interrupts between the address domains
- **Scratchpad** registers are accessible from both address domains, to allow inter-processor communication

2.1.3 Two Virtual Channels (VCs)

The PEX 8524 switch supports two full-featured Virtual Channels (VCs) and eight Traffic Classes (TCs). Traffic-class mapping to port-specific Virtual Channels allows different mappings on different ports. In addition, this device offers user-selectable Virtual Channel arbitration algorithms to enable fine-tuning of Quality of Service (QoS), required for specific applications.

The PEX 8524 switch supports Hardware-fixed and Weighted Round-Robin arbitration schemes for two VCs. This allows QoS fine-tuning, optimum buffer use, and efficient use of system bandwidth.

2.1.4 Low Power with Granular SerDes Control

The PEX 8524 provides **low-power** capability that is fully compliant with the *PCI Express Base r1.0a* Power Management specifications. Unused SerDes can be disabled to reduce power consumption.

The PEX 8524 supports SerDes output software control to allow power and signal strength optimization in a system. The PLX SerDes implementation supports four power levels – *Off*, *Low*, *Typical*, and *High*. The SerDes block also supports Loop-Back modes and Advanced Error Reporting, which enables efficient system debug and management.

2.1.5 Flexible Port-Width Configuration

The lane width per port can be individually configured through auto-negotiation, hardware strapping, upstream software configuration, or an optional serial EEPROM.

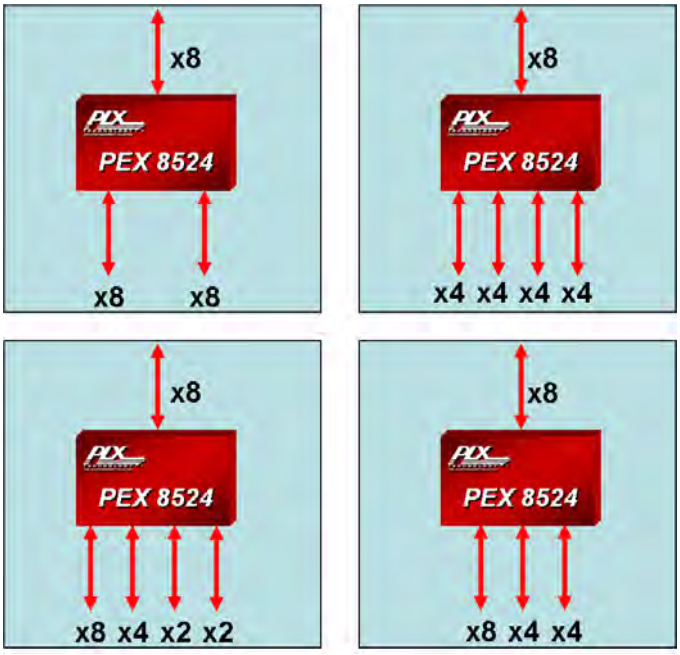
The PEX 8524 supports a large number of port configurations. *For example*, if the PEX 8524 is used in a fan-out application (as illustrated in Figure 2-2), the upstream port can be configured as x8, and the downstream ports can be configured as follows:

- Four x4 ports
- Two x8 ports
- Or any other combination, provided that available lanes or ports are not exceeded

For peer-to-peer applications, all six ports can be configured as x4 or x2, or a combination of the two. In port aggregation applications, four x2 or two x4 ports can be configured for aggregation into one x8 port in Station 0, or x16 port in Station 1. Figure 2-1 illustrates the most common port configurations.

Each port supports lane reversal for system design flexibility.

Figure 2-1. Common Port Width Configurations



2.1.6 Hot Plug in High-Availability Applications

Hot Plug capability allows replacement of hardware modules and maintenance performance without system power down.

The PEX 8524 Hot Plug capability and Advanced Error Reporting features make the PEX 8524 suitable for High-Availability (HA) applications. Each downstream port includes a Standard Hot Plug controller. If the PEX 8524 is used in an application where one or more of its downstream ports connects to PCI Express slots, the individual port Hot Plug Controller is used to manage the Hot Plug event of its associated slot. Additionally, the upstream port is a fully compliant Hot Plug client, and the PEX 8524 can be used on hot-pluggable adapter boards, backplanes, and fabric modules.

2.1.7 Fully Compliant Power Management

For applications that require power management, the PEX 8524 supports Link (L0, L0s, L1, L2/L3 Ready, and L3) and Device (D0 and D3hot) Power Management states, in compliance with the *PCI Express Base r1.0a* Power Management specifications.

2.2 Applications

Suitable for host-centric and peer-to-peer traffic patterns, the PEX 8524 can be configured for a wide variety of form factors and applications, as described in the sections that follow.

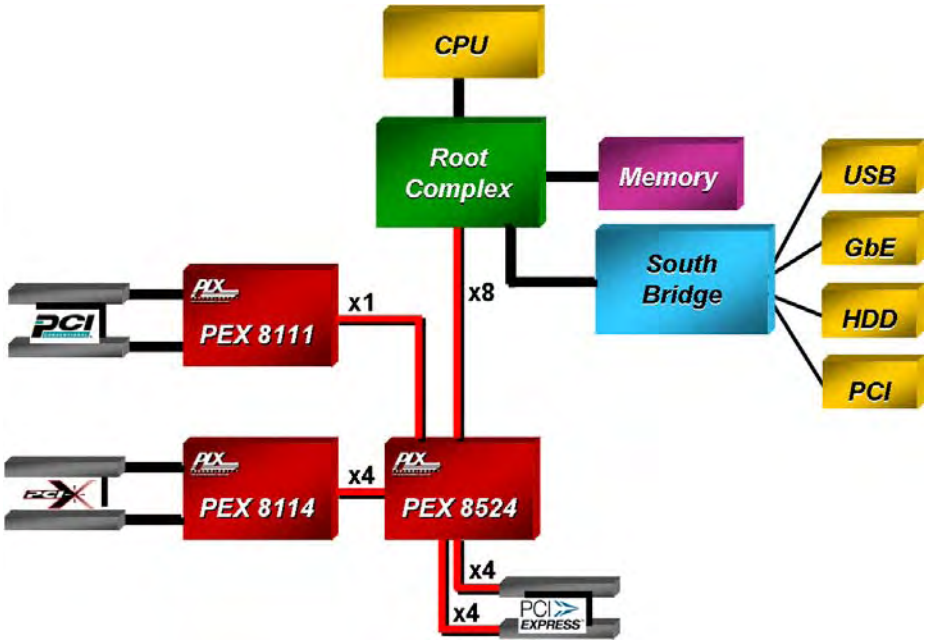
2.2.1 Host-Centric Fan-Out

The PEX 8524, with versatile symmetric or asymmetric lane configuration capability, allows application-specific tuning to a variety of host-centric applications.

Figure 2-2 illustrates a typical server-based design, where the Root Complex provides a PCI Express link needing to be broken into a larger number of smaller ports for a variety of I/O functions with different bandwidth requirements.

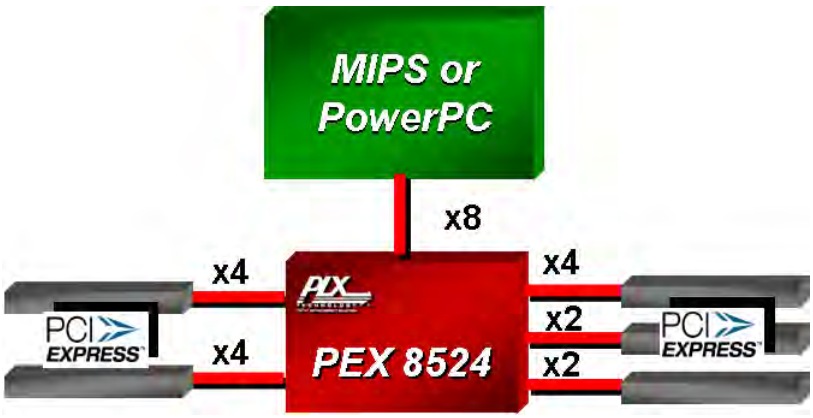
In this example, the PEX 8524 contains one x8 upstream port, and as many as five downstream ports. The downstream ports can be of differing widths, if required. Figure 2-2 also illustrates various ways that the ports can be bridged to provide PCI or PCI-X, using ExpressLane PCI Express bridges (*such as*, the PLX PEX 8114 or PEX 8111).

Figure 2-2. Fan-In/Fan-Out Usage



Almost all (non-x86-based) RISC microprocessor manufacturers offer PCI Express interfaces. For enhanced connectivity, the PEX 8524 can be directly connected to a processor to fan-out its PCI Express port to a larger number of ports, as illustrated in Figure 2-3.

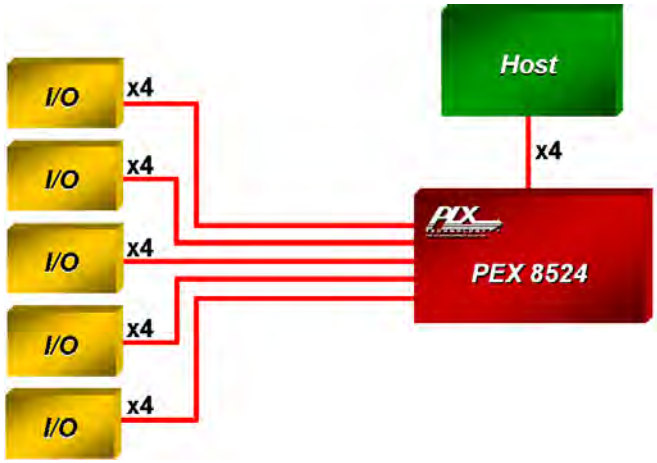
Figure 2-3. PowerPC/MIPS CPUs Fan-Out



2.2.2 Peer-to-Peer Communication

Figure 2-4 represents a PEX 8524 backplane that provides peer-to-peer data exchange for a large number of line cards, wherein the CPU/Host plays the management role.

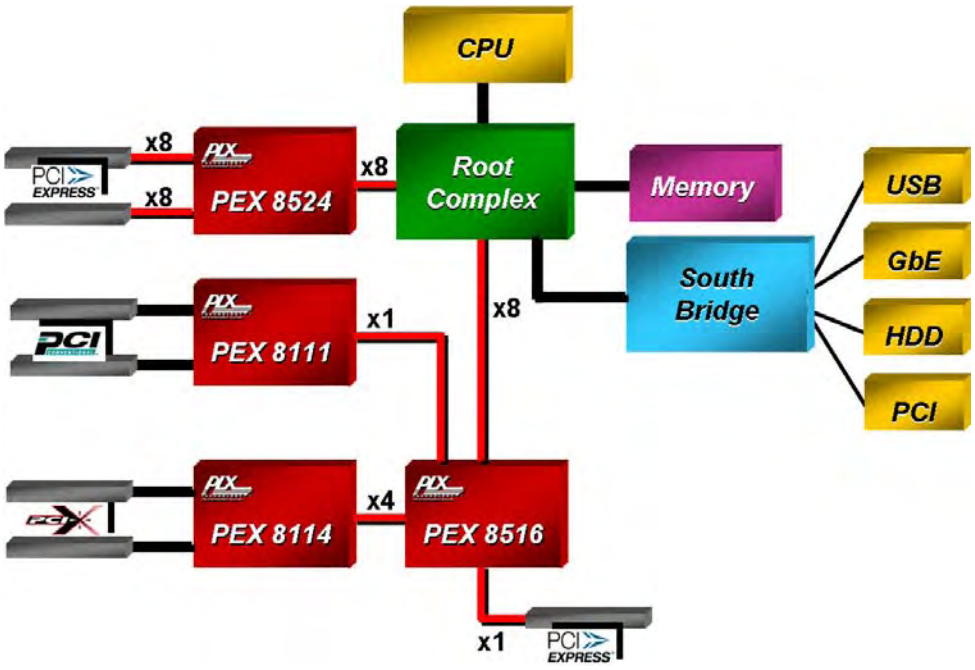
Figure 2-4. Peer-to-Peer Communication



2.2.3 Graphics Fan-Out Switch

The number and variety of PCI Express native-mode devices is rapidly growing. These devices, *such as* PCI Express graphics boards, are expected to rapidly become mainstream. As that occurs, it becomes necessary to use a x8 port on the Root Complex device and fan it out to two x4 (or x8) ports for dual-graphic applications. Root Complex (*North Bridge*) devices are available with multiple PCI Express ports, which can be further expanded to connect to a larger number of I/Os or to support dual-graphics, using the PEX 8524, as illustrated in Figure 2-5.

Figure 2-5. Graphics Fan-Out

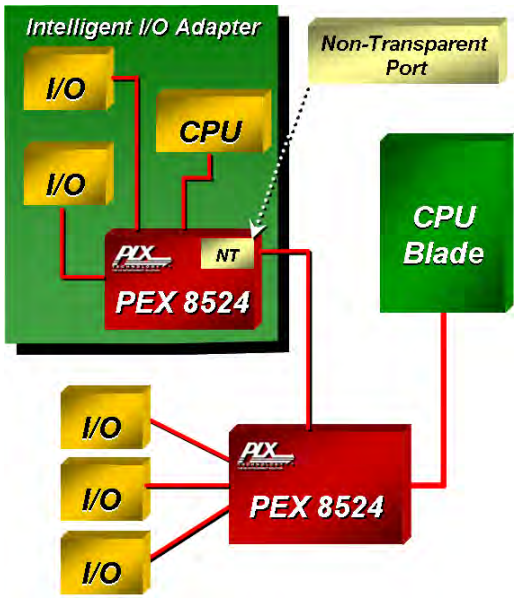


2.2.4 Dual-Host Model

The PEX 8524 supports applications requiring Dual-Host, Host-Failover, and Load-Sharing applications through the Non-Transparency feature.

Figure 2-6 illustrates a dual-host system using an intelligent adapter board. The primary CPU (on the right) is the active host – it configures and enumerates the system, and handles interrupts and error conditions. If the primary host ceases proper operation, the secondary host takes over the system. The PEX 8524 can **dynamically re-assign** the **Upstream port** (from primary to secondary) and the **Non-Transparent** port (from the secondary to the primary), and allow the system to continue operation. Dynamic swapping of the upstream and NT Ports is supported on Ports 0 and 8.

Figure 2-6. Dual-Host Usage

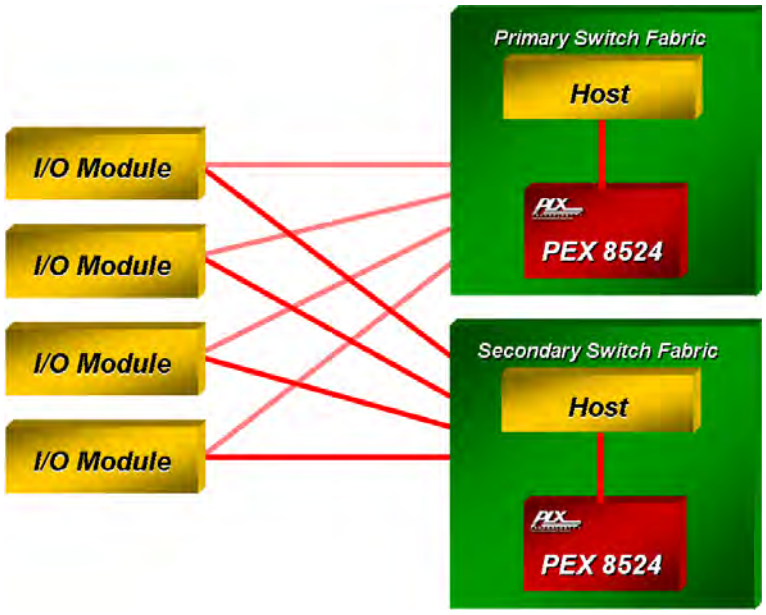


2.2.5 Dual-Fabric Model

High-performance communications, storage, and blade server systems often require more reliability than a dual-host system provides. For these High-Availability systems, all single points of failure must be eliminated. The PEX 8524 can offer this additional level of redundancy by linking two switch fabric boards in a *dual-star* topology. As illustrated in Figure 2-7, the host and fabric are on separate boards, and can be simultaneously active. The PEX 8524 unique non-transparency feature is used to allow one fabric/host board to be the primary and the other the secondary.

This approach is used to provide more than two active processing nodes. It is straightforward to create a generalized multi-processor system with smaller PEX 8524 switches on each board in Non-Transparent mode (NT mode), and several PEX 8524 fabric boards to provide the fabric backbone.

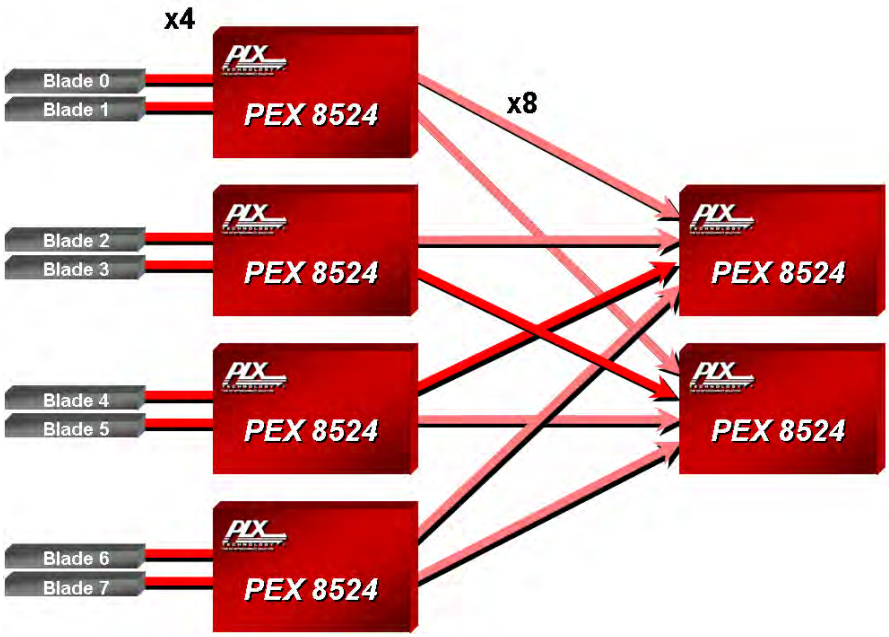
Figure 2-7. Dual-Host and Fabric Usage



2.2.6 Switch-Fabric Module

The PEX 8524 can also be used in blade server Switch Fabric applications. Figure 2-8 illustrates use of the PEX 8524 in a *Benes Switch* configuration. The PEX 8524 non-transparency and peer-to-peer functions enable use of fewer total switching elements and fewer *hops* from source to destination.

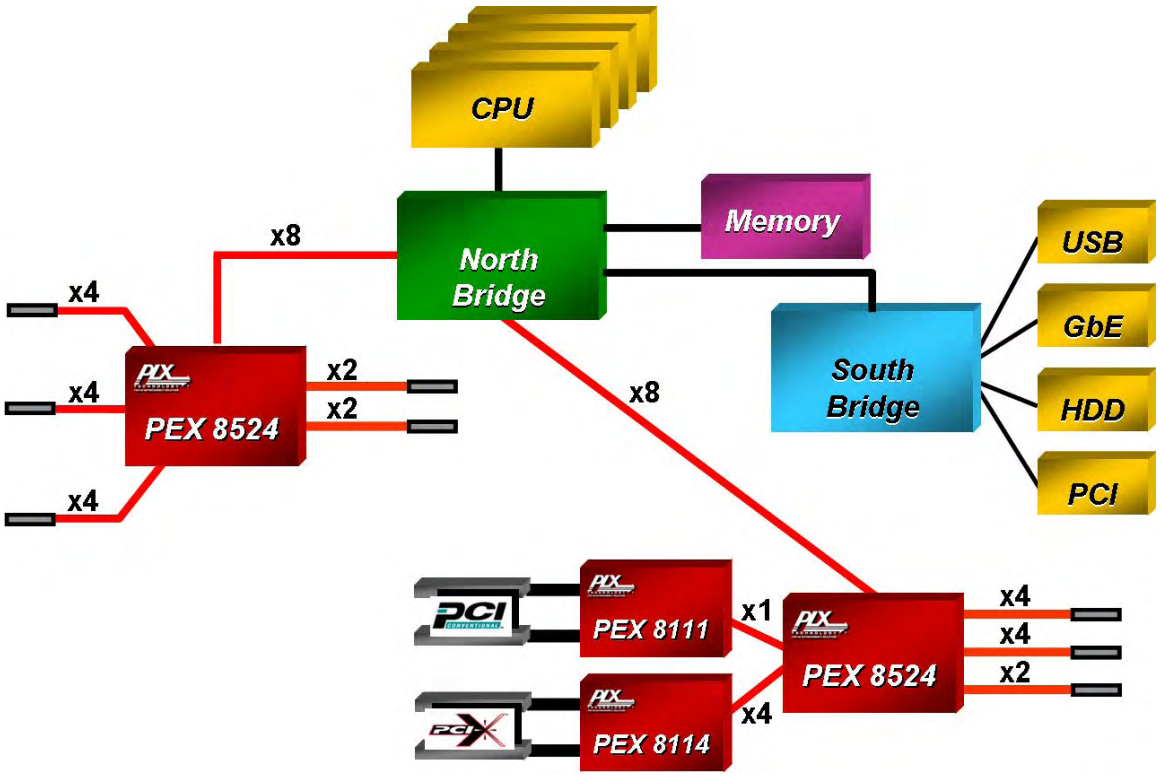
Figure 2-8. Benes Switch Fabric



2.2.7 PCI Express Port Expansion

The PEX 8524 enables, *for example*, two x8 PCI Express ports to be expanded into ten ports. Certain PCI Express ports can be bridged to PCI or PCI-X, using PLX bridging products. Figure 2-9 illustrates one of the many configurations that the PEX 8524 supports.

Figure 2-9. PCI Express Port Expansion



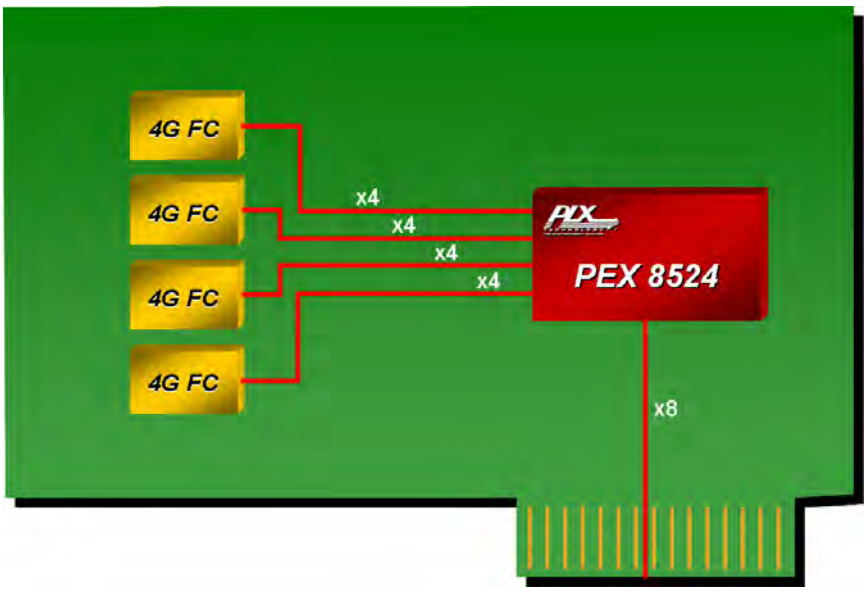
2.2.8 Adapter Board Aggregation

The number and variety of PCI Express native-mode devices is rapidly growing. As these devices become mainstream, it becomes necessary to create multi-function and multi-port adapter boards with PCI Express capability.

The PEX 8524 can be used to create an adapter or mezzanine board that aggregates PCI Express devices into a single port, that can be plugged into a backplane or motherboard. Figure 2-10 illustrates use of the PEX 8524 in this application.

The adapter board in Figure 2-10 can be Transparent, in which case the PCI Express devices are standard I/O products *such as* Ethernet, Fibre Channel, and so forth. Or, the PEX 8524 can provide a Non-Transparent port to the system (by way of the board edge). In this case, one of the PCI Express devices can be a CPU or other "intelligent" device with on-chip processing capability – thereby needing address domain isolation from the remainder of the system. This approach is commonly used in RAID controllers.

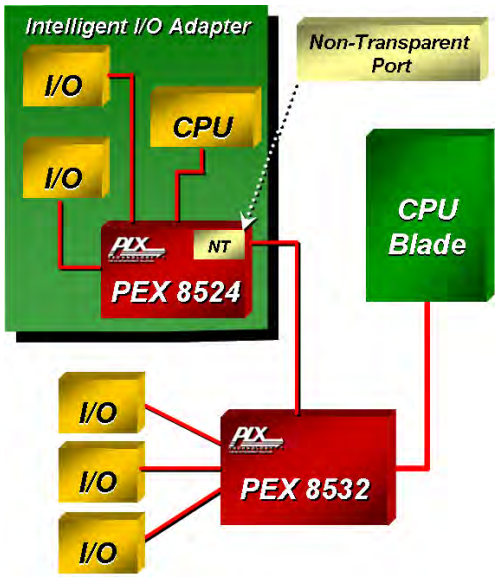
Figure 2-10. Adapter Board Aggregation



2.2.9 Intelligent Adapter Board Usage

The PEX 8524 supports Non-Transparency Bridging (NTB). Figure 2-11 illustrates a host system using an intelligent adapter board, where the adapter board CPU is isolated from the host CPU. The PEX 8524 NT Port allows the two CPUs to be isolated, but communicate with one another through registers designed specifically for that purpose. The host CPU can dynamically re-assign the upstream port and NT Port, allowing system re-configuration.

Figure 2-11. Intelligent Adapter Board Usage



2.3 Software Usage Model

From a system model viewpoint, each PCI Express port is a virtual PCI-to-PCI bridge device, with its own set of PCI Express Configuration registers. The BIOS or Host can configure the other ports by way of the upstream port, using Conventional PCI enumeration. The virtual PCI-to-PCI bridges within the PEX 8524 are compliant to the PCI and PCI Express system models. The Configuration Space registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0 Configuration requests through the virtual primary bus interface (matching Bus, Device, and Function Numbers).

2.3.1 System Configuration

The virtual PCI-to-PCI bridges within the PEX 8524 are compliant with the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0/1 Configuration requests, by way of the virtual primary bus interface (matching Bus, Device, and Function Numbers).

2.3.2 Interrupt Sources and Events

The PEX 8524 supports the INT*x* Interrupt message type (compatible with *PCI r2.3* Interrupt signals) or Message Signaled Interrupts (MSI), when enabled. The PEX 8524 generates messages for PCI Express Baseline and Advanced Error Reporting error reporting mechanisms. The PEX 8524 generates interrupts for Hot Plug events, and device-specific internal errors, and forwards interrupts received from downstream ports. Both forwarded and internally generated interrupts are remapped and collapsed at the upstream port.

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Chapter 3 Signal Ball Description

3.1 Introduction

This chapter provides descriptions of the 680 PEX 8524V and 644 PEX 8524 signal balls. The signals are divided into the following groups.

Table 3-1. PEX 8524 Signal Balls

PEX 8524VAA/BB/BC	PEX 8524BB/BC
• PCI Express Signals – 680-Ball PBGA	• PCI Express Signals – 644-Ball PBGA
• Hot Plug Signals – 680-Ball PBGA	• Hot Plug Signals – 644-Ball PBGA
• Serial EEPROM Signals – 680-Ball PBGA	• Serial EEPROM Signals – 644-Ball PBGA
• Strapping Signals – 680-Ball PBGA	• Strapping Signals – 644-Ball PBGA
• JTAG Interface Signals – 680-Ball PBGA	• JTAG Interface Signals – 644-Ball PBGA
• No Connect Signals – 680-Ball PBGA	• No Connect Signals – 644-Ball PBGA
• Power and Ground Signals – 680-Ball PBGA	• Power and Ground Signals – 644-Ball PBGA

The signal name, type, location, and a brief description are provided for each signal ball, by package type.

3.2 Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 3-2. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
APWR	1.15V ±3% (PEX 8524VAA) Power (VDD10A) balls for SerDes Analog circuits
	1.0V ±5% (PEX 8524VBB/BC, PEX 8524BB/BC) Power (VDD10A) balls for SerDes Analog circuits
CMLCLKn[a]	Differential low-voltage, high-speed, CML negative Clock inputs
CMLCLKp[a]	Differential low-voltage, high-speed, CML positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	1.15V ±3% (PEX 8524VAA) Power (VDD10) balls for low-voltage Core circuits
	1.0V ±5% (PEX 8524VBB/BC, PEX 8524BB/BC) Power (VDD10) balls for low-voltage Core circuits
GND	Common Ground (VSS) for all circuits; also associated with VSS_THERMAL (thermal ground)
I	Input (signals with weak internal pull-up resistors)
I/O	Bi-Directional programmable signal (input or output)
I/OPWR	3.3V Power (VDD33) balls for Input and Output interfaces
O	Output
PLL_GND	PLL Ground connection
PLLPWR	3.3V Power (VDD33A) balls for PLL circuits
PU	Pull-up resistor (recommended value between 3K to 10K Ohms)
SerDes	Differential low-voltage, high-speed, I/O signal pairs (negative and positive)
SPWR	1.15V ±3% (PEX 8524VAA) Power (VDD10S) balls for SerDes Digital circuits
	1.0V ±5% (PEX 8524VBB/BC, PEX 8524BB/BC) Power (VDD10S) balls for SerDes Digital circuits
STRAP	Strapping balls cannot be left floating on the board

a. For REFCLK input, CML source is recommended; however, LVDS source is supported.

3.3 Internal Pull-Up Resistors

The signals listed in Table 3-3 have a weak internal pull-up resistor. If a listed signal is not used and no board trace is connected to the ball, the internal resistor is normally sufficient to keep the signal from toggling. If a listed signal is not used, but is connected to a board trace, the internal resistors might not be strong enough to hold the signal in the inactive state, and therefore it is recommended that the signal be pulled High to VDD33 or Low to VSS (GND), as appropriate, through a 3K- to 10K-Ohm resistor.

Table 3-3. Balls with Internal Pull-Up Resistors

Signal Name		
EE_DO	HP_PRSNT[1:0]#	JTAG_TCK
HP_BUTTON[1:0]#	HP_PRSNT[11:8]#	JTAG_TDI
HP_BUTTON[11:8]#	HP_PWRFLT[1:0]#	JTAG_TMS
HP_MRL[1:0]#	HP_PWRFLT[11:8]#	JTAG_TRST#
HP_MRL[11:8]#		

3.4 Signal Ball Descriptions – PEX 8524V, 680-Ball PBGA

3.4.1 PCI Express Signals – 680-Ball PBGA

The PCI Express SerDes and Control signals are defined in Table 3-4.

Note: *The ball numbers are ordered in sequence to follow the Signal Name sequencing [n to 0].*

Table 3-4. PEX 8524VAA/BB/BC PCI Express Signals, 680-Ball PBGA – 124 Balls

Signal Name	Type	Location	Description
PEX_LANE_GOOD[7:0]#	O	AA3, Y3, W3, V3, U3, T3, R3, P3	**Active-Low PCI Express Lane Status Indicator Outputs for Lanes [7:0] and [31:16] (24 Balls)** These signal balls can directly drive common-anode LED modules.
PEX_LANE_GOOD[31:16]#	O	AB31, AA31, Y31, W31, V31, U31, T31, R31, P4, R4, T4, U4, V4, W4, Y4, AA4	
PEX_NT_RESET#	O	J1	**Active-Low Output Used to Propagate Reset in NT Mode**
PEX_PERn[7:0]	CMLRn	AK18, AK16, AK14, AK12, AK10, AK8, AK6, AK4	**Negative Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PERn[31:16]	CMLRn	E34, E32, E30, E28, E26, E24, E22, E20, E18, E16, E14, E12, E10, E8, E6, E1	**Negative Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_PERp[7:0]	CMLRp	AL18, AL16, AL14, AL12, AL10, AL8, AL6, AL4	**Positive Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PERp[31:16]	CMLRp	D34, D32, D30, D28, D26, D24, D22, D20, D18, D16, D14, D12, D10, D8, D6, D1	**Positive Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_PERST#	I	H1	**PCI Express Reset** Used to cause a Fundamental Reset. (Refer to Chapter 5, "Reset and Initialization," for further details.)
PEX_PETn[7:0]	CMLTn	AP18, AP16, AP14, AP12, AP10, AP8, AP6, AP4	**Negative Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PETn[31:16]	CMLTn	A34, A32, A30, A28, A26, A24, A22, A20, A18, A16, A14, A12, A10, A8, A6, A4	**Negative Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**

Table 3-4. PEX 8524VAA/BB/BC PCI Express Signals, 680-Ball PBGA – 124 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PETp[7:0]	CMLTp	AN18, AN16, AN14, AN12, AN10, AN8, AN6, AN4	**Positive Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PETp[31:16]	CMLTp	B34, B32, B30, B28, B26, B24, B22, B20, B18, B16, B14, B12, B10, B8, B6, B4	**Positive Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_REFCLKn	CMLCLKn	AL1	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair for PEX 8524**
PEX_REFCLKp	CMLCLKp	AL2	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair for PEX 8524**

3.4.2 Hot Plug Signals – 680-Ball PBGA

The PEX 8524 includes nine Hot Plug signals for each PCI Express port (6 ports x 9 signals/port = 54 total signals), defined in Table 3-5. These signals are active only for downstream ports that are configured at start-up. (Refer to Chapter 9, "Hot Plug Support," for further details.)

Table 3-5. PEX 8524VAA/BB/BC Hot Plug Signals, 680-Ball PBGA – 54 Balls

Signal Name	Type	Location	Description
HP_ATNLED[1:0]#	O	L1, Y1	**Hot Plug Attention LED Output for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic output used to drive the Attention Indicator. Output is set Low to turn On the LED. Enabled when the **Slot Capabilities** register *Attention Indicator Present* bit is set (offset 7Ch[3]=1) and controlled by the **Slot Control** register *Attention Indicator Control* field (offset 80h[7:6]). When software writes any value other than 00b (***Reserved***) to the *Attention Indicator Control* field and an Attention_Indicator message is sent to the downstream device, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capabilities** register *Attention Indicator Present* bit is set (offset 7Ch[3]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. An external current-limiting resistor is required.
HP_ATNLED[11:8]#	O	AE33, T33, AF2, U2	**Hot Plug Attention LED Output for Station 1 Ports (4 Balls)** Refer to description for HP_ATNLED[1:0]#.
HP_BUTTON[1:0]#	I PU[a]	K1, W1	**Hot Plug Attention Button Input for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic input, directly connected to the Attention Button, with input assertion status latched in the **Slot Status** register *Attention Button Pressed* field (offset 80h[16]). Enabled when the **Slot Capabilities** register Attention Button Present bit is set (offset 7Ch[0]=1). When the following conditions exist: • HP_BUTTON*x*# is not masked (**Slot Control** register *Attention Button Pressed Enable* bit (offset 80h[0]=1), and • **Slot Capabilities** register *Hot Plug Capable* bit is set (offset 7Ch[6]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated, to notify the Host of intended board insertion or removal. ***Note:*** *HP_BUTTONx# is internally de-bounced, but must remain stable for at least 10 ms.*
HP_BUTTON[11:8]#	I PU[a]	AF33, U33, AG2, V2	**Hot Plug Attention Button Input for Station 1 Ports (4 Balls)** Refer to description for HP_BUTTON[1:0]#.

Table 3-5. PEX 8524VAA/BB/BC Hot Plug Signals, 680-Ball PBGA – 54 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_CLKEN[1:0]#	O	V1, AG1	**Reference Clock Enable Output for Station 0 Ports (2 Balls)** Active-Low output that, when enabled, allows external REFCLK to be provided to the slot. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN*x*# output assertion to HP_CLKEN*x*# output assertion is programmable (through serial EEPROM load) from 16 ms (default) to 128 ms, in the *HPC Tpepv Delay* field (offset 1E0h[4:3]).
HP_CLKEN[11:8]#	O	V33, J33, W2, K2	**Reference Clock Enable Output for Station 1 Ports (4 Balls)** Refer to description for HP_CLKEN[1:0]#.
HP_MRL[1:0]#	I PU[a]	M1, AA1	**Hot Plug Manually Operated Retention Latch Sensor Input for Station 0 Ports (2 Balls)** Active-Low input that triggers Slot Control Logic. Directly connected to an optional MRL Sensor that is logic High when the latch is not closed. HP_MRL*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN*x*# and HP_PWRLED*x*#) and clock (HP_CLKEN*x*#), and de-assert Reset (HP_PERST*x*#) after reset or under software control. A change in the HP_MRL*x*# Input signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL*x*# is not masked (**Slot Control** register *MRL Sensor Changed Enable* bit, offset 80h[2]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated. If the associated Hot Plug-capable downstream port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL*x*# is normally connected to HP_PRSNT*x*# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable downstream port instead connects directly to a device (in which case Hot Plug is not used), pull HP_MRL*x*# Low. ***Note:*** *HP_MRLx# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRLx#, if enabled, is not de-bounced when sampled immediately after reset.*
HP_MRL[11:8]#	I PU[a]	AD33, R33, AE2, T2	**Hot Plug Manually Operated Retention Latch Sensor Input for Station 1 Ports (4 Balls)** Refer to description for HP_MRL[1:0]#.
HP_PERST[1:0]#	O	T1, AE1	**Active-Low Reset Output for Station 0 Ports (2 Balls)** Active-Low Hot Plug output used to reset the slot. Controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]).
HP_PERST[11:8]#	O	Y33, L33, AA2, M2	**Active-Low Reset Output for Station 1 Ports (4 Balls)** Refer to description for HP_PERST[1:0]#.

Table 3-5. PEX 8524VAA/BB/BC Hot Plug Signals, 680-Ball PBGA – 54 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PRSNT[1:0]#	I PU[a]	R1, AD1	**Combination of Hot Plug PRSNT1# and PRSNT2# Input for Station 0 Ports (2 Balls)** Active-Low input connected to the slot's PRSNT2# signal, which on the add-in board connects to the slot's PRSNT1# signal, which is normally grounded on the PRSNT2# signal at the motherboard slot. A change in the HP_PRSNT*x*# Input signal state is latched in the **Slot Status** register *Presence Detect Changed* bit (offset 80h[19]), and the state change can assert an interrupt to notify the Host of board presence or absence. When the following conditions exist: • HP_PRSNT*x*# is not masked (**Slot Control** register *Presence Detect Changed Enable* bit (offset 80h[3]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated. ***Note:*** *HP_PRSNTx# is internally de-bounced, but must remain stable for at least 10 ms.*
HP_PRSNT[11:8]#	I PU[a]	AA33, M33, AB2, N2	**Combination of Hot Plug PRSNT1# and PRSNT2# Input for Station 1 Ports (4 Balls)** Refer to description for HP_PRSNT[1:0]#.
HP_PWREN[1:0]#	O	P1, AC1	**Active-Low Hot Plug Power Enable Output for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic output that controls the slot power state. When this signal is Low, power is enabled to the slot. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1). When software turns the slot's Power Controller On or Off (**Slot Control** register *Power Controller Control* bit, offset 80h[10]), a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. When HP_MRL*x*# is enabled [**Slot Capabilities** register *MRL Sensor Present* bit is set (offset 7Ch[2]=1)], HP_MRL*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power, by asserting HP_PWREN*x*# after reset or under software control.
HP_PWREN[11:8]#	O	AB33, N33, AC2, P2	**Active-Low Hot Plug Power Enable Output for Station 1 Ports (4 Balls)** Refer to description for HP_PWREN[1:0]#.

Table 3-5. PEX 8524VAA/BB/BC Hot Plug Signals, 680-Ball PBGA – 54 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PWRFLT[1:0]#	I PU[a]	N1, AB1	**Hot Plug Power Fault Input for Station 0 Ports (2 Balls)** Active-Low input that indicates the slot's external Power Controller detected a power fault on one or more supply rails. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and input assertion status is latched in the **Slot Status** register *Power Fault Detected* bit (offset 80h[17]). When the following conditions exist: • HP_PWRFLT*x*# is not masked (**Slot Control** register Power Fault Detector Enable bit (offset 80h[1]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated, to notify the Host of a power fault. ***Note:*** *If HP_PWRENx# and HP_CLKENx# are not used, HP_PWRFLTx# can be used as a general-purpose input with status reflected in the **Slot Status** register Power Fault Detected (offset 80h[17]), provided the **Slot Capabilities** register Power Controller Present bit is set (offset 7Ch[1]=1).*
HP_PWRFLT[11:8]#	I PU[a]	AC33, P33, AD2, R2	**Hot Plug Power Fault Input for Station 1 Ports (4 Balls)** Refer to description for HP_PWRFLT[1:0]#.
HP_PWRLED[1:0]#	O	U1, AF1	**Hot Plug Power LED Output for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic output used to drive the Power Indicator. This output is set Low to turn On the LED. Enabled when the **Slot Capabilities** register *Power Indicator Present* bit is set (offset 7Ch[4]=1), and controlled by the **Slot Status** register *Power Indicator Control* field (offset 80h[9:8]). When software writes any value other than 00b (***Reserved***) to the *Power Indicator Control* field and a Power_Indicator message is sent to the downstream device, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capabilities** register *Power Indicator Present* bit is set (offset 7Ch[4]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. An external current-limiting resistor is required.
HP_PWRLED[11:8]#	O	W33, K33, Y2, L2	**Hot Plug Power LED Output for Station 1 Ports (4 Balls)** Refer to description for HP_PWRLED[1:0]#.

a. If Hot Plug outputs (including HP_PERSTx#) are used and HP_MRLx# input is not used, pull HP_MRLx# input Low so that Hot Plug outputs (including HP_PERSTx#) will properly sequence if the serial EEPROM is blank or missing. Default register values enable HP_MRLx#, which must then be asserted to cause Hot Plug outputs to toggle (for example, to de-assert HP_PERSTx# and assert HP_PWRLEDx#).

3.4.3 Serial EEPROM Signals – 680-Ball PBGA

The PEX 8524 includes five signals for interfacing to a serial EEPROM, defined in Table 3-6.

Table 3-6. PEX 8524VAA/BB/BC Serial EEPROM Signals, 680-Ball PBGA – 5 Balls

Signal Name	Type	Location	Description
EE_CS#	O	AG32	**Serial EEPROM Active-Low Chip Select Output**
EE_DI	O	AH34	**PEX 8524 Output to Serial EEPROM Data Input**
EE_DO	I PU	AG34	**PEX 8524 Input from Serial EEPROM Data Output**
EE_PR#	I	AH33	**Serial EEPROM Present Active-Low Input** Must be tied to VSS to indicate serial EEPROM presence.
EE_SK	O	AG33	**7.8 MHz Serial EEPROM Clock Output**

3.4.4 Strapping Signals – 680-Ball PBGA

The PEX 8524 Strapping signals, defined in Table 3-7, set the configuration of upstream and NT Port assignment, port width, and various setup and test modes. These balls must be tied High to VDD33 or Low to VSS (GND). After a Fundamental Reset, the **Link Capabilities**, **Debug Control**, and **Port Configuration** registers capture ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the serial EEPROM.

Table 3-7. PEX 8524VAA/BB/BC Strapping Signals, 680-Ball PBGA – 24 Balls

Signal Name	Type	Location	Description
STRAP_FACTORY_TEST1#	I STRAP	AH2	**For *Factory Test Only*** Must be tied High.
STRAP_MODE_SEL[1:0]	I STRAP	H2, G1	**Mode Selects (2 Balls)** Register/Bits – **Debug Control** register *Mode Select* field (Port 0, offset 1DCh[19:18]) LL = ***Reserved*** LH = Intelligent Adapter mode HL = Dual-Host mode HH = Transparent mode (T mode)
STRAP_NT_UPSTRM_PORTSEL[3:0]	I STRAP	M31, L31, L32, K32	**Select Non-Transparent Upstream Port (4 Balls)** Register/Bits – **Debug Control** register *NT Port Number* field (Port 0, offset 1DCh[27:24]) LLLL = Port 0 LLLH = Port 1 LLHL to LHHH = ***Reserved*** HLLL = Port 8 HLLH = Port 9 HLHL = Port 10 HLHH = Port 11 HHLL to HHHH = ***Reserved*** If NT Port is not used, set to HHHH.
STRAP_STN0_PORTCFG[4:0]	I STRAP	AC32, AC31, AD32, AD31, AE32	**Strapping Signals to Select Number of Lanes in Station 0, Ports 0, 1 (5 Balls)** Register/Bits – **Port Configuration** register *Port Configuration* field (Port 0, offset 224h[4:0]) ***Note:*** *x0 indicates the port is not enabled.* LLLLL = x4, x4 LLLHL = x8 All other configurations are ***reserved*** and default to x4, x4.

Table 3-7. PEX 8524VAA/BB/BC Strapping Signals, 680-Ball PBGA – 24 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_STN1_PORTCFG[3:0]	I STRAP	P31, N32, N31, M32	**Strapping Signals to Select Number of Lanes in Station 1, Ports 8, 9, 10, 11 (4 Balls)** Register/Bits – **Port Configuration** register *Port Configuration* field (Port 8, offset 224h[4:0]) ***Note:*** *x0 indicates the port is not enabled.* LLLL = x4, x4, x4, x4 LLLH = x16, x0, x0, x0 LLHL = x8, x8, x0, x0 LLHH = x8, x4, x4, x0 LHLL = x8, x4, x2, x2 LHLH = x8, x2, x2, x4 LHHL = x8, x2, x4, x2 All other configurations are ***reserved*** and default to x4, x4, x4, x4.
STRAP_TESTMODE[3:0]	I STRAP	H33, H34, G33, G34	**Test Mode Selects (4 Balls)** ***Factory Test Only*** Register – **Physical Layer Test** (Ports 0 and 8, offset 228h) HHHH = Default (Test Modes are disabled)
STRAP_UPSTRM_PORTSEL[3:0]	I STRAP	N4, M4, N3, M3	**Strapping Signals to Select Upstream Port (4 Balls)** Register/Bits – **Debug Control** register *Upstream Port Number* field (Port 0, offset 1DCh[11:8]) LLLL = Port 0 LLLH = Port 1 LLHL to LHHH = ***Reserved*** HLLL = Port 8 HLLH = Port 9 HLHL = Port 10 HLHH = Port 11 HHLL to HHHH = ***Reserved***

3.4.5 JTAG Interface Signals – 680-Ball PBGA

The PEX 8524 includes five signals for performing JTAG boundary scan, defined in Table 3-8. (Refer to Chapter 17, "Test and Debug," for further details.)

Table 3-8. PEX 8524VAA/BB/BC JTAG Interface Signals, 680-Ball PBGA – 5 Balls

Signal Name	Type	Location	Description
JTAG_TCK	I PU	J2	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 10 MHz.
JTAG_TDI	I PU	K3	**JTAG Test Data Input** Serial input to the TAP Controller for test instructions and data.
JTAG_TDO	O	J3	**JTAG Test Data Output** Serial output from the TAP Controller test instructions and data.
JTAG_TMS	I PU	J4	**JTAG Test Mode Select** When high, JTAG Test mode is enabled. Input decoded by the TAP Controller to control test operations.
JTAG_TRST#	I PU	K4	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. Tie to ground through a 1.5K-Ohm resistor, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation. When JTAG functionality is not used, the JTAG_TRST# input should be pulled or driven Low, to place the TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.

3.4.6 No Connect Signals – 680-Ball PBGA

Caution: ***Do not connect the following PEX 8524 balls to board electrical paths, as these balls are not connected within the PEX 8524.***

Table 3-9. PEX 8524VAA/BB/BC No Connect Signals, 680-Ball PBGA – 92 Balls

Signal Name	Type	Location	Description
N/C	***Reserved***	A1, A2, B1, B2, D3, E3, F3, G2, G3, G32, H3, H4, J34, K34, L3, L4, L34, M34, N34, P34, R32, R34, T32, T34, U32, U34, V32, V34, W32, W34, Y32, Y34, AA32, AA34, AB3, AB4, AB32, AB34, AC3, AC4, AC34, AD3, AD4, AD34, AE3, AE4, AE31, AE34, AF3, AF4, AF31, AF32, AF34, AG3, AH3, AH32, AK20, AK22, AK24, AK26, AK28, AK30, AK32, AK34, AL20, AL22, AL24, AL26, AL28, AL30, AL32, AL34, AN1, AN2, AN20, AN22, AN24, AN26, AN28, AN30, AN32, AN34, AP1, AP2, AP20, AP22, AP24, AP26, AP28, AP30, AP32, AP34	**No Connect (92 Balls)** Do not connect these balls to board electrical paths.

3.4.7 Power and Ground Signals – 680-Ball PBGA

Table 3-10. PEX 8524VAA/BB/BC Power and Ground Signals, 680-Ball PBGA – 376 Balls

Signal Name	Type	Location	Description
VDD10	CPWR	E9, E11, E13, E17, E19, E21, E25, E27, E29, F5, G5, G30, J30, K5, M5, M30, P30, T5, T30, V5, V30, AA5, AA30, AC5, AC30, AE5, AE30, AG5, AG30, AJ30, AK9, AK11, AK13, AK17, AK19, AK21, AK23, AK25, AK27, AK29	**1.15V ±3% (PEX 8524VAA) or 1.0V ±5% (PEX 8524VBB/BC) Power for Core Logic (40 Balls)**
VDD10A	APWR	E7, E15, E23, F30, AJ5, AK7, AK15	**1.15V ±3% (PEX 8524VAA) or 1.0V ±5% (PEX 8524VBB/BC) Power for SerDes Analog Circuits (7 Balls)**
VDD10S	SPWR	B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, C3, C7, C11, C15, C19, C23, C27, C31, D4, E5, E31, E33, F33, AJ33, AK5, AK31, AK33, AM3, AM7, AM11, AM15, AM19, AM23, AM27, AM31, AN3, AN5, AN7, AN9, AN11, AN13, AN15, AN17, AN19, AN21, AN23, AN25, AN27, AN29, AN31, AN33	**1.15V ±3% (PEX 8524VAA) or 1.0V ±5% (PEX 8524VBB/BC) Power for SerDes Digital Circuits (57 Balls)**
VDD33	I/OPWR	H5, H32, J31, J32, K30, K31, L5, N5, N30, R5, U5, U30, Y5, Y30, AB5, AB30, AF5, AF30, AG31, AH1, AH30	**3.3V Power for I/O Logic Functions (21 Balls)**
VDD33A	PLLPWR	AH5	**3.3V Power for PLL Circuits**
VSS	GND	A3, A7, A11, A15, A19, A23, A27, A31, C1, C2, C4, C5, C6, C8, C9, C10, C12, C13, C14, C16, C17, C18, C20, C21, C22, C24, C25, C26, C28, C29, C30, C32, C33, C34, D2, D5, D7, D9, D11, D13, D15, D17, D19, D21, D23, D25, D27, D29, D31, D33, E2, E4, F1, F2, F4, F31, F32, F34, G4, G31, H30, H31, J5, L30, P5, P32, R30, W5, W30, AD5, AD30, AG4, AH31, AJ1, AJ2, AJ3, AJ4, AJ31, AJ32, AJ34, AK1, AK2, AK3, AL3, AL5, AL7, AL9, AL11, AL13, AL15, AL17, AL19, AL21, AL23, AL25, AL27, AL29, AL31, AL33, AM1, AM2, AM4, AM5, AM6, AM8, AM9, AM10, AM12, AM13, AM14, AM16, AM17, AM18, AM20, AM21, AM22, AM24, AM25, AM26, AM28, AM29, AM30, AM32, AM33, AM34, AP3, AP7, AP11, AP15, AP19, AP23, AP27, AP31	**Ground Connections (133 Balls)**

Table 3-10. PEX 8524VAA/BB/BC Power and Ground Signals, 680-Ball PBGA – 376 Balls *(Cont.)*

Signal Name	Type	Location	Description
VSS_THERMAL	Thermal-GND	N13, N14, N15, N16, N17, N18, N19, N20, N21, N22, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, V13, V14, V15, V16, V17, V18, V19, V20, V21, V22, W13, W14, W15, W16, W17, W18, W19, W20, W21, W22, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22	**Thermal-Ball Ground Connections (100 Balls)**
VSSA_PLL	PLL_GND	AH4	**PLL Ground Connection**
VTT_PEX[7:0]	Supply	AP33, AP29, AP25, AP21, AP17, AP13, AP9, AP5	**SerDes Termination Supply for Station 0[a] (8 Balls)** Tied to SerDes termination supply voltage (typically 1.5V).
VTT_PEX[15:8]	Supply	A33, A29, A25, A21, A17, A13, A9, A5	**SerDes Termination Supply for Station 1[a] (8 Balls)** Tied to SerDes termination supply voltage (typically 1.5V).

a. PEX_PETn/p[x] SerDes termination voltage controls the transmitter Common mode voltage (V_{TX-CM}) value and output voltage swing ($V_{TX-DIFFp}$), per the following formula:

$$V_{TX-CM} = V_{TT} - V_{TX-DIFFp}$$

3.5 Signal Ball Descriptions – PEX 8524, 644-Ball PBGA

3.5.1 PCI Express Signals – 644-Ball PBGA

The PCI Express SerDes and Control signals are defined in Table 3-11.

Note: *The ball numbers are ordered in sequence to follow the Signal Name sequencing [n to 0].*

Table 3-11. PEX 8524BB/BC PCI Express Signals, 644-Ball PBGA – 124 Balls

Signal Name	Type	Location	Description
PEX_LANE_GOOD[7:0]#	O	W1, V2, U2, T1, R2, P2, N3, M3	**Active-Low PCI Express Lane Status Indicator Outputs for Lanes [7:0] and [31:16] (24 Balls)** These signal balls can directly drive common-anode LED modules.
PEX_LANE_GOOD[31:16]#	O	AB27, AA27, Y27, W27, V27, U30, T30, R30, M2, N2, AD2, R1, AD3, U3, AD1, W2	
PEX_NT_RESET#	O	H3	**Active-Low Output Used to Propagate Reset in NT Mode**
PEX_PERn[7:0]	CMLRn	AF20, AF18, AF16, AF14, AF12, AG10, AF8, AF6	**Negative Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PERn[31:16]	CMLRn	G26, E30, E28, E26, E24, E22, E20, E18, E16, E14, E12, E10, E8, E6, E4, E2	**Negative Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_PERp[7:0]	CMLRp	AG20, AG18, AG16, AG14, AG12, AF10, AG8, AG6	**Positive Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PERp[31:16]	CMLRp	G27, D30, D28, D26, D24, D22, D20, D18, D16, D14, D12, D10, D8, D6, D4, D2	**Positive Half of PCI Express Receiver Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_PERST#	I	G3	**PCI Express Reset** Used to cause a Fundamental Reset. (Refer to Chapter 5, "Reset and Initialization," for further details.)

Table 3-11. PEX 8524BB/BC PCI Express Signals, 644-Ball PBGA – 124 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PETn[7:0]	CMLTn	AK20, AK18, AK16, AK14, AK12, AK10, AK8, AK6	**Negative Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PETn[31:16]	CMLTn	G30, A30, A28, A26, A24, A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2	**Negative Half of PCI Express transmitter Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_PETp[7:0]	CMLTp	AJ20, AJ18, AJ16, AJ14, AJ12, AJ10, AJ8, AJ6	**Positive Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 0 (8 Balls)**
PEX_PETp[31:16]	CMLTp	G29, B30, B28, B26, B24, B22, B20, B18, B16, B14, B12, B10, B8, B6, B4, B2	**Positive Half of PCI Express Transmitter Differential Signal Pairs for PEX 8524 Station 1 (16 Balls)**
PEX_REFCLKn	CMLCLKn	AK4	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair for PEX 8524**
PEX_REFCLKp	CMLCLKp	AJ4	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair for PEX 8524**

3.5.2 Hot Plug Signals – 644-Ball PBGA

The PEX 8524 includes nine Hot Plug signals for each PCI Express port (6 ports x 9 signals/port = 54 total signals), defined in Table 3-12. These signals are active only for downstream ports that are configured at start-up. (Refer to Chapter 9, "Hot Plug Support," for further details.)

Table 3-12. PEX 8524BB/BC Hot Plug Signals, 644-Ball PBGA – 54 Balls

Signal Name	Type	Location	Description
HP_ATNLED[1:0]#	O	K1, U4	**Hot Plug Attention LED Output for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic output used to drive the Attention Indicator. Output is set Low to turn On the LED. Enabled when the **Slot Capabilities** register *Attention Indicator Present* bit is set (offset 7Ch[3]=1) and controlled by the **Slot Control** register *Attention Indicator Control* field (offset 80h[7:6]). When software writes any value other than 00b (***Reserved***) to the *Attention Indicator Control* field and an Attention_Indicator message is sent to the downstream device, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capabilities** register *Attention Indicator Present* bit is set (offset 7Ch[3]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. An external current-limiting resistor is required.
HP_ATNLED[11:8]#	O	AE29, T28, AB2, R3	**Hot Plug Attention LED Output for Station 1 Ports (4 Balls)** Refer to description for HP_ATNLED[1:0]#.
HP_BUTTON[1:0]#	I PU[a]	J3, T4	**Hot Plug Attention Button Input for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic input, directly connected to the Attention Button, with input assertion status latched in the **Slot Status** register *Attention Button Pressed* field (offset 80h[16]). Enabled when the **Slot Capabilities** register Attention Button Present bit is set (offset 7Ch[0]=1). When the following conditions exist: • HP_BUTTON*x*# is not masked (**Slot Control** register *Attention Button Pressed Enable* bit (offset 80h[0]=1), and • **Slot Capabilities** register *Hot Plug Capable* bit is set (offset 7Ch[6]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated, to notify the Host of intended board insertion or removal. ***Note:*** *HP_BUTTONx# is internally de-bounced, but must remain stable for at least 10 ms.*
HP_BUTTON[11:8]#	I PU[a]	AF29, U28, AC1, T2	**Hot Plug Attention Button Input for Station 1 Ports (4 Balls)** Refer to description for HP_BUTTON[1:0]#.

Table 3-12. PEX 8524BB/BC Hot Plug Signals, 644-Ball PBGA – 54 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_CLKEN[1:0]#	O	T3, AB4	**Reference Clock Enable Output for Station 0 Ports (2 Balls)** Active-Low output that, when enabled, allows external REFCLK to be provided to the slot. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN*x*# output assertion to HP_CLKEN*x*# output assertion is programmable (through serial EEPROM load) from 16 ms (default) to 128 ms, in the *HPC Tpepv Delay* field (offset 1E0h[4:3]).
HP_CLKEN[11:8]#	O	V29, K30, U1, J2	**Reference Clock Enable Output for Station 1 Ports (4 Balls)** Refer to description for HP_CLKEN[1:0]#.
HP_MRL[1:0]#	I PU[a]	L1, V3	**Hot Plug Manually Operated Retention Latch Sensor Input for Station 0 Ports (2 Balls)** Active-Low input that triggers Slot Control Logic. Directly connected to an optional MRL Sensor that is logic High when the latch is not closed. HP_MRL*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN*x*# and HP_PWRLED*x*#) and clock (HP_CLKEN*x*#), and de-assert Reset (HP_PERST*x*#) after reset or under software control. A change in the HP_MRL*x*# Input signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL*x*# is not masked (**Slot Control** register *MRL Sensor Changed Enable* bit, offset 80h[2]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated. If the associated Hot Plug-capable downstream port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL*x*# is normally connected to HP_PRSNT*x*# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable downstream port instead connects directly to a device (in which case Hot Plug is not used), pull HP_MRL*x*# Low. ***Note:*** *HP_MRLx# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRLx#, if enabled, is not de-bounced when sampled immediately after reset.*
HP_MRL[11:8]#	I PU[a]	AD29, R28, AA4, P3	**Hot Plug Manually Operated Retention Latch Sensor Input for Station 1 Ports (4 Balls)** Refer to description for HP_MRL[1:0]#.
HP_PERST[1:0]#	O	P4, AA3	**Active-Low Reset Output for Station 0 Ports (2 Balls)** Active-Low Hot Plug output used to reset the slot. Controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]).
HP_PERST[11:8]#	O	Y29, L27, V4, K4	**Active-Low Reset Output for Station 1 Ports (4 Balls)** Refer to description for HP_PERST[1:0]#.

Table 3-12. PEX 8524BB/BC Hot Plug Signals, 644-Ball PBGA – 54 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PRSNT[1:0]#	I PU[a]	P1, Y4	**Combination of Hot Plug PRSNT1# and PRSNT2# Input for Station 0 Ports (2 Balls)** Active-Low input connected to the slot's PRSNT2# signal, which on the add-in board connects to the slot's PRSNT1# signal, which is normally grounded on the PRSNT2# signal at the motherboard slot. A change in the HP_PRSNT*x*# Input signal state is latched in the **Slot Status** register *Presence Detect Changed* bit (offset 80h[19]), and the state change can assert an interrupt to notify the Host of board presence or absence. When the following conditions exist: • HP_PRSNT*x*# is not masked (**Slot Control** register *Presence Detect Changed Enable* bit (offset 80h[3]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated. ***Note:*** *HP_PRSNTx# is internally de-bounced, but must remain stable for at least 10 ms.*
HP_PRSNT[11:8]#	I PU[a]	AA29, M27, W4, L4	**Combination of Hot Plug PRSNT1# and PRSNT2# Input for Station 1 Ports (4 Balls)** Refer to description for HP_PRSNT[1:0]#.
HP_PWREN[1:0]#	O	N1, Y1	**Active-Low Hot Plug Power Enable Output for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic output that controls the slot power state. When this signal is Low, power is enabled to the slot. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1). When software turns the slot's Power Controller On or Off (**Slot Control** register *Power Controller Control* bit, offset 80h[10]), a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. When HP_MRL*x*# is enabled [**Slot Capabilities** register *MRL Sensor Present* bit is set (offset 7Ch[2]=1)], HP_MRL*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power, by asserting HP_PWREN*x*# after reset or under software control.
HP_PWREN[11:8]#	O	AB29, N27, Y2, M4	**Active-Low Hot Plug Power Enable Output for Station 1 Ports (4 Balls)** Refer to description for HP_PWREN[1:0]#.

Table 3-12. PEX 8524BB/BC Hot Plug Signals, 644-Ball PBGA – 54 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PWRFLT[1:0]#	I PU[a]	M1, W3	**Hot Plug Power Fault Input for Station 0 Ports (2 Balls)** Active-Low input that indicates the slot's external Power Controller detected a power fault on one or more supply rails. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and input assertion status is latched in the **Slot Status** register *Power Fault Detected* (offset 80h[17]). When the following conditions exist: • HP_PWRFLT*x*# is not masked (**Slot Control** register Power Fault Detector Enable bit (offset 80h[1]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated, to notify the Host of a power fault. ***Note:*** *If HP_PWRENx# and HP_CLKENx# are not used, HP_PWRFLTx# can be used as a general-purpose input with status reflected in the **Slot Status** register Power Fault Detected (offset 80h[17]), provided the **Slot Capabilities** register Power Controller Present bit is set (offset 7Ch[1]=1).*
HP_PWRFLT[11:8]#	I PU[a]	AC29, P28, AA1, N4	**Hot Plug Power Fault Input for Station 1 Ports (4 Balls)** Refer to description for HP_PWRFLT[1:0]#.
HP_PWRLED[1:0]#	O	R4, AB1	**Hot Plug Power LED Output for Station 0 Ports (2 Balls)** Active-Low Slot Control Logic output used to drive the Power Indicator. This output is set Low to turn On the LED. Enabled when the **Slot Capabilities** register *Power Indicator Present* bit is set (offset 7Ch[4]=1), and controlled by the **Slot Status** register *Power Indicator Control* field (offset 80h[9:8]). When software writes any value other than 00b (***Reserved***) to the *Power Indicator Control* field and a Power_Indicator message is sent to the downstream device, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capabilities** register *Power Indicator Present* bit is set (offset 7Ch[4]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. An external current-limiting resistor is required.
HP_PWRLED[11:8]#	O	W29, K27, V1, J4	**Hot Plug Power LED Output for Station 1 Ports (4 Balls)** Refer to description for HP_PWRLED[1:0]#.

a. If Hot Plug outputs (including HP_PERSTx#) are used and HP_MRLx# input is not used, pull HP_MRLx# input Low so that Hot Plug outputs (including HP_PERSTx#) will properly sequence if the serial EEPROM is blank or missing. Default register values enable HP_MRLx#, which must then be asserted to cause Hot Plug outputs to toggle (for example, to de-assert HP_PERSTx# and assert HP_PWRLEDx#).

3.5.3 Serial EEPROM Signals – 644-Ball PBGA

The PEX 8524 includes five signals for interfacing to a serial EEPROM, defined in Table 3-13.

Table 3-13. PEX 8524BB/BC Serial EEPROM Signals, 644-Ball PBGA – 5 Balls

Signal Name	Type	Location	Description
EE_CS#	O	AG28	**Serial EEPROM Active-Low Chip Select Output**
EE_DI	O	AG27	**PEX 8524 Output to Serial EEPROM Data Input**
EE_DO	I PU	AG30	**PEX 8524 Input from Serial EEPROM Data Output**
EE_PR#	I	AH28	**Serial EEPROM Present Active-Low Input** Must be tied to VSS to indicate serial EEPROM presence.
EE_SK	O	AG29	**7.8 MHz Serial EEPROM Clock Output**

3.5.4 Strapping Signals – 644-Ball PBGA

The PEX 8524 Strapping signals, defined in Table 3-14, set the configuration of upstream and NT Port assignment, port width, and various setup and test modes. These balls must be tied High to VDD33 or Low to VSS (GND). After a Fundamental Reset, the **Link Capabilities**, **Debug Control**, and **Port Configuration** registers capture ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the serial EEPROM.

Table 3-14. PEX 8524BB/BC Strapping Signals, 644-Ball PBGA – 24 Balls

Signal Name	Type	Location	Description
STRAP_FACTORY_TEST1#	I STRAP	AC3	**For Factory Test Only** Must be tied High.
STRAP_MODE_SEL[1:0]	I STRAP	G2, G1	**Mode Selects (2 Balls)** Register/Bits – **Debug Control** register *Mode Select* field (Port 0, offset 1DCh[19:18]) LL = ***Reserved*** LH = Intelligent Adapter mode HL = Dual-Host mode HH = Transparent mode (T mode)
STRAP_NT_UPSTRM_PORTSEL[3:0]	I STRAP	M29, L29, L28, K28	**Select Non-Transparent Upstream Port (4 Balls)** Register/Bits – **Debug Control** register *NT Port Number* field (Port 0, offset 1DCh[27:24]) LLLL = Port 0 LLLH = Port 1 LLHL to LHHH = ***Reserved*** HLLL = Port 8 HLLH = Port 9 HLHL = Port 10 HLHH = Port 11 HHLL to HHHH = ***Reserved*** If NT Port is not used, set to HHHH.
STRAP_STN0_PORTCFG[4:0]	I STRAP	AC28, AC27, AD28, AD27, AE28	**Strapping Signals to Select Number of Lanes in Station 0, Ports 0, 1 (5 Balls)** Register/Bits – **Port Configuration** register *Port Configuration* field (Port 0, offset 224h[4:0]) LLLLL = x4, x4 LLLHL = x8 All other configurations are ***reserved*** and default to x4, x4.

Table 3-14. PEX 8524BB/BC Strapping Signals, 644-Ball PBGA – 24 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_STN1_PORTCFG[3:0]	I STRAP	P29, N28, N29, M28	**Strapping Signals to Select Number of Lanes in Station 1, Ports 8, 9, 10, 11 (4 Balls)** Register/Bits – **Port Configuration** register *Port Configuration* field (Port 8, offset 224h[4:0]) ***Note:*** *x0 indicates the port is not enabled.* LLLL = x4, x4, x4, x4 LLHL = x8, x8, x0, x0 LLHH = x8, x4, x4, x0 LHLL = x8, x4, x2, x2 LHLH = x8, x2, x2, x4 LHHL = x8, x2, x4, x2 All other configurations are ***reserved*** and default to x4, x4, x4, x4.
STRAP_TESTMODE[3:0]	I STRAP	J28, J27, J30, J29	**Test Mode Selects (4 Balls)** ***Factory Test Only*** Register – **Physical Layer Test** (Ports 0 and 8, offset 228h) HHHH = Default (Test Modes are disabled)
STRAP_UPSTRM_PORTSEL[3:0]	I STRAP	L2, K2, L3, K3	**Strapping Signals to Select Upstream Port (4 Balls)** Register/Bits – **Debug Control** register *Upstream Port Number* field (Port 0, offset 1DCh[11:8]) LLLL = Port 0 LLLH = Port 1 LLHL to LHHH = ***Reserved*** HLLL = Port 8 HLLH = Port 9 HLHL = Port 10 HLHH = Port 11 HHLL to HHHH = ***Reserved***

3.5.5 JTAG Interface Signals – 644-Ball PBGA

The PEX 8524 includes five signals for performing JTAG boundary scan, defined in Table 3-15. (Refer to Chapter 17, "Test and Debug," for further details.)

Table 3-15. PEX 8524BB/BC JTAG Interface Signals, 644-Ball PBGA – 5 Balls

Signal Name	Type	Location	Description
JTAG_TCK	I PU	H2	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 10 MHz.
JTAG_TDI	I PU	J1	**JTAG Test Data Input** Serial input to the TAP Controller for test instructions and data.
JTAG_TDO	O	H1	**JTAG Test Data Output** Serial output from the TAP Controller test instructions and data.
JTAG_TMS	I PU	G4	**JTAG Test Mode Select** When high, JTAG Test mode is enabled. Input decoded by the TAP Controller to control test operations.
JTAG_TRST#	I PU	H4	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. Tie to ground through a 1.5K-Ohm resistor, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation. When JTAG functionality is not used, the JTAG_TRST# input should be pulled or driven Low, to place the TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.

3.5.6 No Connect Signals – 644-Ball PBGA

Caution: ***Do not connect the following PEX 8524 balls to board electrical paths, as these balls are not connected within the PEX 8524.***

Table 3-16. PEX 8524BB/BC No Connect Signals, 644-Ball PBGA – 37 Balls

Signal Name	Type	Location	Description
N/C	***Reserved***	K29, L30, M30, N30, P27, P30, R27, R29, T27, T29, U27, U29, V28, V30, W28, W30, Y3, Y28, Y30, AA2, AA28, AA30, AB3, AB28, AB30, AC2, AC30, AD30, AE1, AE2, AE27, AE30, AF27, AF28, AF30, AH27	**No Connect (36 Balls)** Do not connect these balls to board electrical paths.
NC_PROCMON	***Reserved***	AF2	**No Connect** Do not connect this ball to board electrical paths.

3.5.7 Power and Ground Signals – 644-Ball PBGA

Table 3-17. PEX 8524BB/BC Power and Ground Signals, 644-Ball PBGA – 395 Balls

Signal Name	Type	Location	Description
VDD10	CPWR	K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K20, K21, L10, L21, M10, M21, N10, N21, P10, P21, R10, R21, T10, T21, U10, U21, V10, V21, W10, W21, Y10, Y21, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21	**1.0V ±5% (PEX 8524BB/BC) Power for Core Logic (44 Balls)**
VDD10A	APWR	E7, E15, E23, F26, AF11, AF17, AF21	**1.0V ±5% (PEX 8524BB/BC) Power for SerDes Analog Circuits (7 Balls)**
VDD10S	SPWR	A7, A11, A15, A19, A23, A27, B1, B3, B5, B9, B13, B17, B21, B25, B29, C3, C5, C7, C11, C15, C19, C27, D1, D23, E3, E5, E13, E27, E29, F2, F28, F30, H27, H29, AF23, AF25, AG2, AG9, AG13, AG17, AG22, AG24, AH1, AH3, AH7, AH11, AH15, AH19, AH21, AH23, AH25, AJ2, AJ5, AJ9, AJ13, AJ22, AJ24, AK1, AK3, AK7, AK11, AK15, AK17, AK19, AK21, AK23, AK25	**1.0V ±5% (PEX 8524BB/BC) Power for SerDes Digital Circuits (67 Balls)**
VDD33	I/OPWR	H5, J26, K5, L26, M5, N26, P5, R26, T5, U26, V5, W26, Y5, AA26, AB5, AC26, AE3, AE26, AF3, AG26, AH29, AJ26, AJ28, AJ30, AK27, AK29	**3.3V Power for I/O Logic Functions (26 Balls)**
VDD33A	PLLPWR	AF1	**3.3V Power for PLL Circuits**
VSS	GND	A1, A3, A5, A9, A13, A17, A21, A25, A29, B7, B11, B15, B19, B23, B27, C1, C2, C4, C6, C8, C9, C10, C12, C13, C14, C16, C17, C18, C20, C21, C22, C23, C24, C25, C26, C28, C29, C30, D3, D5, D7, D9, D11, D13, D15, D17, D19, D21, D25, D27, D29, E1, F1, F3, F5, F27, F29, G5, G28, H28, H30, J5, K26, L5, M26, N5, P26, R5, T26, U5, V26, W5, Y26, AA5, AB26, AC5, AD4, AD5, AD26, AE4, AE5, AF4, AF5, AF13, AF22, AF24, AF26, AG1, AG3, AG4, AG5, AG7, AG11, AG15, AG19, AG21, AG23, AG25, AH2, AH4, AH5, AH6, AH8, AH9, AH10, AH12, AH13, AH14, AH16, AH17, AH18, AH20, AH22, AH24, AH26, AH30, AJ1, AJ3, AJ7, AJ11, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AK2, AK5, AK9, AK13, AK22, AK24, AK26, AK28, AK30	**Ground Connections (137 Balls)**
VSSA_PLL	PLL_GND	AC4	**PLL Ground Connection**

Table 3-17. PEX 8524BB/BC Power and Ground Signals, 644-Ball PBGA – 395 Balls *(Cont.)*

Signal Name	Type	Location	Description
VSS_THERMAL	Thermal-GND	L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20	**Thermal-Ball Ground Connections (100 Balls)** Not internally connected to the die.
VTT_PEX[3:0]	Supply	AF19, AF15, AF9, AF7	**SerDes Termination for Station 0[a] (4 Balls)** Tied to SerDes termination voltage (typically 1.5V).
VTT_PEX[15:8]	Supply	H26, E25, E21, E19, E17, E11, E9, F4	**SerDes Termination for Station 1[a] (8 Balls)** Tied to SerDes termination voltage (typically 1.5V).

a. PEX_PETn/p[x] SerDes termination voltage controls the transmitter Common mode voltage (V_{TX-CM}) value and output voltage swing ($V_{TX-DIFFp}$), per the following formula:

$$V_{TX-CM} = V_{TT} - V_{TX-DIFFp}$$

3.6 Ball Assignments by Number

Note: *For "Type" definitions, refer to Table 3-2.*

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
A1	N/C	***Reserved***	No Connect	
A2	N/C	***Reserved***	No Connect	
A3	VSS	GND	Ground	
A4	PEX_PETn16	CMLTn	SerDes	
A5	VTT_PEX8	Supply	Power	
A6	PEX_PETn17	CMLTn	SerDes	
A7	VSS	GND	Ground	
A8	PEX_PETn18	CMLTn	SerDes	
A9	VTT_PEX9	Supply	Power	
A10	PEX_PETn19	CMLTn	SerDes	
A11	VSS	GND	Ground	
A12	PEX_PETn20	CMLTn	SerDes	
A13	VTT_PEX10	Supply	Power	
A14	PEX_PETn21	CMLTn	SerDes	
A15	VSS	GND	Ground	
A16	PEX_PETn22	CMLTn	SerDes	
A17	VTT_PEX11	Supply	Power	
A18	PEX_PETn23	CMLTn	SerDes	
A19	VSS	GND	Ground	
A20	PEX_PETn24	CMLTn	SerDes	
A21	VTT_PEX12	Supply	Power	
A22	PEX_PETn25	CMLTn	SerDes	
A23	VSS	GND	Ground	
A24	PEX_PETn26	CMLTn	SerDes	
A25	VTT_PEX13	Supply	Power	
A26	PEX_PETn27	CMLTn	SerDes	
A27	VSS	GND	Ground	
A28	PEX_PETn28	CMLTn	SerDes	
A29	VTT_PEX14	Supply	Power	
A30	PEX_PETn29	CMLTn	SerDes	
A31	VSS	GND	Ground	
A32	PEX_PETn30	CMLTn	SerDes	
A33	VTT_PEX15	Supply	Power	
A34	PEX_PETn31	CMLTn	SerDes	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
B1	N/C	***Reserved***	No Connect	
B2	N/C	***Reserved***	No Connect	
B3	VDD10S	SPWR	Power	
B4	PEX_PETp16	CMLTp	SerDes	
B5	VDD10S	SPWR	Power	
B6	PEX_PETp17	CMLTp	SerDes	
B7	VDD10S	SPWR	Power	
B8	PEX_PETp18	CMLTp	SerDes	
B9	VDD10S	SPWR	Power	
B10	PEX_PETp19	CMLTp	SerDes	
B11	VDD10S	SPWR	Power	
B12	PEX_PETp20	CMLTp	SerDes	
B13	VDD10S	SPWR	Power	
B14	PEX_PETp21	CMLTp	SerDes	
B15	VDD10S	SPWR	Power	
B16	PEX_PETp22	CMLTp	SerDes	
B17	VDD10S	SPWR	Power	
B18	PEX_PETp23	CMLTp	SerDes	
B19	VDD10S	SPWR	Power	
B20	PEX_PETp24	CMLTp	SerDes	
B21	VDD10S	SPWR	Power	
B22	PEX_PETp25	CMLTp	SerDes	
B23	VDD10S	SPWR	Power	
B24	PEX_PETp26	CMLTp	SerDes	
B25	VDD10S	SPWR	Power	
B26	PEX_PETp27	CMLTp	SerDes	
B27	VDD10S	SPWR	Power	
B28	PEX_PETp28	CMLTp	SerDes	
B29	VDD10S	SPWR	Power	
B30	PEX_PETp29	CMLTp	SerDes	
B31	VDD10S	SPWR	Power	
B32	PEX_PETp30	CMLTp	SerDes	
B33	VDD10S	SPWR	Power	
B34	PEX_PETp31	CMLTp	SerDes	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
C1	VSS	GND	Ground	
C2	VSS	GND	Ground	
C3	VDD10S	SPWR	Power	
C4	VSS	GND	Ground	
C5	VSS	GND	Ground	
C6	VSS	GND	Ground	
C7	VDD10S	SPWR	Power	
C8	VSS	GND	Ground	
C9	VSS	GND	Ground	
C10	VSS	GND	Ground	
C11	VDD10S	SPWR	Power	
C12	VSS	GND	Ground	
C13	VSS	GND	Ground	
C14	VSS	GND	Ground	
C15	VDD10S	SPWR	Power	
C16	VSS	GND	Ground	
C17	VSS	GND	Ground	
C18	VSS	GND	Ground	
C19	VDD10S	SPWR	Power	
C20	VSS	GND	Ground	
C21	VSS	GND	Ground	
C22	VSS	GND	Ground	
C23	VDD10S	SPWR	Power	
C24	VSS	GND	Ground	
C25	VSS	GND	Ground	
C26	VSS	GND	Ground	
C27	VDD10S	SPWR	Power	
C28	VSS	GND	Ground	
C29	VSS	GND	Ground	
C30	VSS	GND	Ground	
C31	VDD10S	SPWR	Power	
C32	VSS	GND	Ground	
C33	VSS	GND	Ground	
C34	VSS	GND	Ground	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
D1	PEX_PERp16	CMLRp	SerDes	
D2	VSS	GND	Ground	
D3	N/C	***Reserved***	No Connect	
D4	VDD10S	SPWR	Power	
D5	VSS	GND	Ground	
D6	PEX_PERp17	CMLRp	SerDes	
D7	VSS	GND	Ground	
D8	PEX_PERp18	CMLRp	SerDes	
D9	VSS	GND	Ground	
D10	PEX_PERp19	CMLRp	SerDes	
D11	VSS	GND	Ground	
D12	PEX_PERp20	CMLRp	SerDes	
D13	VSS	GND	Ground	
D14	PEX_PERp21	CMLRp	SerDes	
D15	VSS	GND	Ground	
D16	PEX_PERp22	CMLRp	SerDes	
D17	VSS	GND	Ground	
D18	PEX_PERp23	CMLRp	SerDes	
D19	VSS	GND	Ground	
D20	PEX_PERp24	CMLRp	SerDes	
D21	VSS	GND	Ground	
D22	PEX_PERp25	CMLRp	SerDes	
D23	VSS	GND	Ground	
D24	PEX_PERp26	CMLRp	SerDes	
D25	VSS	GND	Ground	
D26	PEX_PERp27	CMLRp	SerDes	
D27	VSS	GND	Ground	
D28	PEX_PERp28	CMLRp	SerDes	
D29	VSS	GND	Ground	
D30	PEX_PERp29	CMLRp	SerDes	
D31	VSS	GND	Ground	
D32	PEX_PERp30	CMLRp	SerDes	
D33	VSS	GND	Ground	
D34	PEX_PERp31	CMLRp	SerDes	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
E1	PEX_PERn16	CMLRn	SerDes	
E2	VSS	GND	Ground	
E3	N/C	***Reserved***	No Connect	
E4	VSS	GND	Ground	
E5	VDD10S	SPWR	Power	
E6	PEX_PERn17	CMLRn	SerDes	
E7	VDD10A	APWR	Power	
E8	PEX_PERn18	CMLRn	SerDes	
E9	VDD10	CPWR	Power	
E10	PEX_PERn19	CMLRn	SerDes	
E11	VDD10	CPWR	Power	
E12	PEX_PERn20	CMLRn	SerDes	
E13	VDD10	CPWR	Power	
E14	PEX_PERn21	CMLRn	SerDes	
E15	VDD10A	APWR	Power	
E16	PEX_PERn22	CMLRn	SerDes	
E17	VDD10	CPWR	Power	
E18	PEX_PERn23	CMLRn	SerDes	
E19	VDD10	CPWR	Power	
E20	PEX_PERn24	CMLRn	SerDes	
E21	VDD10	CPWR	Power	
E22	PEX_PERn25	CMLRn	SerDes	
E23	VDD10A	APWR	Power	
E24	PEX_PERn26	CMLRn	SerDes	
E25	VDD10	CPWR	Power	
E26	PEX_PERn27	CMLRn	SerDes	
E27	VDD10	CPWR	Power	
E28	PEX_PERn28	CMLRn	SerDes	
E29	VDD10	CPWR	Power	
E30	PEX_PERn29	CMLRn	SerDes	
E31	VDD10S	SPWR	Power	
E32	PEX_PERn30	CMLRn	SerDes	
E33	VDD10S	SPWR	Power	
E34	PEX_PERn31	CMLRn	SerDes	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
F1	VSS	GND	Ground	
F2	VSS	GND	Ground	
F3	N/C	***Reserved***	No Connect	
F4	VSS	GND	Ground	
F5	VDD10	CPWR	Power	
F30	VDD10A	APWR	Power	
F31	VSS	GND	Ground	
F32	VSS	GND	Ground	
F33	VDD10S	SPWR	Power	
F34	VSS	GND	Ground	
G1	STRAP_MODE_SEL0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_MODE_SEL[1:0]
G2	N/C	***Reserved***	No Connect	
G3	N/C	***Reserved***	No Connect	
G4	VSS	GND	Ground	
G5	VDD10	CPWR	Power	
G30	VDD10	CPWR	Power	
G31	VSS	GND	Ground	
G32	N/C	***Reserved***	No Connect	
G33	STRAP_TESTMODE1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_TESTMODE[3:0]
G34	STRAP_TESTMODE0	I	STRAP	
H1	PEX_PERST#	I	PEX Control	
H2	STRAP_MODE_SEL1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_MODE_SEL[1:0]
H3	N/C	***Reserved***	No Connect	
H4	N/C	***Reserved***	No Connect	
H5	VDD33	I/OPWR	Power	
H30	VSS	GND	Ground	
H31	VSS	GND	Ground	
H32	VDD33	I/OPWR	Power	
H33	STRAP_TESTMODE3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_TESTMODE[3:0]
H34	STRAP_TESTMODE2	I	STRAP	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
J1	PEX_NT_RESET#	O	PEX Control	
J2	JTAG_TCK	I, PU	JTAG	
J3	JTAG_TDO	O	JTAG	
J4	JTAG_TMS	I, PU	JTAG	
J5	VSS	GND	Ground	
J30	VDD10	CPWR	Power	
J31	VDD33	I/OPWR	Power	
J32	VDD33	I/OPWR	Power	
J33	HP_CLKEN10#	O	Hot Plug	
J34	N/C	***Reserved***	No Connect	
K1	HP_BUTTON1#	I, PU	Hot Plug	
K2	HP_CLKEN8#	O	Hot Plug	
K3	JTAG_TDI	I, PU	JTAG	
K4	JTAG_TRST#	I, PU	JTAG	
K5	VDD10	CPWR	Power	
K30	VDD33	I/OPWR	Power	
K31	VDD33	I/OPWR	Power	
K32	STRAP_NT_UPSTRM_PORTSEL0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_NT_UPSTRM_PORTSEL[3:0]
K33	HP_PWRLED10#	O	Hot Plug	
K34	N/C	***Reserved***	No Connect	
L1	HP_ATNLED1#	O	Hot Plug	
L2	HP_PWRLED8#	O	Hot Plug	
L3	N/C	***Reserved***	No Connect	
L4	N/C	***Reserved***	No Connect	
L5	VDD33	I/OPWR	Power	
L30	VSS	GND	Ground	
L31	STRAP_NT_UPSTRM_PORTSEL2	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_NT_UPSTRM_PORTSEL[3:0]
L32	STRAP_NT_UPSTRM_PORTSEL1	I	STRAP	
L33	HP_PERST10#	O	Hot Plug	
L34	N/C	***Reserved***	No Connect	
M1	HP_MRL1#	I, PU	Hot Plug	
M2	HP_PERST8#	O	Hot Plug	
M3	STRAP_UPSTRM_PORTSEL0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_UPSTRM_PORTSEL[3:0]
M4	STRAP_UPSTRM_PORTSEL2	I	STRAP	
M5	VDD10	CPWR	Power	
M30	VDD10	CPWR	Power	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
M31	STRAP_NT_UPSTRM_PORTSEL3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_NT_UPSTRM_PORTSEL[3:0]
M32	STRAP_STN1_PORTCFG0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN1_PORTCFG[3:0]
M33	HP_PRSNT10#	I, PU	Hot Plug	
M34	N/C	***Reserved***	No Connect	
N1	HP_PWRFLT1#	I, PU	Hot Plug	
N2	HP_PRSNT8#	I, PU	Hot Plug	
N3	STRAP_UPSTRM_PORTSEL1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_UPSTRM_PORTSEL[3:0]
N4	STRAP_UPSTRM_PORTSEL3	I	STRAP	
N5	VDD33	I/OPWR	Power	
N13	VSS_THERMAL	Thermal-GND	Ground	
N14	VSS_THERMAL	Thermal-GND	Ground	
N15	VSS_THERMAL	Thermal-GND	Ground	
N16	VSS_THERMAL	Thermal-GND	Ground	
N17	VSS_THERMAL	Thermal-GND	Ground	
N18	VSS_THERMAL	Thermal-GND	Ground	
N19	VSS_THERMAL	Thermal-GND	Ground	
N20	VSS_THERMAL	Thermal-GND	Ground	
N21	VSS_THERMAL	Thermal-GND	Ground	
N22	VSS_THERMAL	Thermal-GND	Ground	
N30	VDD33	I/OPWR	Power	
N31	STRAP_STN1_PORTCFG1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN1_PORTCFG[3:0]
N32	STRAP_STN1_PORTCFG2	I	STRAP	
N33	HP_PWREN10#	O	Hot Plug	
N34	N/C	***Reserved***	No Connect	
P1	HP_PWREN1#	O	Hot Plug	
P2	HP_PWREN8#	O	Hot Plug	
P3	PEX_LANE_GOOD0#	O	Lane Status	
P4	PEX_LANE_GOOD23#	O	Lane Status	
P5	VSS	GND	Ground	
P13	VSS_THERMAL	Thermal-GND	Ground	
P14	VSS_THERMAL	Thermal-GND	Ground	
P15	VSS_THERMAL	Thermal-GND	Ground	
P16	VSS_THERMAL	Thermal-GND	Ground	
P17	VSS_THERMAL	Thermal-GND	Ground	
P18	VSS_THERMAL	Thermal-GND	Ground	
P19	VSS_THERMAL	Thermal-GND	Ground	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
P20	VSS_THERMAL	Thermal-GND	Ground	
P21	VSS_THERMAL	Thermal-GND	Ground	
P22	VSS_THERMAL	Thermal-GND	Ground	
P30	VDD10	CPWR	Power	
P31	STRAP_STN1_PORTCFG3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN1_PORTCFG[3:0]
P32	VSS	GND	Ground	
P33	HP_PWRFLT10#	I, PU	Hot Plug	
P34	N/C	***Reserved***	No Connect	
R1	HP_PRSNT1#	I, PU	Hot Plug	
R2	HP_PWRFLT8#	I, PU	Hot Plug	
R3	PEX_LANE_GOOD1#	O	Lane Status	
R4	PEX_LANE_GOOD22#	O	Lane Status	
R5	VDD33	I/OPWR	Power	
R13	VSS_THERMAL	Thermal-GND	Ground	
R14	VSS_THERMAL	Thermal-GND	Ground	
R15	VSS_THERMAL	Thermal-GND	Ground	
R16	VSS_THERMAL	Thermal-GND	Ground	
R17	VSS_THERMAL	Thermal-GND	Ground	
R18	VSS_THERMAL	Thermal-GND	Ground	
R19	VSS_THERMAL	Thermal-GND	Ground	
R20	VSS_THERMAL	Thermal-GND	Ground	
R21	VSS_THERMAL	Thermal-GND	Ground	
R22	VSS_THERMAL	Thermal-GND	Ground	
R30	VSS	GND	Ground	
R31	PEX_LANE_GOOD24#	O	Lane Status	
R32	N/C	***Reserved***	No Connect	
R33	HP_MRL10#	I, PU	Hot Plug	
R34	N/C	***Reserved***	No Connect	
T1	HP_PERST1#	O	Hot Plug	
T2	HP_MRL8#	I, PU	Hot Plug	
T3	PEX_LANE_GOOD2#	O	Lane Status	
T4	PEX_LANE_GOOD21#	O	Lane Status	
T5	VDD10	CPWR	Power	
T13	VSS_THERMAL	Thermal-GND	Ground	
T14	VSS_THERMAL	Thermal-GND	Ground	
T15	VSS_THERMAL	Thermal-GND	Ground	
T16	VSS_THERMAL	Thermal-GND	Ground	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
T17	VSS_THERMAL	Thermal-GND	Ground	
T18	VSS_THERMAL	Thermal-GND	Ground	
T19	VSS_THERMAL	Thermal-GND	Ground	
T20	VSS_THERMAL	Thermal-GND	Ground	
T21	VSS_THERMAL	Thermal-GND	Ground	
T22	VSS_THERMAL	Thermal-GND	Ground	
T30	VDD10	CPWR	Power	
T31	PEX_LANE_GOOD25#	O	Lane Status	
T32	N/C	***Reserved***	No Connect	
T33	HP_ATNLED10#	O	Hot Plug	
T34	N/C	***Reserved***	No Connect	
U1	HP_PWRLED1#	O	Hot Plug	
U2	HP_ATNLED8#	O	Hot Plug	
U3	PEX_LANE_GOOD3#	O	Lane Status	
U4	PEX_LANE_GOOD20#	O	Lane Status	
U5	VDD33	I/OPWR	Power	
U13	VSS_THERMAL	Thermal-GND	Ground	
U14	VSS_THERMAL	Thermal-GND	Ground	
U15	VSS_THERMAL	Thermal-GND	Ground	
U16	VSS_THERMAL	Thermal-GND	Ground	
U17	VSS_THERMAL	Thermal-GND	Ground	
U18	VSS_THERMAL	Thermal-GND	Ground	
U19	VSS_THERMAL	Thermal-GND	Ground	
U20	VSS_THERMAL	Thermal-GND	Ground	
U21	VSS_THERMAL	Thermal-GND	Ground	
U22	VSS_THERMAL	Thermal-GND	Ground	
U30	VDD33	I/OPWR	Power	
U31	PEX_LANE_GOOD26#	O	Lane Status	
U32	N/C	***Reserved***	No Connect	
U33	HP_BUTTON10#	I, PU	Hot Plug	
U34	N/C	***Reserved***	No Connect	
V1	HP_CLKEN1#	O	Hot Plug	
V2	HP_BUTTON8#	I, PU	Hot Plug	
V3	PEX_LANE_GOOD4#	O	Lane Status	
V4	PEX_LANE_GOOD19#	O	Lane Status	
V5	VDD10	CPWR	Power	
V13	VSS_THERMAL	Thermal-GND	Ground	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
V14	VSS_THERMAL	Thermal-GND	Ground	
V15	VSS_THERMAL	Thermal-GND	Ground	
V16	VSS_THERMAL	Thermal-GND	Ground	
V17	VSS_THERMAL	Thermal-GND	Ground	
V18	VSS_THERMAL	Thermal-GND	Ground	
V19	VSS_THERMAL	Thermal-GND	Ground	
V20	VSS_THERMAL	Thermal-GND	Ground	
V21	VSS_THERMAL	Thermal-GND	Ground	
V22	VSS_THERMAL	Thermal-GND	Ground	
V30	VDD10	CPWR	Power	
V31	PEX_LANE_GOOD27#	O	Lane Status	
V32	N/C	***Reserved***	No Connect	
V33	HP_CLKEN11#	O	Hot Plug	
V34	N/C	***Reserved***	No Connect	
W1	HP_BUTTON0#	I, PU	Hot Plug	
W2	HP_CLKEN9#	O	Hot Plug	
W3	PEX_LANE_GOOD5#	O	Lane Status	
W4	PEX_LANE_GOOD18#	O	Lane Status	
W5	VSS	GND	Ground	
W13	VSS_THERMAL	Thermal-GND	Ground	
W14	VSS_THERMAL	Thermal-GND	Ground	
W15	VSS_THERMAL	Thermal-GND	Ground	
W16	VSS_THERMAL	Thermal-GND	Ground	
W17	VSS_THERMAL	Thermal-GND	Ground	
W18	VSS_THERMAL	Thermal-GND	Ground	
W19	VSS_THERMAL	Thermal-GND	Ground	
W20	VSS_THERMAL	Thermal-GND	Ground	
W21	VSS_THERMAL	Thermal-GND	Ground	
W22	VSS_THERMAL	Thermal-GND	Ground	
W30	VSS	GND	Ground	
W31	PEX_LANE_GOOD28#	O	Lane Status	
W32	N/C	***Reserved***	No Connect	
W33	HP_PWRLED11#	O	Hot Plug	
W34	N/C	***Reserved***	No Connect	
Y1	HP_ATNLED0#	O	Hot Plug	
Y2	HP_PWRLED9#	O	Hot Plug	
Y3	PEX_LANE_GOOD6#	O	Lane Status	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
Y4	PEX_LANE_GOOD17#	O	Lane Status	
Y5	VDD33	I/OPWR	Power	
Y13	VSS_THERMAL	Thermal-GND	Ground	
Y14	VSS_THERMAL	Thermal-GND	Ground	
Y15	VSS_THERMAL	Thermal-GND	Ground	
Y16	VSS_THERMAL	Thermal-GND	Ground	
Y17	VSS_THERMAL	Thermal-GND	Ground	
Y18	VSS_THERMAL	Thermal-GND	Ground	
Y19	VSS_THERMAL	Thermal-GND	Ground	
Y20	VSS_THERMAL	Thermal-GND	Ground	
Y21	VSS_THERMAL	Thermal-GND	Ground	
Y22	VSS_THERMAL	Thermal-GND	Ground	
Y30	VDD33	I/OPWR	Power	
Y31	PEX_LANE_GOOD29#	O	Lane Status	
Y32	N/C	***Reserved***	No Connect	
Y33	HP_PERST11#	O	Hot Plug	
Y34	N/C	***Reserved***	No Connect	
AA1	HP_MRL0#	I, PU	Hot Plug	
AA2	HP_PERST9#	O	Hot Plug	
AA3	PEX_LANE_GOOD7#	O	Lane Status	
AA4	PEX_LANE_GOOD16#	O	Lane Status	
AA5	VDD10	CPWR	Power	
AA13	VSS_THERMAL	Thermal-GND	Ground	
AA14	VSS_THERMAL	Thermal-GND	Ground	
AA15	VSS_THERMAL	Thermal-GND	Ground	
AA16	VSS_THERMAL	Thermal-GND	Ground	
AA17	VSS_THERMAL	Thermal-GND	Ground	
AA18	VSS_THERMAL	Thermal-GND	Ground	
AA19	VSS_THERMAL	Thermal-GND	Ground	
AA20	VSS_THERMAL	Thermal-GND	Ground	
AA21	VSS_THERMAL	Thermal-GND	Ground	
AA22	VSS_THERMAL	Thermal-GND	Ground	
AA30	VDD10	CPWR	Power	
AA31	PEX_LANE_GOOD30#	O	Lane Status	
AA32	N/C	***Reserved***	No Connect	
AA33	HP_PRSNT11#	I, PU	Hot Plug	
AA34	N/C	***Reserved***	No Connect	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AB1	HP_PWRFLT0#	I, PU	Hot Plug	
AB2	HP_PRSNT9#	I, PU	Hot Plug	
AB3	N/C	***Reserved***	No Connect	
AB4	N/C	***Reserved***	No Connect	
AB5	VDD33	I/OPWR	Power	
AB13	VSS_THERMAL	Thermal-GND	Ground	
AB14	VSS_THERMAL	Thermal-GND	Ground	
AB15	VSS_THERMAL	Thermal-GND	Ground	
AB16	VSS_THERMAL	Thermal-GND	Ground	
AB17	VSS_THERMAL	Thermal-GND	Ground	
AB18	VSS_THERMAL	Thermal-GND	Ground	
AB19	VSS_THERMAL	Thermal-GND	Ground	
AB20	VSS_THERMAL	Thermal-GND	Ground	
AB21	VSS_THERMAL	Thermal-GND	Ground	
AB22	VSS_THERMAL	Thermal-GND	Ground	
AB30	VDD33	I/OPWR	Power	
AB31	PEX_LANE_GOOD31#	O	Lane Status	
AB32	N/C	***Reserved***	No Connect	
AB33	HP_PWREN11#	O	Hot Plug	
AB34	N/C	***Reserved***	No Connect	
AC1	HP_PWREN0#	O	Hot Plug	
AC2	HP_PWREN9#	O	Hot Plug	
AC3	N/C	***Reserved***	No Connect	
AC4	N/C	***Reserved***	No Connect	
AC5	VDD10	CPWR	Power	
AC30	VDD10	CPWR	Power	
AC31	STRAP_STN0_PORTCFG3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN0_PORTCFG[4:0]
AC32	STRAP_STN0_PORTCFG4	I	STRAP	
AC33	HP_PWRFLT11#	I, PU	Hot Plug	
AC34	N/C	***Reserved***	No Connect	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AD1	HP_PRSNT0#	I, PU	Hot Plug	
AD2	HP_PWRFLT9#	I, PU	Hot Plug	
AD3	N/C	***Reserved***	No Connect	
AD4	N/C	***Reserved***	No Connect	
AD5	VSS	GND	Ground	
AD30	VSS	GND	Ground	
AD31	STRAP_STN0_PORTCFG1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN0_PORTCFG[4:0]
AD32	STRAP_STN0_PORTCFG2	I	STRAP	
AD33	HP_MRL11#	I, PU	Hot Plug	
AD34	N/C	***Reserved***	No Connect	
AE1	HP_PERST0#	O	Hot Plug	
AE2	HP_MRL9#	I, PU	Hot Plug	
AE3	N/C	***Reserved***	No Connect	
AE4	N/C	***Reserved***	No Connect	
AE5	VDD10	CPWR	Power	
AE30	VDD10	CPWR	Power	
AE31	N/C	***Reserved***	No Connect	
AE32	STRAP_STN0_PORTCFG0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN0_PORTCFG[4:0]
AE33	HP_ATNLED11#	O	Hot Plug	
AE34	N/C	***Reserved***	No Connect	
AF1	HP_PWRLED0#	O	Hot Plug	
AF2	HP_ATNLED9#	O	Hot Plug	
AF3	N/C	***Reserved***	No Connect	
AF4	N/C	***Reserved***	No Connect	
AF5	VDD33	I/OPWR	Power	
AF30	VDD33	I/OPWR	Power	
AF31	N/C	***Reserved***	No Connect	
AF32	N/C	***Reserved***	No Connect	
AF33	HP_BUTTON11#	I, PU	Hot Plug	
AF34	N/C	***Reserved***	No Connect	
AG1	HP_CLKEN0#	O	Hot Plug	
AG2	HP_BUTTON9#	I, PU	Hot Plug	
AG3	N/C	***Reserved***	No Connect	
AG4	VSS	GND	Ground	
AG5	VDD10	CPWR	Power	
AG30	VDD10	CPWR	Power	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AG31	VDD33	I/OPWR	Power	
AG32	EE_CS#	O	Serial EEPROM	
AG33	EE_SK	O	Serial EEPROM	
AG34	EE_DO	I, PU	Serial EEPROM	Connected to data output of serial EEPROM
AH1	VDD33	I/OPWR	Power	
AH2	STRAP_FACTORY_TEST1#	I	STRAP	Strapping Ball – tie High
AH3	N/C	***Reserved***	No Connect	
AH4	VSSA_PLL	PLL_GND	Ground	Analog GND for PLL circuit
AH5	VDD33A	PLLPWR	Power	
AH30	VDD33	I/OPWR	Power	
AH31	VSS	GND	Ground	
AH32	N/C	***Reserved***	No Connect	
AH33	EE_PR#	I	Serial EEPROM	
AH34	EE_DI	O	Serial EEPROM	Connected to data input of serial EEPROM
AJ1	VSS	GND	Ground	
AJ2	VSS	GND	Ground	
AJ3	VSS	GND	Ground	
AJ4	VSS	GND	Ground	
AJ5	VDD10A	APWR	Power	
AJ30	VDD10	CPWR	Power	
AJ31	VSS	GND	Ground	
AJ32	VSS	GND	Ground	
AJ33	VDD10S	SPWR	Power	
AJ34	VSS	GND	Ground	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AK1	VSS	GND	Ground	
AK2	VSS	GND	Ground	
AK3	VSS	GND	Ground	
AK4	PEX_PERn0	CMLRn	SerDes	
AK5	VDD10S	SPWR	Power	
AK6	PEX_PERn1	CMLRn	SerDes	
AK7	VDD10A	APWR	Power	
AK8	PEX_PERn2	CMLRn	SerDes	
AK9	VDD10	CPWR	Power	
AK10	PEX_PERn3	CMLRn	SerDes	
AK11	VDD10	CPWR	Power	
AK12	PEX_PERn4	CMLRn	SerDes	
AK13	VDD10	CPWR	Power	
AK14	PEX_PERn5	CMLRn	SerDes	
AK15	VDD10A	APWR	Power	
AK16	PEX_PERn6	CMLRn	SerDes	
AK17	VDD10	CPWR	Power	
AK18	PEX_PERn7	CMLRn	SerDes	
AK19	VDD10	CPWR	Power	
AK20	N/C	***Reserved***	No Connect	
AK21	VDD10	CPWR	Power	
AK22	N/C	***Reserved***	No Connect	
AK23	VDD10	CPWR	Power	
AK24	N/C	***Reserved***	No Connect	
AK25	VDD10	CPWR	Power	
AK26	N/C	***Reserved***	No Connect	
AK27	VDD10	CPWR	Power	
AK28	N/C	***Reserved***	No Connect	
AK29	VDD10	CPWR	Power	
AK30	N/C	***Reserved***	No Connect	
AK31	VDD10S	SPWR	Power	
AK32	N/C	***Reserved***	No Connect	
AK33	VDD10S	SPWR	Power	
AK34	N/C	***Reserved***	No Connect	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AL1	PEX_REFCLKn	CMLCLKn	SerDes / Clock	
AL2	PEX_REFCLKp	CMLCLKp	SerDes / Clock	
AL3	VSS	GND	Ground	
AL4	PEX_PERp0	CMLRp	SerDes	
AL5	VSS	GND	Ground	
AL6	PEX_PERp1	CMLRp	SerDes	
AL7	VSS	GND	Ground	
AL8	PEX_PERp2	CMLRp	SerDes	
AL9	VSS	GND	Ground	
AL10	PEX_PERp3	CMLRp	SerDes	
AL11	VSS	GND	Ground	
AL12	PEX_PERp4	CMLRp	SerDes	
AL13	VSS	GND	Ground	
AL14	PEX_PERp5	CMLRp	SerDes	
AL15	VSS	GND	Ground	
AL16	PEX_PERp6	CMLRp	SerDes	
AL17	VSS	GND	Ground	
AL18	PEX_PERp7	CMLRp	SerDes	
AL19	VSS	GND	Ground	
AL20	N/C	***Reserved***	No Connect	
AL21	VSS	GND	Ground	
AL22	N/C	***Reserved***	No Connect	
AL23	VSS	GND	Ground	
AL24	N/C	***Reserved***	No Connect	
AL25	VSS	GND	Ground	
AL26	N/C	***Reserved***	No Connect	
AL27	VSS	GND	Ground	
AL28	N/C	***Reserved***	No Connect	
AL29	VSS	GND	Ground	
AL30	N/C	***Reserved***	No Connect	
AL31	VSS	GND	Ground	
AL32	N/C	***Reserved***	No Connect	
AL33	VSS	GND	Ground	
AL34	N/C	***Reserved***	No Connect	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AM1	VSS	GND	Ground	
AM2	VSS	GND	Ground	
AM3	VDD10S	SPWR	Power	
AM4	VSS	GND	Ground	
AM5	VSS	GND	Ground	
AM6	VSS	GND	Ground	
AM7	VDD10S	SPWR	Power	
AM8	VSS	GND	Ground	
AM9	VSS	GND	Ground	
AM10	VSS	GND	Ground	
AM11	VDD10S	SPWR	Power	
AM12	VSS	GND	Ground	
AM13	VSS	GND	Ground	
AM14	VSS	GND	Ground	
AM15	VDD10S	SPWR	Power	
AM16	VSS	GND	Ground	
AM17	VSS	GND	Ground	
AM18	VSS	GND	Ground	
AM19	VDD10S	SPWR	Power	
AM20	VSS	GND	Ground	
AM21	VSS	GND	Ground	
AM22	VSS	GND	Ground	
AM23	VDD10S	SPWR	Power	
AM24	VSS	GND	Ground	
AM25	VSS	GND	Ground	
AM26	VSS	GND	Ground	
AM27	VDD10S	SPWR	Power	
AM28	VSS	GND	Ground	
AM29	VSS	GND	Ground	
AM30	VSS	GND	Ground	
AM31	VDD10S	SPWR	Power	
AM32	VSS	GND	Ground	
AM33	VSS	GND	Ground	
AM34	VSS	GND	Ground	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AN1	N/C	***Reserved***	No Connect	
AN2	N/C	***Reserved***	No Connect	
AN3	VDD10S	SPWR	Power	
AN4	PEX_PETp0	CMLTp	SerDes	
AN5	VDD10S	SPWR	Power	
AN6	PEX_PETp1	CMLTp	SerDes	
AN7	VDD10S	SPWR	Power	
AN8	PEX_PETp2	CMLTp	SerDes	
AN9	VDD10S	SPWR	Power	
AN10	PEX_PETp3	CMLTp	SerDes	
AN11	VDD10S	SPWR	Power	
AN12	PEX_PETp4	CMLTp	SerDes	
AN13	VDD10S	SPWR	Power	
AN14	PEX_PETp5	CMLTp	SerDes	
AN15	VDD10S	SPWR	Power	
AN16	PEX_PETp6	CMLTp	SerDes	
AN17	VDD10S	SPWR	Power	
AN18	PEX_PETp7	CMLTp	SerDes	
AN19	VDD10S	SPWR	Power	
AN20	N/C	***Reserved***	No Connect	
AN21	VDD10S	SPWR	Power	
AN22	N/C	***Reserved***	No Connect	
AN23	VDD10S	SPWR	Power	
AN24	N/C	***Reserved***	No Connect	
AN25	VDD10S	SPWR	Power	
AN26	N/C	***Reserved***	No Connect	
AN27	VDD10S	SPWR	Power	
AN28	N/C	***Reserved***	No Connect	
AN29	VDD10S	SPWR	Power	
AN30	N/C	***Reserved***	No Connect	
AN31	VDD10S	SPWR	Power	
AN32	N/C	***Reserved***	No Connect	
AN33	VDD10S	SPWR	Power	
AN34	N/C	***Reserved***	No Connect	

Table 3-18. PEX 8524VAA/BB/BC Switch Ball Assignments by Number – 680-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AP1	N/C	***Reserved***	No Connect	
AP2	N/C	***Reserved***	No Connect	
AP3	VSS	GND	Ground	
AP4	PEX_PETn0	CMLTn	SerDes	
AP5	VTT_PEX0	Supply	Power	
AP6	PEX_PETn1	CMLTn	SerDes	
AP7	VSS	GND	Ground	
AP8	PEX_PETn2	CMLTn	SerDes	
AP9	VTT_PEX1	Supply	Power	
AP10	PEX_PETn3	CMLTn	SerDes	
AP11	VSS	GND	Ground	
AP12	PEX_PETn4	CMLTn	SerDes	
AP13	VTT_PEX2	Supply	Power	
AP14	PEX_PETn5	CMLTn	SerDes	
AP15	VSS	GND	Ground	
AP16	PEX_PETn6	CMLTn	SerDes	
AP17	VTT_PEX3	Supply	Power	
AP18	PEX_PETn7	CMLTn	SerDes	
AP19	VSS	GND	Ground	
AP20	N/C	***Reserved***	No Connect	
AP21	VTT_PEX4	Supply	Power	
AP22	N/C	***Reserved***	No Connect	
AP23	VSS	GND	Ground	
AP24	N/C	***Reserved***	No Connect	
AP25	VTT_PEX5	Supply	Power	
AP26	N/C	***Reserved***	No Connect	
AP27	VSS	GND	Ground	
AP28	N/C	***Reserved***	No Connect	
AP29	VTT_PEX6	Supply	Power	
AP30	N/C	***Reserved***	No Connect	
AP31	VSS	GND	Ground	
AP32	N/C	***Reserved***	No Connect	
AP33	VTT_PEX7	Supply	Power	
AP34	N/C	***Reserved***	No Connect	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
A1	VSS	GND	Ground	
A2	PEX_PETn16	CMLTn	SerDes	
A3	VSS	GND	Ground	
A4	PEX_PETn17	CMLTn	SerDes	
A5	VSS	GND	Ground	
A6	PEX_PETn18	CMLTn	SerDes	
A7	VDD10S	SPWR	Power	
A8	PEX_PETn19	CMLTn	SerDes	
A9	VSS	GND	Ground	
A10	PEX_PETn20	CMLTn	SerDes	
A11	VDD10S	SPWR	Power	
A12	PEX_PETn21	CMLTn	SerDes	
A13	VSS	GND	Ground	
A14	PEX_PETn22	CMLTn	SerDes	
A15	VDD10S	SPWR	Power	
A16	PEX_PETn23	CMLTn	SerDes	
A17	VSS	GND	Ground	
A18	PEX_PETn24	CMLTn	SerDes	
A19	VDD10S	SPWR	Power	
A20	PEX_PETn25	CMLTn	SerDes	
A21	VSS	GND	Ground	
A22	PEX_PETn26	CMLTn	SerDes	
A23	VDD10S	SPWR	Power	
A24	PEX_PETn27	CMLTn	SerDes	
A25	VSS	GND	Ground	
A26	PEX_PETn28	CMLTn	SerDes	
A27	VDD10S	SPWR	Power	
A28	PEX_PETn29	CMLTn	SerDes	
A29	VSS	GND	Ground	
A30	PEX_PETn30	CMLTn	SerDes	
B1	VDD10S	SPWR	Power	
B2	PEX_PETp16	CMLTp	SerDes	
B3	VDD10S	SPWR	Power	
B4	PEX_PETp17	CMLTp	SerDes	
B5	VDD10S	SPWR	Power	
B6	PEX_PETp18	CMLTp	SerDes	
B7	VSS	GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
B8	PEX_PETp19	CMLTp	SerDes	
B9	VDD10S	SPWR	Power	
B10	PEX_PETp20	CMLTp	SerDes	
B11	VSS	GND	Ground	
B12	PEX_PETp21	CMLTp	SerDes	
B13	VDD10S	SPWR	Power	
B14	PEX_PETp22	CMLTp	SerDes	
B15	VSS	GND	Ground	
B16	PEX_PETp23	CMLTp	SerDes	
B17	VDD10S	SPWR	Power	
B18	PEX_PETp24	CMLTp	SerDes	
B19	VSS	GND	Ground	
B20	PEX_PETp25	CMLTp	SerDes	
B21	VDD10S	SPWR	Power	
B22	PEX_PETp26	CMLTp	SerDes	
B23	VSS	GND	Ground	
B24	PEX_PETp27	CMLTp	SerDes	
B25	VDD10S	SPWR	Power	
B26	PEX_PETp28	CMLTp	SerDes	
B27	VSS	GND	Ground	
B28	PEX_PETp29	CMLTp	SerDes	
B29	VDD10S	SPWR	Power	
B30	PEX_PETp30	CMLTp	SerDes	
C1	VSS	GND	Ground	
C2	VSS	GND	Ground	
C3	VDD10S	SPWR	Power	
C4	VSS	GND	Ground	
C5	VDD10S	SPWR	Power	
C6	VSS	GND	Ground	
C7	VDD10S	SPWR	Power	
C8	VSS	GND	Ground	
C9	VSS	GND	Ground	
C10	VSS	GND	Ground	
C11	VDD10S	SPWR	Power	
C12	VSS	GND	Ground	
C13	VSS	GND	Ground	
C14	VSS	GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
C15	VDD10S	SPWR	Power	
C16	VSS	GND	Ground	
C17	VSS	GND	Ground	
C18	VSS	GND	Ground	
C19	VDD10S	SPWR	Power	
C20	VSS	GND	Ground	
C21	VSS	GND	Ground	
C22	VSS	GND	Ground	
C23	VSS	GND	Ground	
C24	VSS	GND	Ground	
C25	VSS	GND	Ground	
C26	VSS	GND	Ground	
C27	VDD10S	SPWR	Power	
C28	VSS	GND	Ground	
C29	VSS	GND	Ground	
C30	VSS	GND	Ground	
D1	VDD10S	SPWR	Power	
D2	PEX_PERp16	CMLRp	SerDes	
D3	VSS	GND	Ground	
D4	PEX_PERp17	CMLRp	SerDes	
D5	VSS	GND	Ground	
D6	PEX_PERp18	CMLRp	SerDes	
D7	VSS	GND	Ground	
D8	PEX_PERp19	CMLRp	SerDes	
D9	VSS	GND	Ground	
D10	PEX_PERp20	CMLRp	SerDes	
D11	VSS	GND	Ground	
D12	PEX_PERp21	CMLRp	SerDes	
D13	VSS	GND	Ground	
D14	PEX_PERp22	CMLRp	SerDes	
D15	VSS	GND	Ground	
D16	PEX_PERp23	CMLRp	SerDes	
D17	VSS	GND	Ground	
D18	PEX_PERp24	CMLRp	SerDes	
D19	VSS	GND	Ground	
D20	PEX_PERp25	CMLRp	SerDes	
D21	VSS	GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
D22	PEX_PERp26	CMLRp	SerDes	
D23	VDD10S	SPWR	Power	
D24	PEX_PERp27	CMLRp	SerDes	
D25	VSS	GND	Ground	
D26	PEX_PERp28	CMLRp	SerDes	
D27	VSS	GND	Ground	
D28	PEX_PERp29	CMLRp	SerDes	
D29	VSS	GND	Ground	
D30	PEX_PERp30	CMLRp	SerDes	
E1	VSS	GND	Ground	
E2	PEX_PERn16	CMLRn	SerDes	
E3	VDD10S	SPWR	Power	
E4	PEX_PERn17	CMLRn	SerDes	
E5	VDD10S	SPWR	Power	
E6	PEX_PERn18	CMLRn	SerDes	
E7	VDD10A	APWR	Power	
E8	PEX_PERn19	CMLRn	SerDes	
E9	VTT_PEX9	Supply	Power	
E10	PEX_PERn20	CMLRn	SerDes	
E11	VTT_PEX10	Supply	Power	
E12	PEX_PERn21	CMLRn	SerDes	
E13	VDD10S	SPWR	Power	
E14	PEX_PERn22	CMLRn	SerDes	
E15	VDD10A	APWR	Power	
E16	PEX_PERn23	CMLRn	SerDes	
E17	VTT_PEX11	Supply	Power	
E18	PEX_PERn24	CMLRn	SerDes	
E19	VTT_PEX12	Supply	Power	
E20	PEX_PERn25	CMLRn	SerDes	
E21	VTT_PEX13	Supply	Power	
E22	PEX_PERn26	CMLRn	SerDes	
E23	VDD10A	APWR	Power	
E24	PEX_PERn27	CMLRn	SerDes	
E25	VTT_PEX14	Supply	Power	
E26	PEX_PERn28	CMLRn	SerDes	
E27	VDD10S	SPWR	Power	
E28	PEX_PERn29	CMLRn	SerDes	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
E29	VDD10S	SPWR	Power	
E30	PEX_PERn30	CMLRn	SerDes	
F1	VSS	GND	Ground	
F2	VDD10S	SPWR	Power	
F3	VSS	GND	Ground	
F4	VTT_PEX8	Supply	Power	
F5	VSS	GND	Ground	
F26	VDD10A	APWR	Power	
F27	VSS	GND	Ground	
F28	VDD10S	SPWR	Power	
F29	VSS	GND	Ground	
F30	VDD10S	SPWR	Power	
G1	STRAP_MODE_SEL0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_MODE_SEL[1:0]
G2	STRAP_MODE_SEL1	I	STRAP	
G3	PEX_PERST#	I	PEX Control	
G4	JTAG_TMS	I, PU	JTAG	
G5	VSS	GND	Ground	
G26	PEX_PERn31	CMLRn	SerDes	
G27	PEX_PERp31	CMLRp	SerDes	
G28	VSS	GND	Ground	
G29	PEX_PETp31	CMLTp	SerDes	
G30	PEX_PETn31	CMLTn	SerDes	
H1	JTAG_TDO	O	JTAG	
H2	JTAG_TCK	I, PU	JTAG	
H3	PEX_NT_RESET#	O	PEX Control	
H4	JTAG_TRST#	I, PU	JTAG	
H5	VDD33	I/OPWR	Power	
H26	VTT_PEX15	Supply	Power	
H27	VDD10S	SPWR	Power	
H28	VSS	GND	Ground	
H29	VDD10S	SPWR	Power	
H30	VSS	GND	Ground	
J1	JTAG_TDI	I, PU	JTAG	
J2	HP_CLKEN8#	O	Hot Plug	
J3	HP_BUTTON1#	I, PU	Hot Plug	
J4	HP_PWRLED8#	O	Hot Plug	
J5	VSS	GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
J26	VDD33	I/OPWR	Power	
J27	STRAP_TESTMODE2	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_TESTMODE[3:0]
J28	STRAP_TESTMODE3	I	STRAP	
J29	STRAP_TESTMODE0	I	STRAP	
J30	STRAP_TESTMODE1	I	STRAP	
K1	HP_ATNLED1#	O	Hot Plug	
K2	STRAP_UPSTRM_PORTSEL2	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_UPSTRM_PORTSEL[3:0]
K3	STRAP_UPSTRM_PORTSEL0	I	STRAP	
K4	HP_PERST8#	O	Hot Plug	
K5	VDD33	I/OPWR	Power	
K10	VDD10	CPWR	Power	
K11	VDD10	CPWR	Power	
K12	VDD10	CPWR	Power	
K13	VDD10	CPWR	Power	
K14	VDD10	CPWR	Power	
K15	VDD10	CPWR	Power	
K16	VDD10	CPWR	Power	
K17	VDD10	CPWR	Power	
K18	VDD10	CPWR	Power	
K19	VDD10	CPWR	Power	
K20	VDD10	CPWR	Power	
K21	VDD10	CPWR	Power	
K26	VSS	GND	Ground	
K27	HP_PWRLED10#	O	Hot Plug	
K28	STRAP_NT_UPSTRM_PORTSEL0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_NT_UPSTRM_PORTSEL[3:0]
K29	N/C	***Reserved***	No Connect	
K30	HP_CLKEN10#	O	Hot Plug	
L1	HP_MRL1#	I, PU	Hot Plug	
L2	STRAP_UPSTRM_PORTSEL3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_UPSTRM_PORTSEL[3:0]
L3	STRAP_UPSTRM_PORTSEL1	I	STRAP	
L4	HP_PRSNT8#	I, PU	Hot Plug	
L5	VSS	GND	Ground	
L10	VDD10	CPWR	Power	
L11	VSS_THERMAL	Thermal-GND	Ground	
L12	VSS_THERMAL	Thermal-GND	Ground	
L13	VSS_THERMAL	Thermal-GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
L14	VSS_THERMAL	Thermal-GND	Ground	
L15	VSS_THERMAL	Thermal-GND	Ground	
L16	VSS_THERMAL	Thermal-GND	Ground	
L17	VSS_THERMAL	Thermal-GND	Ground	
L18	VSS_THERMAL	Thermal-GND	Ground	
L19	VSS_THERMAL	Thermal-GND	Ground	
L20	VSS_THERMAL	Thermal-GND	Ground	
L21	VDD10	CPWR	Power	
L26	VDD33	I/OPWR	Power	
L27	HP_PERST10#	O	Hot Plug	
L28	STRAP_NT_UPSTRM_PORTSEL1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_NT_UPSTRM_PORTSEL[3:0]
L29	STRAP_NT_UPSTRM_PORTSEL2	I	STRAP	
L30	N/C	***Reserved***	No Connect	
M1	HP_PWRFLT1#	I, PU	Hot Plug	
M2	PEX_LANE_GOOD23#	O	Lane Status	
M3	PEX_LANE_GOOD0#	O	Lane Status	
M4	HP_PWREN8#	O	Hot Plug	
M5	VDD33	I/OPWR	Power	
M10	VDD10	CPWR	Power	
M11	VSS_THERMAL	Thermal-GND	Ground	
M12	VSS_THERMAL	Thermal-GND	Ground	
M13	VSS_THERMAL	Thermal-GND	Ground	
M14	VSS_THERMAL	Thermal-GND	Ground	
M15	VSS_THERMAL	Thermal-GND	Ground	
M16	VSS_THERMAL	Thermal-GND	Ground	
M17	VSS_THERMAL	Thermal-GND	Ground	
M18	VSS_THERMAL	Thermal-GND	Ground	
M19	VSS_THERMAL	Thermal-GND	Ground	
M20	VSS_THERMAL	Thermal-GND	Ground	
M21	VDD10	CPWR	Power	
M26	VSS	GND	Ground	
M27	HP_PRSNT10#	I, PU	Hot Plug	
M28	STRAP_STN1_PORTCFG0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN1_PORTCFG[3:0]
M29	STRAP_NT_UPSTRM_PORTSEL3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_NT_UPSTRM_PORTSEL[3:0]
M30	N/C	***Reserved***	No Connect	
N1	HP_PWREN1#	O	Hot Plug	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
N2	PEX_LANE_GOOD22#	O	Lane Status	
N3	PEX_LANE_GOOD1#	O	Lane Status	
N4	HP_PWRFLT8#	I, PU	Hot Plug	
N5	VSS	GND	Ground	
N10	VDD10	CPWR	Power	
N11	VSS_THERMAL	Thermal-GND	Ground	
N12	VSS_THERMAL	Thermal-GND	Ground	
N13	VSS_THERMAL	Thermal-GND	Ground	
N14	VSS_THERMAL	Thermal-GND	Ground	
N15	VSS_THERMAL	Thermal-GND	Ground	
N16	VSS_THERMAL	Thermal-GND	Ground	
N17	VSS_THERMAL	Thermal-GND	Ground	
N18	VSS_THERMAL	Thermal-GND	Ground	
N19	VSS_THERMAL	Thermal-GND	Ground	
N20	VSS_THERMAL	Thermal-GND	Ground	
N21	VDD10	CPWR	Power	
N26	VDD33	I/OPWR	Power	
N27	HP_PWREN10#	O	Hot Plug	
N28	STRAP_STN1_PORTCFG2	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN1_PORTCFG[3:0]
N29	STRAP_STN1_PORTCFG1	I	STRAP	
N30	N/C	***Reserved***	No Connect	
P1	HP_PRSNT1#	I, PU	Hot Plug	
P2	PEX_LANE_GOOD2#	O	Lane Status	
P3	HP_MRL8#	I, PU	Hot Plug	
P4	HP_PERST1#	O	Hot Plug	
P5	VDD33	I/OPWR	Power	
P10	VDD10	CPWR	Power	
P11	VSS_THERMAL	Thermal-GND	Ground	
P12	VSS_THERMAL	Thermal-GND	Ground	
P13	VSS_THERMAL	Thermal-GND	Ground	
P14	VSS_THERMAL	Thermal-GND	Ground	
P15	VSS_THERMAL	Thermal-GND	Ground	
P16	VSS_THERMAL	Thermal-GND	Ground	
P17	VSS_THERMAL	Thermal-GND	Ground	
P18	VSS_THERMAL	Thermal-GND	Ground	
P19	VSS_THERMAL	Thermal-GND	Ground	
P20	VSS_THERMAL	Thermal-GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
P21	VDD10	CPWR	Power	
P26	VSS	GND	Ground	
P27	N/C	***Reserved***	No Connect	
P28	HP_PWRFLT10#	I, PU	Hot Plug	
P29	STRAP_STN1_PORTCFG3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN1_PORTCFG[3:0]
P30	N/C	***Reserved***	No Connect	
R1	PEX_LANE_GOOD20#	O	Lane Status	
R2	PEX_LANE_GOOD3#	O	Lane Status	
R3	HP_ATNLED8#	O	Hot Plug	
R4	HP_PWRLED1#	O	Hot Plug	
R5	VSS	GND	Ground	
R10	VDD10	CPWR	Power	
R11	VSS_THERMAL	Thermal-GND	Ground	
R12	VSS_THERMAL	Thermal-GND	Ground	
R13	VSS_THERMAL	Thermal-GND	Ground	
R14	VSS_THERMAL	Thermal-GND	Ground	
R15	VSS_THERMAL	Thermal-GND	Ground	
R16	VSS_THERMAL	Thermal-GND	Ground	
R17	VSS_THERMAL	Thermal-GND	Ground	
R18	VSS_THERMAL	Thermal-GND	Ground	
R19	VSS_THERMAL	Thermal-GND	Ground	
R20	VSS_THERMAL	Thermal-GND	Ground	
R21	VDD10	CPWR	Power	
R26	VDD33	I/OPWR	Power	
R27	N/C	***Reserved***	No Connect	
R28	HP_MRL10#	I, PU	Hot Plug	
R29	N/C	***Reserved***	No Connect	
R30	PEX_LANE_GOOD24#	O	Lane Status	
T1	PEX_LANE_GOOD4#	O	Lane Status	
T2	HP_BUTTON8#	I, PU	Hot Plug	
T3	HP_CLKEN1#	O	Hot Plug	
T4	HP_BUTTON0#	I, PU	Hot Plug	
T5	VDD33	I/OPWR	Power	
T10	VDD10	CPWR	Power	
T11	VSS_THERMAL	Thermal-GND	Ground	
T12	VSS_THERMAL	Thermal-GND	Ground	
T13	VSS_THERMAL	Thermal-GND	Ground	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
T14	VSS_THERMAL	Thermal-GND	Ground	
T15	VSS_THERMAL	Thermal-GND	Ground	
T16	VSS_THERMAL	Thermal-GND	Ground	
T17	VSS_THERMAL	Thermal-GND	Ground	
T18	VSS_THERMAL	Thermal-GND	Ground	
T19	VSS_THERMAL	Thermal-GND	Ground	
T20	VSS_THERMAL	Thermal-GND	Ground	
T21	VDD10	CPWR	Power	
T26	VSS	GND	Ground	
T27	N/C	***Reserved***	No Connect	
T28	HP_ATNLED10#	O	Hot Plug	
T29	N/C	***Reserved***	No Connect	
T30	PEX_LANE_GOOD25#	O	Lane Status	
U1	HP_CLKEN9#	O	Hot Plug	
U2	PEX_LANE_GOOD5#	O	Lane Status	
U3	PEX_LANE_GOOD18#	O	Lane Status	
U4	HP_ATNLED0#	O	Hot Plug	
U5	VSS	GND	Ground	
U10	VDD10	CPWR	Power	
U11	VSS_THERMAL	Thermal-GND	Ground	
U12	VSS_THERMAL	Thermal-GND	Ground	
U13	VSS_THERMAL	Thermal-GND	Ground	
U14	VSS_THERMAL	Thermal-GND	Ground	
U15	VSS_THERMAL	Thermal-GND	Ground	
U16	VSS_THERMAL	Thermal-GND	Ground	
U17	VSS_THERMAL	Thermal-GND	Ground	
U18	VSS_THERMAL	Thermal-GND	Ground	
U19	VSS_THERMAL	Thermal-GND	Ground	
U20	VSS_THERMAL	Thermal-GND	Ground	
U21	VDD10	CPWR	Power	
U26	VDD33	I/OPWR	Power	
U27	N/C	***Reserved***	No Connect	
U28	HP_BUTTON10#	I, PU	Hot Plug	
U29	N/C	***Reserved***	No Connect	
U30	PEX_LANE_GOOD26#	O	Lane Status	
V1	HP_PWRLED9#	O	Hot Plug	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
V2	PEX_LANE_GOOD6#	O	Lane Status	
V3	HP_MRL0#	I, PU	Hot Plug	
V4	HP_PERST9#	O	Hot Plug	
V5	VDD33	I/OPWR	Power	
V10	VDD10	CPWR	Power	
V11	VSS_THERMAL	Thermal-GND	Ground	
V12	VSS_THERMAL	Thermal-GND	Ground	
V13	VSS_THERMAL	Thermal-GND	Ground	
V14	VSS_THERMAL	Thermal-GND	Ground	
V15	VSS_THERMAL	Thermal-GND	Ground	
V16	VSS_THERMAL	Thermal-GND	Ground	
V17	VSS_THERMAL	Thermal-GND	Ground	
V18	VSS_THERMAL	Thermal-GND	Ground	
V19	VSS_THERMAL	Thermal-GND	Ground	
V20	VSS_THERMAL	Thermal-GND	Ground	
V21	VDD10	CPWR	Power	
V26	VSS	GND	Ground	
V27	PEX_LANE_GOOD27#	O	Lane Status	
V28	N/C	***Reserved***	No Connect	
V29	HP_CLKEN11#	O	Hot Plug	
V30	N/C	***Reserved***	No Connect	
W1	PEX_LANE_GOOD7#	O	Lane Status	
W2	PEX_LANE_GOOD16#	O	Lane Status	
W3	HP_PWRFLT0#	I, PU	Hot Plug	
W4	HP_PRSNT9#	I, PU	Hot Plug	
W5	VSS	GND	Ground	
W10	VDD10	CPWR	Power	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
W11	VSS_THERMAL	Thermal-GND	Ground	
W12	VSS_THERMAL	Thermal-GND	Ground	
W13	VSS_THERMAL	Thermal-GND	Ground	
W14	VSS_THERMAL	Thermal-GND	Ground	
W15	VSS_THERMAL	Thermal-GND	Ground	
W16	VSS_THERMAL	Thermal-GND	Ground	
W17	VSS_THERMAL	Thermal-GND	Ground	
W18	VSS_THERMAL	Thermal-GND	Ground	
W19	VSS_THERMAL	Thermal-GND	Ground	
W20	VSS_THERMAL	Thermal-GND	Ground	
W21	VDD10	CPWR	Power	
W26	VDD33	I/OPWR	Power	
W27	PEX_LANE_GOOD28#	O	Lane Status	
W28	N/C	***Reserved***	No Connect	
W29	HP_PWRLED11#	O	Hot Plug	
W30	N/C	***Reserved***	No Connect	
Y1	HP_PWREN0#	O	Hot Plug	
Y2	HP_PWREN9#	O	Hot Plug	
Y3	N/C	***Reserved***	No Connect	
Y4	HP_PRSNT0#	I, PU	Hot Plug	
Y5	VDD33	I/OPWR	Power	
Y10	VDD10	CPWR	Power	
Y11	VSS_THERMAL	Thermal-GND	Ground	
Y12	VSS_THERMAL	Thermal-GND	Ground	
Y13	VSS_THERMAL	Thermal-GND	Ground	
Y14	VSS_THERMAL	Thermal-GND	Ground	
Y15	VSS_THERMAL	Thermal-GND	Ground	
Y16	VSS_THERMAL	Thermal-GND	Ground	
Y17	VSS_THERMAL	Thermal-GND	Ground	
Y18	VSS_THERMAL	Thermal-GND	Ground	
Y19	VSS_THERMAL	Thermal-GND	Ground	
Y20	VSS_THERMAL	Thermal-GND	Ground	
Y21	VDD10	CPWR	Power	
Y26	VSS	GND	Ground	
Y27	PEX_LANE_GOOD29#	O	Lane Status	
Y28	N/C	***Reserved***	No Connect	
Y29	HP_PERST11#	O	Hot Plug	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
Y30	N/C	***Reserved***	No Connect	
AA1	HP_PWRFLT9#	I, PU	Hot Plug	
AA2	N/C	***Reserved***	No Connect	
AA3	HP_PERST0#	O	Hot Plug	
AA4	HP_MRL9#	I, PU	Hot Plug	
AA5	VSS	GND	Ground	
AA10	VDD10	CPWR	Power	
AA11	VDD10	CPWR	Power	
AA12	VDD10	CPWR	Power	
AA13	VDD10	CPWR	Power	
AA14	VDD10	CPWR	Power	
AA15	VDD10	CPWR	Power	
AA16	VDD10	CPWR	Power	
AA17	VDD10	CPWR	Power	
AA18	VDD10	CPWR	Power	
AA19	VDD10	CPWR	Power	
AA20	VDD10	CPWR	Power	
AA21	VDD10	CPWR	Power	
AA26	VDD33	I/OPWR	Power	
AA27	PEX_LANE_GOOD30#	O	Lane Status	
AA28	N/C	***Reserved***	No Connect	
AA29	HP_PRSNT11#	I, PU	Hot Plug	
AA30	N/C	***Reserved***	No Connect	
AB1	HP_PWRLED0#	O	Hot Plug	
AB2	HP_ATNLED9#	O	Hot Plug	
AB3	N/C	***Reserved***	No Connect	
AB4	HP_CLKEN0#	O	Hot Plug	
AB5	VDD33	I/OPWR	Power	
AB26	VSS	GND	Ground	
AB27	PEX_LANE_GOOD31#	O	Lane Status	
AB28	N/C	***Reserved***	No Connect	
AB29	HP_PWREN11#	O	Hot Plug	
AB30	N/C	***Reserved***	No Connect	
AC1	HP_BUTTON9#	I, PU	Hot Plug	
AC2	N/C	***Reserved***	No Connect	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AC3	STRAP_FACTORY_TEST1#	I	STRAP	Strapping Ball – tie High
AC4	VSSA_PLL	PLL_GND	Ground	Analog GND for PLL circuit
AC5	VSS	GND	Ground	
AC26	VDD33	I/OPWR	Power	
AC27	STRAP_STN0_PORTCFG3	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN0_PORTCFG[4:0]
AC28	STRAP_STN0_PORTCFG4	I	STRAP	
AC29	HP_PWRFLT11#	I, PU	Hot Plug	
AC30	N/C	***Reserved***	No Connect	
AD1	PEX_LANE_GOOD17#	O	Lane Status	
AD2	PEX_LANE_GOOD21#	O	Lane Status	
AD3	PEX_LANE_GOOD19#	O	Lane Status	
AD4	VSS	GND	Ground	
AD5	VSS	GND	Ground	
AD26	VSS	GND	Ground	
AD27	STRAP_STN0_PORTCFG1	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN0_PORTCFG[4:0]
AD28	STRAP_STN0_PORTCFG2	I	STRAP	
AD29	HP_MRL11#	I, PU	Hot Plug	
AD30	N/C	***Reserved***	No Connect	
AE1	N/C	***Reserved***	No Connect	
AE2	N/C	***Reserved***	No Connect	
AE3	VDD33	I/OPWR	Power	
AE4	VSS	GND	Ground	
AE5	VSS	GND	Ground	
AE26	VDD33	I/OPWR	Power	
AE27	N/C	***Reserved***	No Connect	
AE28	STRAP_STN0_PORTCFG0	I	STRAP	Strapping Ball – tie High or Low, as defined in STRAP_STN0_PORTCFG[4:0]
AE29	HP_ATNLED11#	O	Hot Plug	
AE30	N/C	***Reserved***	No Connect	
AF1	VDD33A	PLLPWR	Power	
AF2	NC_PROCMON	***Reserved***	No Connect	
AF3	VDD33	I/OPWR	Power	
AF4	VSS	GND	Ground	
AF5	VSS	GND	Ground	
AF6	PEX_PERn0	CMLRn	SerDes	
AF7	VTT_PEX0	Supply	Power	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AF8	PEX_PERn1	CMLRn	SerDes	
AF9	VTT_PEX1	Supply	Power	
AF10	PEX_PERp2	CMLRp	SerDes	
AF11	VDD10A	APWR	Power	
AF12	PEX_PERn3	CMLRn	SerDes	
AF13	VSS	GND	Ground	
AF14	PEX_PERn4	CMLRn	SerDes	
AF15	VTT_PEX2	Supply	Power	
AF16	PEX_PERn5	CMLRn	SerDes	
AF17	VDD10A	APWR	Power	
AF18	PEX_PERn6	CMLRn	SerDes	
AF19	VTT_PEX3	Supply	Power	
AF20	PEX_PERn7	CMLRn	SerDes	
AF21	VDD10A	APWR	Power	
AF22	VSS	GND	Ground	
AF23	VDD10S	SPWR	Power	
AF24	VSS	GND	Ground	
AF25	VDD10S	SPWR	Power	
AF26	VSS	GND	Ground	
AF27	N/C	***Reserved***	No Connect	
AF28	N/C	***Reserved***	No Connect	
AF29	HP_BUTTON11#	I, PU	Hot Plug	
AF30	N/C	***Reserved***	No Connect	
AG1	VSS	GND	Ground	
AG2	VDD10S	SPWR	Power	
AG3	VSS	GND	Ground	
AG4	VSS	GND	Ground	
AG5	VSS	GND	Ground	
AG6	PEX_PERp0	CMLRp	SerDes	
AG7	VSS	GND	Ground	
AG8	PEX_PERp1	CMLRp	SerDes	
AG9	VDD10S	SPWR	Power	
AG10	PEX_PERn2	CMLRn	SerDes	
AG11	VSS	GND	Ground	
AG12	PEX_PERp3	CMLRp	SerDes	
AG13	VDD10S	SPWR	Power	
AG14	PEX_PERp4	CMLRp	SerDes	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AG15	VSS	GND	Ground	
AG16	PEX_PERp5	CMLRp	SerDes	
AG17	VDD10S	SPWR	Power	
AG18	PEX_PERp6	CMLRp	SerDes	
AG19	VSS	GND	Ground	
AG20	PEX_PERp7	CMLRp	SerDes	
AG21	VSS	GND	Ground	
AG22	VDD10S	SPWR	Power	
AG23	VSS	GND	Ground	
AG24	VDD10S	SPWR	Power	
AG25	VSS	GND	Ground	
AG26	VDD33	I/OPWR	Power	
AG27	EE_DI	O	Serial EEPROM	Connected to data input of serial EEPROM
AG28	EE_CS#	O	Serial EEPROM	
AG29	EE_SK	O	Serial EEPROM	
AG30	EE_DO	I, PU	Serial EEPROM	Connected to data output of serial EEPROM
AH1	VDD10S	SPWR	Power	
AH2	VSS	GND	Ground	
AH3	VDD10S	SPWR	Power	
AH4	VSS	GND	Ground	
AH5	VSS	GND	Ground	
AH6	VSS	GND	Ground	
AH7	VDD10S	SPWR	Power	
AH8	VSS	GND	Ground	
AH9	VSS	GND	Ground	
AH10	VSS	GND	Ground	
AH11	VDD10S	SPWR	Power	
AH12	VSS	GND	Ground	
AH13	VSS	GND	Ground	
AH14	VSS	GND	Ground	
AH15	VDD10S	SPWR	Power	
AH16	VSS	GND	Ground	
AH17	VSS	GND	Ground	
AH18	VSS	GND	Ground	
AH19	VDD10S	SPWR	Power	
AH20	VSS	GND	Ground	
AH21	VDD10S	SPWR	Power	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AH22	VSS	GND	Ground	
AH23	VDD10S	SPWR	Power	
AH24	VSS	GND	Ground	
AH25	VDD10S	SPWR	Power	
AH26	VSS	GND	Ground	
AH27	N/C	***Reserved***	No Connect	
AH28	EE_PR#	I	Serial EEPROM	
AH29	VDD33	I/OPWR	Power	
AH30	VSS	GND	Ground	
AJ1	VSS	GND	Ground	
AJ2	VDD10S	SPWR	Power	
AJ3	VSS	GND	Ground	
AJ4	PEX_REFCLKp	CMLCLKp	SerDes	
AJ5	VDD10S	SPWR	Power	
AJ6	PEX_PETp0	CMLTp	SerDes	
AJ7	VSS	GND	Ground	
AJ8	PEX_PETp1	CMLTp	SerDes	
AJ9	VDD10S	SPWR	Power	
AJ10	PEX_PETp2	CMLTp	SerDes	
AJ11	VSS	GND	Ground	
AJ12	PEX_PETp3	CMLTp	SerDes	
AJ13	VDD10S	SPWR	Power	
AJ14	PEX_PETp4	CMLTp	SerDes	
AJ15	VSS	GND	Ground	
AJ16	PEX_PETp5	CMLTp	SerDes	
AJ17	VSS	GND	Ground	
AJ18	PEX_PETp6	CMLTp	SerDes	
AJ19	VSS	GND	Ground	
AJ20	PEX_PETp7	CMLTp	SerDes	
AJ21	VSS	GND	Ground	
AJ22	VDD10S	SPWR	Power	
AJ23	VSS	GND	Ground	
AJ24	VDD10S	SPWR	Power	
AJ25	VSS	GND	Ground	
AJ26	VDD33	I/OPWR	Power	
AJ27	VSS	GND	Ground	
AJ28	VDD33	I/OPWR	Power	

Table 3-19. PEX 8524BB/BC Switch Ball Assignments by Number – 644-Ball PBGA *(Cont.)*

PEX 8524 Balls				Description
Num	Name	Type	Signal Group	
AJ29	VSS	GND	Ground	
AJ30	VDD33	I/OPWR	Power	
AK1	VDD10S	SPWR	Power	
AK2	VSS	GND	Ground	
AK3	VDD10S	SPWR	Power	
AK4	PEX_REFCLKn	CMLCLKn	SerDes / Clock	
AK5	VSS	GND	Ground	
AK6	PEX_PETn0	CMLTn	SerDes	
AK7	VDD10S	SPWR	Power	
AK8	PEX_PETn1	CMLTn	SerDes	
AK9	VSS	GND	Ground	
AK10	PEX_PETn2	CMLTn	SerDes	
AK11	VDD10S	SPWR	Power	
AK12	PEX_PETn3	CMLTn	SerDes	
AK13	VSS	GND	Ground	
AK14	PEX_PETn4	CMLTn	SerDes	
AK15	VDD10S	SPWR	Power	
AK16	PEX_PETn5	CMLTn	SerDes	
AK17	VDD10S	SPWR	Power	
AK18	PEX_PETn6	CMLTn	SerDes	
AK19	VDD10S	SPWR	Power	
AK20	PEX_PETn7	CMLTn	SerDes	
AK21	VDD10S	SPWR	Power	
AK22	VSS	GND	Ground	
AK23	VDD10S	SPWR	Power	
AK24	VSS	GND	Ground	
AK25	VDD10S	SPWR	Power	
AK26	VSS	GND	Ground	
AK27	VDD33	I/OPWR	Power	
AK28	VSS	GND	Ground	
AK29	VDD33	I/OPWR	Power	
AK30	VSS	GND	Ground	

3.7 PEX 8524 Physical Layouts

Figure 3-1. PEX 8524VAA/BB/BC 680-Ball Physical Ball Assignment (See-Through Top View)

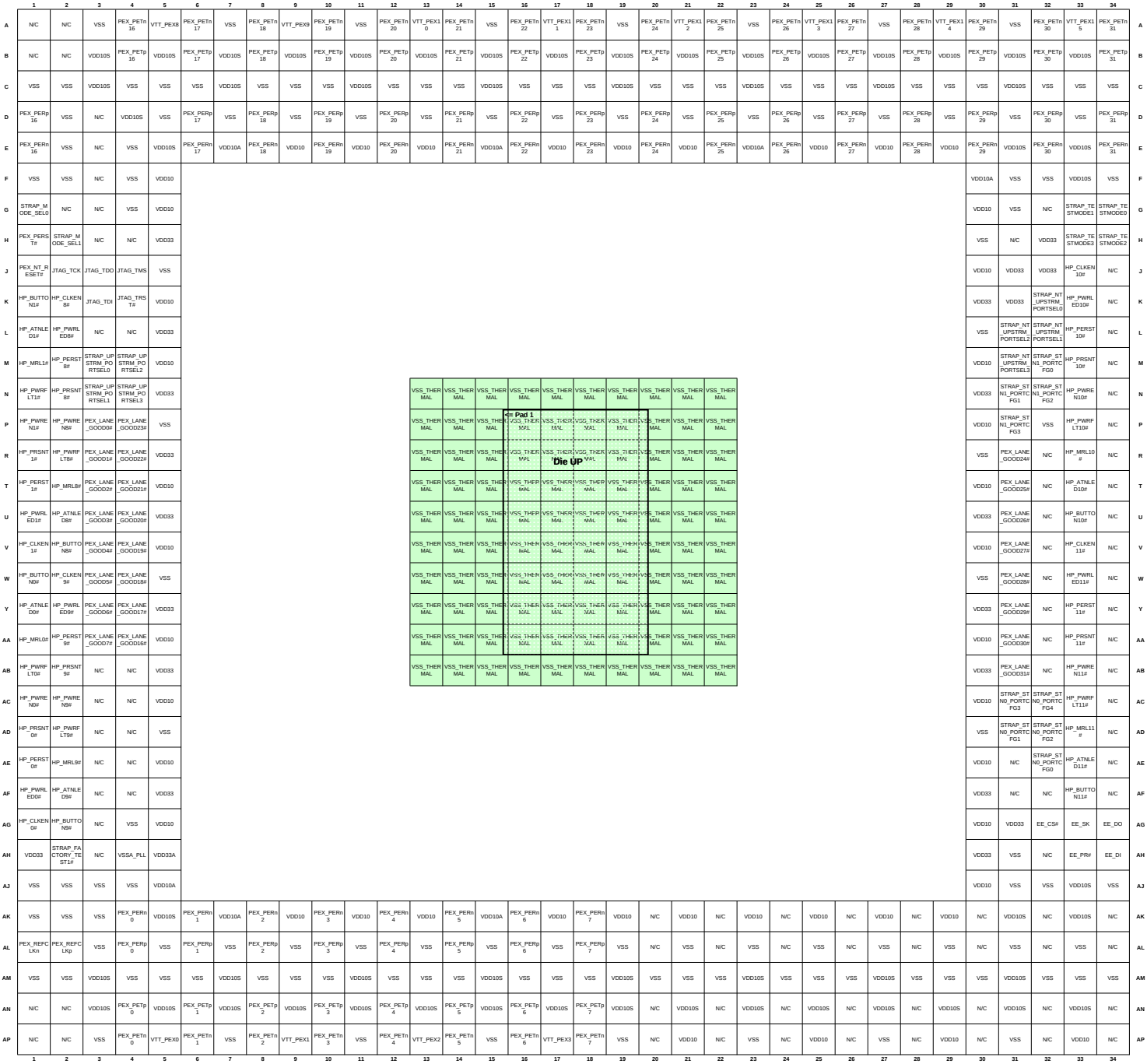
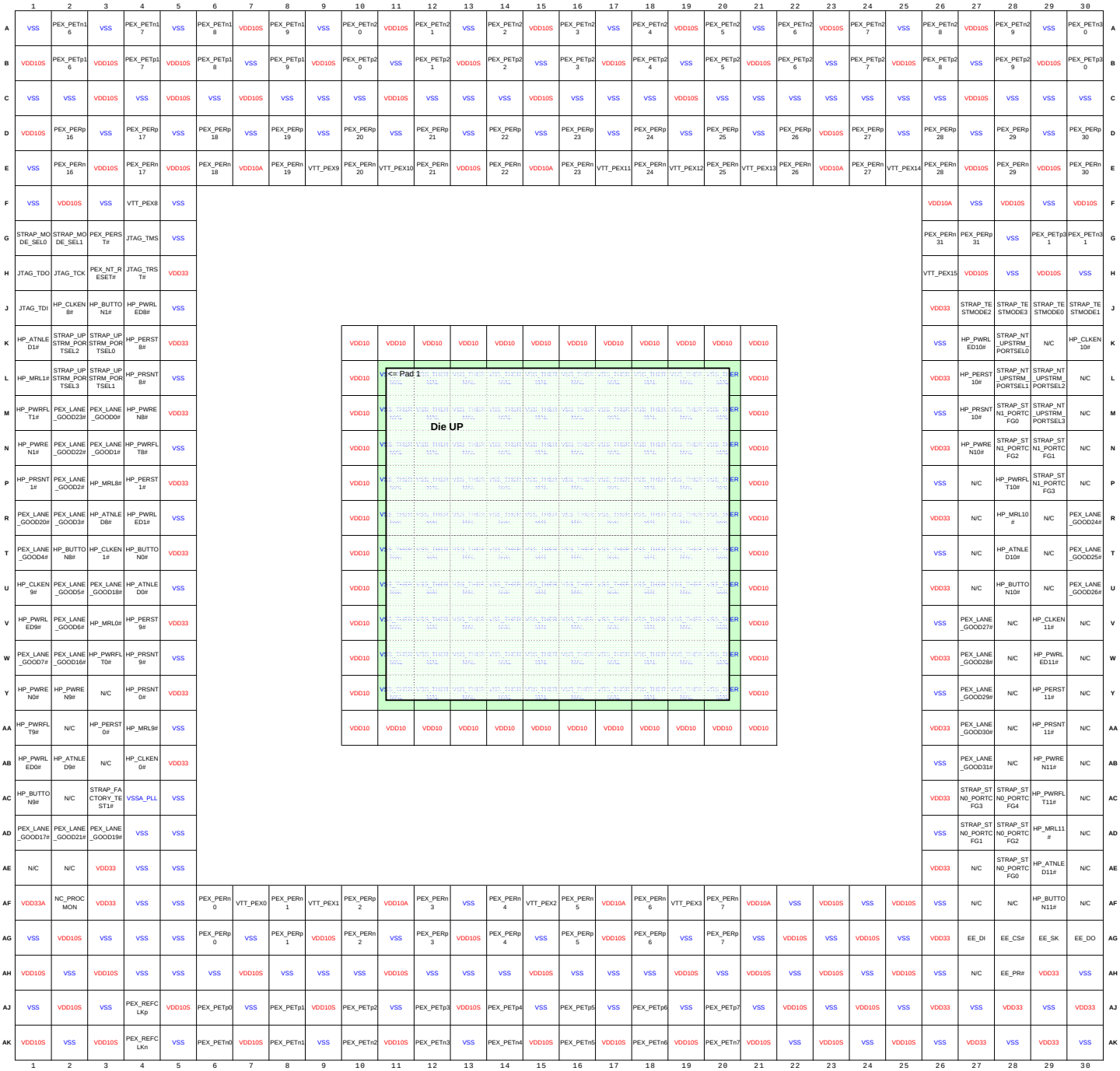


Figure 3-2. PEX 8524BB/BC 644-Ball PBGA Physical Layout (See-Through Top View)

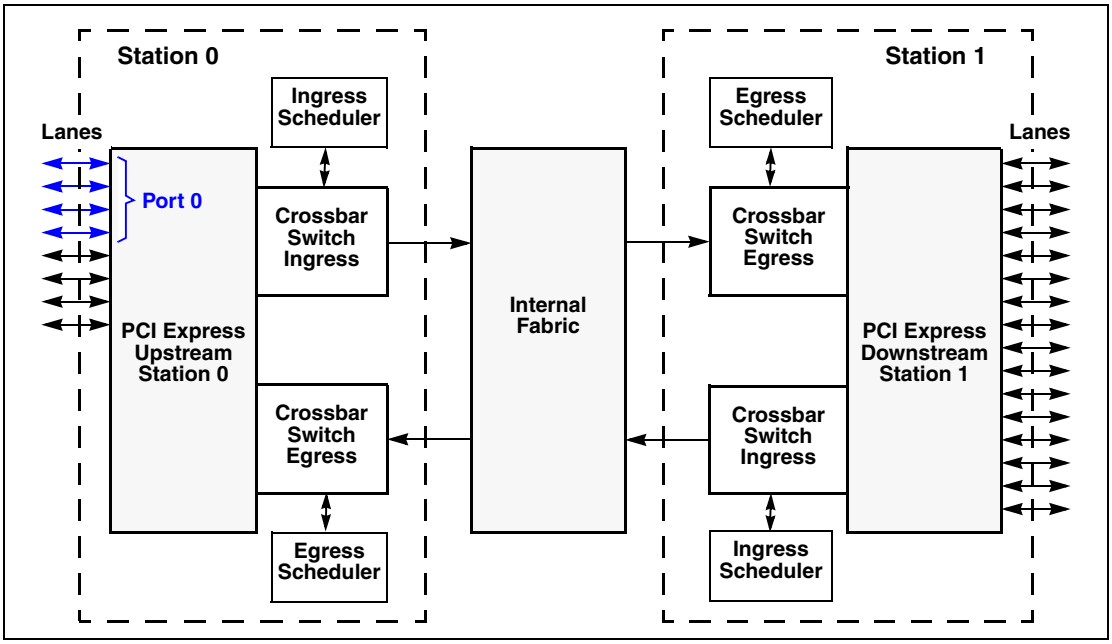


Chapter 4 Functional Overview

4.1 PEX 8524 Architecture

The PEX 8524 switch is designed with a flexible, modular architecture. The two main building blocks of this architecture are the non-blocking Crossbar Switch fabric (internal fabric) and protocol-specific I/O module, termed *station*. Figure 4-1 illustrates a block diagram of the PEX 8524.

Figure 4-1. PEX 8524 Block Diagram



4.1.1 Ingress and Egress Functions

The Crossbar Switch Ingress queue interfaces the PCI Express station to the internal fabric. The queue contains a centralized packet buffer for incoming ports, ingress port scheduler, and internal fabric scheduler.

The Crossbar Switch Egress queue interfaces the non-blocking internal fabric to the PCI Express station. The queue contains a centralized packet buffer for all outgoing ports and the egress port scheduler.

All ingress traffic flows from the PCI Express station by way of the Crossbar Switch Ingress queue, internal fabric, Crossbar Switch Egress queue, and finally to the outgoing PCI Express station. Ingress and egress scheduler modules contain a Virtual Channel (VC) scheduler for each port. The ingress scheduler supports a port-width-based arbitration scheme. The egress scheduler supports a device-specific port arbitration scheme, to avoid port starvation.

4.1.2 Station and Port Functions

Each port implements the *PCI Express Base r1.0a* Physical, Data Link, and Transaction layers. Station 0 can support up to 8 integrated Serializer/De-serializer (SerDes) modules, and Station 1 can support up to 16. The SerDes modules provide the 24 PCI Express hardware interface lanes.

The lanes can be combined, for a total of one to two PCI Express ports in Station 0, and one to four PCI Express ports in Station 1. If the upstream port is in the other station, all enabled ports in the current station are downstream ports. Lanes from different stations cannot be combined to form ports.

From the system model viewpoint, each PCI Express port is a virtual PCI-to-PCI bridge device with its own set of PCI Express Configuration registers. The BIOS enumerates the PEX 8524 ports, using either Conventional PCI Configuration access or PCI Express Enhanced access.

The PEX 8524 port width is configurable by way of Strapped signal balls, or serial EEPROM after reset. The final port width can be made narrower by auto-lane width negotiation, as described in the *PCI Express Base r1.0a*.

4.1.2.1 Port Combinations

The PEX 8524 supports a wide variety of configurations per station (as defined in Table 4-1) and supports two stations and up to two ports on Station 0 and four ports on Station 1, providing an extensive set of possible port/station configurations. Ports that are not configured or enabled are invisible to software. There are 8 lanes [0-7] for Station 0 and 16 lanes [16-31] for Station 1. The configuration value defines the levels set by STRAP_STN0_PORTCFG[4:0] and STRAP_STN1_PORTCFG[3:0].

The equivalent system model contains an upstream port PCI-to-PCI bridge and five downstream port PCI-to-PCI bridges, as illustrated in Figure 4-2. The upstream station contains one upstream PCI-to-PCI bridge and one downstream PCI-to-PCI bridge.

The upstream port and downstream ports' lane widths are initially set by the Strapping balls, which must be tied High to VDD33 or Low to VSS (GND). (Refer to Section 3.4.4, "Strapping Signals – 680-Ball PBGA," or Section 3.5.4, "Strapping Signals – 644-Ball PBGA.") The serial EEPROM option is used to reconfigure the ports by using the options defined in Table 4-1. Serial EEPROM configuration occurs following a Fundamental Reset, and overrides the configuration set by the Strapping balls at that time. (Refer to Section 5.3.3, "Setting Port Configuration Using Serial EEPROM.") The narrowest port on one end of the link determines the maximum link width. Additionally, if a connection is broken on one of the lanes, the training sequence removes the broken lane and negotiates to a narrower width. A x16 port can negotiate down to x8, x4, x2, or x1.

If the port cannot train to x1 (Lane 0 is broken), it reverses its lanes and attempts to train again. *For example*, a x16 port that cannot train to x16 attempts to negotiate down to x8, x4, x2, or x1; if x1 linkup fails, the port then reverses its lanes and attempts again to negotiate link up. Either the lowest lane (Lane 0) or highest lane (if lanes are reversed) of the programmed link width must connect to the other device's Lane 0.

Table 4-1. PEX 8524 Port Configurations

Port Configuration Register Value[a] (Port 0 or 8, Offset 224h[4:0])	Station 0 [Lanes/SerDes]/ Port[b]		Station 1 [Lanes/SerDes]/Port[b]			
	Port 0	Port 1	Port 8	Port 9	Port 10	Port 11
0h	x4 [0-3]	x4 [4-7]	x4 [16-19]	x4 [20-23]	x4 [24-27]	x4 [28-31]
1h	–[c]	–	x16 [16-31][d]	–	–	–
2h	x8 [0-7]	–	x8 [16-23]	x8 [24-31]	–	–
3h	–	–	x8 [16-23]	x4 [24-27]	x4 [28-31]	–
4h	–	–	x8 [16-23]	x4 [24-27]	x2 [28-29]	x2 [30-31]
5h	–	–	x8 [16-23]	x2 [24-25]	x2 [26-27]	x4 [28-31]
6h	–	–	x8 [16-23]	x2 [24-25]	x4 [26-29]	x2 [30-31]

a. The PEX 8524 can be re-configured by link-width negotiation to smaller widths of x4, x2, or x1.

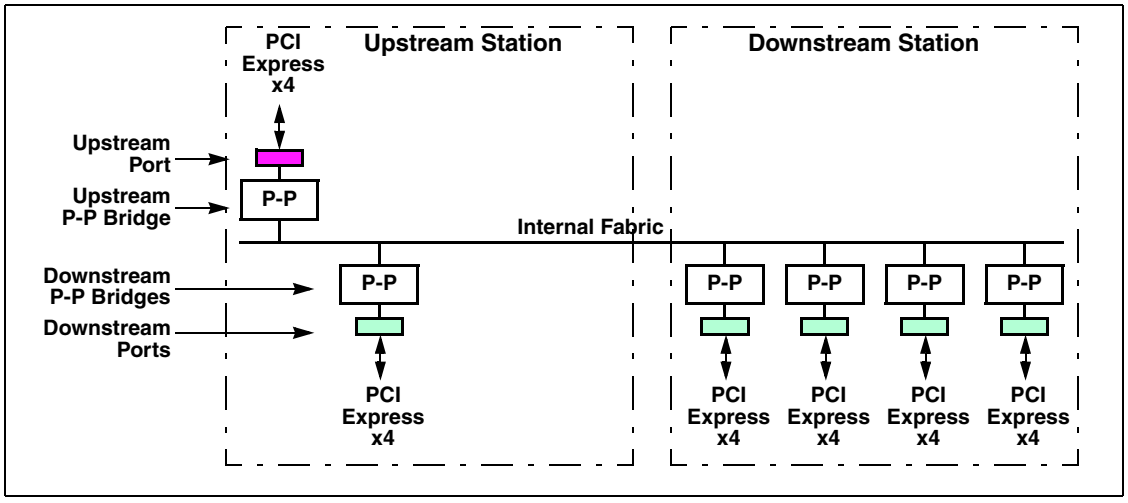
b. The lanes are assigned to each enabled port in sequence, as indicated in [brackets].

*c. Configuration value and port combinations with "–" (no data) are **reserved**.*

d. Ports 8 and 9 can be combined to create a 16-lane (x16) port.

Note: *P-P is used to represent PCI-to-PCI in the illustrations provided in this data book.*

Figure 4-2. Equivalent System Model with Maximum Number of Ports and Lanes



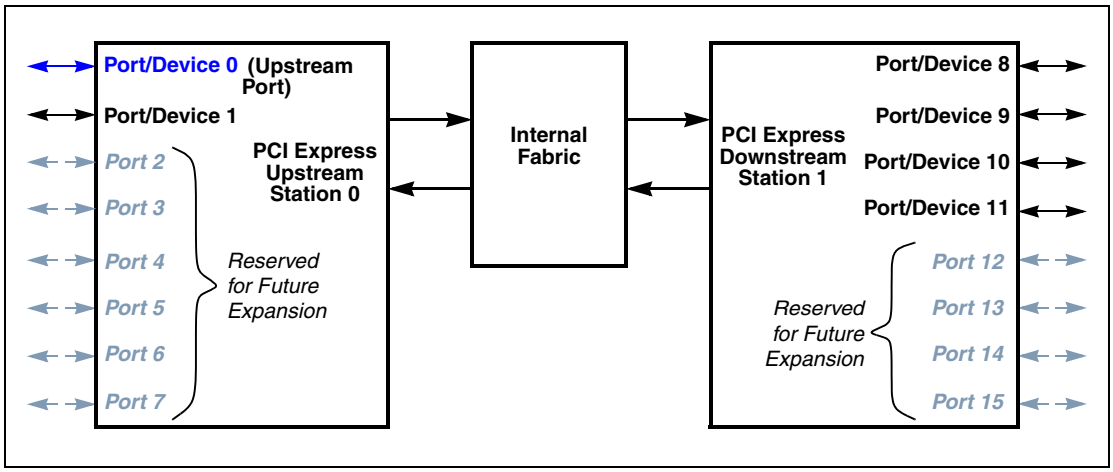
4.1.2.2 Port Numbering

The PEX 8524 Port Numbers are 0, 1 (Station 0) and 8, 9, 10, 11 (Station 1). Ports 2, 3, 4, 5, 6, 7 and 12, 13, 14, 15 are ***reserved*** for future use. (Refer to Table 4-1 and Figure 4-3.) The Port Number and Device Number are the same (in the Type 1 Headers) that map to all ports, with an exception for a non-zero upstream port.

All downstream Device Numbers match their corresponding Port Number. *For example*, if Port 0 is the upstream port, Ports 1, 8, 9, 10, and 11 are the downstream ports. The Device Numbers for the PCI-to-PCI bridges implemented on the downstream ports are 1, 8, 9, 10, and 11, respectively. (Refer to Figure 4-3.)

Any PEX 8524 port can be configured as the upstream port. The PCI-to-PCI bridge implemented on the upstream port does not assume a Device Number – it accepts the Device Number assigned by the upstream device. Generally, the upstream device assigns Device Number 0, according to the *PCI Express Base r1.0a*.

Figure 4-3. PLX Port Numbering Convention Example (When Port 0 Is Upstream Port)



4.2 PCI-Compatible Software Model

The PEX 8524 can be thought of as a hierarchy of PCI-to-PCI bridges, with one upstream PCI-to-PCI bridge and one or more downstream PCI-to-PCI bridges connected by a virtual internal bus. (Refer to Figure 4-4.) PCI-to-PCI bridges are compliant with the PCI and PCI Express system models. Figure 4-4 illustrates the concept of hierarchical PCI-to-PCI bridges, with the bus in the middle being the virtual PCI Bus. The Configuration Space registers (CSRs) in the upstream PCI-to-PCI bridge are accessible by Type 0 Configuration requests targeting the upstream bus interface. The upstream port captures the Type 0 Configuration Write Target Bus Number and Device Number. The upstream port uses this Captured Bus Number and Captured Device Number as part of the Requester ID and Completer ID for the requests and completions generated by the upstream port.

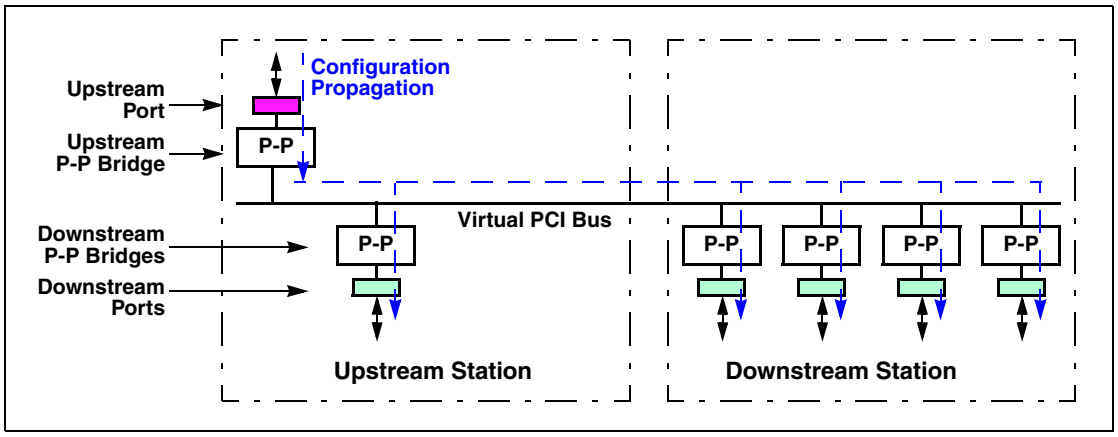
The CSRs in the downstream port PCI-to-PCI bridges are accessible by Type 1 Configuration requests received at the upstream port that target the virtual internal bus, by having a Bus Number value that matches the upstream bridge's Secondary Bus Number value. Each downstream bridge is associated with a unique Device Number, as explained in Section 4.1.2.

The CSRs of downstream devices are hit in two ways. If the Configuration request matches the PEX 8524 downstream port Secondary Bus Number, the PEX 8524 converts the Type 1 Configuration request into a Type 0 Configuration request. However, if the Bus Number does ***not*** match the Secondary Bus Number, but falls within the Subordinate Bus Number range, the Type 1 Configuration request is forwarded out of the PEX 8524, unchanged.

After all PCI devices have been located and assigned Bus and Device Numbers, software can assign a Memory map and I/O map. Requests (Memory or I/O) go downstream if they fall within a bridge's Base and Limit range. In the PEX 8524, each downstream bridge has its own Base and Limit. The Request (Memory or I/O) goes upstream if it does not target anything within the upstream bridge's Base and Limit range.

Completions route by the Bus Number established in the Configuration registers. If the Bus Number is in the Secondary or Subordinate range, the packet goes downstream; otherwise, the packet goes upstream.

Figure 4-4. PEX 8524 System Configuration Propagation



4.2.1 System Reset

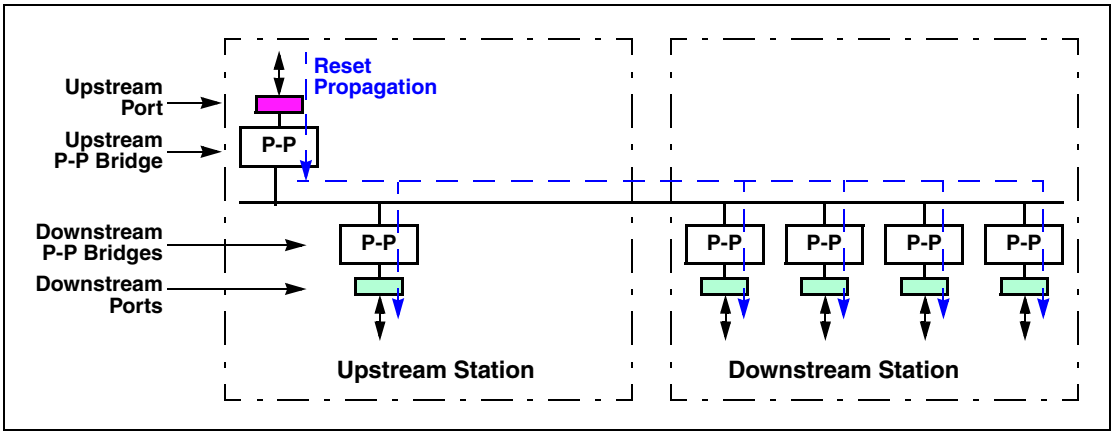
The PEX 8524 can be reset by four different mechanisms (refer to Section 5.1, "Reset Overview," for details):

- Fundamental Reset input, through the PEX_PERST# signal
- In-band Reset propagates from upstream, through the Physical Layer mechanism, which communicates a reset through a training sequence (TS1/TS2 Ordered-Set *Hot Reset* or *Disable Link* bit is set)
- PCI Express link enters the DL_Down state on the upstream port
- Upstream port **Bridge Control** register *Secondary Bus Reset* bit is set (offset 3Ch[22]=1)

Reset is propagated from upstream to downstream. Reset is propagated to the downstream PCI Express device, through the PCI Express link by the Physical Layer mechanism (the TS1/TS2 Ordered-Set *Hot Reset* bit is set), or when the upstream port link enters the *DL_Down* state. (Refer to Section 5.1, "Reset Overview," for further details.)

An example of reset propagation is illustrated in Figure 4-5. Upon receiving a reset from the upstream PCI Express link, the upstream port PCI-to-PCI bridge propagates the reset to the downstream port PCI-to-PCI bridges in the upstream station, as well as to the downstream port PCI-to-PCI bridges in its downstream station.

Figure 4-5. PEX 8524 System Reset Propagation



4.2.2 Interrupts

Generated interrupts are INT*x* Interrupt message-type (compatible with the *PCI r2.3*-defined Interrupt signals) or Message Signaled Interrupts (MSI), when enabled. MSI and INT*x* are mutually exclusive; either can be enabled in a system (depending on which interrupt type the system software supports), but never both. [Refer to the **Message Signaled Interrupt Capability** register (offset 48h) and **Command** register *Interrupt Disable* bit (offset 04h[10]).] The PEX 8524 does not convert received INT*x* messages to MSI messages.

Refer to Chapter 6, "Interrupts," for complete details.

4.2.2.1 Interrupt Sources or Events

The PEX 8524-generated interrupt/message sources include:

- Hot Plug events
- Device-specific error events
- INT*x*

4.2.2.2 INT*x* Switch Mapping

The PEX 8524 remaps and collapses the INT*x virtual wires*, based on downstream port Device Number and received INT*x* message Requester ID Device Number. Each virtual PCI-to-PCI bridge of a downstream port specifies the Port Number associated with the INT*x* (Interrupt) messages received or generated, and forwards the interrupt messages in the upstream direction. Refer to Section 6.2.1, "INTx-Type Interrupt Message Remapping and Collapsing," for interrupt routing information.

4.3 PCI Express Station Functional Description

The PEX 8524 groups 8 SerDes together into Station 0, and 16 SerDes together into Station 1. A station can have one or two ports (Station 0) or one to four ports (Station 1), as defined in Table 4-1. The station forwards ingress packets to the internal fabric, to be routed to the egress station.

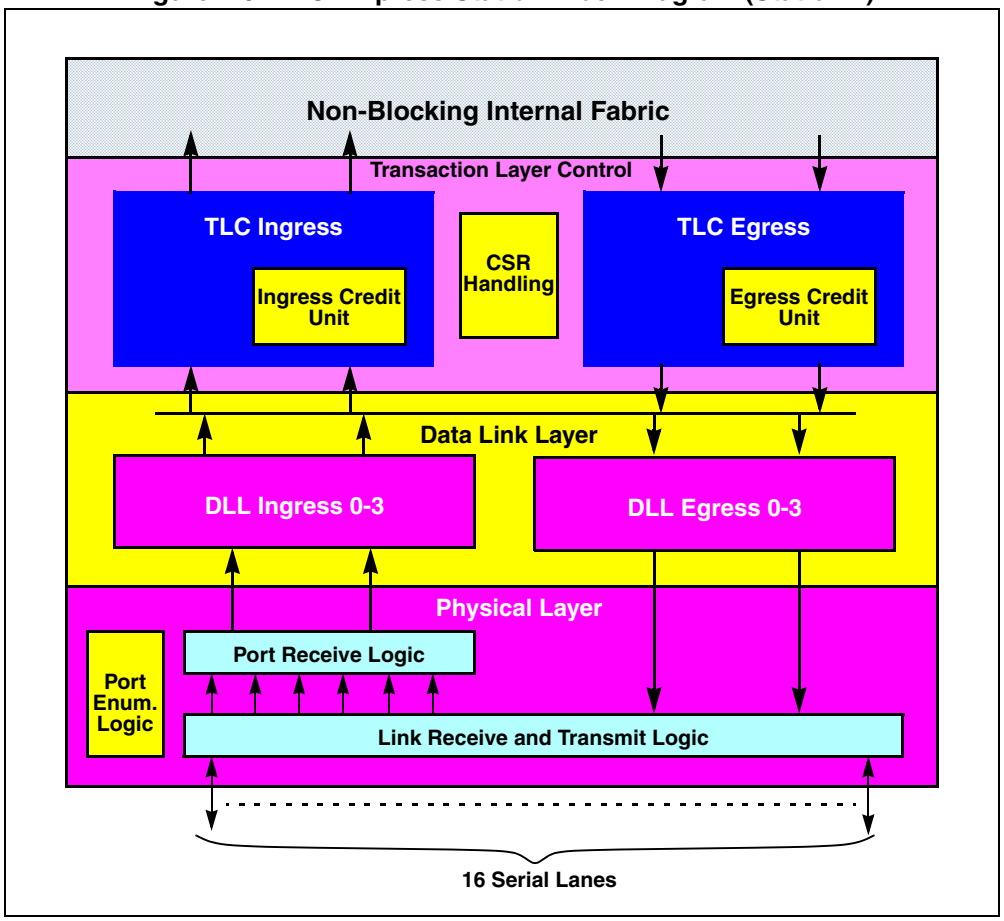
Each station implements the PCI Express Physical (PHY) Layer and Data Link Layer (DLL) functions for each of its ports, and aggregates traffic from these ports on to a transaction-based, non-blocking internal fabric. The PCI Express station also performs many Transaction Layer functions, while the packet queuing and ordering aspects of this layer are handled by the Crossbar Switch Control blocks.

During system initialization, software initiates Configuration requests that set up the PCI Express interfaces, Device Numbers, and Address maps across the various ports. These maps are used to direct traffic between ports during standard system operation. A PCI Express station can contain multiple ports (one upstream and multiple downstream). Traffic flow between different ports of the same station, or ports on different stations, is supported by the central internal fabric.

4.3.1 PEX 8524 Functional Blocks

At the top level, each station has a layered organization consisting of the Physical (PHY), Data Link Layer (DLL), and Transaction Layer Control (TLC) blocks, as illustrated in Figure 4-6. The PHY and DLL blocks have port-specific data paths (one per PCI Express port) that operate independently of one another. The TLC ingress aggregates traffic for all ingress ports in the station, then sends the traffic to the internal fabric. The TLC egress accepts packets, by way of the internal fabric, from all ingress ports, and schedules them to be sent out the appropriate egress port.

Figure 4-6. PCI Express Station Block Diagram (Station 1)



4.3.1.1 Physical Layer

The Physical Layer module interfaces to the PCI Express lanes and implements the PHY Layer functions. The number of ports per station can vary from one to two for Station 0, and one to four for Station 1, with a cumulative lane-bandwidth of x8 (Station 0) or x16 (Station 1). When there are fewer than two (Station 0) or four (Station 1) configured/enabled ports, the x8 (Station 0) or x16 (Station 1) bandwidth can be shared by the remaining active ports, as defined in Table 4-1. PHY Layer functions include:

- Establishing port configurations and SerDes-to-port assignments
- Establishing internal bandwidth division among ports
- Supporting cross-linked upstream and downstream ports
- 8b/10b encoding/decoding
- Data scrambling/unscrambling
- Packet framing
- Loop-Back Master and Slave support
- Pseudo-Random Bit Sequence (PRBS) data generation and checking
- User-defined test pattern with SKIP Ordered-Set insertion and return data checking
- Driver and Input buffers
- Parallel-to-serial and serial-to-parallel conversion
- PLLs and Clock circuitry
- Impedance-matching circuitry
- Interface initialization and maintenance functions

Physical Layer Command and Status Registers

The Physical Layer operating conditions are defined in Section 11.13.2, "Physical Layer Registers." The system host can track the link operating status and re-configure link parameters, by way of these registers.

Hardware Link Interface Configuration

The PEX 8524 Physical Layer of each station can include up to four integrated quad Serializer/De-serializer (SerDes) modules, which provide the PCI Express hardware interface lanes. The SerDes modules provide all physical communication controls and functions required by the *PCI Express Base r1.0a*. SerDes modules are clustered into ports, to provide the links that connect to other PCI Express devices.

4.3.1.2 Data Link Layer

The Data Link Layer (DLL) serves as an intermediate stage between the Transaction Layer and the Physical Layer. The primary responsibility of the Data Link Layer includes link management and data integrity, including error detection and correction.

The transmission side of the Data Link Layer accepts Transaction Layer Packets (TLPs) assembled by the Transaction Layer, calculates and applies data protection code and TLP Sequence Number, and submits them to the Physical Layer for transmission across the link.

The receiving Data Link Layer is responsible for checking the integrity of received TLPs and submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this Layer is responsible for requesting re-transmission of TLPs until the information is correctly received, or the link is determined to have failed.

Data Link Layer Packet (DLLP)

The Data Link Layer also generates and consumes packets used for Link management functions. To differentiate these packets from the TLPs used by the Transaction Layer, the term *Data Link Layer Packet* (*DLLP*) is used when referring to packets generated and consumed at the Data Link Layer. The rules governing the identification and formation of these packets are defined in the *PCI Express Base r1.0a*, Section 3.4.1.

FC Credits

The initial number of flow control credits advertised for Virtual Channel 0 is listed in Section 8.4.2.1, "Ingress Side." The flow control credits are also programmable through the serial EEPROM. The Transaction Layer must schedule an Update FC DLLP for transmission, to replenish the number of advertised credits or to meet an updated VC Timer. When enabled, the Transaction Layer initiates flow credit initialization for VC1, following VC0 initialization.

Packet Arbiter

The Packet Arbiter determines what type of packet to forward to the PHY layer, on a per port basis. The priority algorithm implemented by the Packet Arbiter is discussed in Section 8.4.5.1, "Arbitration between DLLP and TLP," and follows the recommended priority provided in the *PCI Express Base r1.0a*, Section 3.5.2.1.

4.3.1.3 Transaction Layer

The upper layer of the architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, *such as* Read and Write, as well as certain types of events. The Transaction Layer is also responsible for managing credit-based flow control for TLPs.

Request packets requiring a Response packet are implemented as Split Transactions. Each packet contains a unique identifier that enables Response packets to be directed to the correct originator. The packet format supports different forms of addressing, depending on the transaction type – *Memory*, *I/O*, *Configuration*, or *Message*. The packets can also have attributes, *such as No Snoop* and *Relaxed Ordering*.

The Transaction Layer supports four Address spaces – it includes the three PCI Address spaces (Memory, I/O, and Configuration) and adds a Message space. (Refer to Table 4-2.) This specification uses Message space to support all prior sideband signals, *such as* interrupts and Power Management requests, as in-band Message transactions. PCI Express Message transactions are considered *virtual wires*, because their effect is to eliminate the wide array of sideband signals currently used in a platform.

Functions provided by the Transaction Layer include:

- Decoding and checking incoming TLP
- Memory-mapped CSR access
- Checking the incoming packets for malformed packets or Unsupported Requests (UR)
- ECRC checking the incoming packets
- Error signaling for incoming packets
- Destination lookup and TC-VC mapping
- Virtual Channel Management
- TLP packet scheduling
- PCI/PCI-X-compatible ordering
- QoS support
- External Credit Control
- Power Management support
- Hot Plug support
- Message Signal Interrupt or INT*x* generation
- Ordering
- Egress and Ingress Credit Management

Table 4-2. Address Spaces Support Different Transaction Types

Address Space	Transaction Types	Transaction Functions
Configuration	Read/Write	Device configuration or setup.
Input/Output	Read/Write	Transfer data from/to an I/O-mapped location.
Memory	Read/Write	Transfer data from/to a memory location.
Message	Baseline/Virtual Wires	General-purpose messages. Event signaling (*such as* status, interrupts, and so forth).

Transaction Layer Receive/Ingress Protocol

The ingress side Transaction Layer collects and stores inbound TLP traffic in Virtual Channel buffers. The incoming data is checked for ECRC errors, valid *Type* field, length matching the Header *Transfer Size* field, and other TLP-specific errors defined by the *PCI Express Base r1.0a*.

Header and Data Payload are forwarded to the Source Scheduler, to be routed to the switch outgoing port.

Transaction Layer Transmit/Egress Protocol

The egress side Transaction Layer receives information from other switch ports and generates outbound requests and completion TLPs, which it stores in Virtual Channel buffers. This layer assembles Transaction Layer packets, which consist of identification Headers, Data Payloads, and ECRC. Details for these fields are defined in the *PCI Express Base r1.0a*, Section 2.2.

The PEX 8524 implements an egress Flow Control (FC) protocol that ensures it does not transmit a TLP over a link to a remote receiver unless the receiving device contains sufficient Virtual Channel (VC) buffer space to accommodate the packet. This flow control is automatically managed by the hardware and is transparent to software. Software is used only to enable additional buffers, to supplement the initial default buffer assignment.

4.3.1.4 Virtual Channels and Traffic Classes

The PEX 8524 supports two Virtual Channels – VC0 and VC1 – and up to eight Traffic Classes – TC[7:0]). VC0 and TC0 are required by the *PCI Express Base r1.0a*, and configured at device start-up. The second Virtual Channel (VC1) is enabled by the PEX 8524 default configuration procedure, but can be disabled by using serial EEPROM configuration to clear the **Port VC Capability 1** register *Extended VC Count* bit (offset 14Ch[0]).

4.3.1.5 Non-Blocking Crossbar Switch Architecture

The non-blocking Crossbar Switch is an on-chip interconnect switch-fabric module (internal fabric) used to link multiple stations. The physical topology of the Crossbar Switch interconnect is a packet beat-based internal fabric designed to simultaneously connect multiple on-chip logic stations.

The Crossbar Switch protocol is sufficiently flexible and robust to support a variety of embedded system needs. The protocol is specifically designed to ease chip integration by strongly enforcing station boundaries and standardizing communication between stations.

The Crossbar Switch architecture incorporates the following functions:

- Multiple concurrent data transfers with maximum throughput
- Global ordering within the switch
- Internal credit guarantees packet forward progress once scheduled
- Deadlock avoidance
- Priority preemption
- Two independent Virtual Channels (VC0 and VC1)
- PCI Express Ordering rules
- Packet fair queuing
- Oldest first scheduling

4.3.2 Relaxed Ordering

The PEX 8524 does not support the optional Relaxed Ordering capability defined in the *PCI Express Base r1.0a*. However, is does support two PLX-Specific Relaxed Ordering modes:

- PEX 8524 Relaxed Ordering
- PEX 8524 Relaxed Completion Ordering – Silicon Revisions BB/BC Only

4.3.2.1 PEX 8524 Relaxed Ordering

The PEX 8524 does ***not support*** the TLP optional *Relaxed Ordering* bit, as specified in the *PCI Express Base r1.0a*, Table 2-23. By default, all packets entering from a specific port are dispatched to their respective destinations, based on strict ordering.

However, to remove unnecessary head-of-line blocking caused by PCI ordering in applications where ordering is not important, the PEX 8524 offers a PLX-Specific Relaxed Ordering mode. PLX-Specific Relaxed Ordering mode is enabled when any bit within a **PLX-Specific Relaxed Ordering Mode** register *Enable PLX Relaxed Ordering* field is set to 1:

- Port 0 or 8 – offset BFCh[7:0]
- Port 1 or 9 – offset BFCh[15:8]
- Port 10 – offset BFCh[23:16]
- Port 11 – offset BFCh[31:24]

In general, each port has 8 TCs to which it can map.

The ingress scheduler on a specific port (for a specific Traffic Class) selects packets without using ordering requirements and dispatches the packets to the egress ports. If using the Relaxed Ordering feature, ensure that it is used only for packets of a specific Traffic Class. This allows those packets to be distinguished from packets on other Traffic Classes in which the Relaxed Ordering feature is not enabled.

After the packets reach the egress ports, strict ordering is used in these queues, irrespective of the bits set on the ingress port.

Refer to Section 8.3.2.3, "PLX-Specific Relaxed Ordering," for further details.

4.3.2.2 PEX 8524 Relaxed Completion Ordering – Silicon Revisions BB/BC Only

The PEX 8524 provides a Relaxed Completion Ordering feature that enables Completion transactions to pass enqueued Posted transactions that are blocked. This feature is available on VC0, and is enabled by setting the following bits in the Device-Specific Configuration space:

- **PLX-Specific Relaxed Ordering Enable** register *PLX-Specific Relaxed Ordering Enable* bit (Ports 0, 1, 8, 9, 10, and/or 11, offset 1F0h[20]) is set to 1, and
- **PLX-Specific Relaxed Completion Ordering (Ingress)** register Enable PLX-Specific Relaxed Completion Ordering bit (Port 0 or 8, offset BECh[0]) is set to 1, and
- Any bit within a **PLX-Specific Relaxed Ordering Mode** register *Enable PLX Relaxed Ordering* field is set to 1
  - Port 0 or 8 – offset BFCh[7:0]
  - Port 1 or 9 – offset BFCh[15:8]
  - Port 10 – offset BFCh[23:16]
  - Port 11 – offset BFCh[31:24]

In general, each port has 8 TCs to which it can map.

4.3.2.3 No Snoop Enable – Silicon Revisions BB/BC Only

In NT mode, the PEX 8524 provides a No Snoop Disable feature to force the *No Snoop* attribute bit in the packet header to 0, for all packets transferred between the NT Link and Virtual Interfaces (across the NT boundary, in both directions). This capability can be used to handle cache coherency-related issues in a system. To enable this feature, set the **Ingress Control** register No Snoop Disable bit (offset 660h[24]) to 1.

4.4 Non-Transparent Bridging Implementation

The PEX 8524 supports Non-Transparent (NT) bridge functionality, which is used to implement High-Availability systems or Intelligent I/O modules using PCI Express technology. The following discusses the basic Non-Transparent bridging concept, as it applies to a PCI Express system.

NT bridges allow systems to isolate address spaces by appearing as an endpoint to the Host. An NT bridge exposes a Type 0 CSR header and forwards transactions from one domain to the other, using address translation. An NT bridge is used to connect two independent address/host domains. The NT bridge includes **Doorbell** registers for transmitting interrupts from one side of the bridge to the other. The bridge also includes **Scratchpad** registers, accessible from both domains for inter-host communication. The PEX 8524 PCI Express switch, with a single port configured to operate in NT Bridge mode, supports two system models:

- Intelligent Adapter Mode
- Dual-Host Mode

The PEX 8524 switch initial operating mode is determined by the STRAP_MODE_SEL[1:0] balls. The mode can later be changed by the serial EEPROM, by writing to the **Debug Control** register *Mode Select* field.

4.4.1 Intelligent Adapter Mode

The use of Non-Transparent bridges in PCI systems is well established for supporting intelligent adapters in enterprise and multi-host systems. The same concept is used in PCI Express bridges and switches.

In Figure 4-7, there are two Type 0 CSR headers in the Non-Transparent PCI-to-PCI bridge. The one nearer the internal virtual bus is referred to as the *Virtual Interface*. The one nearer the PCI Express link is referred to as the *Link Interface*.

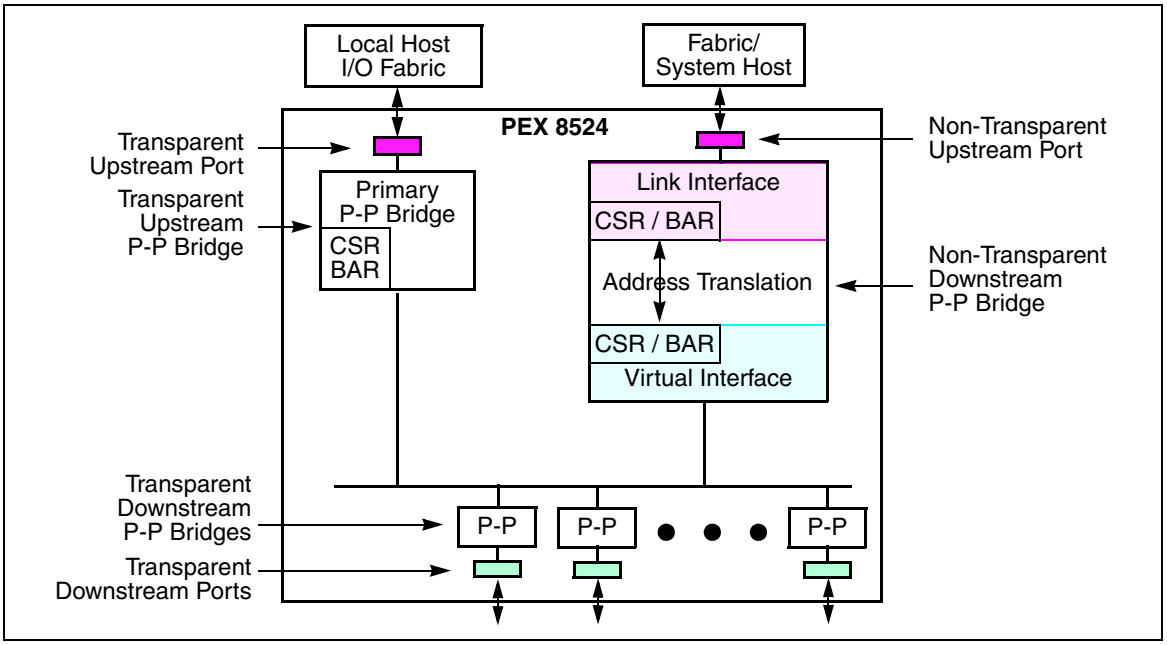
In Intelligent Adapter mode, the NT Port Link Interface is connected to the System domain. The System Host manages only the NT Port Link Interface Type 0 function. The Local Host manages all PEX 8524 Transparent Port Type 1 and NT Port Virtual Interface Type 0 functions. Cross-domain traffic is routed through an Address Translation mechanism. (Refer to Section 12.1.6, "Address Translation.")

After power-up, the PEX 8524 Non-Transparent Type 1 ports, including the NT Port Virtual Interface, are enumerated by the Local Host connected to the PEX 8524 upstream port. The Local Host enables and resizes the **Base Address** registers (BARs) by programming the **NT Port Link Interface BAR Setup/Limit** registers, before the System Host assigns resources for these BARs. This behavior is changed with serial EEPROM initialization.

After the Local Host finishes its enumeration, it enables the NT Port Link Interface to be enumerated by the System Host connected to the interface. The NT Port Link Interface Retries the System Host Configuration transaction until the Local Host enables the NT Port Link Interface to process the System Host Configuration transaction. The **Debug Control** register *Virtual Interface Access Enable* bit (offset 1DCh[28]) enables access to the Virtual Interface Configuration registers. The *Link Interface Access Enable* bit (offset 1DCh[29]) enables access to the Link Interface Configuration registers. These bits do not affect normal Memory, Memory-Mapped CSRs, nor I/O-Mapped CSR transactions.

Intelligent Adapter mode does ***not support*** Host-Failover applications.

Figure 4-7. PEX 8524 Intelligent Adapter Software Model



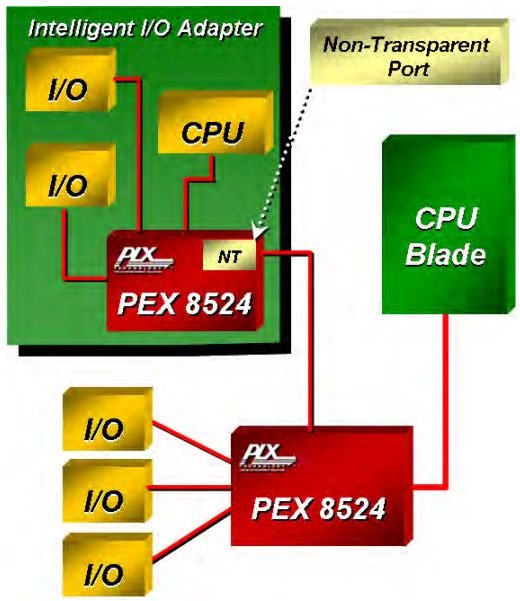
4.4.2 Dual-Host Mode

The PEX 8524 can concurrently support two hosts. The PEX 8524 transparent upstream port is connected to the Active Host, and the NT Port Link Interface is connected to the Backup Host.

After power-up, the Active and Backup Hosts can enumerate their domain at the same time, which is modified using the serial EEPROM. The serial EEPROM is necessary to enable or resize the **BAR Setup/Limit** registers.

Dual-Host mode **supports** Host-Failover applications, described in Section 4.4.2.1.

Figure 4-8. Dual-Host Model



4.4.2.1 Host-Failover Application

The Host-Failover application is based on the basic Dual-Host configuration. The Active Host periodically transmits Heartbeat messages, by way of the switch, to the Backup Host to indicate that it remains active. When the Backup Host fails to receive Heartbeat messages before its Fail Detect Timer expires, it starts the failover process. The Backup Host halts cross-domain traffic before it starts the failover. The Backup Host uses the Memory-Mapped access to the **PCI Express Capability List and Capabilities** register (offset 68h) to execute the failover. The Backup Host performs the following procedure to take control:

1. Failover detected.
2. Upstream port demotion.
3. NT Port (self-) promotion as a new upstream port.

Note: *Refer to Section 14.2.4, "Host-Failover Application," for further details.*

Dynamic swapping of the upstream and NT Ports is supported on Ports 0 and 8.

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Chapter 5 Reset and Initialization

5.1 Reset Overview

Reset is a mechanism that returns a device to its initial state. Hardware or software mechanisms can trigger a reset. The re-initialized states following a reset vary, depending on the reset type and condition.

The *PCI Express Base r1.0a*, Section 6.6, defines the hardware mechanism as *Fundamental Reset*. Two actions can trigger a Fundamental Reset:

- Cold Reset
- Warm Reset

There is also a type of reset triggered by an in-band signal from an upstream PCI Express link to all its downstream ports, which is called a Hot Reset.

There is also a *Secondary Bus Reset*. Any PCI-to-PCI bridge can reset its downstream hierarchy by setting the **Bridge Control** register (**BCR**) *Secondary Bus Reset* bit (offset 3Ch[22]=1).

Upon exit from a Cold or Warm Reset, all port configurations, port registers, and state machines are set to initial (start-up) values, as specified in Section 5.2, "Initialization Procedure."

5.1.1 Cold Reset

A Cold Reset is a Fundamental Reset that occurs following a proper PEX 8524 power-on. When the PEX_PERST# signal is held Low following the proper application of power to the device, a Fundamental Reset occurs.

A Fundamental Reset initializes the entire PEX 8524 device (*such as* configuration information, clocks, state machines, registers, and so forth).

When power is removed from the device, or travels outside the required ranges, all settings and configuration information is lost. The device must cycle through the entire Initialization Procedure after power is accurately re-applied.

5.1.2 Warm Reset

The Fundamental Reset mechanism can also be triggered by driving the PEX 8524 hardware Reset signal (PEX_PERST#) Low, without the removal and re-application (recycling) of power. This is considered a Warm Reset.

PEX_PERST# can be controlled by on-board toggle switches or other external hardware resets to the device. The device must cycle through the entire Initialization Procedure after the PEX_PERST# input signal is returned to High.

5.1.3 Hot Reset

A Hot Reset is equivalent to a traditional Software Reset. Triggered by an in-band signal from an upstream PCI Express link to all downstream ports, a Hot Reset causes all ports that are downstream from the initiating port to set their registers and state machines to initial values. This type of reset does not require power cycling, nor does it cause PEX 8524 port re-configuration. However, a Hot Reset:

- Causes all TLPs held in the PEX 8524 to be dropped
- Returns all State machines to their initial (default) values
- Returns all Non-Sticky register bits to their initial (default) conditions (refer to Table 11-3, "Register Types, Grouped by User Accessibility," for further details regarding Sticky register bit types)

A Hot Reset is triggered by the following actions:

- Physical Layer (at the upstream port) receives a reset through a training sequence leading to a Hot Reset
- Upstream PCI Express port enters the *DL_Inactive* state, which has the same effect as a Hot Reset

Note: *In the following sections, the terms "virtual PCI-to-PCI bridge" and "port" refer to a given Station port.*

5.1.3.1 Hot Reset Propagation

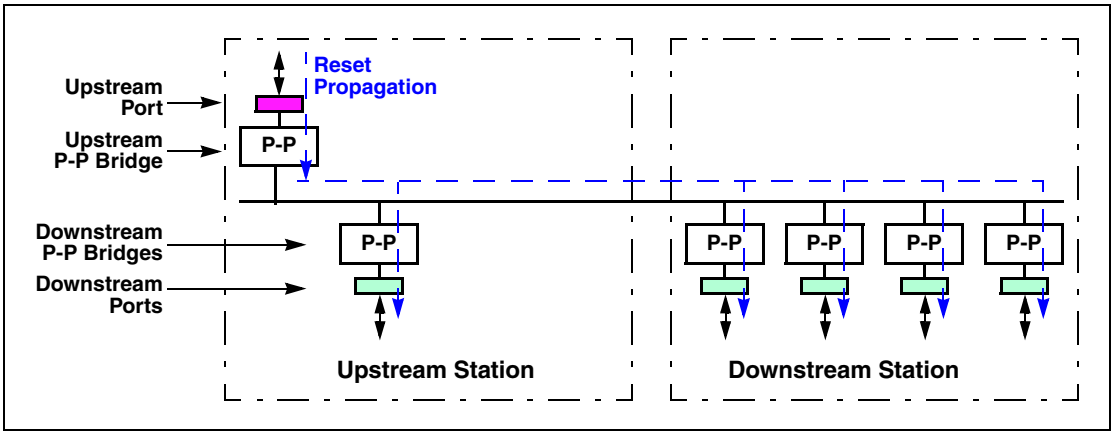
Reset is propagated to a downstream PCI Express device through the PCI Express link, using the Physical Layer Hot Reset mechanism (*that is*, a Reset bit in the Training Sequence Ordered-Set from the upstream device is set).

PCI Express views a *switch* as a hierarchy of virtual PCI-to-PCI bridges.

An example of reset propagation across the PEX 8524 switch is illustrated in Figure 5-1. Upon receiving a Hot Reset from the upstream PCI Express link, the virtual primary PCI-to-PCI bridge propagates the reset to virtual secondary PCI-to-PCI bridges in the upstream and downstream ports. Each virtual secondary PCI-to-PCI bridge propagates the reset to its downstream links, and initializes its internal states to initial/default conditions.

A Hot Reset does not impact Clock Logic, Port Configuration, nor Sticky register bits.

Figure 5-1. PEX 8524 System Reset Propagation Example



5.1.3.2 Hot Reset Disable

The PEX 8524 includes a configuration option – **Debug Control** register *Upstream Port Hot Reset and Link Down Reset Propagation Disable* bit (Port 0, offset 1DCh[20]) – to ignore the Hot Reset sequence from the upstream PCI Express link. Setting this bit enables the upstream port to ignore a Hot Reset training sequence, blocks the switch from manifesting an internal reset due a DL_Down event, and prevents the downstream ports from issuing a Hot Reset to downstream devices when either a Hot Reset or DL_Down event occurs on the upstream link.

5.1.4 Secondary Bus Reset

When the **upstream** PCI-to-PCI bridge **Bridge Control** register (**BCR**) *Secondary Bus Reset* bit (offset 3Ch[22]) is set to 1, all ports that are downstream from that port are reset to their initial/default states. The downstream ports propagate an in-band Hot Reset to their respective downstream links. In addition, the downstream ports' Configuration Space registers (CSRs) are re-initialized. The upstream PCI-to-PCI bridge (upstream port) and its CSRs are not affected; however, the queues to/from all downstream ports are drained, because their upstream-to-downstream virtual connections are re-initialized.

When the **downstream** PCI-to-PCI bridge **BCR** *Secondary Bus Reset* bit is set to 1, a Hot Reset is transmitted to its single downstream port, which resets all devices downstream from that port to their initial/default states. The reset port drops any incoming traffic. All other PEX 8524 traffic not flowing to the reset port is unaffected.

The downstream links are held in reset until software removes the condition by clearing the **BCR** *Secondary Bus Reset* bit. The PHY layer of the downstream port in question propagates the reset condition in-band to its downstream link, and remains in the Hot Reset state until the reset condition (BCR) is cleared. The Transaction Layer draining of non-empty queues to/from the affected port(s) is handled in a manner similar to the case of that port proceeding to the *DL_Inactive* state, as defined in the *PCI Express Base r1.0a*, Section 2.9.

5.2 Initialization Procedure

Upon exit from a Fundamental Reset, the PEX 8524 initialization process is started. There are two or three steps in the process, depending on the availability of an external initialization serial EEPROM.

The initialization sequence executed is as follows:

1. PEX 8524 reads the Strapping signal balls to determine System mode, upstream port, and lane configuration of all ports.
2. If the serial EEPROM is present (EE_PR# ball is Low), serial EEPROM data is downloaded to the PEX 8524 Configuration registers. The configuration from the Strapping signal balls can be changed by serial EEPROM data.
3. After the configuration from the Strapping signal balls and/or serial EEPROM completes, the Physical Layer of the configured ports attempts to bring up the links. After both components on a link enter the initial Link Training state, they proceed through Physical Layer Link initialization and then through Flow Control initialization for VC0, preparing the Data Link and Transaction Layers to use the link. Following Flow Control initialization for VC0, it is possible for VC0 Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) to be transmitted across the link.

5.2.1 Default Port Configuration

The default upstream port selection and overall port lane-width configuration is determined by Strapping signal ball levels. All Strapping balls must be tied High to VDD33 or Low to VSS (GND), which sets the default device configuration. (Refer to Section 3.4.4, "Strapping Signals – 680-Ball PBGA," or Section 3.5.4, "Strapping Signals – 644-Ball PBGA.") Some of these settings can be changed by downloading serial EEPROM data, or through initial port negotiation.

5.2.2 Default Register Initialization

Each PEX 8524 port defined in the Port Configuration process has a set of assigned registers that control port activities and status during normal operation. These registers are set to default/initial settings, as defined in:

- Chapter 11, "PEX 8524 Transparent Mode Port Registers"
- Chapter 15, "NT Port Virtual Interface Registers"
- Chapter 16, "NT Port Link Interface Registers"

Following a Fundamental Reset, the basic PCI Express Support registers are initially set to the values specified in the *PCI Express Base r1.0a*. The **PLX-Specific** registers are set to the values specified in their register description tables. These registers can be changed by loading new data with the attached serial EEPROM, or by way of Transaction Layer Configuration Space register (CSR) accesses using Configuration or Memory Writes; however, registers identified as Read-Only (RO) ***cannot*** be modified by Configuration nor Memory Write requests.

The PEX 8524 supports three mechanisms for accessing registers by way of the Transaction Layer, as described in the following sections:

- Section 11.4.1, "PCI r2.3-Compatible Configuration Mechanism"
- Section 11.4.2, "PCI Express Enhanced Configuration Mechanism"
- Section 11.4.3, "PLX-Specific Memory-Mapped Configuration Mechanism"

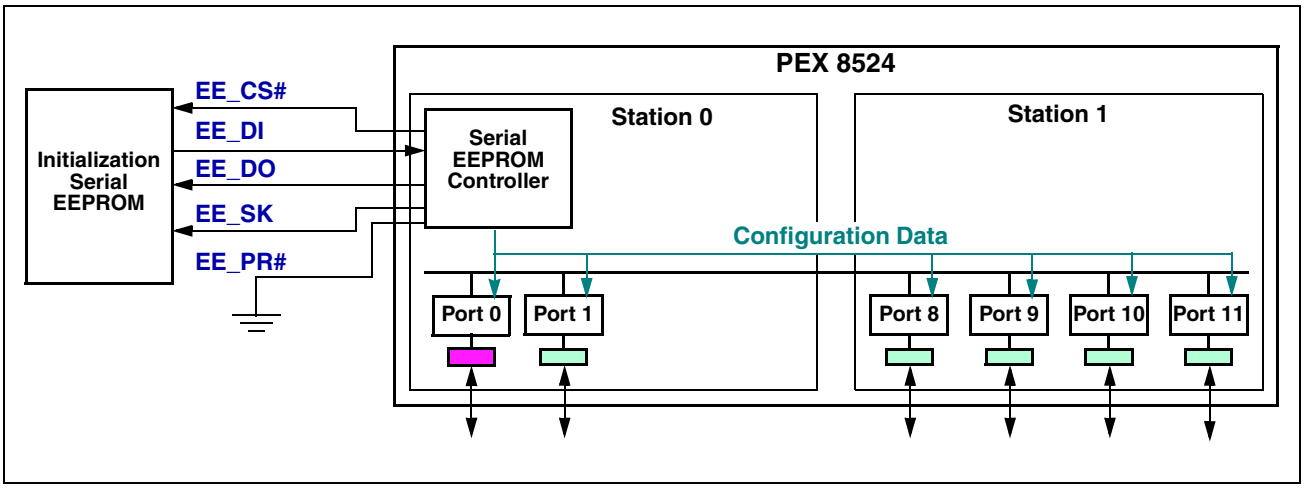
5.2.3 Serial EEPROM Initialization

Note: *For further details, refer to the PEX 85XX EEPROM – PEX 8532/8524/8516 Design Note.*

The on-chip Serial EEPROM Controller is integrated in PEX 8524 Station 0, as illustrated in Figure 5-2. The Controller performs a serial EEPROM download when a serial EEPROM is present, as indicated by the EE_PR# Strapping ball = Low, and when one of the following events occur:

- PEX_PERST# is returned High, following a Fundamental Reset (*such as,* a Cold or Warm Reset)
- Hot Reset is received at the upstream port (downloading upon this event can be optionally disabled), by setting the Port 0 register at offset 1DCh[16, 17, and/or 20]
- Upstream port exits a DL_Down condition (downloading upon this event can be optionally disabled), by setting the Port 0 register at offset 1DCh[16, 17, and/or 20]

Figure 5-2. PEX 8524 Serial EEPROM Connections



5.2.3.1 Configuration Data Download

Serial data is downloaded from the serial EEPROM and converted to parallel data, which is then routed to the PEX 8524 ports. The Serial EEPROM Controller generates a 7.8-MHz EE_SK signal and reads a total of 3,044 DWords from the serial EEPROM, which represents the data necessary to initialize the PEX 8524 registers.

The serial EEPROM Memory map reflects the basic PEX 8524 register map, for registers discussed in the following chapters:

- Chapter 11, "PEX 8524 Transparent Mode Port Registers"
- Chapter 15, "NT Port Virtual Interface Registers"
- Chapter 16, "NT Port Link Interface Registers"

Because these registers are duplicated for each port, the serial EEPROM data starts with Station 0, Port 0, offset 00h, and progresses through the registers for all six ports, in sequence. Certain general device registers are appended at the end of the space for Port 0, and various Address spaces are skipped due to ***unused/reserved*** register space. A detailed description of the serial EEPROM Memory map is provided in Appendix A.

While downloading the data, the PEX 8524 generates a CRC value from the Read data. When the serial EEPROM download is complete, the generated CRC value is compared to a CRC value stored in the last DWord location of the serial EEPROM. If the CRC values match, the PEX 8524 sets the **Serial EEPROM Status** register *Serial EEPROM Present* field (Port 0, offset 260h[17:16]) to 01b (serial EEPROM download complete and serial EEPROM CRC is validated).

If the CRC fails:

- The **Serial EEPROM Status** register *Serial EEPROM Present* field is set to 11b to indicate that the serial EEPROM is present but a CRC error was detected, and,
- If the **Serial EEPROM Status** register *CRC Disable* bit (Port 0, offset 260h[21]) value is 0 (default), all registers that are serial EEPROM-programmable are reset/initialized to default values, or,
- If the **Serial EEPROM Status** register *CRC Disable* bit value is 1, the CRC error is ignored and all registers that are serial EEPROM-programmable are initialized with the values that were downloaded from the serial EEPROM.

Caution: ***Setting the CRC Disable bit is strongly discouraged because a corrupted serial EEPROM download could render the PEX 8524 inoperable until a Fundamental Reset is applied (by asserting PEX_PERST# input).***

During the serial EEPROM download, the Class Code 060400h is monitored. If the correct code is not found, the download is terminated.

Note: *It is the system software's responsibility to verify whether the serial EEPROM download completes without error.*

5.3 PCI Express Configuration, Control, and Status Registers

The PCI Express Configuration, Control, and Status registers that can be initialized are discussed in the following sections. However, this is not a complete list of programmable registers. For a complete list, refer to Chapter 11, "PEX 8524 Transparent Mode Port Registers," and Appendix A, "Serial EEPROM Memory Map."

- Section 5.3.1, "Selecting Configuration Values Using Serial EEPROM"
- Section 5.3.2, "Selecting Upstream Port Using Serial EEPROM"
- Section 5.3.3, "Setting Port Configuration Using Serial EEPROM"
- Section 5.3.4, "Power Management Parameters Using Serial EEPROM"
- Section 5.3.5, "Message Signaled Interrupt Capability Using Serial EEPROM"
- Section 5.3.6, "PCI Express Capability Using Serial EEPROM"
- Section 5.3.7, "Device Serial Number Extended Capability Using Serial EEPROM"
- Section 5.3.8, "Power Budgeting Extended Capability Using Serial EEPROM"
- Section 5.3.9, "Virtual Channel Extended Capability Using Serial EEPROM"
- Section 5.3.10, "Advanced Error Reporting Capability Using Serial EEPROM"

The Device-Specific registers cannot be accessed by Configuration requests; however, software can access these registers with Memory requests.

5.3.1 Selecting Configuration Values Using Serial EEPROM

Configuration values, for the registers defined in Section 11.6, "Configuration Header Registers," can be changed using the serial EEPROM, with the exception of those fixed by the *PCI Express Base r1.0a* or ***not supported*** by the PEX 8524.

5.3.2 Selecting Upstream Port Using Serial EEPROM

The **Debug Control** register *Upstream Port Number* field (offset 1DCh[11:8]) values defined in Table 5-1 determine the upstream port selection.

Table 5-1. Debug Control Register *Upstream Port Number* Field (Offset 1DCh[11:8]) Values

Station 0	Station 1
0h = Port 0	8h = Port 8
1h = Port 1	9h = Port 9
2h to 7h = ***Reserved***	Ah = Port 10
	Bh = Port 11
	Ch to Fh = ***Reserved***

5.3.3 Setting Port Configuration Using Serial EEPROM

To use the serial EEPROM to set the port configuration, program the following registers:

- **Port Configuration** register Port Configuration field – Sets the port configuration (Ports 0 and 8, offset 224h[4:0])
- **Debug Control** register – Sets the Port Number and parameters for the upstream port

The **Port Configuration** register *Port Configuration* field value determines the number of enabled ports per station, as well as the maximum link widths of those ports, as defined in Table 5-2.

Table 5-2. PEX 8524 Port Configurations

Port Configuration Register Value[a] (Port 0 or 8, Offset 224h[4:0])	Station 0 [Lanes/SerDes]/ Port[b]		Station 1 [Lanes/SerDes]/Port[b]			
	Port 0	Port 1	Port 8	Port 9	Port 10	Port 11
0h	x4 [0-3]	x4 [4-7]	x4 [16-19]	x4 [20-23]	x4 [24-27]	x4 [28-31]
1h	–[c]	–	x16 [16-31][d]	–	–	–
2h	x8 [0-7]	–	x8 [16-23]	x8 [24-31]	–	–
3h	–	–	x8 [16-23]	x4 [24-27]	x4 [28-31]	–
4h	–	–	x8 [16-23]	x4 [24-27]	x2 [28-29]	x2 [30-31]
5h	–	–	x8 [16-23]	x2 [24-25]	x2 [26-27]	x4 [28-31]
6h	–	–	x8 [16-23]	x2 [24-25]	x4 [26-29]	x2 [30-31]

a. The PEX 8524 can be re-configured by link-width negotiation to smaller widths of x4, x2, or x1.

b. The lanes are assigned to each enabled port in sequence, as indicated in [brackets].

*c. Configuration value and port combinations with "–" (no data) are **reserved**.*

d. Ports 8 and 9 can be combined to create a 16-lane (x16) port.

5.3.4 Power Management Parameters Using Serial EEPROM

Power Management parameters, for the registers defined in Section 11.7, "Power Management Capability Registers," can be changed using the serial EEPROM, with the exception of those fixed by the *PCI Express Base r1.0a* or ***not supported*** by the PEX 8524.

5.3.5 Message Signaled Interrupt Capability Using Serial EEPROM

Message Signaled Interrupt (MSI) Capability parameters, for the registers defined in Section 11.8, "Message Signaled Interrupt Capability Registers," can be changed using the serial EEPROM, with the exception of those fixed by the *PCI Express Base r1.0a* or ***not supported*** by the PEX 8524.

5.3.6 PCI Express Capability Using Serial EEPROM

PCI Express Capability parameters, for the registers defined in Section 11.9, "PCI Express Capability Registers," can be changed using the serial EEPROM, with the exception of those fixed by the *PCI Express Base r1.0a* or ***not supported*** by the PEX 8524.

5.3.6.1 Configuring Hot Plug Controller Slot Power-Up Sequence Features with Serial EEPROM

Refer to Section 9.4.1.1, "Configuring Hot Plug Controller Slot Power-Up Sequence Features with Serial EEPROM," for details.

5.3.7 Device Serial Number Extended Capability Using Serial EEPROM

Device Serial Number Extended Capability parameters, for the registers defined in Section 11.10, "Device Serial Number Extended Capability Registers," can be changed using the serial EEPROM.

5.3.8 Power Budgeting Extended Capability Using Serial EEPROM

Power Budgeting Extended Capability parameters, for the registers defined in Section 11.11, "Power Budgeting Extended Capability Registers," can be changed using the serial EEPROM.

5.3.9 Virtual Channel Extended Capability Using Serial EEPROM

Virtual Channel Extended Capability parameters, for the registers defined in Section 11.12, "Virtual Channel Extended Capability Registers," can be changed using the serial EEPROM.

5.3.10 Advanced Error Reporting Capability Using Serial EEPROM

The PEX 8524 supports Advanced Error Reporting, as defined in the *PCI Express Base r1.0a*. Advanced Error Reporting Capability parameters, for the registers defined in Section 11.14, "Advanced Error Reporting Capability Registers," can be changed using the serial EEPROM.

5.3.11 PLX-Specific Registers

The following registers are unique to the PEX 8524 device, and are not referenced in PCI Express documentation. The PLX-Specific registers are organized into the following sections:

- Section 11.13.1, "Error Checking and Debug Registers"
- Section 11.13.2, "Physical Layer Registers"
- Section 11.13.3, "CAM Routing Registers"
- Section 11.13.4, "Ingress Control Registers"
- Section 11.13.5, "I/O CAM Base and Limit Upper 16 Bits Registers"
- Section 11.13.6, "Base Address Registers (BARs)"
- Section 11.13.7, "Shadow Virtual Channel (VC) Capability Registers"
- Section 11.13.8, "Ingress Credit Handler (INCH) Registers"
- Section 11.13.9, "Ingress One-Bit ECC Error Count Register"
- Section 11.13.10, "Relaxed Completion Ordering (Ingress) Register – Silicon Revisions BB/BC Only"
- Section 11.13.11, "Relaxed Ordering Mode (Ingress) Register"
- Section 11.13.12, "Internal Credit Handler (ITCH) VC&T Threshold Registers"

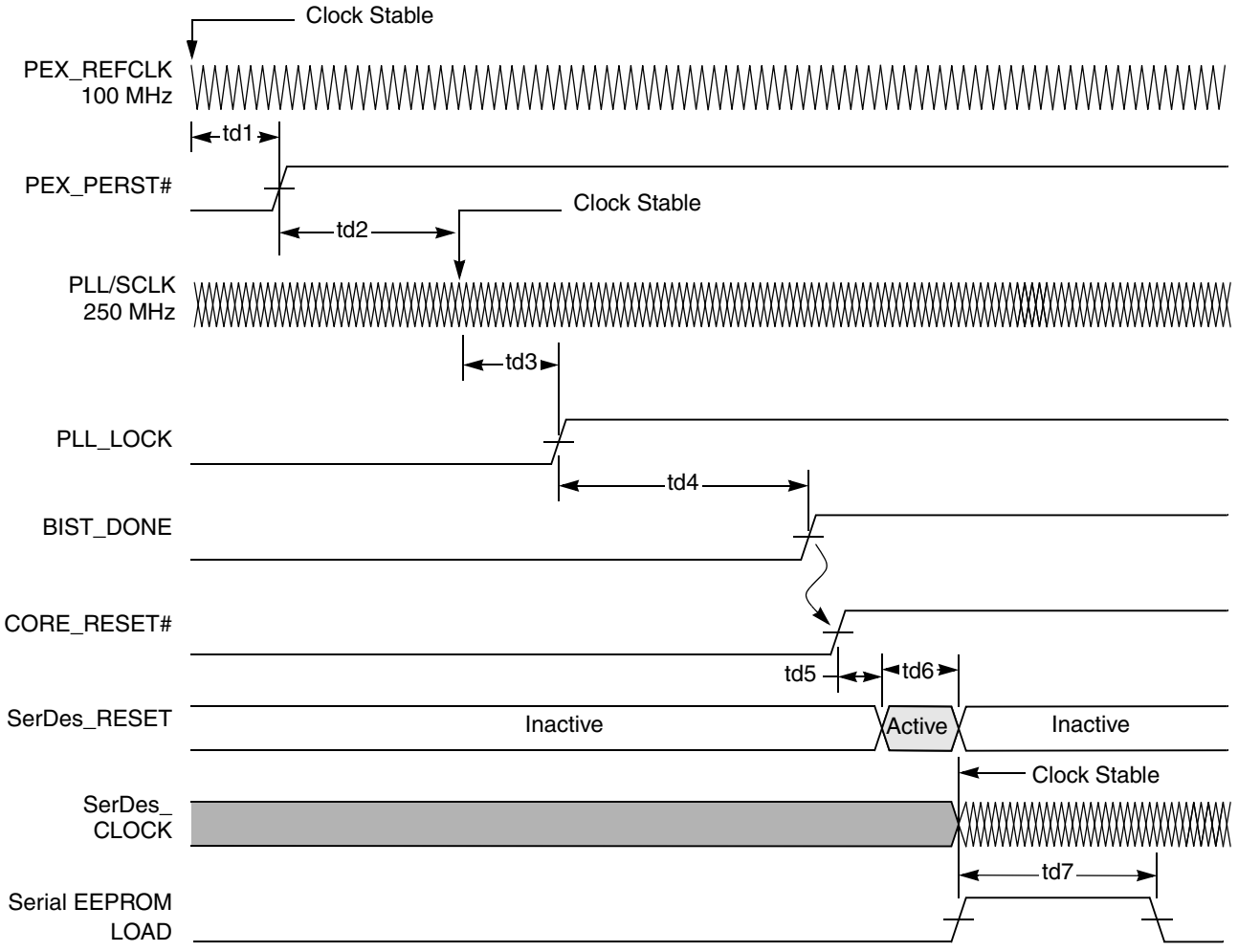
The Device-Specific registers cannot be accessed by Configuration requests; however, software can access these registers with Memory requests.

5.3.12 Reset and Clock Initialization Timing

Table 5-3. Reset and Clock Initialization Timing

Symbol	Description	Typical Delay
td1	REF Clock stable to PEX_Reset release time	100 µs
td2	PEX_Reset release to PLL Clock Stable and Reset de-bounce	1.32 ms
td3	Clock and Reset Stable to PLL Lock	125 µs
td4	PLL Lock to BIST Done time, which causes Core Reset release	4.5 ms
td5	Core Reset release to SerDes Resets active delay	10 µs
td6	SerDes Reset active time	60 µs
td7	Serial EEPROM load time	12.6 ms

Figure 5-3. Reset and Clock Initialization Timing



Chapter 6 Interrupts

6.1 Interrupt Support

The PEX 8524 supports the PCI Express interrupt model, which uses two mechanisms:

- INT*x* emulation
- Message Signaled Interrupt (MSI)

For Conventional PCI compatibility, the PCI INT*x* emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifics. The PCI INT*x* emulation mechanism virtualizes PCI physical Interrupt signals by using an in-band signaling mechanism.

In addition to PCI INT*x*-compatible interrupt emulation, the PEX 8524 supports the Message Signaled Interrupt (MSI) mechanism. The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r2.3*.

The following events are supported for interrupts:

- Hot Plug
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Presence Detect Changed
  - Command Completed
- Device-specific errors
  - ECC Error detected in internal packet RAM
  - Ingress Credit Underrun
  - Internal Error FIFO Overflow

6.1.1 PEX 8524 Interrupt Handling

The PEX 8524 provides an Interrupt Generation module with each port. The module reads the request for interrupts from different sources and generates an MSI or PCI-compatible Assert_INT*x*/ Deassert_INT*x* Interrupt message. The MSI supports a PCI Express edge-triggered interrupt, whereas Assert_INT*x* and Deassert_INT*x* Message transactions emulate PCI level-triggered interrupt signaling. The System Interrupt Controller functions include:

- Sensing Interrupt events
- Signaling the interrupt, by way of the INT*x* mechanism, and setting the Interrupt Status bit
- Signaling interrupt by way of the MSI mechanism
- Handling INT*x*-type Interrupt messages from downstream devices

6.2 INT*x* Emulation Support

The PEX 8524 supports PCI INT*x* emulation, to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software. PCI INT*x* emulation virtualizes PCI physical Interrupt signals, by using the in-band signaling mechanism.

PCI **Interrupt** registers (the **Interrupt** registers defined in the *PCI r2.3*) are supported. The *PCI r2.3* **Command** register *Interrupt Disable* and **Status** register *Interrupt Status* bits are also supported (offset 04h[10, 19], respectively).

Although the *PCI Express Base r1.0a* provides INTA#, INTB#, INTC#, and INTD# for INT*x* signaling, the PEX 8524 uses only INTA# for internal Interrupt message generation, because it is a single-function device. However, incoming messages from downstream devices can be of INTA#, INTB#, INTC#, or INTD# type. Internally generated INTA# messages from the downstream port are also remapped and collapsed at the upstream port, according to the downstream port's Device Number, with its own Device Number and Received Device Number from the downstream device. When an interrupt is requested, the **Status** register *Interrupt Status* bit is set. If INT*x* interrupts are enabled [**Command** register *Interrupt Disable* and **Message Control** register *MSI Enable* bits (offsets 04h[10] and 48h[16], respectively) are cleared to 0], an Assert_INT*x* message is generated and transmitted upstream to indicate the port interrupt status. For each interrupt event, there is a corresponding Mask bit. The Interrupt request can be generated only when the Mask bit is not set. Software reads and clears the event and *Interrupt Status* bit after servicing the interrupt.

6.2.1 INT*x*-Type Interrupt Message Remapping and Collapsing

INT*x*-type Interrupt messages from downstream devices are directly forwarded to the upstream port, rather than being terminated and regenerated by the downstream port. The upstream port remaps and collapses the INT*x* message type received at the downstream port, based upon the downstream port's Device Number and Received INT*x* message Requester ID Device Number, and generates a new Interrupt message, according to the mapping defined in Table 6-1.

A downstream port transmits an Assert_INTA/Deassert_INTA message to the upstream port, due to a device-specific error.

Internally generated INT*x* messages always originate as type INTA messages, because the PEX 8524 is a single-function device. Internally generated Interrupt INTA messages from downstream ports are remapped at the upstream port to INTA, INTB, INTC, or INTD messages, according to the mapping defined in Table 6-1.

INT*x* messages from downstream devices and from internally generated Interrupt messages are ORed together to generate INTA, INTB, INTC, or INTD level-sensitive signals, and edge-detection circuitry in the upstream port generates the Assert_INT*x* and Deassert_INT*x* messages. The upstream port then forwards the new messages upstream, by way of its link.

Table 6-1. Downstream/Upstream Port INT*x* Interrupt Message Mapping

Device Number	At Downstream Port	By Upstream Port
0, 8	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
1, 9	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA
10	INTA	INTC
	INTB	INTD
	INTC	INTA
	INTD	INTB
11	INTA	INTD
	INTB	INTA
	INTC	INTB
	INTD	INTC

6.3 Message Signaled Interrupt (MSI) Support

One of the interrupt schemes supported by the PEX 8524 is the MSI mechanism, which is required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSIs are edge-triggered interrupts.

Note: *MSI and INTx are mutually exclusive. These interrupt mechanisms* ***cannot*** *be simultaneously enabled.*

6.3.1 MSI Operation

At configuration time, system software traverses the function Capability list. If a Capability ID of 05h is found, the function implements MSI. System software reads the MSI Capability Structure registers to determine function capabilities.

The PEX 8524 supports only one message for MSI; therefore, the **Message Control** register *Multiple Message Enable* and *Multiple Message Capable* fields (offset 48h[22:20, 19:17], respectively) are always cleared to 000b.

The **Message Control** register *MSI 64-Bit Address Capable* bit is enabled (offset 48h[23]=1), by default.

System software initializes the MSI Capability Structure registers with a system-specified message. If the MSI function is enabled, after an Interrupt event occurs, the Interrupt Generation module generates a DWord Memory Write to the address specified by the **Message Address[31:0]** register (offset 4Ch) contents. Data written is the contents of the **Message Data** register (offset 54h) lower two bytes and zeros (0) in the upper two bytes. Because the **Message Control** register *Multiple Message Enable* field (offset 48h[22:20]) field is always cleared to 000b, the Interrupt Generation module is not allowed to change the low-order bits of Message data.

When the Hot Plug and/or device-specific error events that caused the interrupt are serviced, the device can generate a new MSI Memory Write as a result of new events.

6.3.2 MSI Capability Registers

MSI Capability registers are described in Section 11.8, "Message Signaled Interrupt Capability Registers."

Chapter 7 Software Architecture

7.1 PEX 8524 Software Model

The PEX 8524 requires software support in the following areas:

- Switch configuration and configuration of all switch downstream links
- Moving data forward and back through the links
- Monitoring and servicing interrupts throughout the connected fabric
- Monitoring and adjusting performance-related mechanisms

The Configuration Mechanisms are straightforward and use Conventional PCI software structures and procedures to set up and identify all ports and links connected through the PEX 8524. The PEX 8524 supports an optional serial EEPROM interface, to simplify downloading of Configuration data to the switch. (Refer to Section 7.3.)

After the PEX 8524 and its links are set up, data can be routed through the PEX 8524, from one port to another. Responses and other communications are returned, by way of the same links, to the Initiator. The PEX 8524 is transparent to these Data transfers. (Refer to Section 7.3.1.3.)

When errors occur during data transfer due to data corruption in the internal RAM, or an external device violates its credits, an interrupt is returned, through the internal fabric to the Host, identifying the problem. It is the responsibility of the Host software to implement interrupt-service routines to handle the problem. (Refer to Chapter 6, "Interrupts," for further details.)

7.2 Configuration Mechanisms

The PEX 8524 supports the two Configuration mechanisms described in the *PCI Express Base r1.0a*:

- **PCI r2.3-Compatible Configuration Mechanism**

  This mechanism supports 100% binary compatibility with the *PCI r2.3* and its corresponding Bus Enumeration and Configuration software. The mechanism allows access to the lower 256 bytes (64 DWords) of the 4-KB Configuration space of each port. Access to the entire 4-KB Configuration Space requires 10 Address bits, which are defined in a PCI Express Configuration Request packet to include a 6-bit *Register Number* field and a 4-bit *Extended Register Number* field. The mechanism maps all six of its Address bits into the *Register Number* field, and clears the *Extended Register Number* field in the packet to 0h. Therefore, the mechanism cannot access the upper 960 DWords (PCI Express Extended Configuration space) that are implemented in each port.

- **PCI Express Enhanced Configuration Mechanism**

  This mechanism increases the size of available Configuration space and optimizes Configuration mechanisms. The mechanism allows access to the entire 4-KB Configuration space defined by the *PCI Express Base r1.0a*. Registers within the PEX 8524 that are defined by the *PCI Express Base r1.0a* can be accessed by this mechanism. PEX 8524 device-specific registers (which are not defined by the *PCI Express Base r1.0a*) cannot be accessed by this mechanism.

The PEX 8524 also supports a third Configuration mechanism:

- **PLX-Specific Memory-Mapped Configuration Mechanism**

  This mechanism supports access to all PEX 8524 registers, with the use of Memory Read and Memory Write commands and a 128-KB Address space that includes the 4-KB register sets of all ports, that is located at the Base address assigned to the upstream port's **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively).

From a software point of view, each PEX 8524 port is a PCI-to-PCI bridge. A PCI-to-PCI bridge must have uniquely assigned Bus and Device Numbers. The upstream port has its own Primary Bus Number, while all downstream ports share the same (internal) Bus Number and different Device Numbers.

For further details, refer to Section 11.4, "Register Access."

Note: *When enumerating the PEX 8524V, the BIOS detects eight, rather than six, PCI-to-PCI bridges. The downstream ports of two of these bridges (Ports 2 and 3) are not connected to PCI Express SerDes lanes. Hence, the ports associated with these bridges cannot be connected to endpoints.*

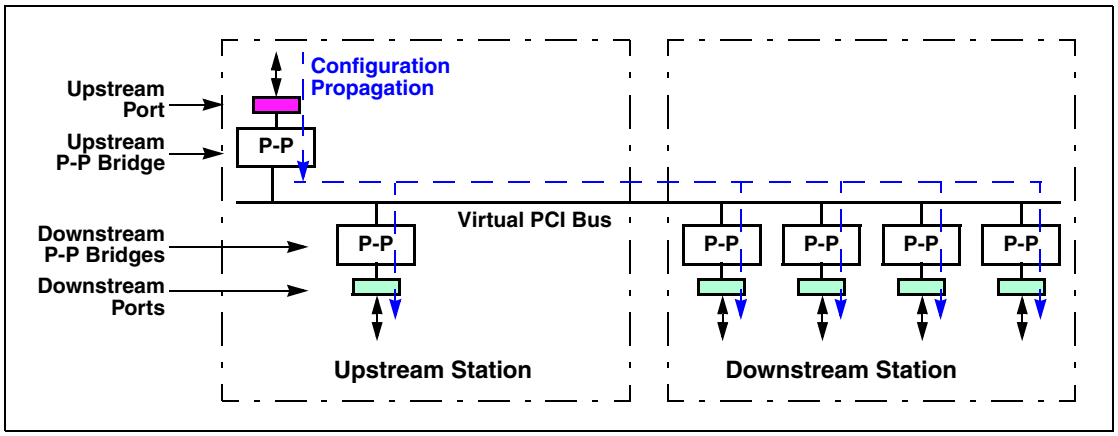
7.2.1 Software Configuration and Routing

Configuration requests must be routed from the Host, through the PEX 8524's upstream port. All Type 0 Configuration requests access the PEX 8524's upstream port Configuration registers.

The upstream port's PCI-to-PCI bridge forwards Type 1 Configuration requests from its upstream interface to its downstream interface. The Secondary Bus Number of the upstream port matches the Primary Bus Number of every downstream port. If the Bus Number value encoded in the Configuration Request matches the upstream port's Secondary Bus Number, the Configuration request is targeting a downstream port's registers, and therefore the upstream port converts the Type 1 Configuration request to a Type 0 Configuration request. To access the PCI-to-PCI bridge registers of a specific downstream port, the Device Number value encoded in this Configuration Request (which the upstream port converted to Type 0) must match the Device Number (Port Number) of the downstream port (the Device Number of a downstream port is always the same value as the designated Port number). If the Bus Number value encoded in the Configuration request matches the upstream port's Secondary Bus Number, the Configuration Request is targeting a downstream port's registers, and therefore, the upstream port converts the Type 1 Configuration Request to a Type 0 Configuration Request. To access the PCI-to-PCI bridge registers of a specific downstream port, the Type 1 Configuration request Bus Number value must match the upstream port's Secondary Bus Number, and the Device Number must match the enabled downstream port's Device Number. All other Device Numbers are non-existent devices, and the Configuration request terminates with an Unsupported Request (UR) completion.

To configure additional devices in the PCI hierarchy, the switch downstream ports must have their Secondary and Subordinate Bus Numbers set. Any match on a downstream port PCI-to-PCI bridge's Secondary Bus Numbers results in the PEX 8524 converting the incoming Type 1 Configuration request to an outgoing Type 0 Configuration request, and the Device Number must be 0.

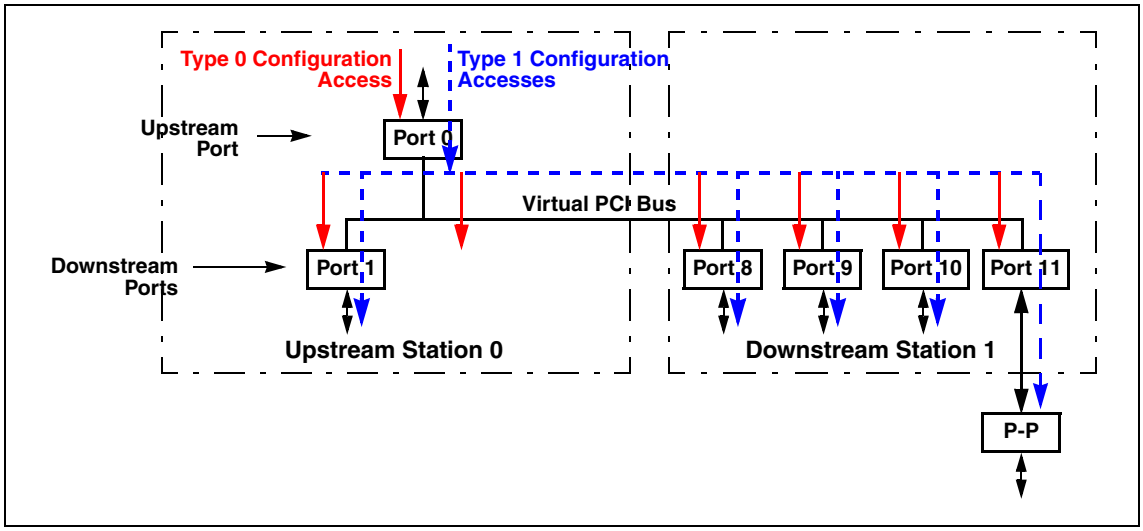
Figure 7-1. PEX 8524 System Configuration Propagation



7.3 Sample Configuration Procedure

Consideration must be given to the configuration procedure when setting up and initializing a PEX 8524 switch. Certain items are processed by initial hardware configuration, connections, and operating selections. The PCI/PCI-Express Configuration software can be written from the Host, by way of the upstream port to all downstream ports and their links, or from a serial EEPROM, by way of the serial EEPROM interface. Figure 7-2 illustrates an example of PEX 8524 system configuration.

Figure 7-2. PEX 8524 System Configuration Example



Note: *In Figure 7-2, Port 0 is designated as the upstream port; however, any port can be designated as the upstream port.*

The sequence executed to set up and initialize a PEX 8524 switch is as follows:

1. Ports and lanes, per port:
   - Refer to Section 4.1.2.1, "Port Combinations," for options
   - PEX 8524 must be connected to PCI Express-compatible devices
   - Strapping balls must be set to identify the selected port configuration
     - For Station 0, refer to STRAP_STN0_PORTCFG[4:0]
     - For Station 1, refer to STRAP_STN1_PORTCFG[3:0]
   - Serial EEPROM overrides the Strapping ball selections
2. Select the upstream port – Set Strapping balls STRAP_UPSTRM_PORTSEL[3:0].
3. Software/serial EEPROM programs the following registers for the **upstream port**:
   - **Primary Bus Number** – Identifies the upstream link (**Bus Number** register, offset 18h[7:0])
   - **Secondary Bus Number** – Identifies the switch internal Virtual PCI Bus (**Bus Number** register, offset 18h[15:8])
   - **Subordinate Bus Number** – Must be the last (largest) Bus Number in the downstream hierarchy of this upstream port (**Bus Number** register, offset 18h[23:16])
   - Set the **Command** register *Bus Master Enable* and *Memory Access Enable* bits (offset 04h[2:1], respectively)
   - **Base** and **Limit** registers – Combines the memory of all downstream devices into one large space, with the total size given by Limit - Base, and the Start address given by Base
   - **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively) (Base address for Memory-Mapped CSR access on the PEX 8524)
4. Software/serial EEPROM programs the following registers for the **downstream ports**:
   - **Primary Bus Number** – All downstream port numbers are the Device Numbers on the internal virtual PCI Bus (**Bus Number** register, offset [7:0])
   - **Secondary Bus Number** – Identifies the port's downstream link (**Bus Number** register, offset [15:8])
   - **Subordinate Bus Number** – Must be the last (largest) Bus Number in the downstream hierarchy of each downstream port (**Bus Number** register, offset 18h[23:16])
   - Set the **Command** register *Bus Master Enable* and *Memory Access Enable* bits (offset 04h[2:1], respectively)
   - **Base** and **Limit** registers – Combines the memory of all downstream devices into one large space, with the total size given by Limit - Base, and the Start address given by Base

On the upstream port, the primary side is accessed by a Type 0 Configuration access. The downstream ports are accessed with a Type 1 Configuration access on the primary side of the upstream port, with the Bus Number of each transaction equal to the upstream port Secondary Bus Number (Virtual PCI Bus).

7.3.1 Switch Device Number Assignment Example

The following is an example of how to access the PEX 8524's upstream port and downstream ports. Assume that the PEX 8524 consists of six ports, with one x4 upstream (default is Port 0) and five x4 downstream ports (Ports 1, 8, 9, 10, 11). Further assume that the upstream Bus Number is 1, and that each downstream port uses only one Bus Number, and that bus numbering is linear.

A diagram of the system is illustrated in Figure 7-2.

- The upstream port (which is configured as Port 0 with 8 lanes for this example), by default, and is assigned a primary Bus Number of 1 and a secondary Bus Number of 2. With four of the downstream ports each having one bus and a fifth downstream port having two buses, the Subordinate Bus Number is 2 + (4 * 1) + (1 * 2) = 8. The Device Number, regardless of which port is the upstream port, is always 00h.
- Port 1 registers are accessed with a Type 1 Configuration transaction:
  - Bus Number is the internal Virtual PCI Bus (upstream port Secondary Bus Number, 2)
  - Device Number is 01h
  - Function Number to be 000b
- Port 8 registers are accessed with a Type 1 Configuration transaction:
  - Bus Number is 2
  - Device Number is 08h
  - Function Number is 000b
- Port 9 registers are accessed with a Type 1 Configuration transaction:
  - Bus Number is 2
  - Device Number is 09h
  - Function Number is 000b
- Port 10 registers are accessed with a Type 1 Configuration transaction:
  - Bus Number is 2
  - Device Number is 0Ah
  - Function Number is 000b
- Port 11 registers are accessed with a Type 1 Configuration transaction:
  - Bus Number is 2
  - Device Number is 0Bh
  - Function Number is 000b

7.3.1.1 Configuration Register Programming Sequence

Registers that are defined by PCI-SIG Specifications can be accessed by Configuration mechanisms or Memory command; device-specific registers can be accessed by Memory command, but not by Configuration mechanisms (except for limited, indirect access through the NT Port Cursor Mechanism Control Registers, when Non-Transparent mode is enabled).

Upstream port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively) map internal registers for Memory-Mapped I/O access. **BAR0**, is a 128-KB, Non-Prefetchable BAR [the *Prefetchable* bit (bit 3) with default value 0 is ***not*** programmable]. Because **BAR0** maps to Non-Prefetchable Address space and the Address space is relatively small, it is recommended that **BAR0** be configured as a 32-bit BAR (default, with bits [2:1]=00b), rather than as a 64-bit BAR, to be mapped below the 4-GB Address Boundary space.

With **BAR0** configured as a 32-bit BAR, **BAR1** (which contains the upper 32 bits of address if **BAR0** is configured as a 64-bit BAR) must remain the default value 0h. If **BAR0** is configured as a 64-bit BAR and the **BAR1** value is 0h, a 64-bit access to **BAR0/1** returns an Unsupported Request (UR) error.

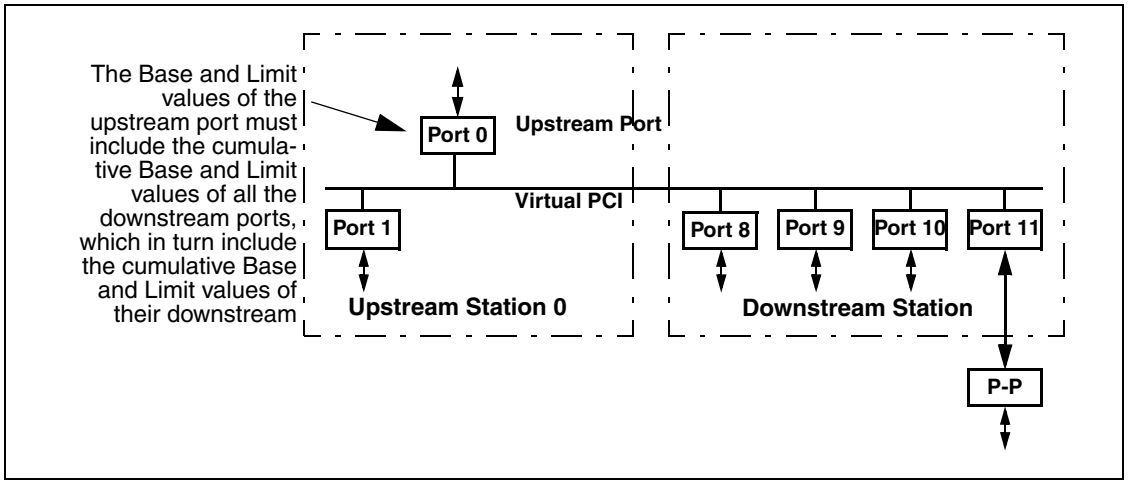
BAR0 and **BAR1** can be disabled by setting the **Ingress Control** register *Disable Upstream Port BAR0 and BAR1 Registers* bit (Ports 0 and 8, offset 660h[25]). *(**Note:** This feature is **not** available in Silicon Revision AA.)*

Register access must be 1 DWord (Byte Enables can select individual bytes). If a Memory Read requests more than 1 DWord, the PEX 8524 returns the first DWord, with a Completion status of *Completer Abort*. This error is flagged in the upstream port **Device Status** register (offset 70h) and **Uncorrectable Error Status** register *Completer Abort Status* bit (offset FB8h[15]).

To program access to internal registers:

1. Program the **Bus Number** register in the upstream port (offset 18h).
2. Program the **Bus Number** registers in all downstream ports (offset 18h).
3. Program the **Memory Base and Limit Address** register (offset 20h) in all downstream ports.
4. Program **BAR0/1** on the upstream port. (Optional, but necessary for Memory-Mapped access to internal registers.)
5. Program the **Memory Base and Limit Address** register (offset 20h) in the upstream port, ensuring the values claim all the space requested by all downstream ports.
6. Program the **Command** register *Bus Master Enable* and *Memory Access Enable* bits on all ports (offset 04h[2:1], respectively).

Figure 7-3. Programming Base and Limit Values



7.3.1.2 Sample Pseudo Code

The following sample pseudo code demonstrates how to configure the PEX 8524's upstream and downstream ports after they are previously discovered by system enumeration software.

```
CFGTYPE0 Write busnum 01,devicenum 00 function 0 address 18h data 0009_0201h
    // Primary Bus Number 01, secondary Bus Number 02 and subordinate Bus
    Number 09. At this step, the virtual PCI bus in the PEX 8524 gets the Bus
    Number 02. After this, any access to Bus Number 02 from the upstream port
    would refer to this bus.
CFGTYPE1 Write busnum 02,devicenum 01 function 0 address 18h data 0003_0302h
    // Primary Bus Number 02, secondary Bus Number 03 and subordinate Bus
    Number 03. an endpoint is attached to Port 1.
CFGTYPE1 Write busnum 02,devicenum 08 function 0 address 18h data 0005_0502h
    // Primary Bus Number 02,secondary Bus Number 05 and subordinate Bus
    Number 05. an endpoint attached to Port 8.
CFGTYPE1 Write busnum 02,devicenum 09 function 0 address 18h data 0006_0602h
    // Primary Bus Number 02,secondary Bus Number 06 and subordinate Bus
    Number 06. an endpoint attached to Port 9.
CFGTYPE1 Write busnum 02,devicenum 10 function 0 address 18h data 0007_0702h
    // Primary Bus Number 02,secondary Bus Number 07 and subordinate Bus
    Number 07. an endpoint attached to Port 10.
CFGTYPE1 Write busnum 02,devicenum 11 function 0 address 18h data 0008_0802h
    // Primary Bus Number 02,secondary Bus Number 08 and subordinate Bus
    Number 09. This means that we have a P2P bridge attached to Port 11 of
    PEX 8524 and only 1 more level of PCI hierarchy.
CFGTYPE1 Write busnum 02,devicenum 01 function 0 address 20h data 02FF_0200h
    // need 0200_0000h to 02FF_FFFFh memory space for Port 1.
CFGTYPE1 Write busnum 02,devicenum 08 function 0 address 20h data 04FF_0400h
    // need 0400_0000h to 04FF_FFFFh memory space for Port 8.
CFGTYPE1 Write busnum 02,devicenum 09 function 0 address 20h data 05FF_0500h
    // need 0500_0000h to 05FF_FFFFh memory space for Port 9.
CFGTYPE1 Write busnum 02,devicenum 10 function 0 address 20h data 06FF_0600h
    // need 0600_0000h to 06FF_FFFFh memory space for Port 10.
CFGTYPE1 Write busnum 02,devicenum 11 function 0 address 20h data 07FF_0700h
    // need 0700_0000h to 07FF_FFFFh memory space for Port 11.
CFGTYPE0 Write busnum 01,devicenum 00 function 0 address 20h data 07FF_0200h
    // the PEX 8524 will claim all Memory accesses from 0200_0000h to 07FF_FFFFh
    and would send it to the appropriate port. Any memory address not within any
    of the downstream Address spaces will go to the upstream port.
    // Now set the Bus Master Enable and Memory Access Enable bits on the upstream
    port and all downstream ports.
CFGTYPE0 Write busnum 01,devicenum 00 function 0 address 04h data 0000_0006h
CFGTYPE1 Write busnum 02,devicenum 01 function 0 address 04h data 0000_0006h
CFGTYPE1 Write busnum 02,devicenum 08 function 0 address 04h data 0000_0006h
CFGTYPE1 Write busnum 02,devicenum 09 function 0 address 04h data 0000_0006h
CFGTYPE1 Write busnum 02,devicenum 10 function 0 address 04h data 0000_0006h
CFGTYPE1 Write busnum 02,devicenum 11 function 0 address 04h data 0000_0006h
    // For each port configured above, registers 24h, 28h, and 2Ch can be
    programmed to enable a 64-bit device Prefetchable Memory space for
    downstream devices.
    // Memory-Mapped access of all configuration registers listed above
    can also be performed by programming the BAR0 and BAR1 registers
    (for 64-bit Memory spaces) for busnum 01, devicenum 00.
```

7.3.1.3 Sample Packet Transfer

When all ports are configured using the sample code provided in Section 7.3.1.2, the following occurs:

- 32-bit Memory transactions from the upstream port, destined between addresses 0200_0000h to 07FF_FFFFh, advance to the appropriate downstream port
- 32-bit Memory transactions from a downstream port, between addresses 0200_0000h to 07FF_FFFFh, advance to the appropriate downstream port (if the transactions are not within the Base-Limit range of that port)
- Transactions from a downstream port, outside the range of addresses 0200_0000h to 07FF_FFFFh and outside PEX 8524 Memory-Mapped Register space (refer to Section 7.3.2 for details regarding Register space), advance to the upstream port

7.3.2 Using Base Address Registers (BARs) to Access Registers

Configuration requests can access only those registers that are defined by the *PCI Express Base r1.0a*. These registers and the Device-Specific registers can all be accessed by Memory requests that target the Memory space defined by the upstream port **Base Address 0** and **Base Address 1** (**BAR0** and **BAR1**) registers (offsets 10h and 14h, respectively).

- Upstream port **BAR0** register requests 128-KB Memory space set aside for internal PEX 8524 registers.
- Optionally, the upstream port **BAR1** register can be used to place this internal register Memory space anywhere in 64-bit System Memory space.
- After the upstream port **BAR0** (and optionally, **BAR1**) register is programmed, all register locations inside the PEX 8524 can be accessed from any port, using either Memory requests or Configuration requests.
- Each port consumes 4 KB of Memory space for internal registers. Port 0 is at 0000h to 0FFFh, Port 1 is at 1000h to 1FFFh, Port 8 is at 8000h to 8FFFh, and so forth.

For example, if the upstream port **BAR0** register is programmed to 0100_0000h (using a Type 0 Configuration transaction) and the upstream port **Command** register *Memory Access Enable* bit is set (offset 04h[1]=1; again, programmed using a Type 0 Configuration transaction), then all PEX 8524 registers can be accessed using Memory-Mapped Register accesses.

The following sections describe information specific to Transparent and Non-Transparent modes.

7.3.2.1 Transparent Mode Registers

The formula to locate register addresses for Transparent ports is as follows:

```
BAR0 + (port * 1000h) + register_offset
```

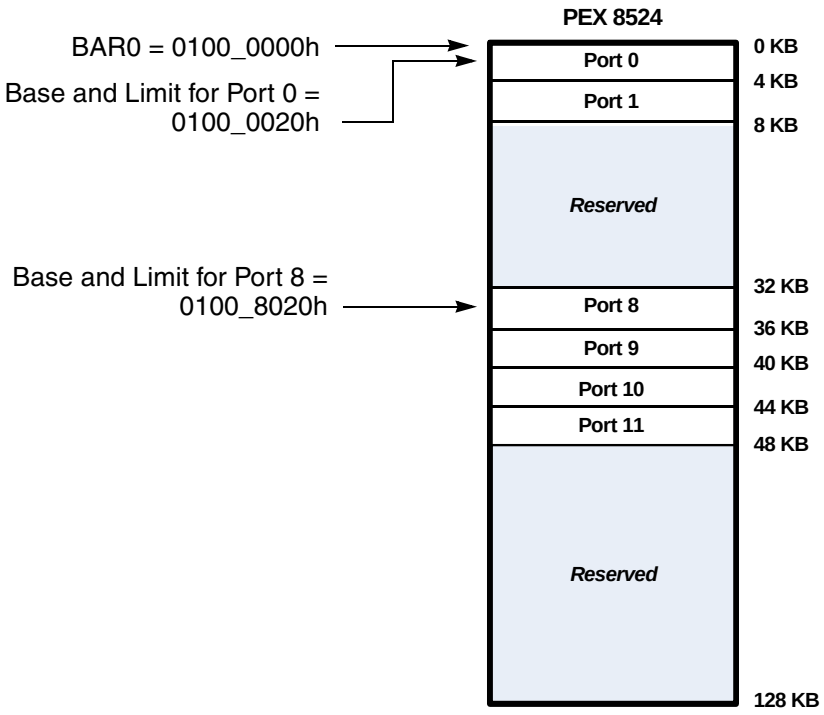
For example, to hit the **Memory Base and Limit Address** (offset 20h) for each port, refer to Table 7-1 and Figure 7-4. Table 7-1 defines how the registers in each port can be reached. All registers for all ports sit in the same BAR. Using the formula 1000h x Port Number provides the start address for the first register in a port. Figure 7-4 provides a graphical view of the BAR Memory space.

Table 7-1. PEX 8524 Memory-Mapped Register Access

Register	Location Address
Port 0 Base and Limit	0100_0020h
Port 1 Base and Limit	0100_1020h
Port 8 Base and Limit	0100_8020h
Port 9 Base and Limit	0100_9020h
Port 10 Base and Limit	0100_A020h
Port 11 Base and Limit	0100_B020h

Note: *For a complete listing of Memory-Mapped Register accesses, refer to Section A.1, "Serial EEPROM Memory Map."*

Figure 7-4. Using Memory-Mapped Access for PEX 8524 in Transparent Mode



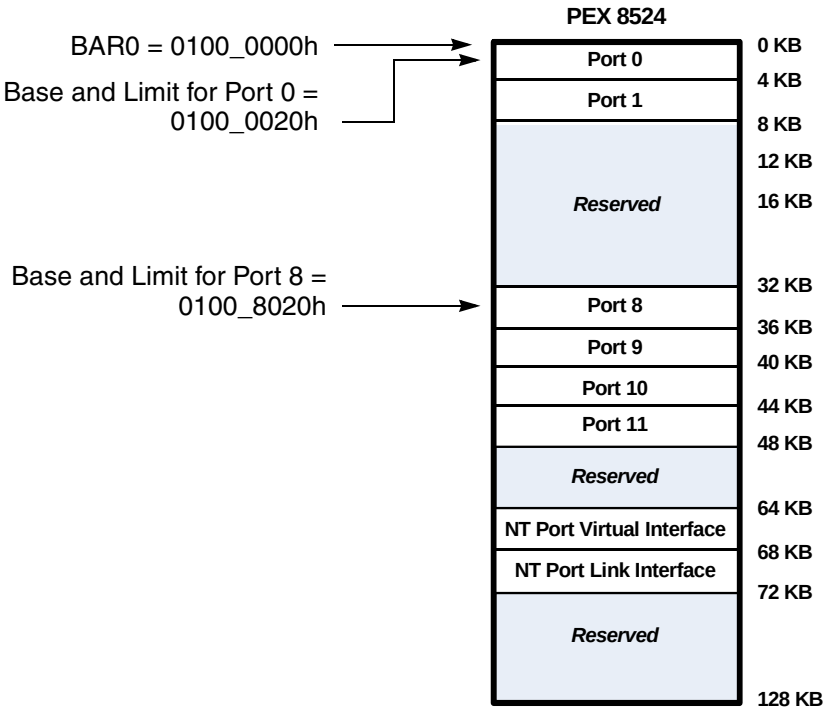
7.3.2.2 Non-Transparent Mode Registers

In NT mode, there are additional registers representing the NT Virtual and Link Interface endpoints. These exist at the fixed offsets of (refer to Figure 7-5):

- Virtual Endpoint – `BAR0 + 10000h`
- Link Endpoint – `BAR0 + 11000h`

Note: *For a complete listing of Memory-Mapped Register accesses, refer to Section A.1, "Serial EEPROM Memory Map."*

Figure 7-5. Using Memory-Mapped Access for PEX 8524 in Non-Transparent Mode



7.4 Interrupt Support

The PEX 8524 supports the PCI Express interrupt model, which uses two mechanisms:

- INT*x* Emulation
- Message Signaled Interrupt (MSI)

These interrupt mechanisms are discussed in Chapter 6, "Interrupts."

7.5 Hot Plug Support

The PEX 8524 supports the standard Hot Plug Controller (HPC) on all downstream ports. Hot Plug mechanisms are discussed in Chapter 9, "Hot Plug Support."

Note: *Refer to the PEX 85XX EEPROM – PEX 8532/8524/8516 Design Note for additional register programming information.*

Chapter 8 Performance Metrics

8.1 Overview

The PEX 8524 includes features that optimize performance under several application scenarios. This chapter discusses the four major performance metrics:

- Internal fabric non-blocking nature
- Quality of Service (QoS)
- Sustained link throughput
- Port-to-port latency

These approaches emphasize metric optimization. In general, host-centric applications, with transactions traveling between a wide upstream port and narrow downstream ports, are more *latency*-oriented. In comparison, peer-to-peer applications, where transactions are evenly distributed among all ports in a switch, are more *throughput*-oriented. However, achieving best performance is strongly application-dependent and the above principles are not necessarily always correct.

For example, if the PEX 8524 is linked with a graphics board in a host-centric application, graphics port *throughput* becomes the most important performance consideration, not *latency.* Conversely, if the traffic pattern in a peer-to-peer application is lightly loaded and bursty, *latency* can overweigh *throughput*, to become the highest performance concern.

Therefore, when tuning performance, it is important to understand the interaction and dynamics among performance metrics. *For example*, some tunings, in which the sending of traffic from multiple ingress ports to a narrow egress port is avoided, improves overall throughput and latency by reducing hot-spot queuing within the system. Other tunings, *such as* aggregating traffic from multiple ports into a wider data path and processing them in a time-multiplexed manner, can optimize throughput at the cost of slightly longer port-to-port latency.

Once the system dynamics are understood, it is easier to exchange performance metrics against one another.

8.2 Non-Blocking Switch

In switch literature, *non-blocking* is used to indicate that a packet can be routed from an ingress port to an egress port, provided that not more than one packet is received by the same ingress port and not more than one packet is destined to the same egress port. A non-blocking switch is expected to fully route all packets for independent ingress traffic streams, with the destination uniformly distributed. The PEX 8524 is a non-blocking switch.

8.2.1 Queuing Topology

Three major queuing topologies are used in switch architecture:

- **Output Queuing (OQ)** – When a packet arrives at an ingress port, it is immediately placed into a buffer that resides in the corresponding egress port. If, in the worst case, there are *N* ingress ports simultaneously attempting to transmit packets to the same egress port, the output buffer is required to enqueue traffic *N* times faster than the egress port's dequeuing rate.
- **Input Queuing (IQ)** – In this architecture, ingress port packets have a set of *Virtual Output Queues* (VOQ). One of the packets, among all head packets in different VOQs to the same egress port, is allowed to be scheduled out of that ingress port during a given time slot. The key factor in achieving high performance using VOQ is the global scheduling algorithm, which is responsible for the selection of packets to transmit from the ingress ports to the egress ports in each time unit. The complexity of such scheduling algorithm is $O(N^2)$.
- **Combined Input-Output Queuing (CIOQ)** – This approach adopts a queuing structure that is a combination of input and output queuing. It provides VOQ buffers at the ingress side, and also provides *O(1)* bandwidth buffers at the egress side. The design goal is to achieve the same level of throughput and non-blocking nature as an OQ switch, but without requiring *O(N)* times bandwidth to buffers as an OQ switch and without building a centralized scheduler whose complexity is proportional to $O(N^2)$ as an IQ switch. To achieve this goal, moderate internal fabric speedup is required in the CIOQ approach, to compensate for transient conflict.

The PEX 8524 uses CIOQ as its internal switching topology to process traffic arriving from different stations. Packets from one or more ports are aggregated first into a station, whose data path is sufficiently wide to accommodate traffic from all ports within it at any time. The PEX 8524 implementation includes two stations. In the future, this architecture will be directly scaled up, to deal with more than two stations.

For independent ingress traffic, it is possible for the *CIOQ* approach to achieve complete egress throughput with internal fabric to issue a speedup of only 2 – 1/N. *That is*, for the two-station PEX 8524 implementation, the internal speedup factor of 1 (no speedup), is sufficient to achieve non-blocking status.

After extensive simulation to consider standard switching performance factors including input traffic distribution, packet size distribution, output throughput, port-to-port latency, latency jitter, egress-to-ingress backpressure, as well as PCI Express-specific performance factors *such as* Physical Layer, Data Link Layer overhead, and packet-to-packet dependency caused by PCI ordering, PLX determined that using an internal speed-up factor of 1.25 allows the PEX 8524 to be non-blocking.

8.2.2 Port-to-Station Aggregation

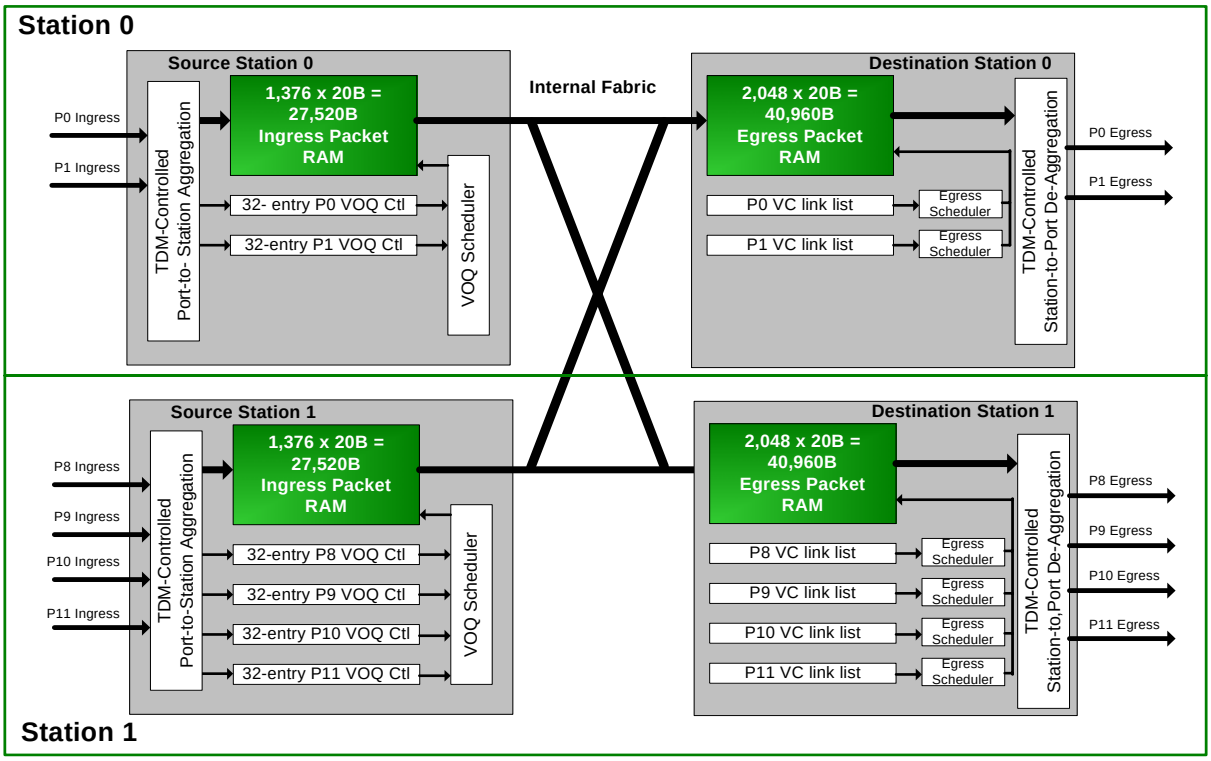
As previously stated, a single PEX 8524 PCI Express station is aggregated from multiple ports, provided that the combined port width is less than or equal to 8 lanes for Station 0, and 16 lanes for Station 1. Figure 8-1 redraws the PEX 8524 Transaction Layer architecture, by explicitly dividing a PCI Express station into individual ingress and egress parts.

In a PCI Express source station, the write port to the ingress packet RAM is shared by up to four ingress ports in a Time Domain Multiplex (TDM) manner. The wider the port, the more TDM slots are assigned to that port. Within VOQs of a single source station, if multiple packets from different ingress ports are available to be dispatched to the same destination, a Round-Robin arbiter controls which ingress port to select next.

Moving to the internal fabric, the Read ports to ingress packet RAM and Write ports to egress packet RAM are controlled by the PLX implementation of the CIOQ scheduling algorithm, where a unit in scheduling is a station, rather than a port.

In a PCI Express destination station, the Read port to the egress packet RAM is shared by up to four egress ports in a TDM manner as well. Furthermore, there are four independent egress schedulers. Egress schedulers follow Virtual Channel arbitration, as required by the *PCI Express Base r1.0a*.

Figure 8-1. PEX 8524 Queuing Data Structures



8.2.3 RAM and Queue Size

Table 8-1 defines the RAM and Queue Size built into the PEX 8524. The smallest unit of ingress and egress packet RAM is defined as a *beat*, which can store 20 bytes of data. In the PEX 8524, the smallest packet (12B header) takes 1 beat to store in a packet RAM, and the largest packet (16B header + 256B payload + 4B digest = 276B) takes 14 beats to store in packet RAM.

In Table 8-1, the number 32 under the cell **Ingress VOQ Entries**, **Per Port** indicates the maximum number of VOQ entries allocated to each ingress port. Each VOQ entry holds one Transaction Layer packet. For ingress ports, the incoming packet can travel to two destination stations, with each station containing up to four egress ports. Also, for egress ports, up to two VCs are supported, with each VC potentially having three different packet types – Posted, Non-Posted, and Completion (P, NP, and Cpl, respectively).

Each port on the egress side can contain up to six queues, to hold packets from two supported VCs and three supported packet types. A queue that stores packets of a unique VC and a unique type is referred to as a *VC&T queue*. Again, some queues can be completely empty and some queues can contain more than one packet. The maximum number of packets held by a single egress port is limited by the number of egress packet RAM beats allocated to that port.

It can be calculated from Table 8-1 that the total packet RAM size for the PEX 8524 is 136,960 bytes. Assume the maximum Transaction Layer Packet (TLP) size is 276B with a Maximum Payload Size (MPS) of 256B. Theoretically, the PEX 8524 can store up to 496 MPS packets.

Table 8-1. PEX 8524 Data Structure Size

Data Structure Name	Per Port	Per Station	Overall
Ingress Packet Name	Programmable	1,376 beats or 27,520 bytes	55,040 bytes
Ingress VOQ Entries	32	128	256
Egress Packet RAM	1,024 beats or 20,480 bytes for 1 to 2 ports; 512 beats or 10,240 bytes for 3 to 4 ports	2,048 beats or 40,960 bytes	81,920 bytes
Egress VC&T Queues	6	24	48

8.3 Quality of Service (QoS) Support

Quality of Service (QoS) is a performance differentiation feature offered by PCI Express to manage multiple traffic classes of different characteristics. An application assigns a Traffic Class (TC) value to individual Transaction Layer packets, according to the QoS requested by the class to which the transaction belongs. The static TC value tagged to each packet is dynamically mapped to a VC as it passes through a system PCI Express-capable device. The TC value ultimately determines the relative priority of a single packet as it traverses the PCI Express fabric, as well as the accumulated bandwidth allocated to the packets that belong to the same class.

8.3.1 Virtual Channel (VC) Support

The PEX 8524 supports up to two Virtual Channels (VCs), VC0 and VC1. Each VC has its own buffer resource allocation and data path. For a single port, VC configuration and property are determined by the Virtual Channel Extended Capability Register map (offset 148h to 1C4h).

Registers described in the Virtual Channel Extended Capability Register map apply to the switch egress and ingress ports. Registers related to packet arbitration are egress-specific, whereas registers defining TC/VC mapping and Low-Priority VC Count are applicable to both egress and ingress ports. [Refer to Table 11-10, "PEX 8524 Virtual Channel Extended Capability Register Map (All Ports)," for further Virtual Channel mapping information.]

Virtual Channel and traffic labeling allow independent physical resources to handle differentiated traffic. The **VC0 Resource Control** and **VC1 Resource Control** registers (offsets 15Ch and 168h, respectively) contain bits that control TC/VC mapping.

Across various ports, the PEX 8524 supports both symmetric and asymmetric TC/VC mapping. In the latter approach, the TC/VC mapping is port-independent and configured with different values per port.

The PEX 8524 default configuration sets all TC[7:0] to VC0, as provided in the *TC/VC0 Map* bits. For applications requiring two VCs, TC[7:1] can be mapped to VC1 by removing them from the *TC/VC0 Map* bits and adding them to the *TC/VC1 Map* bits.

8.3.2 Packet Arbitration

Because of CIOQ switch architecture and multiple VC support, the PEX 8524 functions with several arbitration/scheduling points distributed in the data path from an ingress port to an egress port.

This section discusses the arbitration/scheduling/backpressure algorithm used in the Source Scheduler, internal fabric, and egress scheduler.

8.3.2.1 Source Scheduler

Source Scheduler is essentially the VOQ scheduler depicted in Figure 8-1. The Source Scheduler functions as follows:

- From all 32 VOQ entries (each entry represents a single packet) belonging to a single ingress port, identifies one packet to be dispatched to the appropriate destination station, when egress RAM space is available
- Arbitrates among multiple-ready packets from different ingress ports with a Round-Robin mechanism
- Breaks deadlock potential by following PCI Ordering rules

Note: *Packets to different egress ports are selected with oldest first criteria on a per-queue basis. This policy offers optimum fairness and performance properties at low complexity. Packets to different VCs are selected by allowing VC1 higher priority, if configured as such. PCI Ordering rules are enforced.*

The Source Scheduler is capable of handling variable-length packets. It can schedule one packet out of a source station every Clock cycle, regardless of packet size.

There are two programmable fields in the Source Scheduler:

- High-Priority Virtual Channel
- PLX-Specific Relaxed Ordering

8.3.2.2 High-Priority Virtual Channel

When two VCs are enabled, packets from VC1 are scheduled with high priority by clearing the **Port VC Capability 1** register (offset 14Ch) *Low-Priority Extended VC Count* bit. Default setup can be changed by serial EEPROM initialization.

8.3.2.3 PLX-Specific Relaxed Ordering

PLX Relaxed Ordering capability is supported to enhance the performance of "push-only" traffic (Posted packets, *such as* Memory Writes and messages) in the PEX 8524. PLX-Specific Relaxed Ordering mode is enabled when any bit within the **PLX-Specific Relaxed Ordering Mode (Ingress)** register *Enable PLX Relaxed Ordering* field is set to 1:

- Port 0 or 8 – offset BFCh[7:0]
- Port 1 or 9 – offset BFCh[15:8]
- Port 10 – offset BFCh[23:16]
- Port 11 – offset BFCh[31:24]

According to PCI Ordering rules, Posted packets are not allowed to bypass previously posted packets of the same VC&T, regardless of whether they are targeting different egress ports. In applications *such as* storage area networks or IP networks, where Posted PCI Express packets are used to transmit encapsulated data traffic through switches, unnecessary serial dependency might be created in the Source Scheduler for those Posted packets coming from the same ingress ports, but going to different egress ports, if strict PCI Ordering rules were followed. This can result in dramatically degraded overall switch throughput.

The **PLX-Specific Relaxed Ordering Mode (Ingress)** register can be used to enable the PLX-Specific Relaxed Ordering capability. There is an Enable bit for TCs in each ingress port. All packets are allowed to bypass older packets from the same ingress port and TC. Packets targeting different egress ports are free to proceed without waiting for ordering dependency to be cleared. Meanwhile, packets targeting the same egress port are processed "in order," because there is no performance gain.

Because the Enable bit is TC-based, taking advantage of PLX-Specific Relaxed Ordering mode requires the PEX 8524 to be programmed with symmetric TC/VC mapping first.

Posted traffic benefits most from this mode. To take advantage of PLX-Specific Relaxed Ordering mode, without violating other ordering rules defined by the *PCI r2.3*, it is suggested to restrict outstanding traffic flow to be "Posted only" and shut down all Non-Posted packets.

There are two usage models:

- Restrict all Posted traffic requiring high-throughput in VC1 and program all TCs belonging to VC1 to enable Relaxed Ordering.
- Software disables PLX-Specific Relaxed Ordering mode in all TCs beforehand, performing all setups that involve Non-Posted packets, and then setting Any bit within a **PLX-Specific Relaxed Ordering Mode** register *Enable PLX Relaxed Ordering* field (offset BFCh[31:0]) to 1 when the system enters pure Data Transfer mode. When the Data transfer completes, disable PLX-Specific Relaxed Ordering mode.

Note: ***Silicon Revisions BB/BC only*** *– A variation of this feature, Relaxed Completion Ordering, allows only Completions to bypass Posted packets, while preserving the remainder of PCI ordering. Refer to Section 4.3.2.2, "PEX 8524 Relaxed Completion Ordering – Silicon Revisions BB/BC Only," for details.*

8.3.2.4 Internal Fabric Backpressure

Internal fabric provides egress packet RAM space available status from destination stations to source stations. The Source Scheduler never transmits a packet to overflow egress packet RAM. Moreover, to prevent packets in a particular VC&T from occupying the majority of egress packet RAM, and to speed up backpressure from Egress queues to Ingress queues and ultimately to external devices in the case of congestion avoidance, VC&T-based (VC and Type – P, NP, Cpl) packet cutoff information is passed from egress ports to each source station.

Egress queue congestion occurs when the packet arrival rate overcomes the packet dispatching rate. There are two causes of congestion:

- Insufficient credit to transmit the packets
- Insufficient bandwidth to transmit the packets as quickly as they arrive

In either case, if the cause continues, eventually the Egress queues of the congested port fill.

The PEX 8524 utilizes a watermark mechanism to cut off additional packets from the ingress side when the Egress queues back up. With some egress ports cut off, Ingress queues that contain packets targeting those egress ports could then fill. A filled Ingress queue prevents additional credit to its link partner, which causes that external device to stop transmitting packets in that VC&T.

The **ITCH VC&T Threshold** registers are per-VC&T-based in an egress port. All ports in a station share the same programmed value. Each VC&T has its own upper and lower limit. If more data than the programmed upper limit is queued, no more packets of that VC&T can be scheduled across the internal fabric, thereby cutting off that VC&T flow. After cutting off the VC&T flow, an Egress queue eventually drops below its lower limit, as packets are scheduled out of the egress port. This event turns on the internal fabric VC&T-enabling flags, which allow that VC&T to resume flow. [Refer to the **ITCH VC&T Threshold_1** through **ITCH VC&T Threshold_3** registers (offset C00h through C08h, respectively) for further details.]

There are two rules used for programming the **ITCH VC&T Threshold** registers:

- The unit value for the upper and lower limits is equivalent to 8 beats. The maximum value programmable in the upper limit is a function of the port width, defined in Table 8-2.

  A x8 egress port can handle no more than 1,024 beats, a meaningful value for the upper and lower limits is bounded by 1,024/8 = 128 (or 80h). In the device, the default value used by the upper and lower limits (FFh) is larger than its maximum legal value (80h). Therefore, by default, the backpressure mechanism is not triggered.
- The upper and lower limits must be different, with the upper number being larger than the lower number by at least two units.

Table 8-2. VC&T Threshold Limits

Port Width	Maximum Upper Limit in Beats
x1	128
x2	256
x4	512
x8	1,024
x16 (Station 1 only)	2,048

For example, programming upper = 14 and lower = 7 for VC0 posted allows each port in the station to accumulate 14 x 8 beats = 112 beats = 112 x 20 bytes = 2,240B VC0 Posted bytes before any one port cuts off VC0 Posted internal traffic. If there are four ports in the station, then 8,960 bytes can be stored in the RAM without the upper limit being crossed. After a port receives more than 112 beats of VC0 posted, no further VC0 posted is forwarded from the ingress port. The egress port must drain 7 x 8 beats before resuming VC0 posted forwarding.

The main objective is to avoid clogging the egress RAM with excessive packets of the same type that might prevent packets of other types from making fast forward progress inside the switch. If necessary, program the upper and lower limits.

8.3.2.5 Egress Scheduler

In each egress port, the PEX 8524 strictly follows VC and port arbitration mechanisms, as defined by the *PCI Express Base r1.0a*.

Virtual Channel Arbitration

In the context of scheduling traffic in VC0 and VC1, the main goal of the egress scheduler's VC arbitration is to provide differentiated services between data flows within the fabric. There are three VC arbitration choices:

- **Strict priority** – VC1 always prevails over VC0
- **Round-Robin, or "Hardware-Fixed Arbitration" in the** *PCI Express Base r1.0a* – Alternate between VC0 and VC1
- **Weighted Round-Robin (WRR) with 32 phases** – Select VC0 or VC1, based on 32 values programmed with the VC&T Arbitration table (refer to Table 8-3)

The strict priority selection is made by clearing the **Port VC Capability 1** register *Low-Priority Extended VC Count* bit to 0. The default value is strict priority, and can only be changed by serial EEPROM initialization.

If the *Low-Priority Extended VC Count* bit is set to 1 (by way of serial EEPROM), then VC0 and VC1 share the low-priority pool. Within the low-priority pool, Round-Robin or Weighted Round-Robin arbitration can be selected. The **Port VC Capability 2** register *VC Arbitration Capability* bits (offset 150h[1:0]) describe the two types of VC arbitration for mechanisms supported by the PEX 8524. The **Port VC Control** register *VC Arbitration Select* bit (offset 154h[1]) defines programming.

When using Weighted Round-Robin, the 32-phase VC Arbitration Table must be programmed before loading the table. Table entries represent one phase that is loaded by software with a low-priority VC ID value. The VC arbiter repeatedly sequentially scans all table entries, and transmits transactions from the VC buffer specified in the table entries. After a transaction is dispatched, the arbiter moves to the next phase. (Refer to Table 8-3 and the **VC Arbitration Table Phase n** register.)

Table 8-3. Virtual Channel Arbitration Table Register Map

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	1B8h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	1BCh
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	1C0h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	1C4h

Egress Port Arbitration

Regarding egress ports, the PEX 8524 supports only one port arbitration mechanism – non-configurable hardware arbitration scheme. In particular, the oldest ready packet from all ingress ports arriving at the current egress port are selected first. *Ready* packet is defined as a packet with available egress credit and no ordering violations.

8.4 Throughput

8.4.1 Theoretical Upper Limit

PCI Express allows for bi-directional traffic capability and scalable widths, allowing it to closely match the necessary bandwidth. As discussed in this section, compared to the 2.5-Gbps raw bandwidth provided by each SerDes lane, the achievable data payload efficiency, assume the Maximum Payload Size (MPS) of 256B is approximately 70%.

8.4.1.1 Physical Layer Overhead

The 2.5-Gbps serial data on a SerDes is encoded with additional information for clock recovery and error detection through 8b/10b encoding. When the additional information is removed, a 2.0-Gbps data rate remains, which is 80% of the starting bandwidth.

The PHY Layer also adds a 1-byte start symbol (STP) and a 1-byte end symbol (END or EDB) to the packet size, thereby introducing 2 bytes of overhead per TLP.

Also in the PHY Layer, SKIP Ordered-Sets are used to compensate for differences in frequency between bit rates at opposite ends of a Link. The *PCI Express Base r1.0a* specifies a clock frequency tolerance of 600 parts per million (ppm), which in turn requires a SKIP Ordered-Sets to transmit within the range of 1,180 to 1,530 symbol times. This causes the achievable efficiency to drop another 4/1,180 = 0.34%.

8.4.1.2 Data Link Layer Overhead

To ensure data integrity passing over the wire, the *PCI Express Base r1.0a* states that the DLL (Data Link Layer) adds a sequence number at the start of the packet and an LCRC integrity check at the end of the packet. The sequence number is 2 bytes, and the LCRC is 4 bytes, thereby introducing 6 bytes of overhead per TLP.

In addition to the overhead inherent in TLP payload transmission, the *PCI Express Base r1.0a* uses the same wire to transmit DLLPs (Data Link Layer Packets). ACK (acknowledge) and UpdateFC are the two most frequently used types of DLLPs during standard run time, where throughput matters. ACK is used to acknowledge TLP receipt. UpdateFC is used to provide additional credits, which enables additional TLP transactions.

DLLPs are structured so that a single ACK can represent receiving multiple TLPs, reducing the total number of ACKs required. Similarly, a single UpdateFC is structured so that credit for more than one packet can be extended at a time, reducing the number of required UpdateFCs per TLP. The size of a single DLLP is 8 bytes. In the worst case, two outgoing DLLPs are formed for each incoming TLP, which equals 16B in per TLP overhead. In the best case, there is zero DLLP overhead for incoming TLPs. DLLPs flow in the opposite direction of TLPs, as they are feedback mechanisms. For one-way TLP traffic, the DLLP overhead does not impact overall link utilization.

8.4.1.3 Transaction Layer Overhead

All PCI Express payloads are encapsulated in a TLP. A TLP contains a header portion that provides the PEX 8524 with routing information for the packet. The header can be 12 or 16 bytes.

According to the *PCI Express Base r1.0a*, Maximum Payload Size (MPS) can range from 128 to 4,096 bytes. The PEX 8524 supports MPS of up to 256 bytes.

The **Device Control** register Maximum Payload Size field (offset 70h[7:5]) default MPS is 128 bytes. Software can change the default value; however, the entire system must have a consistent MPS. In general, longer payloads are more efficient, but require more on-chip resources to buffer, and can cause much worse hot spot congestion in bursty traffic flows.

A TLP can also incur additional overhead when end-to-end data integrity is essential. In such cases, a 4-byte ECRC is added as another type of overhead to the end of the packet.

Note: *Refer to the **Device Control** register Maximum Payload Size field (offset 70h[7:5]) for MPS limitations.*

8.4.1.4 PCI Express Efficiency Upper Bound Summary

Table 8-4 summarizes PCI Express inherent efficiency for 0B, 4B, 8B, 40B, 128B, 256B, and 4,096B payload sizes on various negotiated link widths. The 4,096B table row is provided for reference only, as the PEX 8524 supports MPS of up to 256 bytes.

The table columns provide three types of variations:

- Comparing to raw SerDes bandwidth of 2.5 Gbps versus 2.0 Gbps after 8b/10b decoding.
- 0% additional DLLP generation versus 100% DLLP generation, assuming traffic is equal in both directions. 0% DLLP assumes that DLLP traffic is not injected into the TLP stream, *such as* a uni-directional traffic stream. 100% DLLP assumes that for every TLP transmitted, an additional ACK DLLP and UpdateFC DLLP are generated in the reverse direction for a bi-directional fully loaded traffic stream.
- Non-payload TLP overhead of 12B versus 20B (16B header + ECRC).

In summary, the larger the payload, the more efficient the PCI Express communication. For 256-byte Maximum Payload Size supported by the PEX 8524, the limit efficiency compared to the raw 2.5-Gbps bandwidth is between 68 to 73.92%.

Note: *Not all factors are reflected in this table. SKIP Ordered-Set drops another 0.3%. Any credit shortage or transient congestion can significantly drop.*

Table 8-4. Throughput Theoretical Upper Limit

Bytes of Payload	2.5 Gbps Raw Bandwidth				2.0 Gbps Raw Bandwidth after 8b/10b Decoding			
	0% DLLP		100% DLLP		0% DLLP		100% DLLP	
	12B	20B+	12B	20B+	12B	20B+	12B	20B+ ECRC
0	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
4	13.28%	10.00%	8.00%	6.64%	16.60%	12.50%	10.00%	8.30%
8	22.80%	17.68%	14.48%	12.24%	28.50%	22.10%	18.10%	15.30%
40	53.12%	46.88%	42.00%	38.00%	66.40%	58.60%	52.50%	47.50%
128	68.96%	65.44%	62.24%	59.36%	86.20%	81.80%	77.80%	74.20%
256	73.92%	71.84%	69.92%	68.00%	92.40%	89.80%	87.40%	85.00%
4,096	79.36%	79.20%	79.04%	78.88%	99.20%	99.00%	98.80%	98.60%

8.4.2 Single-Stream Throughput

When data flows in a single-packet stream from a fixed-ingress to fixed-egress port, its throughput can be optimized on both the ingress and egress sides. The method for optimizing throughput on both sides is discussed in the following sections.

8.4.2.1 Ingress Side

Accept More than One Packet in Same Symbol Time

The PEX 8524 ingress port is designed to accept incoming traffic at the fastest rate possible. For x8 ports, the PEX 8524 allows the ending part of a TLP and beginning part of the next TLP to arrive in the same symbol time. It also allows a partial TLP and a partial or full DLLP to simultaneously arrive.

Optimize Ingress Credit Allocation

A TLP cannot be transmitted to the switch without the switch providing sufficient ingress credits beforehand. When a credit is advertised, it indicates a guaranteed storage available in the credit transmitter at that time. If there is insufficient or untimely ingress credits advertised from the PEX 8524 to its link partner, the incoming TLP stream does not sustain at the highest possible rate.

Amount of Ingress Credit Required Calculation

The PEX 8524 supports up to six VC&Ts per port. The amount of ingress credits advertised in each VC&T is expected to be sufficient to cover the round-trip delay from the time the external device schedules a TLP for transmission in its Transaction Layer to the time the external device receives the replenishing credit from the PEX 8524 in the same VC&T.

To enable a burst of TLPs of the same VC&T to enter the PEX 8524 without interruption, use the following empirical equation:

```
Ingress_Credit_Advertised = (Round_trip_time_in_symbol times x link_width)
/ packet_size_in_bytes
```

Round-trip latency, which can range from 160 to 400 ns (40 to 100 symbol times), is determined by both the PEX 8524 and external device and consists of the following:

- Latency for incoming TLP to travel the entire PEX 8524 ingress data path
- Delay from writing the first byte of the packet into ingress packet RAM until writing the last byte of the packet into ingress packet RAM
- Latency for Source Scheduler to transmit the packet to egress packet RAM and free up the ingress buffers for this TLP packet
- Latency for the PEX 8524's ingress credit scheduler to generate an UpdateFC packet
- Latency for this UpdateFC DLLP to travel the PEX 8524 egress data path to SerDes
- Delay in SerDes
- Latency for this UpdateFC DLLP to travel the ingress data path of the external device
- Latency for external device to process the UpdateFC DLLP and update its Credit Limit Counter
- Latency for external device to schedule the next TLP in the same VC&T out
- Latency for the external device to move the new TLP across its egress data path to the SerDes
- Final delay in SerDes

For example, suppose a link with a 400 ns round-trip time contains eight lanes and a stream of Posted transactions is broken into packets of 64B payload each. The amount of posted type header credit needed to sustain a steady incoming traffic flow is approximately 100 x 8 / (16 + 64) = 10.

The smaller the payload size, the higher demand on the ingress header credit to be advertised. Using the same example provided above, but changing payload size from 64B to 4B, the number of ingress header credits required is 40. As previously stated, the PEX 8524 contains a total of 32 VOQ entries in its ingress ports. Although 30 VOQ entries can be allocated to the posted traffic, there is no way to sustain the incoming traffic without stalling due to lack of credits.

Program Ingress Credit Threshold Rules

The PEX 8524 provides the capability to program the ingress credit value for each VC&T in the ingress ports. Refer to Section 11.13.8.1, "INCH Threshold Port Virtual Channel Registers," to view the registers used to program the ingress credit value. The registers range from offsets A00h to A5Ch.

In the INCH Threshold Port Virtual Channel registers, header credit and payload credit thresholds are writable. The following rules are used to program these registers:

- One unit of header credit threshold represents one packet. A value of 1 allows the PEX 8524 to advertise 1 header credit, *2* allows 2 header credits, and so forth. Bits [13:9] allow a maximum of 31 header credits to be programmed to VC&T.
- One unit of payload credit threshold represents 16B of data. When the PEX 8524 Maximum Payload Size is set as 256, a value of at least *16* is required to be programmed for Posted and Completion packets. Bits [8:0] allow a maximum value of 2^9 payload credit units to be advertised. For Posted and Completion types, bits [2:0] are ***reserved***, which forces the payload credit threshold to be powers of 8. This effectively makes the granularity for Posted and Completion credit threshold types increase to 16B x 8 = 128B. For Non-Posted types, similar restrictions do not apply, because the payload size is never more than 4B.
- For all ingress VC&Ts, the total header credit cannot exceed 32 in a port.
- For all VC&Ts in all potential ports in a source station, the total payload credit cannot exceed 1,376.

The default ingress header credit threshold for VC0 Posted, Non-Posted, and Completion types are as follows:

- **Silicon Revision AA** – 5, 9, and 5, respectively
- **Silicon Revisions BB, BC** – 12, 7, and 10 respectively

The default ingress data payload credit threshold for VC0 Posted, Non-Posted, and Completion types are as follows:

- **Silicon Revision AA** – 88, 9, and 88, respectively
- **Silicon Revisions BB, BC** – 144, 7, and 128 respectively

It is strongly recommended that to achieve better ingress throughput for a particular type, fine-tuning ingress credit thresholds is an indispensable step. *For example*, when the PEX 8524 is "talking" to a x8 graphics board, almost 28.5% throughput boost is observed by modifying the ingress header credit for VC0 Posted, Non-Posted, and Completion types to be 15, 4, 13, and ingress payload credit to be 40, 4, and 40, respectively.

Ingress Credit Threshold Programming

There are methods for changing the ingress credit threshold – by way of a serial EEPROM or direct CSR programming. The first approach is straightforward – program the required values and the link produces the programmed values. However, the latter approach requires further explanation.

In the direct CSR programming method, if a credit threshold requires an increase, perform a CSR Write. This immediately results in a new UpdateFC to be transmitted, carrying the newly increased credits. In contrast, if a credit threshold requires a decrease, the *PCI Express Base r1.0a* does not provide a pre-defined method for reclaiming unused credit previously advertised to the external device. The danger of programming a smaller credit threshold than the initial value is that ingress packet storage can overflow if the external device is not aware of the credit threshold, and continues sending packets according to the initial credit threshold. Use the following approach to avoid packet RAM overflow:

- Upstream port
  - Use CSR access to program the VC&Ts whose credit requires a decrease.
  - Transmit "side-impact free" traffic from host to those VC&Ts, to deplete all credits to be reclaimed. Before the surplus credits are completely reclaimed, the PEX 8524 transmits UpdateFC for that VC&T. After the amount of incoming traffic attains the difference between the old and new credit thresholds, the PEX 8524 starts transmitting fresh UpdateFC DLLPs for incoming TLPs.
- Downstream ports
  - Program all ingress credit threshold CSRs in all VC&Ts to the required values.
  - Execute a Secondary Bus Reset in the **Bridge Control** register (offset 3Ch[22]=1)
  - Release the reset. The newly programmed values take effect afterward.

Ingress credit threshold registers are not sticky after a primary reset; therefore, this sequence requires repeating after any primary reset.

Tip: *If a serial EEPROM is available and you want to experiment with credit values, initially program all thresholds to 1. There is no impact in increasing the credit (up to the maximum of PEX 8524 resources). This allows for the most flexibility in your experiments.*

8.4.2.2 Egress Side

Provide Sufficient Egress Credit

The simplest way to improve an egress port's throughput is to provide the PEX 8524 with sufficient egress credit. In general, the number of egress credit required by the PEX 8524 follows the same equation as the ingress credit calculation:

```
Egress_Credit_Required = (Round_trip_time_in_clocks x link_width) /
packet_size_in_bytes
```

For the PEX 8524 to achieve pipelined performance, the external device is suggested to advertise at least two MPS worth of payload credits. For 128B MPS, the payload credit is greater than or equal to 16 (16 credits = 296B = 2 MPS). For 256B MPS, the payload credit must be greater than or equal to 32 (2 MPS). Although a packet's payload is smaller than MPS, without a 2 MPS credit, the PEX 8524 schedules one packet out, waits for the updateFC to return, then schedules the next packet out.

Egress Schedulers Select Frequency

To simplify the egress scheduler design, one limitation incurred is that one packet can be scheduled out every other Clock cycle. For port widths narrower than x16, this restriction does not cause a performance degradation. For Station 1 x16 port widths, the throughput of header-only packets (16B or less) is not sustained.

x8 and x16 Port PAD Slots

When a PEX 8524 port is configured as x8 or x16 (Station 1 only), only bytes belonging to one TLP are transmitted in single-symbol time. The residue lanes are filled with PAD.

Also, for x8 or x16 ports, the PEX 8524 does not attempt to optimize throughput by placing a partial TLP and DLLP in single-symbol time.

8.4.3 Multiple Stream Throughput

8.4.3.1 Enable PLX-Specific Relaxed Ordering

The PEX 8524 does not support optional Relaxed Ordering bits in TLP, as specified in the *PCI Express Base r1.0a*, Table 2-23. By default, all packets entering from a specific port are dispatched to their respective destinations, based on strict ordering.

However, as described in Section 8.3.2.1, "Source Scheduler," the PEX 8524 provides its own Relaxed Ordering to overcome the packet-to-packet dependency in a burst of posted traffic from the same ingress port, but to different egress ports.

8.4.3.2 Avoid Hot Spots

A hot spot forms when multiple ingress ports attempt to transmit packets to the same egress port, and the overall influx bandwidth outweighs the efflux bandwidth. If the hot spot is not transient, the hot spot port throughput can appear high. However, eventually the Egress queues fill, backpressuring the Ingress queues. When the Ingress queues fill, ingress traffic is backpressured, potentially impacting traffic flow not targeting the congested egress port. As a result, the switch overall average throughput is dramatically reduced. PCI Express does not provide a mechanism to recognize and avoid hot spots. It is therefore left to the system designers to understand and avoid this pitfall.

8.4.4 Throughput and Packet Size Relationship

In general, sustained throughput increases as Payload Size increases due to the increased PCI Express protocol efficiency. However, the following secondary effects can also affect throughput:

- In peer-to-peer applications, longer packets can result in less interleaved or randomized egress port distribution compared to shorter packets. This increases the chance of building up transient congestion in egress ports, and can negatively impact overall throughput.
- Longer packets require fewer header credits per unit time, and are therefore less likely to idle the link while waiting for additional header credit.
- Longer packets burn up payload credits faster and can stall DLLPs behind the long TLP longer, potentially causing credit starvation. If there is insufficient link credit (3 TLPs worth or more), shorter packets may provide better throughput.
- Posted packets block younger packets of other types (Non-Posted and Completions). In a system with minimal credits, Posted packets should receive the strongest consideration when allocating credits.

It is recommended to carefully compare the benefits and drawbacks of using longer packets.

8.4.5 Data Link Layer Considerations

8.4.5.1 Arbitration between DLLP and TLP

To reduce DLLP overhead on the wire, the PEX 8524 uses the following fixed-priority scheme to determine what transmits next:

1. Completion of a TLP or DLLP currently in transmission.
2. Initialization Flow Control (FC-Init) DLLPs.
3. NAK DLLP.
4. ACK DLLP, due to receipt of a duplicate TLP or ACK Latency Timer expiration. *
5. Update FC DLLP, due to the FC Update Pending Timer expiration. *
6. Retry Buffer TLP, due to received NAK or Retry timeout.
7. New TLPs. *
8. Update FC DLLP, due to change in available credits. *
9. Power Management DLLP.
10. ACK DLLP for the last received TLP. *

Among these ten categories, the five most frequently seen new packets are noted with an asterisk (*). Updated-FC, InitFC, and ACK DLLPs appear twice – once as higher priority than TLPs, and once as lower priority than TLPs. A regular DLLP turns into a higher priority DLLP based on a programmable timer. The basic idea is to reduce the number of DLLPs, the timers provide the opportunity to collapse multiple DLLPs into 1. The timers are discussed in Sections 8.4.5.2 and 8.4.5.3.

8.4.5.2 DLLP ACK Frequency Control

The **ACK Transmission Latency Limit** register (offset 1F8h) indicates a minimum amount of time (in 4 ns clocks) that the switch waits before prioritizing an ACK. By setting this register to the minimum value of 2 (refer to note below), ACKs are typically always transmitted with high priority, allowing the most DLLP traffic and the smallest possible Retry buffer in the other device on the link.

Note: *2 is the minimum value that has an effect; 0 or 1 wait for 255 clocks.*

The larger the number written into this CSR, the larger the chance of ACK collapse, and the more efficient the outgoing TLP throughput can be.

However, by setting the *ACK Transmission Latency Limit* to the maximum (255), 255 symbol times (4 ns each) to occur before prioritizing an ACK. If the Retry buffer in the external device is not sufficiently deep, it can slow the incoming TLP rate. On a x4 link, 1,020B can be transmitted in 255 symbol times, which is 51 20B packets. The external device would need to have a Retry buffer that could store more than 51 TLPs, so as not to impact the back-to-back burst of incoming TLPs.

Because programming a smaller value into this CSR decreases egress TLP throughput but can increase the ingress TLP throughput, a tradeoff must be addressed.

If there is no TLP traffic, an ACK can be transmitted earlier than the timer indicates as a low-priority DLLP.

The initial value depends on the programmed link width. However, the value can be overwritten by serial EEPROM or a regular CSR Write.

8.4.5.3 DLLP UpdateFC Frequency Control

The **INCH FC Update Pending Timer** register (offset 9F4h) controls the amount of time a port can wait before prioritizing an UpdateFC DLLP. Before the timer expires, TLPs have priority over UpdateFC DLLPs. After the timer expires, UpdateFC DLLPs move to higher priority. The value programmed into this CSR is a counter expiration value. All six VC&Ts in an ingress port share the same counter upper limit; however, each has its own set of counters, for counting up.

The smaller the value written into these registers, the sooner an UpdateFC DLLP becomes higher priority; therefore, the sooner the UpdateFC DLLP is transmitted. The sooner an UpdateFC is transmitted, the less likely the chance to collapse two VC&T UpdateFCs. However, even for small timer values, only one UpdateFC is typically sent per each incoming TLP. The UpdateFC is broken into multiple DLLPs for each incoming TLP only if there are insufficient resources to replace the credit.

Note: *Each VC and type has its own UpdateFC. Only UpdateFCs for the same VC&T can be collapsed.*

The *PCI Express Base r1.0a* guidelines for the FC Update Pending Timer are provided in Table 8-5.

For implementation, a value of 01h or 00h into the CSR results in waiting 255 symbol times. The smallest value is 10h. The initial value of 00h is effectively 255 symbol times.

Table 8-5. FC Update Pending Timer Guidelines

Maximum Packet Size	Link Width	Recommended Timer Count
128 bytes	x1	76h
	x2	40h
	x4	24h
	x8	21h
	x16 (Station 1 only)	18h
256 bytes	x1	D0h
	x2	6Ch
	x4	3Bh
	x8	36h
	x16 (Station 1 only)	24h

8.5 Latency

8.5.1 Queuing Effect

In switches with large internal buffers, the latency increases once internal queuing is developed. The packet at the end of an egress VC&T queue does not transmit until all packets in front of it are transmitted. Assume the egress RAM of a x4 port is packed with packets of the same VC&T, draining the entire egress RAM takes 2,560 clocks (512 beats x 20B per beat / 4B/clock). Worst-case packet latency can be as long as 10 µs.

To overcome the queuing effect, attempt the following:

- Avoid creating hot spots. In particular, ensure that the upstream port width in a host-centric application matches the sum width of all active downstream ports. Otherwise, the upstream port can easily become a hot spot when all downstream ports are attempting to transmit packets to it.
- Program a small Egress queue packet upper and lower limit, to avoid packet accumulation in an egress port. Section 8.3.2.4 describes how to program these thresholds. Lower latency is achieved at the cost of reducing the PEX 8524's capability to buffer transient congestion.
- Reduce traffic load. Lighter traffic is less likely to experience congestion and can drain relatively faster, as the egress links can drain at the full link rate.

8.5.2 Time Division Multiplex Effect

As previously illustrated, the PEX 8524 source station employs port-to-station aggregation, and the destination station employs station-to-port de-aggregation. Time Division Multiplex (TDM) controls aggregation and de-aggregation. Usually, waiting for a proper TDM slot to process packet coming from or going to a particular port increases the latency. The wider the port, the more TDM slots that port owns; therefore, the less latency contributed by TDM.

Within a station, only a subset of 8 lanes for Station 0 and up to 16 lanes for Station 1 are connected to SerDes. One approach to reduce latency is to strap the port as a wider port and allow it to negotiate down to the expected link width. *For example,* if there is only a x2 port owned by a station, the port can be strapped as x8 (Station 0) or x16 (Station 1), and allowed to become x2 later through the normal link training process. As a result, all TDM slots in this station are acquired by the x2 port. The worst case TDM effect for a x1 or x2 port is 14 symbol times = 57 ns.

8.5.3 High-Priority Packets

The previous sections discussed methods for optimizing latency in a single VC system. However, a better solution for some traffic scenarios that require consistently low latency is to use a different VC.

The PEX 8524 does not support isochronous traffic that requires high-priority packets by way of a switch with a time limit. However, it does provide a high-priority packet path throughout the entire switch if there are two VCs and VC1 is configured with higher priority compared to VC0 in both the ingress and egress ports.

VC1 includes independent credit, storage, and scheduling with respect to VC0. However, it shares the wires in and out of the switch. At any point where there can be congestion between the two VCs, VC1 is treated separately and preferentially to VC0. This occurs at the Ingress queues, internal fabric, and Egress queues. For contention, VC1 packets are given priority over VC0 packets.

In this case, VC0 is earmarked for slower, bulk data transfer, and VC1 processes packets with a much shorter latency if there is no over-subscription.

Two conditions are required to make the high-priority path meaningful:

- TC/VC mapping is symmetric across all ports
- All ports configure the Low-Priority Extended VC Count as 0, in the egress **Port VC Capability 1** register (offset 14Ch; default) to give VC1 the higher priority
- Certain TCs map to VC1 [**VC0 Resource Control** or **VC1 Resource Control** registers (offsets 15Ch and 168h, respectively)] and the high-priority TLPs use the TCs that map to VC1
- VC1 is enabled on ingress and egress ports

8.5.4 Smaller Size Packets

The PEX 8524 uses a store-and-forward architecture. Without cut through, a packet must be completely written into the PEX 8524's internal packet RAM before the first byte of the packet can be transmitted out of the egress port. Fall-through latency is a function of the packet size; therefore, the smaller the packet size, the shorter the fall-through latency. The bulk of the latency is dictated by the amount of time it takes for the packet to arrive. Narrower ingress ports contain correspondingly higher latency than wider egress ports.

8.5.5 Power Management

Saving power and optimizing latency are typically two conflicting tasks. After a chip enters Power Saving mode, the wakeup time when new Burst packets arrive always contributes to latency. For latency-sensitive applications, it is recommended to use software to turn off the ASPM L0s entrance/exit, as well as the L1 entrance/exit.

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Chapter 9 Hot Plug Support

9.1 Hot Plug Purpose and Capability

Note: *The PEX 8524's Hot Plug Controllers are compliant with the PCI Hot Plug r1.1 and PCI Standard Hot Plug Controller and Subsystem r1.0.*

Hot Plug capability allows board insertion and extraction from a running system, without adversely affecting the system. Boards are typically inserted or extracted to repair faulty boards or re-configure the system without system down time. Hot Plug capability allows systems to isolate faulty boards in the event of a failure. The PEX 8524 includes one Hot Plug Controller per downstream port.

9.1.1 Hot Plug Controller Capabilities

- Insertion and removal of PCI Express boards, without removing system power
- Board-present and MRL (Manually operated Retention Latch) Sensor signals supported
- Power Indicator and Attention Indicator Output signals controlled
- Attention Button monitored
- Power fault detection and Faulty board isolation
- Power switch for controlling downstream device power
- Generates PME (Power Management Event) for Hot Plug events in sleeping systems (D3hot)
- Presence detect is accomplished through an in-band SerDes receiver detect mechanism or by using the HP_PRSNT*x*# signal
- Hot Plug interrupts can be sent in-band using INT*x* or MSI messages

9.1.2 Hot Plug Port External Signals

The PEX 8524's Hot Plug Controllers include nine Hot Plug signals for each PCI Express port (6 ports x 9 signals/port = 54 total signals), defined in Table 9-1. (Refer to Table 3-5, "PEX 8524VAA/BB/BC Hot Plug Signals, 680-Ball PBGA – 54 Balls," or Table 3-12, "PEX 8524BB/BC Hot Plug Signals, 644-Ball PBGA – 54 Balls," for signal-to-ball mapping.)

Table 9-1. Hot Plug Signals

Signal Name	Type	Description
HP_ATNLED*x*#	O	**Hot Plug Attention LED Output Per Port** Active-Low Slot Control Logic output used to drive the Attention Indicator. Output is set Low to turn On the LED. Enabled when the **Slot Capabilities** register *Attention Indicator Present* bit is set (offset 7Ch[3]=1) and controlled by the **Slot Control** register *Attention Indicator Control* field (offset 80h[7:6]). When software writes any value other than 00b (***Reserved***) to the *Attention Indicator Control* field and an Attention_Indicator message is sent to the downstream device, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capabilities** register *Attention Indicator Present* bit is set (offset 7Ch[3]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. An external current-limiting resistor is required.
HP_BUTTON*x*#	I PU	**Hot Plug Attention Button Input Per Port** Active-Low Slot Control Logic input, directly connected to the Attention Button, with input assertion status latched in the **Slot Status** register *Attention Button Pressed* field (offset 80h[16]). Enabled when the **Slot Capabilities** register Attention Button Present bit is set (offset 7Ch[0]=1). When the following conditions exist: • HP_BUTTON*x*# is not masked (**Slot Control** register *Attention Button Pressed Enable* bit (offset 80h[0]=1), and • **Slot Capabilities** register *Hot Plug Capable* bit is set (offset 7Ch[6]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated, to notify the Host of intended board insertion or removal. ***Note:*** *HP_BUTTONx# is internally de-bounced, but must remain stable for at least 10 ms.*
HP_CLKEN*x*#	O	**Reference Clock Enable Output Per Port** Active-Low output that, when enabled, allows external REFCLK to be provided to the slot. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN*x*# output assertion to HP_CLKEN*x*# output assertion is programmable (through serial EEPROM load) from 16 ms (default) to 128 ms, in the *HPC Tpepv Delay* field (offset 1E0h[4:3]).

Table 9-1. Hot Plug Signals *(Cont.)*

Signal Name	Type	Description
HP_MRL*x*#	I PU	**Hot Plug Manually Operated Retention Latch Sensor Input Per Port** Active-Low input that triggers Slot Control Logic. Directly connected to an optional MRL Sensor that is logic High when the latch is not closed. HP_MRL*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN*x*# and HP_PWRLED*x*#) and clock (HP_CLKEN*x*#), and de-assert Reset (HP_PERST*x*#) after reset or under software control. A change in the HP_MRL*x*# Input signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL*x*# is not masked (**Slot Control** register *MRL Sensor Changed Enable* bit, offset 80h[2]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated. If the associated Hot Plug-capable downstream port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL*x*# is normally connected to HP_PRSNT*x*# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable downstream port instead connects directly to a device (in which case Hot Plug is not used), pull HP_MRL*x*# Low. ***Note:*** *HP_MRLx# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRLx#, if enabled, is not de-bounced when sampled immediately after reset.*
HP_PERST*x*#	O	**Reset Output Per Port** Active-Low Hot Plug output used to reset the slot. Controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]).
HP_PRSNT*x*#	I PU	**Combination of Hot Plug PRSNT1# and PRSNT2# Input Per Port** Active-Low input connected to the slot's PRSNT2# signal, which on the add-in board connects to the slot's PRSNT1# signal, which is normally grounded on the PRSNT2# signal at the motherboard slot. A change in the HP_PRSNT*x*# Input signal state is latched in the **Slot Status** register *Presence Detect Changed* bit (offset 80h[19]), and the state change can assert an interrupt to notify the Host of board presence or absence. When the following conditions exist: • HP_PRSNT*x*# is not masked (**Slot Control** register *Presence Detect Changed Enable* bit (offset 80h[3]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated. ***Note:*** *HP_PRSNTx# is internally de-bounced, but must remain stable for at least 10 ms.*

Table 9-1. Hot Plug Signals *(Cont.)*

Signal Name	Type	Description
HP_PWREN*x*#	O	**Active-Low Hot Plug Power Enable Output Per Port** Active-Low Slot Control Logic output that controls the slot power state. When this signal is Low, power is enabled to the slot. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1). When software turns the slot's Power Controller On or Off (**Slot Control** register *Power Controller Control* bit, offset 80h[10]), a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. When HP_MRL*x*# is enabled [**Slot Capabilities** register *MRL Sensor Present* bit is set (offset 7Ch[2]=1)], HP_MRL*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power, by asserting HP_PWREN*x*# after reset or under software control.
HP_PWRFLT*x*#	I PU	**Hot Plug Power Fault Input Per Port** Active-Low input that indicates the slot's external Power Controller detected a power fault on one or more supply rails. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and input assertion status is latched in the **Slot Status** register *Power Fault Detected* (offset 80h[17]). When the following conditions exist: • HP_PWRFLT*x*# is not masked (**Slot Control** register Power Fault Detector Enable bit (offset 80h[1]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated, to notify the Host of a power fault. ***Note:*** *If HP_PWRENx# and HP_CLKENx# are not used, HP_PWRFLTx# can be used as a general-purpose input with status reflected in the **Slot Status** register Power Fault Detected (offset 80h[17]), provided the **Slot Capabilities** register Power Controller Present bit is set (offset 7Ch[1]=1).*
HP_PWRLED*x*#	O	**Hot Plug Power LED Output Per Port** Active-Low Slot Control Logic output used to drive the Power Indicator. This output is set Low to turn On the LED. Enabled when the **Slot Capabilities** register *Power Indicator Present* bit is set (offset 7Ch[4]=1), and controlled by the **Slot Status** register *Power Indicator Control* field (offset 80h[9:8]). When software writes any value other than 00b (***Reserved***) to the *Power Indicator Control* field and a Power_Indicator message is sent to the downstream device, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capabilities** register *Power Indicator Present* bit is set (offset 7Ch[4]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is set (offset 80h[5]=1), an interrupt (MSI, or INT*x* message, both mutually exclusive) can be generated to the Host. An external current-limiting resistor is required.

Note: *If Hot Plug outputs (including HP_PERSTx#) are used and HP_MRLx# input is not used, pull HP_MRLx# Low so that Hot Plug outputs (including HP_PERSTx#) will properly sequence if the serial EEPROM is blank or missing. Default register values enable HP_MRLx#, which must then be asserted to cause Hot Plug outputs to toggle (for example, to de-assert HP_PERSTx# and assert HP_PWRLEDx#).*

9.1.3 Hot Plug Output Signal States for Disabled Hot Plug Slots

When a Hot Plug slot is disabled, the Hot Plug Output balls for that port are in the logic states defined in Table 9-2.

Table 9-2. Hot Plug Outputs for Disabled Hot Plug Slot

Output Signal	Logic	Comments
HP_ATNLED*x*#	High	Attention LED is turned Off
HP_CLKEN*x*#	High	Reference Clock is not driven to the slot
HP_PERST*x*#	Low	Slot remains in reset
HP_PWREN*x*#	High	Power Controller is turned Off
HP_PWRLED*x*#	High	Power LED is turned Off

9.2 PCI Express Capability Registers for Hot Plug

The Hot Plug Configuration, Capability, Command, Status, and Events are described in Section 11.9, "PCI Express Capability Registers." The applicable registers are as follows:

- **Slot Capabilities** (offset 7Ch)
- **Slot Status and Control** (offset 80h)

Note: *Hot Plug **Slot Status** and other Hot Plug control-related registers are "don't care" for the NT Port Virtual Interface, and should not be modified by the user.*

9.3 Hot Plug Interrupts

Each Hot Plug Controller supports Hot Plug interrupt generation on the following events:

- Attention Button Pressed
- Power Fault Detected
- MRL Sensor Changed
- Presence Detect Changed
- Command Completed

Hot Plug interrupts can be signaled by in-band INT*x* or MSI messages. Only one interrupt mechanism can be selected, and all Hot Plug ports must use the same mechanism.

INT*x* interrupts are enabled if:

- INTA messages are enabled (**Command** register *Interrupt Disable* bit, offset 04h[10]=0) and,
- MSI is disabled (**Message Control** register *MSI Enable* bit, offset 48h[16]=0)

MSI interrupts are enabled if:

- INTA messages are disabled (**Command** register *Interrupt Disable* bit, offset 04h[10]=1) and,
- MSI is enabled (**Message Control** register *MSI Enable* bit, offset 48h[16]=1)

Depending on the downstream port power state, a Hot Plug event can generate a system interrupt or PME. When a PEX 8524 downstream port is in the D0 power state, Hot Plug events generate a system interrupt; when not in the D0 state, a PME interrupt message is generated by Hot Plug events. The **Slot Status** register *Command Completed* bit (offset 80h[20]) does not generate a PME interrupt message. When the system is in Sleep mode, Hot Plug operation uses PME logic to wake up the system.

9.4 Hot Plug Controller Power-Up/Down Sequence

If a Transparent downstream port is enabled, the port's Hot Plug Controller can power-up or power-down the slot. This section describes how this process occurs.

9.4.1 Slot Power-Up Sequence

If a downstream port is connected to a slot, that port's Hot Plug Controller can power up the slot, with or without an external serial EEPROM. Hot Plug Controller sequencing is determined by the states of the following bits:

- **Slot Capabilities** register *Power Controller Present* bit (offset 7Ch[1])
- **Slot Capabilities** register *MRL Sensor Present* bit (offset 7Ch[2])
  (*MRL* is Manually operated Retention Latch)
- **Slot Control** register *Power Controller Control* bit (offset 80h[10])

and the HP_MRL*x*# input state, if the *MRL Sensor Present* bit is set to 1. Hot Plug-configurable features are programmable only by the serial EEPROM.

9.4.1.1 Configuring Hot Plug Controller Slot Power-Up Sequence Features with Serial EEPROM

An external serial EEPROM can be used to configure the Hot Plug Controller and Hot Plug outputs. Features can be changed by using the registers defined in Table 9-3. The Hot Plug Controller outputs remain in the default state described in Table 9-2, before the serial EEPROM image is loaded into the device.

After the serial EEPROM image is loaded, the Hot Plug Controller starts a power-up sequence on each slot that has the **Slot Capabilities** register *Power Controller Present* bit set (offset 7Ch[1]=1) and the **Slot Control** register *Power Controller Control* bit cleared (offset 80h[10]=0).

Table 9-3. Configuring Power-Up Sequence Features with Serial EEPROM

Register Bit	Hot Plug Controller and Hot Plug Output Signal Configurable Features
Power Controller Present (**Slot Capabilities** register, offset 7Ch[1])	The *Power Controller Present* bit enables or disables the Hot Plug Controller on the PEX 8524 downstream ports. If the *Power Controller Present* bit is cleared to 0, the Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state, as defined in Table 9-2. If the *Power Controller Present* bit is enabled (set to 1), the Hot Plug Controller powers up the slot when the MRL is closed and the **Slot Control** register *Power Controller Control* bit is cleared (offset 80h[10]=0). Otherwise, if the *MRL Sensor Present* bit is disabled (cleared to 0), the MRL's position has no effect on powering up the slot.
MRL Sensor Present (**Slot Capabilities** register, offset 7Ch[2])	When enabled (set to 1), the PEX 8524 senses whether the MRL is open or closed for a slot. If this bit is set to 1, the MRL should be Low for power-on for that slot. If this bit is cleared to 0, the MRL position is "don't care" for that slot.
HPC Tpepv Delay (**Power Management Hot Plug User Configuration** register, offset 1E0h[4:3])	This field controls the delay from when HP_PWREN*x*# is asserted Low, to when power is valid at a slot. (Refer to Section 9.4.1.2.) This register is Read-Only and can be set by serial EEPROM. Values for this field are as follows: **Bits [4:3]** — **Delay Value** 00b — 16 ms (default) 01b — 32 ms 10b — 64 ms 11b — 128 ms
HPC Tpvperl Delay (**Power Management Hot Plug User Configuration** register, offset 1E0h[6])	This bit controls the delay from when Power is valid at the slot to when HP_PERST*x*# is de-asserted high. (Refer to Section 9.4.1.2.) Two settings can be specified through the serial EEPROM: **Bit 6** — **Delay Value** 0 — 20 ms 1 — 100 ms (default)
Attention Indicator Present (**Slot Capabilities** register, offset 7Ch[3])	When set to 1, this bit controls whether the HP_ATNLED*x*# output for the slot drives out Active-Low. Otherwise, this output is not functional on the slot.
Power Indicator Present (**Slot Capabilities** register, offset 7Ch[4])	When set to 1, this bit controls whether the HP_PWRLED*x*# output for the slot drives out Active-Low. Otherwise, this output is not functional on the slot.

9.4.1.2 Slot Power-Up Sequencing when *Power Controller Present* Bit Is Set

By default, the *Power Controller Present*, *MRL Sensor Present*, and *Power Controller Control* (when the MRL is open) bits are set to 1. When the serial EEPROM is not present, present but blank, or programmed with default register values, the Hot Plug Controller is initially powered up, and the PEX 8524 is in the following state:

1. Hot Plug Controller is enabled for all slots.
2. All slots are enabled to be powered up.
3. Attention LED (HP_ATNLED*x*#) and Power LED (HP_PWRLED*x*#) are High on the slot chassis.

Immediately after the PEX 8524 exits Reset (PEX_PERST# input goes high), if a downstream port's *MRL Sensor Present* bit is set to 1 (default), the HP_MRL*x*# input for that slot is sampled. If the HP_MRL*x*# input is enabled and asserted (value of 0), the PEX 8524 clears the *Power Controller Control* bit to 0, to enable slot power-up. If the *Power Controller Control* bit is not cleared, either by initially enabling it (default) and asserting HP_MRL*x*#, or by programming both the *MRL Sensor Present* and *Power Controller Control* bit values to 0 in the serial EEPROM, the downstream slot is not powered up and remains in the disabled state, as defined in Table 9-2 and illustrated in Figure 9-3.

If a slot's *Power Controller Present* bit is set to 1, and the *Power Controller Control* bit is cleared to 0 (either by initially enabling and asserting HP_MRL*x*# or by programming the *MRL Sensor Present* and *Power Controller Control* bit values to 0 in the serial EEPROM), the slot starts power-up sequencing with HP_PWREN*x*# and HP_PWRLED*x*# assertion, following PEX_PERST# input de-assertion:

- If the serial EEPROM is not present, HP_PWREN*x*# and HP_PWRLED*x*# are asserted approximately 6.1 ms after PEX_PERST# input is de-asserted
- If the serial EEPROM is present, HP_PWREN*x*# and HP_PWRLED*x*# are asserted approximately 18.7 ms after PEX_PERST# input is de-asserted

The power-up sequence is as follows:

1. The Hot Plug Controller drives HP_PWRLED*x*# Low, to turn On the Power Indicator, and drives HP_PWREN*x*# Low to turn On the external Power Controller.
2. After the programmable T_{pepv} time delay following HP_PWREN*x*# assertion, power to the slot is valid and the Hot Plug Controller drives HP_CLKEN*x*# Low to turn on the Reference Clock (PEX_REFCLKn/p) to the slot. The T_{pepv} time delay is specified by setting the **Power Management Hot Plug User Configuration** register *HPC Tpepv Delay* field (offset 1E0h[4:3]) to a non-zero value. By default, this field is cleared to 00b, indicating a 16-ms time delay from the time HP_PWREN*x*# goes Low to power becoming valid at the slot.
3. After the programmable T_{pvperl} time delay following HP_CLKEN*x*# assertion, the Hot Plug Controller de-asserts HP_PERST*x*# to release slot reset. The T_{pvperl} time delay is specified in the **Power Management Hot Plug User Configuration** register *HPC Tpvperl Delay* bit (offset 1E0h[6]). By default, this bit is set to 1, indicating a 100-ms delay.

   With this default delay, if the serial EEPROM is not present, HP_PERST*x*# output is de-asserted approximately 122 ms after PEX_PERST# input is de-asserted. However, if the serial EEPROM is present, HP_PERST*x*# output is de-asserted approximately 135 ms after PEX_PERST# input is de-asserted.

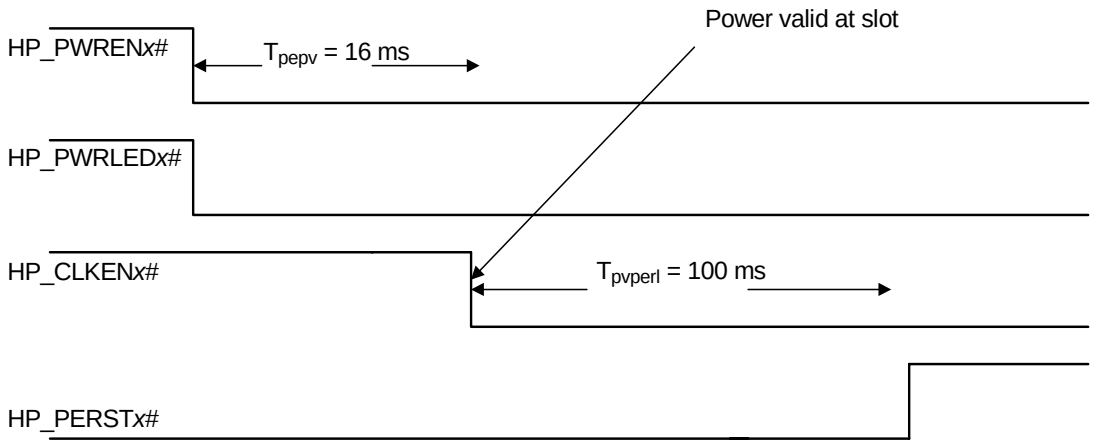
   Because the *PCI Express Base r1.0a* allows the host to start Configuration accesses 100 ms after the Root Complex de-asserts its PERST# output, it is recommended that a programmed serial EEPROM be used to clear the *HPC Tpvperl Delay* bit to 0, to reduce the T_{pvperl} time delay to 20 ms, so that HP_PERST*x*# is de-asserted approximately 55 ms after PEX_PERST# input is de-asserted.

Figure 9-1 illustrates the timing sequence with the *Power Controller Present* bit (offset 7Ch[1]) set to 1. This timing sequence occurs at system power-up, or when a slot is being powered up by the user.

If HP_MRL*x*# is enabled but not asserted to power-up the slot immediately after reset, HP_MRL*x*# can be asserted at runtime to start the slot power-up sequence, provided the *Power Controller Present* and *MRL Sensor Present* bits are set (offset 7Ch[2:1]=11b, either by default values when the serial EEPROM is not present or blank, or by programming the serial EEPROM to set these bits), and the *Power Controller Control* bit is cleared (offset 80h[10]=0, either by the programmed serial EEPROM or by software). Power-up sequencing at runtime is controlled by software clearing the *Power Controller Control* bit after HP_MRL*x*# assertion causes an interrupt, if enabled [the **Slot Control** register *Hot Plug Interrupt Enable* and MRL Sensor Changed Enable bits must be set (offset 80h[5, 2]=11b)]. HP_MRL*x*# assertion and de-assertion at runtime is not latched until the 10-ms de-bounce ensures that the state change is stable.

Slots with the MRL Sensor not present can use the Attention Button Pressed interrupt to generate an event and start the Slot Power-Up sequence at runtime. (Refer to Figure 9-1.)

Figure 9-1. Slot Power-Up Timing when *Power Controller Present* Bit Is Set



Note: *HP_PWRLEDx# is not asserted if the serial EEPROM clears the Power Indicator Present bit (offset 7Ch[4]) to 0.*

9.4.1.3 HP_PERST*x*# (Reset) and HP_PWRLED*x*# Output Power-Up Sequencing when *Power Controller Present* Bit Is Clear

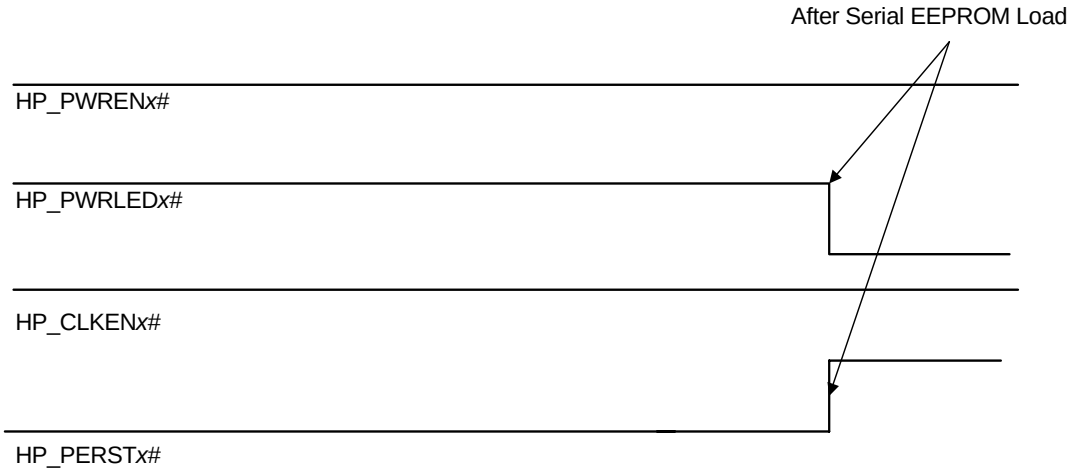
The HP_PERST*x*# and HP_PWRLED*x*# outputs can be used without enabling the Hot Plug Power Controller (HP_PWREN*x*# and HP_CLKEN*x*# outputs and HP_PWRFLT*x*# input). *For example*, HP_PERST*x*# can be used to reset an on-board downstream device.

If the *Power Controller Present* (offset 7Ch[1]) and *Power Controller Control* (offset 80h[10]) bits are cleared to 0 by the serial EEPROM, HP_PERST*x*# is de-asserted (High) and HP_PWRLED*x*# is asserted (Low), after the Root Complex PERST# input is de-asserted, as illustrated in Figure 9-2. However, HP_PWRLED*x*# is not asserted if the serial EEPROM also cleared the *Power Indicator Present* bit (offset 7Ch[4]) to 0.

If the serial EEPROM is initially blank, causing register default values to be loaded, HP_PERST*x*# is not de-asserted and HP_PWRLED*x*# is not asserted unless HP_MRL*x*# is Low. Therefore, if the HP_PERST*x*# and/or HP_PWRLED*x*# outputs are used [and a Manually operated Retention Latch (MRL) is ***not*** used], pull HP_MRL*x*# Low, to allow the outputs to toggle, regardless of whether the serial EEPROM is blank.

HP_PERST*x*# can also be toggled at runtime by toggling the *Power Controller Control* bit, provided that either the *Power Controller Present* bit is cleared, or that HP_PERST*x*# is initially de-asserted during slot power-up sequencing, as described in Section 9.4.1.2. A value of 1 asserts HP_PERST*x*# (Low). A value of 0 de-asserts HP_PERST*x*# (High).

Figure 9-2. Hot Plug Outputs when *Power Controller Present* and *Power Controller Control* Bits Are Cleared



Note: *HP_PWRLEDx# is not asserted if the serial EEPROM clears the Power Indicator Present bit (offset 7Ch[4]) to 0.*

9.4.1.4 Disabling Power-Up Hot Plug Output Sequencing

If the *Power Controller Control* bit is set to 1, after reset, the HP_PWREN*x*#, HP_PWRLED*x*#, and HP_CLKEN*x*# outputs remain High, and the HP_PERST*x*# output remains Low. The HP_PWREN*x*#, HP_PWRLED*x*#, and HP_CLKEN*x*# outputs also remain High if HP_MRL*x*# is not asserted in the default Hot Plug power-up sequencing described in Section 9.4.1.2. (Refer to Figure 9-3.)

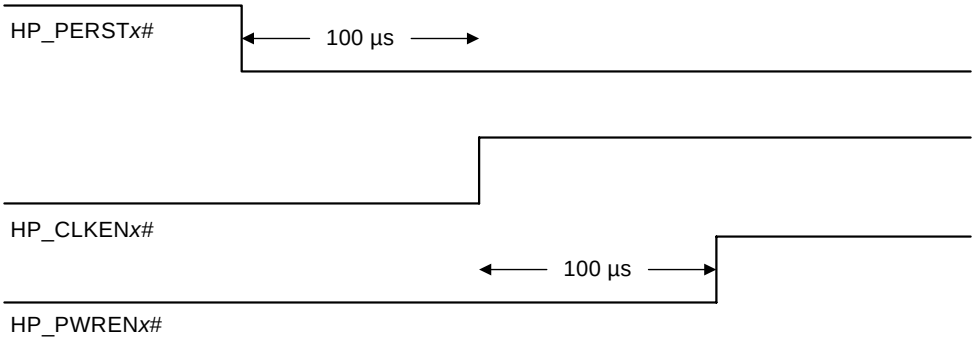
Figure 9-3. Hot Plug Outputs when *Power Controller Control* Bit Is Set

9.4.2 Slot Power-Down Sequence

Software can power-down slots by setting the *Power Controller Control* bit (offset 80h[10]=1). If the *MRL Sensor Present* bit is set (offset 7Ch[2]=1), the Hot Plug Controller can power down the slot if the MRL is open. Figure 9-4 illustrates the following power-down timing sequence for either event:

1. HP_PERST*x*# to the port is asserted.
2. HP_CLKEN*x*# is de-asserted to the slot 100 µs after HP_PERST*x*# is asserted.
3. HP_PWREN*x*# is de-asserted to the slot 100 µs after HP_CLKEN*x*# is de-asserted.

Figure 9-4. Hot Plug Automatic Power-Down Sequence



9.5 Hot Plug Board Insertion and Removal Process

Table 9-4 defines the board insertion procedure supported by the PEX 8524. Table 9-5 defines the board removal procedure.

Table 9-4. Hot Plug Board Insertion Process

Operator / Action	Hot Plug Controller	Software
A. Places board in slot.	**1.** Sets *Presence Detect State* bit to 1. **2.** Sets *Presence Detect Changed* bit to 1. **3.** Generates Interrupt message due to Presence Detect change, if enabled.	Clears *Presence Detect Changed* bit to 0.
	4. Transmits Interrupt de-assertion message, if enabled.	
B. Locks MRL.	**5.** Clears *MRL Sensor State* bit to 0. **6.** Sets *MRL Sensor Changed* bit to 1. **7.** Generates Interrupt message due to MRL Sensor state change, if enabled.	Clears *MRL Sensor Changed* bit to 0.
	8. Transmits Interrupt de-assertion message, if enabled.	
C. Presses Attention Button.	**9.** Sets *Attention Button Pressed* bit to 1. **10.** Generates Interrupt message due to Attention Button Pressed event, if enabled.	Clears *Attention Button Pressed* bit to 0.
	11. Transmits Interrupt de-assertion message, if enabled.	Writes to the **Slot Control** register *Power Indicator Control* field, to blink the Power Indicator LED, which indicates that the board is being powered up.

Continued …

Table 9-4. Hot Plug Board Insertion Process *(Cont.)*

Operator / Action	Hot Plug Controller	Software
D. Power Indicator blinks.	**12.** Sets *Power Indicator Control* field to 10b. **13.** Power Indicator Blink message is transmitted to the downstream device. **14.** Sets *Command Completed* bit to 1. **15.** Generates Interrupt message due to Power Indicator Turn On command completion, if enabled.	Clears *Command Completed* bit to 0.
	16. Transmits Interrupt de-assertion message, if enabled.	Clears **Slot Control** register *Power Controller Control* bit to 0, to turn On power to the port.
	17. Slot is powered up. **18.** After a T_{pepv} delay, sets *Command Completed* bit to 1. **19.** Generates Interrupt message due to Power Turn On command completion, if enabled.	Clears *Command Completed* bit to 0.
	20. Transmits Interrupt de-assertion message, if enabled.	Writes to the **Slot Control** register *Power Indicator Control* field, to turn On the Power Indicator LED, which indicates that the slot is fully powered On.
	21. Sets *Power Indicator Control* field to 01b. **22.** Transmits Interrupt assertion message due to Power Indicator Turn On command completion, if enabled.	Clears *Command Completed* bit to 0.
E. Power Indicator On.	**23.** Transmits Interrupt de-assertion message, if enabled.	

Table 9-5. Hot Plug Board Removal Process

Operator / Action	Hot Plug Controller	Software
A. Presses Attention Button.	**1.** Sets *Attention Button Pressed* bit to 1. **2.** Generates Interrupt message due to Attention Button pressed, if enabled.	Clears *Attention Button Pressed* bit to 0.
	3. Transmits Interrupt de-assertion message, if enabled.	Writes to the **Slot Control** register *Power Indicator Control* field, to blink the Power Indicator LED, which indicates that the board is being powered down.
B. Power Indicator blinks.	**4.** Sets *Power Indicator Control* field to 10b. **5.** Power Indicator Blink message is transmitted to the downstream device. **6.** Sets *Command Completed* bit to 1. **7.** Generates Interrupt message due to Power Indicator command completion, if enabled.	Clears *Command Completed* bit to 0.
	8. Transmits Interrupt de-assertion message, if enabled.	Sets **Slot Control** register *Power Controller Control* bit to 1, to turn Off power to the port.
C. Power Indicator Off.	**9.** Slot is powered Off. **10.** After a T_{pepv} delay, sets the *Command Completed* bit to 1. **11.** Generates Interrupt message due to Power Turn Off command completion, if enabled.	Clears *Command Completed* bit to 0. Clears *Power Indicator Control* field to 00b, to turn Off the Power Indicator LED, which indicates that the slot is fully powered Off and the board can be removed.
D. Power Indicator Off, board ready to be removed.	**12.** Clears *Power Indicator Control* field to 00b. **13.** Sets *Command Completed* bit to 1, due to Power Indicator Off command completion.	Clears *Command Completed* bit to 0.
	14. Transmits Interrupt de-assertion message, if enabled.	
E. Unlocks MRL.	**15.** Sets *MRL Sensor State* bit to 1. **16.** Sets *MRL Sensor Changed* bit to 1. **17.** Generates Interrupt message due to MRL Sensor state change, if enabled.	Clears *MRL Sensor Changed* bit to 0.
	18. Transmits Interrupt de-assertion message, if enabled.	
F. Removes board from slot.	**19.** Clears *Presence Detect State* bit to 0. **20.** Sets *Presence Detect Changed* bit to 1. **21.** Generates Interrupt message due to Presence Detect change, if enabled.	Clears *Presence Detect Changed* bit to 0.
	22. Transmits Interrupt de-assertion message, if enabled.	

Chapter 10 Power Management

10.1 Power Management Capability

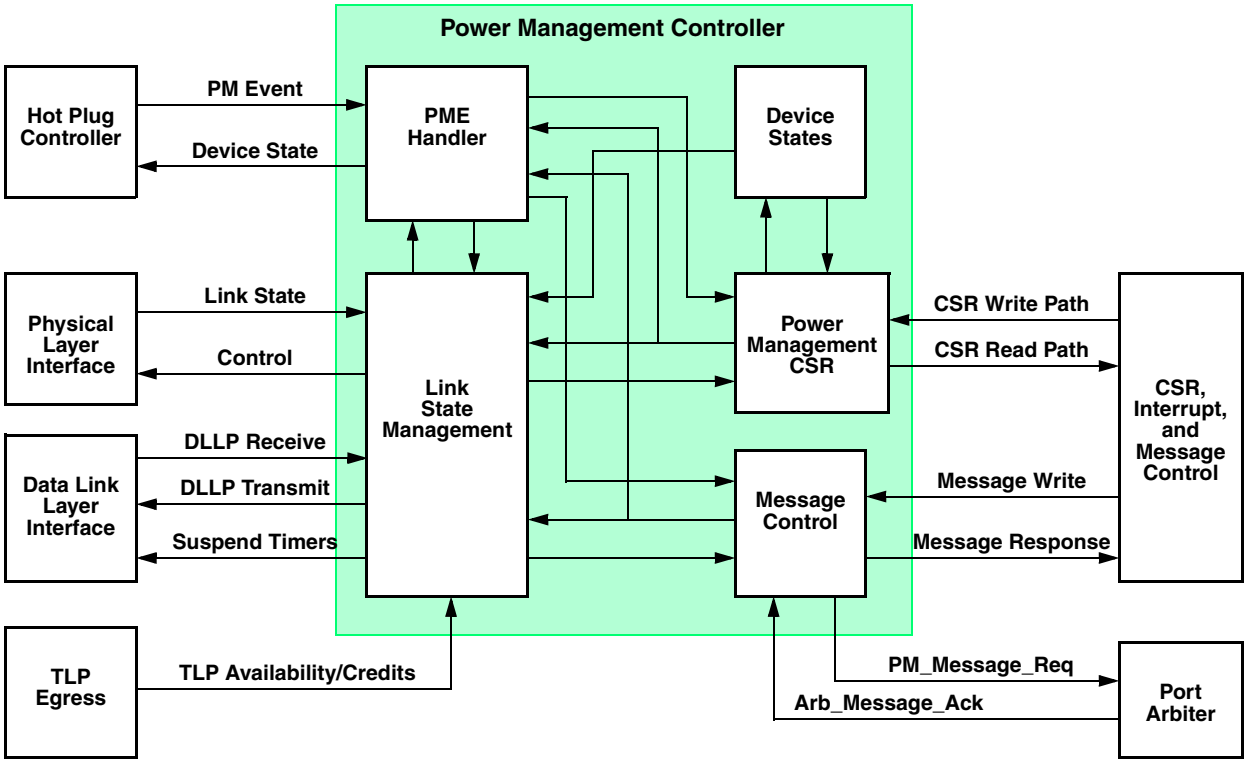
The PEX 8524 Power Management (PM) module interfaces with chip sections to reduce power consumption. The PEX 8524 supports:

- Link Power Management States (L-States)
  - PCI Bus Power Management – L0, L1, L2/L3 Ready, and L3 (Auxiliary power is ***not supported***)
  - Active State Power Management – L0s and L1
- Device Power Management State (D-States) – D0 (D0_uninitialized and D0_active) and D3 (D3hot and D3cold) support
- Power Management Event (PME) support from D3hot
- Power Management Event due to Hot Plug events
- Downstream ports generate and forward PME_Turn_Off broadcast messages
- Implements *PCI Power Mgmt. r1.1*

Note: *Because the PEX 8524 does* ***not support*** *AUX-Power, PME generation from D3cold is* ***not supported****.*

The PM module interfaces with the Physical Layer electrical sub-block to transition the Link state into low-power states when the module receives a Power State Change request from an upstream component, or an internal event forces the Link State entry into low-power states in Hardware-Autonomous PM (Active Link State PM) mode. PCI Express Link states are not directly visible to Conventional PCI Bus driver software; instead, they are derived from the Power Management state of the components residing on those links. A functional block diagram of the PEX 8524's Power Management Controller is illustrated in Figure 10-1.

Figure 10-1. Power Management Controller Functional Block Diagram



Note: *The Hot Plug Controller is available only on downstream ports.*

10.1.1 Device Power States

The PEX 8524 supports the PCI Express PCI-PM D0, D3hot, and D3cold (no VAUX) Device Power Management states. The D1 and D2 states, which are optional in the *PCI Express Base r1.0a*, are ***not supported*** by the PEX 8524.

The D3hot state can be entered from the D0 state, when system software programs the **Power Management Status and Control** register Power State field (offset 44h[1:0]=11b) for the appropriate port. The D0_uninitialized state can be entered from the D3hot state when the upstream and downstream links are in the L0s state and system software clears the **Power Management Status and Control** register *Power State* field (offset 44h[1:0]=00b).

10.1.1.1 D0 State

D0 is divided into two distinct substates – *uninitialized* and *active*. When power is initially applied to a PCI Express component, it defaults to the D0_uninitialized state. The component remains in the D0_uninitialized state until the serial EEPROM load completes.

A device enters the D0_active state when:

- Any single Memory Access Enable occurs
- System software sets any combination of the **Command** register *Bus Master Enable*, *Memory Access Enable*, and/or *I/O Access Enable* bits (offset 04h[2, 1, and/or 0], respectively)

10.1.1.2 D3hot State

A device in the D3hot state must be able to respond to Configuration accesses, allowing transition by software to the D0_uninitialized state. Once in the D3hot state, the device can later be transitioned into the D3cold state by removing power from the device. In the D3hot state, Hot Plug operations cause a PME in the PEX 8524.

10.1.1.3 D3cold State

The PEX 8524 transitions to the D3cold state when power is removed. Re-applying power causes the PEX 8524 to transition from the D3cold state into the D0_uninitialized state, followed by a configuration and link training sequence. The D3cold state assumes that all previous context is lost; therefore, software must save the required context while the PEX 8524 remains in the D3hot state.

The PEX 8524 does ***not support*** AUX-Power; therefore, PME generation from D3cold is ***not supported***.

10.1.2 Link Power Management State

The Power Management state of a link is determined by the D-state of its downstream link. The PEX 8524 holds its upstream and downstream links in the L0 state when it is in standard operating mode (PCI PM state in D0_active). Active-State Link Power Management defines a protocol for components in the D0 state, to reduce link power by placing their links into a low-power state and instructs the opposite end of the link to do likewise. This capability allows Hardware-Autonomous, dynamic-link power reduction beyond what is achievable by Software-Only Power Management. Table 10-1 defines the relationship between a PEX 8524 power state and its downstream link.

Table 10-1. Power States of Connected Link Components

Downstream Component D State	PEX 8524 D State	Permissible Interconnect State	Power Saving Actions
D0	D0	L0	Full power.
		L0s, L1 (optional)	PHY Transmit lanes in high-impedance state.
D1	D0	L1	PHY Transmit lanes in high-impedance state.
D2	D0	L1	
D3hot	D0 or D3hot[a]	L1, L2/L3 Ready	PHY Transmit lanes in high-impedance state. FC and DLL ACK/NAK timers suspended. PLL can be disabled.
D3cold (no AUX Power)	D0, D3hot, or D3cold	L3	Link-Off State. No power to component.

a. The PEX 8524 initiates a link-state transition of its upstream port to L1 when the port is programmed to D3hot.

10.1.3 PEX 8524 PCI Express Power Management Support

The PEX 8524 supports PCI Express features that are required or important for PCI Express switch Power Management. Table 10-2 lists supported and non-supported features and the register bits/fields used for configuration or activation.

Table 10-2. Supported PCI Express Power Management Capabilities

Register		Description	Supported	
Offset	Bit(s)		Yes	No
40h		**Power Management Capability**		
	7:0	**Capability ID** Set to 01h, indicating that the data structure currently being pointed to is the PCI Power Management data structure.	✔	
	15:8	**Next Capability Pointer** Default 48h points to the **Message Signaled Interrupt Capability** register.	✔	
	18:16	**Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1*.	✔	
	19	**PME Clock** Cleared to 0, as required by the *PCI Express Base r1.0a*.	✔	
	21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.		✔
	24:22	**AUX Current** Default 000b indicates that the PEX 8524 does ***not support*** Auxiliary Current requirements.		✔
	25	**D1 Support** Default 0 indicates that the PEX 8524 does ***not support*** the D1 power state.		✔
	26	**D2 Support** Default 0 indicates that the PEX 8524 does ***not support*** the D2 power state.		✔
	31:27	**PME Support** Default 11001b indicates that the corresponding PEX 8524 port forwards PME messages in the D0, D3hot, and D3cold power states.	✔	

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h		**Power Management Status and Control**		
	1:0	**Power State** This field is used to determine the current power state of the port, and to set the port into a new power state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	✔	
	8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8524 port[a] 1 = Enables PME generation by the corresponding PEX 8524 port	✔	
	12:9	**Data Select** RW by Serial EEPROM mode only[b]. Bits [12:9] select the **Data** and **Data Scale** registers. 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	✔	
		RO for hardware auto-configuration.		✔
	14:13	**Data Scale** RW by Serial EEPROM mode only[b]. There are four internal **Data Scale** registers per port. Bits [12:9], *Data Select*, select the **Data Scale** register.	✔	
	15	**PME Status** 0 = PME is not generated by the corresponding PEX 8524 port[a] 1 = PME is being generated by the corresponding PEX 8524 port	✔	
		Power Management Control/Status Bridge Extensions		
	22	**B2/B3 Support** Cleared to 0, as required by the *PCI Power Mgmt. r1.1*.		✔
	23	**Bus Power/Clock Control Enable** Cleared to 0, as required by the *PCI Power Mgmt. r1.1*.		✔
		Power Management Data		
	31:24	**Data** RW by Serial EEPROM mode only[b]. There are four internal **Data** registers per port. Bits [12:9], *Data Select*, select the **Data** register.	✔	

a. Because the PEX 8524 does not support auxiliary power, this bit is not sticky, and is always cleared to 0 at power-on reset.

*b. With no serial EEPROM, reads return 00h for the **Data Scale** and **Data** registers (for all Data Selects).*

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
6Ch		**Device Capabilities**		
	8:6	**Endpoint L0s Acceptable Latency** Because the PEX 8524 is a switch and not an endpoint, it does ***not support*** this feature. 000b = Disables the capability		✔
	11:9	**Endpoint L1 Acceptable Latency** Because the PEX 8524 is a switch and not an endpoint, it does ***not support*** this feature. 000b = Disables the capability		✔
	12	**Attention Button Present (Upstream Port)** For the PEX 8524 upstream port, value of 1 indicates that an Attention Button is implemented on that adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Button is ***not*** present on an adapter board for which the PEX 8524 provides the system interface. Do not change for downstream ports.	✔	
	13	**Attention Indicator Present (Upstream Port)** For the PEX 8524 upstream port, value of 1 indicates that an Attention Indicator is implemented on the adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Indicator is ***not*** present on an adapter board for which the PEX 8524 provides the system interface. Do not change for downstream ports.	✔	
	14	**Power Indicator Present (Upstream Port)** For the PEX 8524 upstream port, value of 1 indicates that a Power Indicator is implemented on the adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that a Power Indicator is ***not*** present on an adapter board for which the PEX 8524 provides the system interface. Do not change for downstream ports.	✔	
	25:18	**Captured Slot Power Limit Value (Upstream Port)** For the PEX 8524 upstream port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Scale* field. Do not change for downstream ports	✔	
	27:26	**Captured Slot Power Limit Scale (Upstream Port)** For the PEX 8524 upstream port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Value* field. 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001 Do not change for downstream ports.	✔	

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
		Device Status and Control		
70h	10	**Auxiliary (AUX) Power PM Enable** Cleared to 0 for each port.		✔
	20	**Auxiliary (AUX) Power Detected** Cleared to 0 for each port.		✔
		Link Capabilities		
74h	11:10	**Active State Power Management (ASPM) Support** Indicates the level of ASPM supported by the port. 01b = L0s link power state entry is supported 10b = L0s and L1 link power states are supported All other values are ***reserved***.	✔	
	14:12	**L0s Exit Latency** 101b = Corresponding PEX 8524 port L0s Exit Latency is between 1 and 2 µs	✔	
	17:15	**L1 Exit Latency** 101b = Corresponding PEX 8524 port L1 Exit Latency is between 16 and 32 µs	✔	
		Link Status and Control		
78h	1:0	**Active State Power Management (ASPM) Control** 00b = Disables L0s and L1 Entries for the corresponding PEX 8524 port[c] 01b = Enables only L0s Entry 10b = Enables only L1 Entry 11b = Enables both L0s and L1 Entries	✔	
		Slot Capabilities (for Downstream Ports)		
7Ch	0	**Attention Button Present** 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8524 downstream port Do not change for upstream port.	✔	
	1	**Power Controller Present** 0 = Power Controller is not implemented 1 = Power Controller is implemented for the slot of the corresponding PEX 8524 downstream port Do not change for upstream port.	✔	
	2	**MRL Sensor Present** 0 = MRL Sensor is not implemented 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8524 downstream port Do not change for upstream port.	✔	
	3	**Attention Indicator Present** 0 = Attention Indicator is not implemented 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8524 downstream port Do not change for upstream port.	✔	

c. The port receiver must be capable of entering the L0s state, regardless of whether the state is disabled.

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
7Ch		**Slot Capabilities (for Downstream Ports) *(Cont.)***		
	4	**Power Indicator Present** 0 = Power Indicator is not implemented 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8524 downstream port Do not change for upstream port.	✔	
	5	**Hot Plug Surprise** 0 = No device in the corresponding PEX 8524 downstream port slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8524 downstream port slot can be removed from the system without prior notification Do not change for upstream port.	✔	
	6	**Hot Plug Capable** 0 = Corresponding PEX 8524 downstream port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8524 downstream port slot is capable of supporting Hot Plug operations Do not change for upstream port.	✔	
	14:7	**Slot Power Limit Value** The maximum power available from the corresponding PEX 8524 downstream port is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the value specified by the *Slot Power Limit Scale* field. Do not change for upstream port.	✔	
	16:15	**Slot Power Limit Scale** The maximum power available from the corresponding PEX 8524 downstream port is determined by multiplying the value in this field by the *Slot Power Limit Value* field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x Do not change for upstream port.	✔	

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
80h		**Slot Status and Control (for Downstream Ports)**		
	1	**Power Fault Detector Enable** 0 = Function is disabled 1 = Enables software notification with a Hot Plug interrupt if the port is in the D0 Power State (**Power Management Status and Control** register Power State field, offset 44h[1:0]=00b), or with a PME message if the port is in the D3hot state (offset 44h[1:0]=11b), for a Power Fault event on the corresponding PEX 8524 downstream port. Do not change for upstream port.	✔	
	9:8	**Power Indicator Control** Controls the Power Indicator on the corresponding PEX 8524 downstream port slot. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator Software must use a Byte or Word Write (and not a DWord Write) to control the HP_PWRLED*x*# Output signal. Reads return the corresponding PEX 8524 downstream port Power Indicator's current state. Do not change for upstream port.	✔	
	10	**Power Controller Control** Controls the Power Controller on the corresponding PEX 8524 downstream port slot. 0 = Turns On Power Controller; requires some delay to be effective 1 = Turns Off Power Controller Software must use a Byte or Word Write (and not a DWord Write) to control the Power Controller Output signals. ***Note:*** *Value of 0 requires some delay to be effective.*	✔	
	17	**Power Fault Detected** Set to 1 when the Power Controller of the corresponding PEX 8524 downstream port slot detects a Power Fault at the slot. Do not change for upstream port.	✔	
138h		**Power Budgeting Extended Capability**		
	15:0	**Extended Capability ID** Set to 0004h, as required by the *PCI Express Base r1.0a*.	✔	
	19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base r1.0a*.	✔	
	31:20	**Next Capability Offset** Set to 148h, which addresses the PEX 8524 **Virtual Channel Extended Capability** registers.	✔	
13Ch		**Data Select**		
	7:0	**Data Select** Indexes the Power Budgeting Data reported by way of eight **Power Budgeting Data** registers per port and selects the DWord of Power Budgeting Data that appears in each **Power Budgeting Data** register. Index values start at 0, to select the first DWord of Power Budgeting Data; subsequent DWords of Power Budgeting Data are selected by increasing index values 1 to 7.	✔	

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
140h		**Power Budgeting Data**		
	7:0	**Base Power** Eight registers/port. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the *Data Scale* to produce the actual power consumption value.	✔	
	9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption of the device is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	
	12:10	**PM Sub-State** 000b = Corresponding PEX 8524 port is in the default Power Management sub-state	✔	
	14:13	**PM State** Current power state. 00b = D0 state 01b = ***Not used – D1 state not supported*** 10b = ***Not used – D2 state not supported*** 11b = D3 state	✔	
	17:15	**Type** Type of operating condition. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other values are ***reserved***.	✔	
	20:18	**Power Rail** Power Rail of operating condition. 000b = Power is 12V 001b = Power is 3.3V 010b = Power is 1.8V 111b = Thermal All other values are ***reserved***.	✔	
	Note: *There are eight registers per port that can be programmed, through the serial EEPROM. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (offset 13Ch[7:0]).*			

Table 10-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
144h		**Power Budget Capability**		
	0	**System Allocated** 1 = Power budget for the device is included within the system power budget	✔	
1E0h		**Power Management Hot Plug User Configuration**		
	0	**L0s Entry Idle Count** Time to meet to enter L0s. 0 = Idle condition lasts for 1 µs 1 = Idle condition lasts for 4 µs	✔	
	1	**L1 Upstream Port Receiver Idle Count** For active L1 entry. 0 = Upstream port receiver idle for 2 µs 1 = Upstream port receiver idle for 3 µs	✔	
	2	**HPC PME Turn-Off Enable** 1 = PME Turn-off message is transmitted before the port is turned Off on a downstream port	✔	
	4:3	**HPC T_{pepv} Delay** Slot power-applied to power-valid delay time. 00b = 16 ms 01b = 32 ms 10b = 64 ms 11b = 128 ms	✔	
	5	**HPC Inband Presence-Detect Enable** 0 = HP_PRSNT[1:0]# or HP_PRSNT[11:8]# Input balls are used to detect a board present in the slot 1 = SerDes receiver detect mechanism is used to detect a board present in the slot	✔	
	6	**HPC T_{pvperl} Delay** Downstream port power-valid to reset signal release time. 0 = 20 ms 1 = 100 ms (default)	✔	

Chapter 11 PEX 8524 Transparent Mode Port Registers

11.1 Introduction

This chapter defines the PEX 8524 Transparent mode port registers. The PEX 8524 ports have their own Configuration, Capability, Control, and Status register space. The register mapping is the same for each port. (Refer to Table 11-1.) This chapter also presents the PEX 8524 programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in the upstream and downstream ports. (Refer to Figure 11-1.)

NT Port registers are defined in Chapter 15, "NT Port Virtual Interface Registers," and Chapter 16, "NT Port Link Interface Registers."

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r2.3*
- *PCI Power Mgmt. r1.1*
- *PCI-to-PCI Bridge r1.1*
- *PCI Express Base r1.0a*

Note: *For the PEX 8524 to properly route Memory and I/O requests and Completions, each station contains Content Addressable Memory (CAM) registers that hold mirror copies of certain registers in each port. Refer to the PEX 85XX EEPROM – PEX 8532/8524/8516 Design Note, Section 6.12, "Shadowed Registers." If the registers that are shadowed are programmed by the serial EEPROM to non-default values, the corresponding CAM registers must be programmed by serial EEPROM to contain the same values as the shadowed registers.*

11.2 Type 1 PEX 8524 Port Register Map

Table 11-1. Type 1 PEX 8524 Port Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Configuration Header Registers	Capability Pointer (40h)	00h … 34h … 3Ch
Next Capability Pointer (48h)	Capability ID (01h)	40h
Power Management Capability Registers		44h
Next Capability Pointer (68h)	Capability ID (05h)	48h
Message Signaled Interrupt Capability Registers		… 64h
Next Capability Pointer (00h)	Capability ID (10h)	68h
PCI Express Capability Registers		… 80h
Reserved		84h – FCh
Next Capability Offset (FB4h)	1h / Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers		104h 108h
Reserved		10Ch – 134h
Next Capability Offset (148h)	1h / Extended Capability ID (0004h)	138h
Power Budgeting Extended Capability Registers		… 144h
Next Capability Offset (000h)	1h / Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers		… 1C4h
PLX-Specific Registers		1C8h … C08h
Reserved		C3Ch – FB0h
Next Capability Offset (138h)	1h / PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Capability Registers		… FFCh

11.3 PEX 8524 Port Register Configuration and Map

The PEX 8524 port registers are configured similarly – not all the same. Port 0 of Station 0 and Port 8 of Station 1 include more device-specific registers than the other station ports. The registers for these ports contain setup and control information specific to the station. Also, Port 0 of Station 0 contains registers used to set up and control the switch, and serial EEPROM interface logic and control.

The port register map is defined in Table 11-2. (Refer to Appendix A, "Serial EEPROM Memory Map," for a detailed description of this register map.)

Table 11-2. PEX 8524 Port Register Configuration and Map

Register Types	Station 0, Port 0	Station 1, Port 8	Station 0, Port 1 Station 1, Ports 9, 10, 11
Configuration Header Registers	00h - 3Ch	00h - 3Ch	00h - 3Ch
Power Management Capability Registers	40h - 44h	40h - 44h	40h - 44h
Message Signaled Interrupt Capability Registers	48h - 64h	48h - 64h	48h - 64h
PCI Express Capability Registers	68h - 8Ch	68h - 8Ch	68h - 8Ch
Device Serial Number Extended Capability Registers	100h - 108h	100h - 108h	100h - 108h
Power Budgeting Extended Capability Registers	138h - 144h	138h - 144h	138h - 144h
Virtual Channel Extended Capability Registers	148h - 1C4h	148h - 1C4h	148h - 1C4h
ECC Check Disable	1C8h	1C8h	
Device-Specific Error	1CCh - 1D0h	1CCh - 1D0h	
Debug	1D4h - 1DCh	1D4h - 1D8h	
Power Management, Hot Plug, and Miscellaneous Control	1E0h - 1FCh	1E0h - 1ECh, 1F8h - 1FCh	1E0h - 1ECh, 1F8h - 1FCh
Physical Layer (all except for Serial EEPROM-related)	200h - 25Ch	200h - 25Ch	
Serial EEPROM	260h - 264h		
Bus Number CAM Station 0, Station 1	2C8h - 2F4h	2C8h - 2F4h	
I/O CAM Station 0, Station 1	308h - 31Ch	308h - 31Ch	
AMCAM Memory Base and Limit	348h - 404h	348h - 404h	
Ingress Control Registers	660h - 73Ch	660h - 73Ch	
I/O CAM Upper Station 0, Station 1	680h - 6ACh	680h - 6ACh	
Station 0 BAR, Station 1 BAR	6C0h - 71Ch	6C0h - 71Ch	
Virtual Channel Station 0, Station 1	740h - 79Ch 840h - 9ECh	740h - 79Ch 840h - 9ECh	740h
Ingress Credit Handler (INCH) Registers	9F0h - B7Ch	9F4h- B7Ch	A00h - B7Ch
Ingress One-Bit ECC Error Count Register	BE8h	BE8h	
Relaxed Completion Ordering (Ingress) Register – Silicon Revisions BB/BC Only	BECh	BECh	
Relaxed Ordering Mode (Ingress) Register	BF0h - BFCh	BF0h - BFCh	
Internal Credit Handler (ITCH) VC&T Threshold Registers	C00h - C08h	C00h - C08h	
Advanced Error Reporting Capability Registers	FB4h - FFCh	FB4h - FFCh	FB4h - FFCh

11.4 Register Access

Each PEX 8524 port implements a 4-KB Configuration space. The lower 256 bytes (offsets 00h through FFh) is the PCI-compatible Configuration space, and the upper 960 Dwords (offsets 100h through FFFh) is the PCI Express Extended Configuration space. The PEX 8524 supports three mechanisms for accessing registers:

- PCI r2.3-Compatible Configuration Mechanism
- PCI Express Enhanced Configuration Mechanism
- PLX-Specific Memory-Mapped Configuration Mechanism

11.4.1 *PCI r2.3*-Compatible Configuration Mechanism

The *PCI r2.3*-Compatible Configuration mechanism provides standard access to the PEX 8524 ports' first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration space. This mechanism is used to access the PEX 8524 port Type 1 (PCI-to-PCI Bridge) registers:

- Configuration Header Registers
- Power Management Capability Registers
- Message Signaled Interrupt Capability Registers
- PCI Express Capability Registers

The *PCI r2.3*-Compatible Configuration mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8524 Configuration registers. The PEX 8524 upstream port captures the Bus and Device Numbers assigned by the upstream device on the PCI Express link attached to the PEX 8524 upstream port, as required by the *PCI Express Base r1.0a*.

The PEX 8524 decodes all Type 1 Configuration accesses received on its upstream port, when any of the following conditions exist:

- If the Bus Number specified in the Configuration access is the number of the PEX 8524 internal Virtual PCI Bus, the PEX 8524 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the PCI-to-PCI bridge in one of the PEX 8524 downstream ports, the PEX 8524 processes the Read or Write request to the specified downstream port register specified in the original Type 1 Configuration access.
  - If the specified Device Number does not correspond to any of the PEX 8524 downstream port Device Numbers, the PEX 8524 responds with an *Unsupported Request* (UR).
    - If the specified Bus Number in the Type 1 Configuration access is not the number of the PEX 8524 internal virtual PCI Bus, but is the number of one of the PEX 8524 downstream port secondary/subordinate buses, the PEX 8524 passes the configuration access onto the PCI Express link attached to that PEX 8524 downstream port.
    - If the specified Bus Number is the downstream port Secondary Bus Number, and the specified Device Number is 0, the PEX 8524 converts the Type 1 Configuration access to a Type 0 Configuration access before passing it on.
    - If the specified Device Number is not 0, the downstream port drops the TLP and generates a UR.
    - If the specified Bus Number is not the downstream port Secondary Bus Number, the PEX 8524 passes along the Type 1 Configuration access, without change.

Because the *PCI r2.3*-Compatible Configuration mechanism is limited to the first 256 bytes of the PCI Express Configuration Space of the PEX 8524 ports, the PCI Express Enhanced Configuration mechanism (described in Section 11.4.2) or PLX-Specific Memory-Mapped Configuration mechanism (described in Section 11.4.3) must be used to access beyond byte FFh. The PCI Express Enhanced Configuration mechanism can access the registers in the PCI-compatible region, as well as those in the PCI Express Extended Configuration space that are defined by PCI Express specifications; however, it generally cannot access the PEX 8524 device-specific registers above 100h. The PLX-Specific Memory-Mapped Configuration mechanism can access all PEX 8524 registers.

11.4.2 PCI Express Enhanced Configuration Mechanism

The PCI Express Enhanced Configuration mechanism is implemented on all PCI Express PCs and on systems that do not implement a processor-specific firmware interface to the Configuration space, providing a Memory-Mapped Address space in the Root Complex through which the Root Complex translates a Memory access into one or more Configuration requests. Device drivers normally use an application programming interface (API) provided by the Operating System, to use the PCI Express Enhanced Configuration mechanism.

The PCI Express Enhanced Configuration mechanism is used to access the PEX 8524 port Type 1 (PCI-to-PCI Bridge) registers that are defined by PCI Express specifications:

- Configuration Header Registers
- Power Management Capability Registers
- Message Signaled Interrupt Capability Registers
- PCI Express Capability Registers
- Device Serial Number Extended Capability Registers
- Power Budgeting Extended Capability Registers
- Virtual Channel Extended Capability Registers
- Advanced Error Reporting Capability Registers

The PEX 8524 device-specific registers that exist in the PCI Express Extended Configuration space (above 100h) generally cannot be accessed by the PCI Express Enhanced Configuration mechanism. The PLX-Specific Memory-Mapped Configuration mechanism (described in Section 11.4.3) can access all PEX 8524 registers.

11.4.3 PLX-Specific Memory-Mapped Configuration Mechanism

The PLX-Specific Memory-Mapped Configuration mechanism provides a method to access the Configuration registers of each port in a single Memory map, as illustrated in Figure 11-1. The registers of all ports are contained within a 4-KB range. The PEX 8524 supports up to six simultaneously active ports.

The PEX 8524 requires a single contiguous Memory space of 128 KB to contain all the PEX 8524 Configuration registers and sufficient Memory space to support software compatibility for future device expansion.

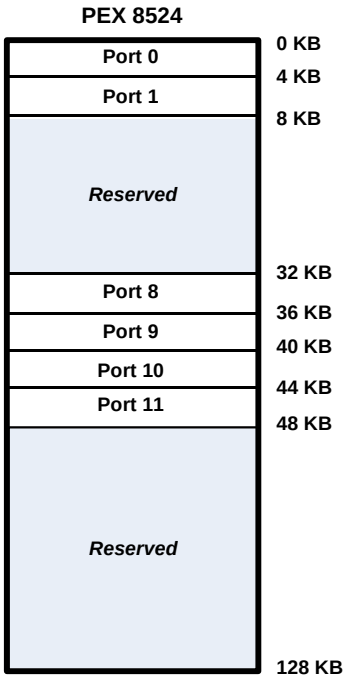
To use the PLX-Specific Memory-Mapped Configuration mechanism, program the upstream port's Type 1 Configuration Space **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively) registers. After the PEX 8524 upstream port Memory-Mapped register Base Address registers are configured, Port 0 registers can be accessed with Memory Reads from and Writes to the first 4 KB (0h to FFFh), Port 1 registers can be accessed with Memory Reads from and Writes to the second 4 KB (1000h to 1FFFh), Port 8 registers can be accessed with Memory Reads from and Writes to the ninth 4 KB (8000h to 8FFFh), and so forth. Within each of these 4-KB windows, individual registers are located at the DWord offsets indicated in Table 11-1.

The upstream port **BAR0** and **BAR1** registers are typically enumerated at boot time, by BIOS or the Operating System (OS) software. When the registers are written (by serial EEPROM or software), the PEX 8524 automatically copies the values into the **BAR0** and **BAR1** Shadow registers that exist in Ports 0 and 8, located at offsets 6C0h through 71Ch. The particular registers used within this block depend upon which port is the upstream port.

If the upstream port **BAR0** and **BAR1** registers are enumerated by serial EEPROM, rather than by BIOS/OS, the serial EEPROM must be programmed to also load the same values to the corresponding **BAR0** and **BAR1** Shadow registers in each station.

Note: *The shadow registers provide for another option. After **BAR0** and **BAR1** are programmed, it is possible to overwrite the "shadowed" location (using the serial EEPROM or software) to set up non-tree hierarchies, in which each station can have different Memory windows. If doing this, it is recommended to match the upstream station shadow register with the BARs.*

Figure 11-1. PEX 8524 Register Offset from Upstream Port BAR0/1 Base Address (Transparent Mode)



11.5 Register Descriptions

The remainder of this chapter details the PEX 8524 registers, including:

- Bit/field names
- Description of register functions for the PEX 8524 upstream port and downstream ports
- Type (*such as* RW or HwInit; refer to Table 11-3 for Type descriptions)
- Whether the power-on/reset value can be modified by way of the PEX 8524 serial EEPROM initialization feature
- Default power-on/reset value

Table 11-3. Register Types, Grouped by User Accessibility

Type	Description
HwInit	**Hardware Initialized** Refers to the PEX 8524 Hardware Initialization mechanism or PEX 8524 Serial EEPROM register initialization feature. Read-Only after initialization and can only be reset with a Fundamental Reset.
RW	**Read-Write** Read/Write and is set or cleared to the needed state by software.
RW1C	**Read-Only Status, Write 1 to Clear** Write 1 to clear status register or bit. Indicates status when read. A status bit set by the system to 1 (to indicate status) is cleared by writing 1 to that bit. Writing 0 has no effect.
RW1CS	**Read-Only Status, Write 1 to Clear, Sticky** Same as RW1C, except that bits are not modified by a Hot Reset.
RW1S	**Read-Write, Write 1 to Set, Sticky** Non-Transparent ports contain these types of Device-Specific Control registers. Software writes 1 to the register to enable control and 1 to a register with RW1C privilege to clear the control. Writing 0 has no effect.
RWS	**Read-Write, Sticky** Same as RW, except that bits are not modified by a Hot Reset.
RO	**Read-Only** Read-Only and cannot be altered by software. Initialized by the PEX 8524 hardware initialization mechanism or PEX 8524 serial EEPROM register initialization feature.
ROS	**Read-Only, Sticky** Same as RO, except that bits are not initialized nor modified by a Hot Reset.

11.6 Configuration Header Registers

Table 11-4. Configuration Header Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST *(Not Supported)*	Header Type and Multi-Function	Primary Latency Timer	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit	I/O Base	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Upper Base Address[63:32]				28h
Prefetchable Memory Upper Limit Address[63:32]				2Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		30h
Reserved			Capability Pointer (40h)	34h
Expansion ROM Base Address *(Not Supported)*				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch

Register 11-1. 00h Product Identification (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Vendor ID** Unless overwritten by the serial EEPROM, returns the PLX PCI-SIG-assigned Vendor ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Vendor ID with another Vendor ID.	HwInit	Yes	10B5h
31:16	**Device ID** Unless overwritten by the serial EEPROM, 8532h is returned by the PEX 8524V and 8524h is returned by the PEX 8524, the PLX-assigned Device ID. The Serial EEPROM register initialization capability is used to replace the PLX-assigned Device ID with another Device ID.	HwInit	Yes	8532h (PEX 8524V) 8524h (PEX 8524)

Register 11-2. 04h Command/Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
	Command			
0	**I/O Access Enable** 0 = PEX 8524 ignores I/O accesses on the corresponding port's primary interface 1 = PEX 8524 responds to I/O accesses on the corresponding port's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8524 ignores Memory accesses on the corresponding port's primary interface 1 = PEX 8524 responds to Memory accesses on the corresponding port's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls the PEX 8524 Memory and I/O request forwarding in the upstream direction. Neither affect message forwarding nor Completions in the upstream or downstream direction. 0 = PEX 8524 handles Memory and I/O requests received on the corresponding port downstream/secondary interface as Unsupported Requests (UR); for Non-Posted Requests, the PEX 8524 returns a Completion with UR Completion status 1 = PEX 8524 forwards Memory and I/O requests in the upstream direction	RW	Yes	0
3	**Special Cycle Enable** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
4	**Memory Write and Invalidate** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
5	**VGA Palette Snoop** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
6	**Parity Error Response Enable** Controls the *Master Data Parity Error* bit.	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
8	**SERR# Enable** Controls the *Signaled System Error* bit. When = 1, enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex.	RW	Yes	0
9	**Fast Back-to-Back Transactions Enabled** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
10	**Interrupt Disable** 0 = Corresponding PEX 8524 port is enabled to generate INT*x* Interrupt messages 1 = Corresponding PEX 8524 port is prevented from generating INT*x* Interrupt messages	RW	Yes	0
15:11	***Reserved***			00h

Register 11-2. 04h Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Status			
18:16	***Reserved***			000b
19	**Interrupt Status** 0 = No INT*x* Interrupt message is pending 1 = INT*x* Interrupt message is pending internally to the corresponding PEX 8524 port	RO	Yes	0
20	**Capabilities List** Required by the *PCI Express Base r1.0a* to be 1 at all times.	RO	Yes	1
21	**66 MHz Capable** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
22	***Reserved***			0
23	**Fast Back-to-Back Transactions Capable** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
24	**Master Data Parity Error** If the *Parity Error Response Enable* bit is set to 1, the corresponding PEX 8524 port sets this bit to 1 when the port: • Forwards the poisoned TLP Write request from the secondary to the primary interface, **or** • Receives a Completion marked as poisoned on the primary interface If the *Parity Error Response Enable* bit is cleared to 0, the PEX 8524 never sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL Timing** Cleared to 00b, as required by the *PCI Express Base r1.0a.*	RO	No	00b
27	**Signaled Target Abort** When a Memory-Mapped access payload length is greater than one DWord, the PEX 8524 upstream port sets this bit to 1. This error is natively reported by the **Uncorrectable Error Status** register *Completer Abort Status* bit (offset FB8h[15]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 11-2. 04h Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
28	**Received Target Abort** Cleared to 0. It is never set to 1.	RO	No	0
29	**Received Master Abort** Cleared to 0. It is never set to 1.	RO	No	0
30	**Signaled System Error** When the *SERR# Enable* bit is set to 1, the corresponding PEX 8524 port sets this bit to 1 when it transmits an ERR_FATAL or ERR_NONFATAL message to its upstream device. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** Set to 1 when the corresponding port receives a Poisoned TLP on its primary side, regardless of the *Parity Error Response Enable* bit state. This error is natively reported by the upstream port's **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 11-3. 08h Class Code and Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the silicon revision (AAh, BBh, or BCh for PEX 8524V; BBh or BCh for PEX 8524), the PLX-assigned Revision ID for this version of the PEX 8524. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Revision ID with another Revision ID. ***Note:*** ***Silicon Revision BB only*** *– Bit 0 is hardwired to 1 and is not programmable by serial EEPROM.* ***Silicon Revision BC only*** *– Bits [2:0] are hardwired to 100b and are not programmable by serial EEPROM.*	RO	Yes (Refer to Note)	AAh, BBh, or BCh (PEX 8524V) or BBh or BCh (PEX 8524)
Class Code				**060400h**
15:8	**Programming Interface** PEX 8524 ports support the *PCI-to-PCI Bridge r1.1* requirements, but not subtractive decoding, on its upstream interface.	RO	Yes	00h
23:16	**Sub-Class Code** PCI-to-PCI bridge.	RO	Yes	04h
31:24	**Base Class Code** Bridge device.	RO	Yes	06h

Register 11-4. 0Ch Miscellaneous Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Cache Line Size** Implemented as a Read-Write field for Conventional PCI-compatibility purposes and does not impact PEX 8524 functionality.	RW	Yes	00h
15:8	**Primary Latency Timer** Cleared to 00h, as required by the *PCI Express Base r1.0a.*	RO	No	00h
22:16	**Header Type** Corresponding PEX 8524 port Configuration Space header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the *PCI-to-PCI Bridge r1.1*.	RO	Yes	01h
23	**Multi-Function** Always 0, because the PEX 8524 is a single-function device.	RO	Yes	0
31:24	**BIST** ***Not supported***	RO	No	00h

Register 11-5. 10h Base Address 0 (Upstream Port Only; *Reserved* for Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
0	**Memory Space Indicator** When enabled, the Base Address register maps the corresponding PEX 8524 port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	Upstream	RO	No	0
	Reserved for downstream ports.	Downstream			0
2:1	**Memory Map Type** 00b = Corresponding PEX 8524 port Configuration registers can be mapped anywhere in 32-bit Memory Address space 10b = Corresponding PEX 8524 port Configuration registers can be mapped anywhere in 64-bit Memory Address space 01b, 11b = ***Reserved***	Upstream	RO	Yes	00b
	Reserved for downstream ports.	Downstream			00b
3	**Prefetchable** The Base Address register maps the corresponding PEX 8524 port Configuration registers into Non-Prefetchable Memory space by default. ***Note:*** *Hardwired to 0.*	Upstream	RO	No	0
	Reserved for downstream ports.	Downstream			0
16:4	***Reserved***			No	0-0h
31:17	**Base Address** Base Address for PLX-Specific Memory-Mapped Configuration mechanism.	Upstream	RW	Yes	0000h
	Reserved for downstream ports.	Downstream			0000h

Register 11-6. 14h Base Address 1 (Upstream Port Only; *Reserved* for Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
31:0	**Base Address 1** For 64-bit addressing (**Base Address 0** register *Memory Map Type* field is set to 10b), Base Address 1 extends Base Address 0 to provide the upper 32 Address bits.	Upstream	RW	Yes	0000_0000h
	Read-Only when the **Base Address 0** register *Memory Map Type* field indicates 32-bit memory addressing (offset 10h[2:1]=00b).		RO	No	
	Reserved for downstream ports.	Downstream			0000_0000h

Register 11-7. 18h Bus Number (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Records the Bus Number of the PCI Bus segment to which the primary interface of this port is connected. Set by Configuration software.	RW	Yes	00h
15:8	**Secondary Bus Number** Records the Bus Number of the PCI Bus segment that is the secondary interface of this port. Set by Configuration software.	RW	Yes	00h
23:16	**Subordinate Bus Number** Records the Bus Number of the highest numbered PCI Bus segment that is subordinate to this port. Set by Configuration software.	RW	Yes	00h
31:24	**Secondary Latency Timer** Cleared to 00h, as required by the *PCI Express Base r1.0a.*	RO	No	00h

Register 11-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
	I/O Base			
3:0	**I/O Base Addressing Capability** 1h = 32-bit Address decoding is supported Other values are not allowed.	RO	Yes	1h
7:4	**I/O Base Address[15:12]** The PEX 8524 ports use their **I/O Base** and **I/O Limit** registers to determine the address range of I/O transactions to forward from the primary interface to the secondary interface or vice versa. I/O Base Address[15:12] bits specify the corresponding PEX 8524 port I/O Base Address[15:12]. The PEX 8524 assumes I/O Base Address[11:0] = 000h. For 16-bit I/O addressing, the PEX 8524 assumes Address[31:16] = 0000h. For 32-bit addressing, the PEX 8524 decodes Address[31:0], and uses the *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits*.	RW	Yes	Fh
	I/O Limit			
11:8	**I/O Limit Addressing Capability** 1h = 32-bit Address decoding is supported Other values are not allowed.	RO	Yes	1h
15:12	**I/O Limit Address[15:12]** The PEX 8524 ports use their **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from the primary interface to the secondary interface or vice versa. I/O Limit Address[15:12] specify the corresponding PEX 8524 port I/O Limit Address[15:12]. The PEX 8524 assumes Address bits [11:0] of the I/O Limit Address are FFFh. For 16-bit I/O addressing, the PEX 8524 decodes Address bits [31:16] and assumes Address bits [31:16] of the I/O Limit Address are 0000h. For 32-bit addressing, the PEX 8524 decodes Address bits [31:0], and uses the *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits*. If the I/O Limit Address is less than the I/O Base Address, the PEX 8524 does not forward I/O transactions from the corresponding port primary/upstream bus to its secondary/downstream bus. However, the PEX 8524 forwards all I/O transactions from the secondary bus of the corresponding port to its primary bus.	RW	Yes	0h

Register 11-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Secondary Status			
20:16	***Reserved***			0-0h
21	**66 MHz Capable** ***Not supported*** 0 = Not enabled, as PCI Express does ***not support*** 66 MHz	RO	No	0
22	***Reserved***			0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** 0 = Not enabled, as PCI Express does ***not support*** this function	RO	No	0
24	**Master Data Parity Error** If the *Parity Error Response Enable* bit value is 1, the corresponding PEX 8524 port sets this bit to 1 when it transmits or receives a TLP on its downstream side, and when either of the following two conditions occur: • Port receives Completion marked poisoned • Port forwards poisoned TLP write request If the *Parity Error Response Enable* bit = 0, the PEX 8524 never sets this bit.	RW1C	Yes	0
26:25	**DEVSEL Timing** Cleared to 00b, as required by the *PCI Express Base r1.0a.*	RO	No	00b
29:27	***Reserved***			000b
30	**Received System Error** Set to 1 when a port receives an ERR_FATAL or ERR_NONFATAL message on its secondary interface.	RW1C	Yes	0
31	**Detected Parity Error** Set to 1 by the secondary side of a Type 1 Configuration Space Header device when the device receives a poisoned TLP, regardless of the *Parity Error Response Enable* bit state.	RW1C	Yes	0

Register 11-9. 20h Memory Base and Limit Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Memory Base Address				
3:0	***Reserved***			0h
15:4	**Memory Base Address[31:20]** Specifies the corresponding PEX 8524 port Memory Base Address[31:20]. The PEX 8524 assumes Memory Base Address[19:0]=00000h.	RW	Yes	FFFh
Memory Limit Address				
19:16	***Reserved***			0h
31:20	**Memory Limit Address[31:20]** Specifies the corresponding PEX 8524 port Non-Prefetchable Memory Limit Address[31:20]. The PEX 8524 assumes Memory Limit Address[19:0]=FFFFFh.	RW	Yes	000h

Note: *The PEX 8524 port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Memory Base Address*** *and* ***Memory Limit Address*** *registers (when the Base is less than or equal to the Limit).*

Conversely, the PEX 8524 port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range [provided the address is not within the range defined by the ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16])] registers.*

Register 11-10. 24h Prefetchable Memory Base and Limit Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Prefetchable Memory Base Address				
3:0	**Prefetchable Memory Base Capability** 1h = Corresponding PEX 8524 port defaults to 64-bit Prefetchable Memory Addressing support ***Note:*** *If the application needs 32-bit only Prefetchable space, the serial EEPROM must not equal the value of this field and bits [19:16] (***Prefetchable Memory Limit Address*** register Prefetchable Memory Limit Capability field).*	RO	Yes	1h
15:4	**Prefetchable Memory Base Address[31:20]** Specifies the corresponding PEX 8524 port Prefetchable Memory Base Address[31:20]. The PEX 8524 assumes Prefetchable Memory Base Address[19:0]=00000h.	RW	Yes	FFFh
Prefetchable Memory Limit Address				
19:16	**Prefetchable Memory Limit Capability** 1h = Corresponding PEX 8524 port defaults to 64-bit Prefetchable Memory Addressing support	RO	Yes	1h
31:20	**Prefetchable Memory Limit Address[31:20]** Specifies the corresponding PEX 8524 port Prefetchable Memory Base Address[31:20]. The PEX 8524 assumes Prefetchable Memory Base Address[19:0]=FFFFFh.	RW	Yes	000h

Note: *The PEX 8524 port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16]) registers (when the Base is less than or equal to the Limit).*

Conversely, the PEX 8524 port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range [provided the address is not within the range defined by the ***Memory Base Address*** *and* ***Memory Limit Address*** *registers (offset 20h).*

Register 11-11. 28h Prefetchable Memory Upper Base Address[63:32] (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base Address[63:32]** **Silicon Revision AA** The PEX 8524 uses this register for Prefetchable Memory Upper Base Address[63:32].	RW	Yes	FFFF_FFFFh
	Silicon Revisions BB/BC The PEX 8524 uses this register for Prefetchable Memory Upper Base Address[63:32].	RW	Yes	0000_0000h

Register 11-12. 2Ch Prefetchable Memory Upper Limit Address[63:32] (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit Address[63:32]** The PEX 8524 uses this register for Prefetchable Memory Upper Limit Address[63:32].	RW	Yes	0000_0000h

Register 11-13. 30h I/O Base Address[31:16] and I/O Limit Address[31:16] (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/O Base Upper 16 Bits** The PEX 8524 uses this register for I/O Base Address[31:16].	RW	Yes	FFFFh
31:16	**I/O Limit Upper 16 Bits** The PEX 8524 uses this register for I/O Limit Address[31:16].	RW	Yes	0000h

Register 11-14. 34h Capabilities Pointer (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Capability Pointer** Default 40h points to the **Power Management Capability** register.	RO	Yes	40h
31:8	***Reserved***			0000_00h

Register 11-15. 38h Expansion ROM Base Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Expansion ROM Base Address** ***Not supported*** Cleared to 0000_0000h.	RO	No	0000_0000h

Register 11-16. 3Ch Bridge Control and Interrupt Signal (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Interrupt Line** The PEX 8524 does ***not*** use this register, but provides it for operating system and device driver use.	RW	Yes	00h
15:8	**Interrupt Pin** Identifies the Conventional PCI interrupt message(s) that the device (or device function) uses. When values = 01h, 02h, 03h, and 04h, maps to Conventional PCI interrupt messages for INTA#, INTB#, INTC#, and INTD#, respectively. When 00h, indicates that the device does not use Conventional PCI interrupt message(s). Only values 00h or 01h are allowed in the PEX 8524.	RO	Yes	01h

Register 11-16. 3Ch Bridge Control and Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Bridge Control			
16	**Parity Error Response Enable** Controls the response to Poisoned TLPs. 1 = Enables the secondary *Master Data Parity Error* bit	RW	Yes	0
17	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When set to 1, and the **Command** register *SERR# Enable* bit value is 1, enables the *Signaled System Error* bit.	RW	Yes	0
18	**ISA Enable** **Silicon Revision AA** ***Not supported*** Cleared to 0.		No	0
	Silicon Revisions BB/BC Modifies the PEX 8524's response to ISA I/O addresses enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. 1 = PEX 8524 blocks forwarding from the primary to secondary interface, of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	Yes	0
19	**VGA Enable** **Silicon Revision AA** ***Not supported*** Cleared to 0.		No	0
	Silicon Revisions BB/BC Modifies the PEX 8524's response to VGA-compatible addresses. When set, the bridge on the switch's appropriate port positively decodes and forwards the following accesses on the primary to secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A_0000h to 000B_FFFFh • I/O address in the first 64 KB of the I/O Address space [Address[31:16] for PCI Express are zero (0000h)] and where Address[9:0] is within the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) When the *VGA Enable* bit is set, VGA address forwarding is independent of the *ISA Enable* bit value, and the I/O Address range and Memory Address ranges defined by the **I/O Base** and **I/O Limit**, **Memory Base Address** and **Memory Limit Address**, and **Prefetchable Memory Base Address** and **Prefetchable Memory Limit Address** registers. VGA address forwarding is qualified by the **Command** register *I/O Access Enable* and *Memory Access Enable* bits. 0 = Does not forward VGA-compatible Memory and I/O addresses from the primary to secondary interface (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forwards VGA-compatible Memory and I/O addresses (addresses defined above) from the primary to secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	Yes	0

Register 11-16. 3Ch Bridge Control and Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
20	**VGA 16-Bit Decode** **Silicon Revision AA** ***Not supported*** Cleared to 0.	RW	No	0
	Silicon Revisions BB/BC Enables the PEX 8524 to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 19 (*VGA Enable*) of this register is also set to 1, enabling VGA I/O decoding and bridge forwarding. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the primary to secondary interface, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
21	**Master Abort Mode** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
22	**Secondary Bus Reset** 1 = Causes a Hot Reset on the corresponding PEX 8524 port secondary/ downstream PCI Bus	RW	Yes	0
23	**Fast Back-to-Back Transactions Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
24	**Primary Discard Timer** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
25	**Secondary Discard Timer** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
26	**Discard Timer Status** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
27	**Discard Timer SERR# Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
31:28	***Reserved***			0h

11.7 Power Management Capability Registers

This section details the PEX 8524 Power Management Capability registers. The register map is defined in Table 11-5.

Table 11-5. Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
Data	Power Management Control/ Status Bridge Extensions	Power Management Status and Control		44h

Register 11-17. 40h Power Management Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Capability ID** Set to 01h, indicating that the data structure currently being pointed to is the PCI Power Management data structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **Message Signaled Interrupt Capability** register.	RO	Yes	48h
18:16	**Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1.*	RO	Yes	010b
19	**PME Clock** Cleared to 0, as required by the *PCI Express Base r1.0a.*	RO	No	0
20	***Reserved***			0
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** ***Not supported*** Default 000b indicates that the PEX 8524 does ***not support*** Auxiliary Current requirements.	RO	Yes	000b
25	**D1 Support** ***Not supported*** Default 0 indicates that the PEX 8524 does ***not support*** the D1 power state.	RO	No	0
26	**D2 Support** ***Not supported*** Default 0 indicates that the PEX 8524 does ***not support*** the D2 power state.	RO	No	0
31:27	**PME Support** Default 11001b indicates that the corresponding PEX 8524 port forwards PME messages in the D0, D3hot, and D3cold power states.	RO	Yes	11001b

Register 11-18. 44h Power Management Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
	Power Management Status and Control			
1:0	**Power State** This field is used to determine the current power state of the port, and to set the port into a new power state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
7:2	***Reserved***	RO	No	0h
8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8524 port[a] 1 = Enables PME generation by the corresponding PEX 8524 port	RWS	No	0
12:9	**Data Select** RW by Serial EEPROM mode only[b]. Bits [12:9] select the **Data** and **Data Scale** registers. 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	RO	Yes	0h
	RO for hardware auto-configuration. ***Not supported***	RO	No	0h
14:13	**Data Scale** RW by Serial EEPROM mode only[b]. There are four internal **Data Scale** registers per port. Bits [12:9], *Data Select*, select the **Data Scale** register.	RO	Yes	00b
15	**PME Status** 0 = PME is not generated by the corresponding PEX 8524 port[a] 1 = PME is being generated by the corresponding PEX 8524 port	RW1C	No	0

Register 11-18. 44h Power Management Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
Power Management Control/Status Bridge Extensions				
21:16	***Reserved***			0-0h
22	**B2/B3 Support** Cleared to 0, as required by the *PCI Power Mgmt. r1.1*.	RO	No	0
23	**Bus Power/Clock Control Enable** Cleared to 0, as required by the *PCI Power Mgmt. r1.1*.	RO	No	0
Power Management Data				
31:24	**Data** RW by Serial EEPROM mode only[b]. There are four internal **Data** registers per port. Bits [12:9], *Data Select*, select the **Data** register.	RO	Yes	00h

a. Because the PEX 8524 does not support auxiliary power, this bit is not sticky, and is always cleared to 0 at power-on reset.

*b. With no serial EEPROM, reads return 00h for the **Data Scale** and **Data** registers (for all Data Selects).*

11.8 Message Signaled Interrupt Capability Registers

This section details the PEX 8524 Message Signaled Interrupt (MSI) Capability registers. The register map is defined in Table 11-6.

Table 11-6. Message Signaled Interrupt Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	Message Control	Next Capability Pointer (68h)	Capability ID (05h)	48h
Message Address[31:0]				4Ch
Message Upper Address[63:32]				50h
Reserved		Message Data		54h
Reserved				58h – 64h

Register 11-19. 48h Message Signaled Interrupt Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
MSI Capability Header				
7:0	**Capability ID** Set to 05h, as required by the *PCI r2.3*.	RO	Yes	05h
15:8	**Next Capability Pointer** Set to 68h to point to the PEX 8524 PCI Express Capability registers.	RO	Yes	68h
Message Control				
16	**MSI Enable** 0 = Message Signaled Interrupts for the corresponding port are disabled 1 = Message Signaled Interrupts for the corresponding port are enabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = PEX 8524 port is requesting one message – the only value supported	RO	Yes	000b
22:20	**Multiple Message Enable** 000b = PEX 8524 port contains only one allocated message – the only value supported	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 1 = PEX 8524 is capable of generating 64-bit Message Signaled Interrupt addresses	RO	Yes	1
31:24	***Reserved***			00h

Register 11-20. 4Ch Message Address[31:0] (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	***Reserved***			00b
31:2	**Message Address[31:2]** MSI Write transaction lower address[31:2]. ***Note:*** *Refer to register offset 50h for Message Upper Address[63:32].*	RW	Yes	0000_0000h

Register 11-21. 50h Message Upper Address[63:32] (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Message Address[63:32]** MSI Write transaction upper address[63:32]. ***Note:*** *Refer to register offset 4Ch for Message Address[31:0].*	RW	Yes	0000_0000h

Register 11-22. 54h Message Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Message Data** MSI Write transaction TLP payload.	RW	Yes	0000h
31:16	***Reserved***			0000h

11.9 PCI Express Capability Registers

This section details the PEX 8524 PCI Express Capability registers. Hot Plug Capability, Command, Status, and Events are included in these registers. The register map is defined in Table 11-7.

Table 11-7. PCI Express Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capabilities		Next Capability Pointer (00h)	Capability ID (10h)	68h
Device Capabilities				6Ch
Device Status		Device Control		70h
Link Capabilities				74h
Link Status		Link Control		78h
Slot Capabilities				7Ch
Slot Status		Slot Control		80h
Reserved				84h – 8Ch

Register 11-23. 68h PCI Express Capability List and Capabilities (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
PCI Express Capability List					
7:0	**Capability ID** Set to 10h, as required by the *PCI Express Base r1.0a.*		RO	Yes	10h
15:8	**Next Capability Pointer** 00h = PCI Express Capability is the last capability in the PEX 8524 port Capabilities list The PEX 8524 port Extended Capabilities list starts at 100h.		RO	Yes	00h
PCI Express Capabilities					
19:16	**Capability Version** The PEX 8524 ports sets this field to 1h, as required by the *PCI Express Base r1.0a.*		RO	Yes	1h
23:20	**Device/Port Type** Set at reset, as required by the *PCI Express Base r1.0a.*	Upstream	RO	Yes	5h
		Downstream	RO	Yes	6h
24	**Slot Implemented** 0 = Disables or connects to an upstream port	Upstream	RO	No	0
	0 = Disables or connects to an integrated component[a] 1 = Indicates that the downstream port connects to a slot, as opposed to being connected to an integrated component or being disabled	Downstream	RO	Yes	1
29:25	**Interrupt Message Number** The serial EEPROM writes 0000_0b, because the Base message and MSI messages are the same.		RO	Yes	0000_0b
31:30	***Reserved***				00b

a. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0h, indicating that the corresponding PEX 8524 downstream port connects to an integrated component or is disabled.

Register 11-24. 6Ch Device Capabilities (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
2:0	**Maximum Payload Size Supported** 000b = PEX 8524 ports support 128-byte maximum payload 001b = PEX 8524 ports support 256-byte maximum payload No other values are supported. ***Note:*** *Serial EEPROM must not load greater than 256 bytes Maximum Payload Size.*		RO	Yes	001b
4:3	**Phantom Functions Supported** ***Not supported*** Cleared to 00b.		RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum Tag field is 5 bits 1 = Maximum Tag field is 8 bits		RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** ***Not supported*** Because the PEX 8524 is a switch and not an endpoint, it does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency** ***Not supported*** Because the PEX 8524 is a switch and not an endpoint, it does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b

Register 11-24. 6Ch Device Capabilities (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
12	**Attention Button Present** For the PEX 8524 upstream port, value of 1 indicates that an Attention Button is implemented on that adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Button is ***not*** present on an adapter board for which the PEX 8524 provides the system interface.	Upstream	HwInit	Yes	1
	Not valid for downstream ports.	Downstream	RO	No	0
13	**Attention Indicator Present** For the PEX 8524 upstream port, value of 1 indicates that an Attention Indicator is implemented on the adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Indicator is ***not*** present on an adapter board for which the PEX 8524 provides the system interface.	Upstream	HwInit	Yes	1
	Not valid for downstream ports.	Downstream	RO	No	0
14	**Power Indicator Present** For the PEX 8524 upstream port, value of 1 indicates that a Power Indicator is implemented on the adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that a Power Indicator is ***not*** present on an adapter board for which the PEX 8524 provides the system interface.	Upstream	HwInit	Yes	1
	Not valid for downstream ports.	Downstream	RO	No	0
17:15	***Reserved***				000b
25:18	**Captured Slot Power Limit Value** For the PEX 8524 upstream port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Scale* field.	Upstream	RO	Yes	00h
	Not valid for downstream ports.	Downstream	RO	No	0
27:26	**Captured Slot Power Limit Scale** For the PEX 8524 upstream port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Value* field. 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	Upstream	RO	Yes	00b
	Not valid for downstream ports.	Downstream	RO	No	0
31:28	***Reserved***				0h

Register 11-25. 70h Device Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables corresponding PEX 8524 port to report Correctable errors	RW	Yes	0
1	**Non-Fatal Error Enable** 0 = Disables 1 = Enables corresponding PEX 8524 port to report Non-Fatal errors	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables corresponding PEX 8524 port to report Fatal errors	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables corresponding PEX 8524 port to report Unsupported Request errors	RW	Yes	0
4	**PCI Express Relaxed Ordering Enable** ***Not supported*** Cleared to 0.	RO	No	0
7:5	**Maximum Payload Size** Software can change this field to configure the PEX 8524 ports to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capabilities** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]). 000b = Indicates that initially the PEX 8524 port is configured to support a Maximum Payload Size of 128 bytes 001b = Indicates that initially the PEX 8524 port is configured to support a Maximum Payload Size of 256 bytes No other values are supported.	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported*** Cleared to 0.	RO	No	0
9	**Phantom Functions Enable** ***Not supported*** Cleared to 0.	RO	No	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported*** Cleared to 0.	RO	No	0
11	**No Snoop Enable** ***Not supported*** Cleared to 0.	RO	No	0
14:12	**Maximum Read Request Size** ***Not supported*** Cleared to 000b.	RO	No	000b
15	***Reserved***			0

Register 11-25. 70h Device Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Device Status			
16	**Correctable Error Detected** 1 = Corresponding PEX 8524 port detected a Correctable error Set when the corresponding port detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable* bit) state.	RW1C	Yes	0
17	**Non-Fatal Error Detected** 1 = Corresponding PEX 8524 port detected a Non-Fatal error Set when the corresponding port detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Enable* bit) state.	RW1C	Yes	0
18	**Fatal Error Detected** 1 = Corresponding PEX 8524 port detected a Fatal error Set when the corresponding port detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable* bit) state.	RW1C	Yes	0
19	**Unsupported Request Detected** 1 = Corresponding PEX 8524 port detected an Unsupported Request Set when the corresponding port detects an Unsupported Request, regardless of the bit 3 (*Unsupported Request Reporting Enable* bit) state.	RW1C	Yes	0
20	**Auxiliary (AUX) Power Detected** ***Not supported*** Cleared to 0.	RO	No	0
21	**Transactions Pending** ***Not supported*** Cleared to 0.	RO	No	0
31:22	***Reserved***			000h

Register 11-26. 74h Link Capabilities (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Maximum Link Speed** Set to 0001b, as required by the *PCI Express Base r1.0a.*	RO	Yes	0001b
9:4	**Maximum Link Width** Actual link width is set by signal ball strapping options. The PEX 8524 Maximum Link Width is x8 = 00_1000b (Station 0), or x16 = 01_0000b (Station 1).	RO	No	Strap levels
11:10	**Active State Power Management (ASPM) Support** Indicates the level of ASPM supported by the port. 01b = L0s link power state entry is supported 10b = L0s and L1 link power states are supported All other values are ***reserved***.	RO	Yes	11b
14:12	**L0s Exit Latency** 101b = Corresponding PEX 8524 port L0s Exit Latency is between 1 and 2 µs	RO	No	101b
17:15	**L1 Exit Latency** 101b = Corresponding PEX 8524 port L1 Exit Latency is between 16 and 32 µs	RO	Yes	101b
23:18	***Reserved***			0-0h
31:24	**Port Number** The Port Number is set by signal ball strapping options: STRAP_STN0_PORTCFG[4:0] – Ports 0, 1 STRAP_STN1_PORTCFG[3:0] – Ports 8, 9, 10, 11	HwInit	No	Set by strap levels

Register 11-27. 78h Link Status and Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
	Link Control				
1:0	**Active State Power Management (ASPM) Control** 00b = Disables L0s and L1 Entries for the corresponding PEX 8524 port[a] 01b = Enables only L0s Entry 10b = Enables only L1 Entry 11b = Enables both L0s and L1 Entries		RW	Yes	00b
2	***Reserved***				0
3	**Read Completion Boundary (RCB)** Cleared to 0, as required by the *PCI Express Base r1.0a.*		RO	Yes	0
4	**Link Disable** Not valid for the upstream port.	Upstream	RO	No	0
	Setting to 1 places the link on the corresponding PEX 8524 downstream port to the Disabled Link Training state.	Downstream	RW	Yes	0
5	**Retrain Link** Not valid for the upstream port.	Upstream	RO	No	0
	For PEX 8524 ports, when read, always returns 0. Writing 1 to this bit causes the corresponding PEX 8524 downstream port to initiate retraining of its PCI Express link.	Downstream	RW	Yes	0
6	**Common Clock Configuration** 0 = Corresponding PEX 8524 port and the device at the other end of the corresponding port's PCI Express link are operating with an **asynchronous** reference clock 1 = Corresponding PEX 8524 port and the device at the other end of the corresponding port's PCI Express link are operating with a **distributed** common reference clock		RW	Yes	0
7	**Extended Sync** Set to 1 causes the corresponding PEX 8524 port to transmit: • 4,096 FTS Ordered-Sets in the L0s state, • Followed by a single SKIP Ordered-Set prior to entering the L0 state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the Recovery state.		RW	Yes	0
15:8	***Reserved***				00h

Register 11-27. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
Link Status					
19:16	**Link Speed** Set to 1h, as required by the *PCI Express Base r1.0a* for a 2.5 Gbps PCI Express link.		RO	Yes	1h
25:20	**Negotiated Link Width** Link width is determined by negotiated value with attached port/lane: 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 (Station 1 only) All other values are ***not supported***. The value in this field is undefined when the link is not up.		RO	Yes	00_0001b
26	**Training Error** Not valid for the upstream port.	Upstream	RO	No	0
	When set to 1, indicates that the corresponding PEX 8524 port detected a Link Training error.	Downstream	RO	Yes	0
27	**Link Training** Not valid for the upstream port.	Upstream	RO	No	0
	When set to 1, indicates that the corresponding PEX 8524 downstream port requested link training and either the link training is in process or about to start.	Downstream	RO	No	0
28	**Slot Clock Configuration** 0 = Indicates PEX 8524 uses an independent clock 1 = Indicates PEX 8524 uses the same physical reference clock that the platform provides on the connector		HwInit	Yes	0
31:29	***Reserved***				000b

a. The port receiver must be capable of entering L0s state, regardless of whether the state is disabled.

Note: *Register offset 7Ch is used only for downstream ports.*

Register 11-28. 7Ch Slot Capabilities (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
0	**Attention Button Present** Not valid for the upstream port.	Upstream			0
	0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8524 downstream port	Downstream	HwInit	Yes	1
1	**Power Controller Present** Not valid for the upstream port.	Upstream			0
	0 = Power Controller is not implemented 1 = Power Controller is implemented for the slot of the corresponding PEX 8524 downstream port	Downstream	HwInit	Yes	1
2	**MRL Sensor Present** Not valid for the upstream port.	Upstream			0
	0 = MRL Sensor is not implemented 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8524 downstream port	Downstream	HwInit	Yes	1
3	**Attention Indicator Present** Not valid for the upstream port.	Upstream			0
	0 = Attention Indicator is not implemented 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8524 downstream port	Downstream	HwInit	Yes	1

Register 11-28. 7Ch Slot Capabilities (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
4	**Power Indicator Present** Not valid for the upstream port.	Upstream			0
	0 = Power Indicator is not implemented 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8524 downstream port	Downstream	HwInit	Yes	1
5	**Hot Plug Surprise** Not valid for the upstream port.	Upstream			0
	0 = No device in the corresponding PEX 8524 downstream port slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8524 downstream port slot can be removed from the system without prior notification	Downstream	HwInit	Yes	0
6	**Hot Plug Capable** Not valid for the upstream port.	Upstream			0
	0 = Corresponding PEX 8524 downstream port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8524 downstream port slot is capable of supporting Hot Plug operations	Downstream	HwInit	Yes	1
14:7	**Slot Power Limit Value** Do not change for upstream port.	Upstream			00h
	The maximum power available from the corresponding PEX 8524 downstream port is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the value specified by the *Slot Power Limit Scale* field.	Downstream	HwInit	Yes	19h
16:15	**Slot Power Limit Scale** Not valid for the upstream port.	Upstream			00b
	The maximum power available from the corresponding PEX 8524 downstream port is determined by multiplying the value in this field by the *Slot Power Limit Value* field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Downstream	HwInit	Yes	00b
18:17	***Reserved***				00b
31:19	**Physical Slot Number** Not valid for the upstream port.	Upstream			0-0h
	Specifies a non-zero identification number for the corresponding PEX 8524 downstream port slot.	Downstream	HwInit	Yes	0-0h

Notes: *Register offset 80h is used only for downstream ports.*

If the Power Indicator Present and/or Attention Indicator Present bits (offset 7Ch[4:3]) are set, writes to the ***Slot Control*** *register (offset 80h[15:0]) cause the downstream port to send the appropriate Power_Indicator_* and Attention_Indicator_* messages (On/Blink/Off) to the downstream device, unless the Power Indicator Control and Attention Indicator Control field (offset 80h[9:8 and 7:6], respectively) values that are written are the* ***reserved*** *value 00b. Writing 00b to each of these fields is ignored (the stored value is not changed and the Hot Plug message is not sent). Therefore, when writing to this register, the value written to both fields should be 00b unless the purpose of the Write command is to change the state of the port's HP_ATNLEDx# or HP_PWRLEDx# Output signals, in which case Byte Writes can be used to target only one of the two Control fields.*

Register 11-29. 80h Slot Status and Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
Slot Control					
0	**Attention Button Pressed Enable** Not valid for the upstream port.	Upstream	RO	No	0
	0 = Function is disabled 1 = Enables software notification with a Hot Plug interrupt if the port is in the D0 Power State (**Power Management Status and Control** register Power State field, offset 44h[1:0]=00b), or with a PME message if the port is in the D3hot state (offset 44h[1:0]=11b), for an Attention Button Pressed event on the corresponding PEX 8524 downstream port.	Downstream	RW	Yes	0
1	**Power Fault Detector Enable** Not valid for the upstream port.	Upstream	RO	No	0
	0 = Function is disabled 1 = Enables software notification with a Hot Plug interrupt if the port is in the D0 Power State (**Power Management Status and Control** register *Power State* field, offset 44h[1:0]=00b), or with a PME message if the port is in the D3hot state (offset 44h[1:0]=11b), for a Power Fault event on the corresponding PEX 8524 downstream port.	Downstream	RW	Yes	0

Register 11-29. 80h Slot Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
2	**MRL Sensor Changed Enable** Not valid for the upstream port.	Upstream	RO	No	0
	0 = Function is disabled 1 = Enables software notification with a Hot Plug interrupt if the port is in the D0 Power State (**Power Management Status and Control** register *Power State* field, offset 44h[1:0]=00b), or with a PME message if the port is in the D3hot state (offset 44h[1:0]=11b), for an MRL Sensor Changed event on the corresponding PEX 8524 downstream port.	Downstream	RW	Yes	0
3	**Presence Detect Changed Enable** Not valid for the upstream port.	Upstream	RO	No	0
	0 = Function is disabled 1 = Enables software notification with a Hot Plug interrupt if the port is in the D0 Power State (**Power Management Status and Control** register *Power State* field, offset 44h[1:0]=00b), or with a PME message if the port is in the D3hot state (offset 44h[1:0]=11b), for a Presence Detect Changed event on the corresponding PEX 8524 downstream port. A Presence Detect Changed event is triggered from one of two sources, depending on the state of the *HPC Inband Presence Detect Enable* bit (1E0h[5]): • If the *HPC Inband Presence Detect Enable* bit is cleared (offset 1E0h[5]=0, default), Presence Detect is input from the HP_PRSNT*x*# signal on the corresponding PEX 8524 downstream port • If the *HPC Inband Presence Detect Enable* bit is set (offset 1E0h[5]=1), Presence Detect is input from the SerDes Receiver Detect on the corresponding PEX 8524 downstream port	Downstream	RW	Yes	0

Register 11-29. 80h Slot Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
4	**Command Completed Interrupt Enable** Not valid for the upstream port.	Upstream	RO	No	0
	0 = Function is disabled 1 = Enables software notification with a Hot Plug interrupt when a command is completed by the Hot Plug Controller on the corresponding PEX 8524 downstream port	Downstream	RW	Yes	0
5	**Hot Plug Interrupt Enable** Not valid for the upstream port.	Upstream	RO	No	0
	0 = Function is disabled 1 = Enables a Hot Plug Interrupt on enabled Hot Plug events for the corresponding PEX 8524 downstream port	Downstream	RW	Yes	0
7:6	**Attention Indicator Control** Do not change for upstream port.	Upstream	RO	No	00b
	Control the Attention Indicator on the corresponding PEX 8524 downstream port slot. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator Software must use a Byte or Word Write (and not a DWord Write) to control the HP_ATNLED*x*# Output signal. Reads return the corresponding PEX 8524 downstream port Attention Indicator's current state.	Downstream	RW	Yes	11b

Register 11-29. 80h Slot Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
9:8	**Power Indicator Control** Do not change for upstream port.	Upstream	RO	No	00b
	Controls the Power Indicator on the corresponding PEX 8524 downstream port slot. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator Software must use a Byte or Word Write (and not a DWord Write) to control the HP_PWRLED*x*# Output signal. Reads return the corresponding PEX 8524 downstream port Power Indicator's current state.	Downstream	RW	Yes	11b (MRL open) 01b (MRL closed)
10	**Power Controller Control** Not valid for the upstream port.	Upstream	RO	No	0
	Controls the Power Controller on the corresponding PEX 8524 downstream port slot. 0 = Turns On Power Controller; requires some delay to be effective 1 = Turns Off Power Controller Software must use a Byte or Word Write (and not a DWord Write) to control the Power Controller Output signals. ***Note:*** *Value of 0 requires some delay to be effective.*	Downstream	RW	Yes	1 (MRL open) 0 (MRL closed)
15:11	***Reserved***				0-0h

Register 11-29. 80h Slot Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
Slot Status					
16	**Attention Button Pressed** Not valid for the upstream port.	Upstream	RO	No	0
	Set to 1 when the Attention Button of the corresponding PEX 8524 downstream port slot is pressed.	Downstream	RW1C	Yes	0
17	**Power Fault Detected** Not valid for the upstream port.	Upstream	RO	No	0
	Set to 1 when the Power Controller of the corresponding PEX 8524 downstream port slot detects a Power Fault at the slot.	Downstream	RW1C	Yes	0
18	**MRL Sensor Changed** Not valid for the upstream port.	Upstream	RO	No	0
	Set to 1 when an MRL state change is detected on the corresponding PEX 8524 downstream port slot.	Downstream	RW1C	Yes	0
19	**Presence Detect Changed** Not valid for the upstream port.	Upstream	RO	No	0
	Set to 1 when a Presence Detect Change is detected on the corresponding PEX 8524 downstream port slot. A Presence Detect Changed event is triggered from one of two sources, depending on the state of the *HPC Inband Presence Detect Enable* bit (1E0h[5]): • If the *HPC Inband Presence Detect Enable* bit is cleared (offset 1E0h[5]=0, default), Presence Detect is input from the HP_PRSNT*x*# signal on the corresponding PEX 8524 downstream port • If the *HPC Inband Presence Detect Enable* bit is set (offset 1E0h[5]=1), Presence Detect is input from the SerDes Receiver Detect on the corresponding PEX 8524 downstream port	Downstream	RW1C	Yes	0

Register 11-29. 80h Slot Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
20	**Command Completed** Do not change for upstream port.	Upstream	RO	No	0
	Set to 1 when the Hot Plug Controller on the corresponding PEX 8524 downstream port slot completes an issued command.	Downstream	RW1C	Yes	0
21	**MRL Sensor State** Do not change for upstream port.	Upstream	RO	No	0
	Reveals the corresponding PEX 8524 downstream port MRL sensor's current state. 0 = MRL sensor closed 1 = MRL sensor open	Downstream	RO	Yes	0
22	**Presence Detect State** Do not use for upstream port.	Upstream	RO	No	0
	Reveals the corresponding PEX 8524 downstream port's current Presence state. Presence is determined from one of two sources, depending on the state of the *HPC Inband Presence Detect Enable* bit (1E0h[5]): • If the *HPC Inband Presence Detect Enable* bit is cleared (offset 1E0h[5]=0, default), Presence Detect is input from the HP_PRSNT*x*# signal on the corresponding PEX 8524 downstream port • If the *HPC Inband Presence Detect Enable* bit is set (offset 1E0h[5]=1), Presence Detect is input from the SerDes Receiver Detect on the corresponding PEX 8524 downstream port 0 = Slot is empty, or device is not present 1 = Slot is occupied, or device is present	Downstream	RO	Yes	0
31:23	***Reserved***				0-0h

11.10 Device Serial Number Extended Capability Registers

This section details the PEX 8524 Device Serial Number Extended Capability registers. The register map is defined in Table 11-8.

Table 11-8. PEX 8524 Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h)	Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Higher DW)		108h

Register 11-30. 100h Device Serial Number Extended Capability

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Extended Capability ID** Set to 0003h, as required by the *PCI Express Base r1.0a.*	RO	Yes	0003h
19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base r1.0a.*	RO	Yes	1h
31:20	**Next Capability Offset** Set to FB4h, which is the **PCI Express Enhanced Capability Header** registers.	RO	Yes	FB4h

Register 11-31. 104h Serial Number (Lower DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Serial Number[31:0]** Lower half of a 64-bit register. Value set by Serial EEPROM register initialization.	RO	Yes	0000_0EDFh

Register 11-32. 108h Serial Number (Higher DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Serial Number[63:32]** Upper half of a 64-bit register. Value set by Serial EEPROM register initialization.	RO	Yes	0000_0001h

11.11 Power Budgeting Extended Capability Registers

This section details the PEX 8524 Power Budgeting Extended Capability registers. The register map is defined in Table 11-9.

Table 11-9. PEX 8524 Power Budgeting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h) / Capability Version (1h)	Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budgeting Data		140h
Reserved	Power Budget Capability	144h

Register 11-33. 138h Power Budgeting Extended Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Extended Capability ID** Set to 0004h, as required by the *PCI Express Base r1.0a.*	RO	Yes	0004h
19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base r1.0a.*	RO	Yes	1h
31:20	**Next Capability Offset** Set to 148h, which addresses the PEX 8524 **Virtual Channel Extended Capability** registers.	RO	Yes	148h

Register 11-34. 13Ch Data Select (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Data Select** Indexes the Power Budgeting Data reported by way of eight **Power Budgeting Data** registers per port and selects the DWord of Power Budgeting Data that appears in each **Power Budgeting Data** register. Index values start at 0, to select the first DWord of Power Budgeting Data; subsequent DWords of Power Budgeting Data are selected by increasing index values 1 to 7.	RW	Yes	00h
31:8	***Reserved***			0-0h

Register 11-35. 140h Power Budgeting Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Base Power** Eight registers/port. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the *Data Scale* to produce the actual power consumption value.	RO	Yes	00h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The power consumption of the device is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	Yes	00b
12:10	**PM Sub-State** 000b = Corresponding PEX 8524 port is in the default Power Management sub-state	RO	Yes	000b
14:13	**PM State** Current power state. 00b = D0 state 01b = ***Not used – D1 state not supported*** 10b = ***Not used – D2 state not supported*** 11b = D3 state	RO	Yes	00b
17:15	**Type** Type of operating condition. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other values are ***reserved***.	RO	Yes	000b
20:18	**Power Rail** Power Rail of operating condition. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other values are ***reserved***.	RO	Yes	000b
31:21	***Reserved***			0-0h

Note: *There are eight registers per port that can be programmed, through the serial EEPROM. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (offset 13Ch[7:0]).*

Register 11-36. 144h Power Budget Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**System Allocated** 1 = Power budget for the device is included within the system power budget	HwInit	Yes	1
31:1	***Reserved***			0-0h

11.12 Virtual Channel Extended Capability Registers

This section details the PEX 8524 Virtual Channel Extended Capability registers. These registers are duplicated for each port. The register map for one port is defined in Table 11-10.

Table 11-10. PEX 8524 Virtual Channel Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (000h) / Capability Version (1h)	Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
VC1 Resource Capability		164h
VC1 Resource Control		168h
VC1 Resource Status	***Reserved***	16Ch
Reserved		170h – 1B4h
Virtual Channel Arbitration Table		1B8h … 1C4h

Register 11-37. 148h Virtual Channel Extended Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Extended Capability ID** Set to 0002h, as required by the *PCI Express Base r1.0a*.	RO	Yes	0002h
19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base r1.0a*.	RO	Yes	1h
31:20	**Next Capability Offset** Set to 000h, indicating that the Virtual Channel Extended Capability is the last extended capability in the port Extended Capability list.	RO	Yes	000h

Register 11-38. 14Ch Port VC Capability 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Extended VC Count** 0 = PEX 8524 supports only the default Virtual Channel (VC0) 1 = PEX 8524 ports support **one** extended Virtual Channel (VC1)	RO	Yes	1
3:1	***Reserved***			000b
4	**Low-Priority Extended VC Count** For Strict Priority arbitration, this bit indicates the number of extended Virtual Channels (those in addition to the default Virtual Channel 0) that belong to the Low-Priority Virtual Channel group for this PEX 8524 port. PEX 8524 Serial EEPROM register initialization capability is used to change this field to 1 to also set VC1 to the Low-Priority Virtual Channel group. 0 = For this PEX 8524 port, only the default Virtual Channel 0 belongs to the Low-Priority Virtual Channel group 1 = For this PEX 8524 port, VC0 and VC1 belong to the Low-priority Virtual Channel group	RO	Yes	0
7:5	***Reserved***			000b
9:8	**Reference Clock** ***Not supported*** Cleared to 00b.	RO	No	00b
11:10	**Port Arbitration Table Entry Size** ***Not supported*** Cleared to 00b.	RO	No	00b
31:12	***Reserved***			0-0h

Register 11-39. 150h Port VC Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	**VC Arbitration Capability** Bit 0 value of 1 indicates Round-Robin (Hardware-Fixed) Arbitration scheme is supported. Bit 1 value of 1 indicates Weighted Round-Robin Arbitration with 32 phases is supported.	RO	Yes	11b
23:2	***Reserved***			0-0h
31:24	**VC Arbitration Table Offset** Virtual Channel Arbitration Table zero-based offset in Quad DWords (16 bytes) from the base address of PEX 8524 port Virtual Channel Capability structure.	RO	Yes	07h

Register 11-40. 154h Port VC Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
	Port VC Control			
0	**Load VC Arbitration Table** Writing 1 updates the VC Arbitration table for the corresponding PEX 8524 port. Reading this bit always returns 0.	RW	Yes	0
1	**VC Arbitration Select** Selects the VC arbitration type for the corresponding PEX 8524 port. Indicates the bit number in the **Port VC Capability 2** register *VC Arbitration Capability* field that corresponds to the arbitration type: 0 = bit 0; Round-Robin (Hardware-Fixed) arbitration scheme 1 = bit 1; Weighted Round-Robin with 32 Phases Select only an arbitration type, that corresponds to a bit set in the *VC Arbitration Capability* field. Cannot be modified when more than one LPVC group VC is enabled.	RW	Yes	0
15:2	***Reserved***			0-0h
	Port VC Status			
16	**VC Arbitration Table Status** Set to 1 when there is a Write to the VC Arbitration table. Cleared by the corresponding PEX 8524 port when the port completes loading the values stored in its VC Arbitration table after software sets the *Load VC Arbitration Table* bit.	RO	Yes	0
31:17	***Reserved***			0-0h

Register 11-41. 158h VC0 Resource Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Port Arbitration Capability** 1 = Non-configurable hardware-fixed port arbitration The only configuration supported by the PEX 8524.	RO	Yes	1
13:1	***Reserved***			0-0h
14	**Advanced Packet Switching** ***Not supported*** Cleared to 0.	RO	No	0
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, this bit is cleared to 0.	RO	No	0
22:16	**Maximum Time Slots** ***Not supported*** Cleared to 000_0000b.	RO	No	000_0000b
23	***Reserved***			0-0h
31:24	**Port Arbitration Table Offset** ***Not supported*** Cleared to 00h.	RO	No	00h

Register 11-42. 15Ch VC0 Resource Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC/VC0 Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped into Virtual Channel 0. Traffic Class 0 (TC0) must be mapped to Virtual Channel 0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	Yes	FFh
7:1		RW	Yes	
15:8	***Reserved***			00h
16	**Load Port Arbitration Table** ***Not supported*** Cleared to 0.	RO	No	0
19:17	**Port Arbitration Select** ***Not supported*** Cleared to 000b.	RO	No	000b
23:20	***Reserved***			0-0h
26:24	**VC0 ID** Defines the corresponding PEX 8524 port Virtual Channel 0 ID code. Because this is the default VC0, it is cleared to 000b.	RO	Yes	000b
30:27	***Reserved***			0-0h
31	**VC0 Enable** 0 = Not allowed 1 = Enables corresponding PEX 8524 port default Virtual Channel 0	RO	Yes	1

Register 11-43. 160h VC0 Resource Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	***Reserved***			0000h
16	**Port Arbitration Table Status** ***Not supported*** Cleared to 0.	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation completed 1 = VC0 initialization is not complete for the corresponding PEX 8524 port	RO	Yes	1
31:18	***Reserved***			0-0h

Register 11-44. 164h VC1 Resource Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Port Arbitration Capability** 1 = Non-configurable hardware-fixed port arbitration The only configuration supported by PEX 8524.	RO	Yes	1
13:1	***Reserved***			0-0h
14	**Advanced Packet Switching** ***Not supported*** Cleared to 0.	RO	No	0
15	**Reject Snoop Transactions** Not valid for PEX 8524.	RO	No	0
22:16	**Maximum Time Slots** ***Not supported*** Cleared to 000_0000b.	RO	No	000_0000b
23	***Reserved***			0
31:24	**Port Arbitration Table Offset** ***Not supported*** Cleared to 00h.	RO	No	00h

Register 11-45. 168h VC1 Resource Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC/VC1 Map** Defines Traffic Classes [7:1], respectively, and indicates which TCs are mapped into Virtual Channel 1. Traffic Class 0 must be mapped to Virtual Channel 0. Traffic Classes [7:1] can be mapped to VC1.	RO	No	00h
7:1		RW	Yes	
15:8	***Reserved***			0-0h
16	**Load Port Arbitration Table** ***Not supported*** Cleared to 0.	RO	No	0
19:17	**Port Arbitration Select** ***Not supported*** Cleared to 000b.	RO	No	000b
23:20	***Reserved***			0-0h
26:24	**VC1 ID** Defines the ID code for the corresponding PEX 8524 port Virtual Channel 1 (001b is the only supported value).	RW	Yes	001b
30:27	***Reserved***			0000b
31	**VC1 Enable** 0 = Disables corresponding PEX 8524 port Virtual Channel 1 1 = Enables corresponding PEX 8524 port Virtual Channel 1	RW	Yes	0

Register 11-46. 16Ch VC1 Resource Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	***Reserved***			0000h
16	**Port Arbitration Table Status** ***Not supported*** Cleared to 0.	RO	No	0
17	**VC1 Negotiation Pending** 0 = VC1 negotiation completed 1 = VC1 initialization or disabling is pending for the corresponding PEX 8524 port	RO	Yes	0
31:18	***Reserved***			0-0h

11.12.1 Virtual Channel Arbitration Table

This section details the PEX 8524 Virtual Channel Arbitration registers. The register map is defined in Table 11-11.

Table 11-11. Virtual Channel Arbitration Table Register Map (All Ports)

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	1B8h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	1BCh
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	1C0h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	1C4h

Register 11-47. 1B8h - 1C4h VC Arbitration Table Phase *n* Definition (where *n* = 0 to 31)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**PHASE*n*[0]** VC Arbitration Table phases are used to determine the weighting of the two Virtual Channels during "Weighted Round-Robin with 32 Phases" virtual channel arbitration. This table is used only if Weighted Round-Robin with 32 phases virtual channel arbitration is selected by way of the *VC Arbitration Select* bit. Phases are assigned by setting PHASE*n*[0] of that Phase: 0 = Virtual Channel 0 1 = Virtual Channel 1	RW	Yes	0
3:1	**PHASE*n*[3:1]**	RO	No	000b

11.13 PLX-Specific Registers

PLX-Specific registers are unique to the PEX 8524 device and are not referenced in the *PCI Express Base r1.0a*. Table 11-12 defines the register map.

Note: *This register group is accessed using a Memory-Mapped cycle. It is recommended that these register values* ***not*** *be changed.*

Table 11-12. PLX-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Error Checking and Debug Registers	1C8h … 1FCh
Physical Layer Registers	200h … 2C4h
CAM Routing Registers	2C8h … 344h
Ingress Control Registers	660h … 668h
I/O CAM Base and Limit Upper 16 Bits Registers	680h … 6ACh
Base Address Registers (BARs)	6C0h … 73Ch
Shadow Virtual Channel (VC) Capability Registers	740h … 9ECh
Ingress Credit Handler (INCH) Registers	9F0h … B7Ch
Reserved	B80h – BE4h
Ingress One-Bit ECC Error Count Register	BE8h
Relaxed Completion Ordering (Ingress) Register – Silicon Revisions BB/BC Only	BECh
Relaxed Ordering Mode (Ingress) Register	BF0h … BFCh
Internal Credit Handler (ITCH) VC&T Threshold Registers	C00h … C08h

11.13.1 Error Checking and Debug Registers

Table 11-13. PLX-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
ECC Check Disable				1C8h
Error Handler 32-Bit Error Status ***(Factory Test Only)***				1CCh
Error Handler 32-Bit Error Mask ***(Factory Test Only)***				1D0h
Factory Test Only				1D4h – 1D8h
Debug Control				1DCh
Power Management Hot Plug User Configuration				1E0h
Egress Control and Status				1E4h
Reserved			Bad TLP Count	1E8h
Reserved			Bad DLLP Count	1ECh
PLX-Specific Relaxed Ordering Enable				1F0h
Software-Controlled Lane Status				1F4h
Reserved		ACK Transmission Latency Limit		1F8h
Reserved				1FCh

a. Certain registers are port-specific, some are station-specific, while others are device-specific.

Register 11-48. 1C8h ECC Check Disable (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**ECC 1-Bit Error Check Disable** 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	RW	Yes	0
1	**ECC 2-Bit Error Check Disable** 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	RW	Yes	0
31:2	***Reserved***			0-0h

Note: *All errors in register offset 1CCh generate MSI/INTx interrupts, when enabled.*

Register 11-49. 1CCh Error Handler 32-Bit Error Status (Only Port 0, *Factory Test Only)*

Bit(s)	Description	Bit Exists Only on Port(s)	Type	Serial EEPROM	Default
0	**Completion FIFO Overflow Status** 0 = No overflow detected 1 = Completion FIFO Overflow detected when 4-deep completion FIFO for ingress, or 2-deep completion FIFO for egress, overflows	0, 1, 8, 9, 10, 11	RW1CS	Yes	0
1	**Egress PRAM Soft-Error Overflow** Egress Packet RAM 1-bit Soft Error Counter Overflow. 0 = No error detected 1 = Egress PRAM 1-bit Soft-Error (8-bit counter) overflow; when destination packet RAM 1-bit Soft Error Count is greater than or equal to 256, generates an MSI/INT*x* interrupt, if enabled	0, 8	RW1CS	Yes	0
2	**Egress LLIST Soft-Error Overflow** Egress Link-List RAM 1-bit Soft Error Counter Overflow. 0 = No error detected 1 = Egress Link-List 1-bit Soft-Error (8-bit Counter) overflow; when destination module link lists RAM 1-bit Soft Error Count is greater than or equal to 256, generates an MSI/INT*x* interrupt, if enabled	0, 8	RW1CS	Yes	0
3	**Egress PRAM ECC Error** Egress Packet RAM 2-bit error detection. 0 = No error detected 1 = Egress PRAM 2-bit ECC error detected	0, 8	RW1CS	Yes	0
4	**Egress LLIST ECC Error** Egress Link-List RAM 2-bit error detection. 0 = No error detected 1 = Egress Link-List 2-bit ECC error detected	0, 8	RW1CS	Yes	0
5	**Ingress RAM 1-Bit ECC Error** Source Packet RAM 1-bit soft error detection. 0 = No error detected 1 = Ingress RAM 1-BIT ECC error detected	0, 8	RW1CS	Yes	0
6	**Egress Memory Allocation Unit (MAU) 1-Bit Soft Error Counter Overflow** Egress Memory Allocation/De-allocation RAM 1-bit Soft Error Count is greater than or equal to 8. 0 = No error detected 1 = Egress MAU 1-bit soft-error overflow	0, 8	RW1CS	Yes	0
7	**Egress Memory Allocation Unit (MAU) 2-Bit Soft Error** Egress Packet Memory Allocation/De-allocation RAM 2-bit error detection. 0 = No 2-bit error detected 1 = Egress MAU 2-bit soft error detected	0, 8	RW1CS	Yes	0

Register 11-49. 1CCh Error Handler 32-Bit Error Status *(*Only Port 0, *Factory Test Only) (Cont.)*

Bit(s)	Description	Bit Exists Only on Port(s)	Type	Serial EEPROM	Default
8	**Ingress RAM Uncorrectable ECC Error** Ingress Packet RAM 2-bit Error detection. 0 = No 2-bit error detected 1 = Packet RAM Uncorrectable ECC error detected	0, 8	RW1CS	Yes	0
9	**Ingress LLIST 1-Bit ECC Error** Ingress Link-List RAM 1-bit soft error detection. 0 = No error detected 1 = 1-bit ECC error detected	0, 8	RW1CS	Yes	0
10	**Ingress LLIST Uncorrectable ECC Error** Ingress packet Link-List RAM 2-bit error detection. 0 = No 2-bit error detected 1 = Ingress Link-List Uncorrectable ECC Error detected	0, 8	RW1CS	Yes	0
11	**Credit Update Timeout Status** No useful credit update to make forward progress for 512 ms or 1s (disabled by default). 0 = No Credit Update Timeout detected 1 = Credit Update Timeout completed	0, 1, 8, 9, 10, 11	RW1CS	Yes	0
12	**INCH Underrun Error** Ingress Credit Underrun. 0 = No error detected 1 = Credit underrun error detected	0, 1, 8, 9, 10, 11	RW1CS	Yes	0
13	**Ingress Memory Allocation Unit 1-Bit Soft Error Counter Overflow** Ingress Memory Allocation/De-allocation RAM 1-bit soft-error count greater than or equal to 8. 0 = No error detected 1 = 1-bit Soft Error Counter is ≥ 8	0, 8	RW1CS	Yes	0
14	**Ingress Memory Allocation Unit 2-Bit Soft Error** Ingress Memory Allocation/De-allocation RAM 2-bit error detection for Transaction Layer Ingress Memory Allocation/De-allocation unit. 0 = No error detected 1 = 2-bit soft error detected	0, 8	RW1CS	Yes	0
31:15	***Reserved***				0-0h

Note: *Error logging is enabled in register offset 1D0h, by default.*

Register 11-50. 1D0h Error Handler 32-Bit Error Mask (Only Port 0, *Factory Test Only)*

Bit(s)	Description	Bit Exists Only on Port(s)	Type	Serial EEPROM	Default
0	**Completion FIFO Overflow Mask** 0 = If enabled, error generates MSI/INT*x* interrupt 1 = *Completion FIFO Overflow Status* bit is masked/ disabled	0, 8	RWS	Yes	1
1	**Egress PRAM Soft-Error Overflow Mask** 0 = No effect on reporting activity 1 = *Egress PRAM Soft-Error Overflow* bit is masked/ disabled	0, 1, 8, 9, 10, 11	RWS	Yes	1
2	**Egress LLIST Soft-Error Overflow Mask** 0 = No effect on reporting activity 1 = *Egress LLIST Soft-Error Overflow* bit is masked/ disabled	0, 8	RWS	Yes	1
3	**Egress PRAM ECC Error Mask** 0 = No effect on reporting activity 1 = *Egress PRAM ECC Error* bit is masked/disabled	0, 8	RWS	Yes	1
4	**Egress LLIST ECC Error Mask** 0 = No effect on reporting activity 1 = *Egress LLIST ECC Error* bit is masked/disabled	0, 8	RWS	Yes	1
5	**Ingress RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM 1-Bit ECC Error* bit is masked/disabled	0, 8	RWS	Yes	1
6	**Egress Memory Allocation Unit 1-Bit Soft-Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Egress Memory Allocation Unit (MAU) 1-Bit Soft Error Counter Overflow* bit is masked/disabled	0, 8	RWS	Yes	1
7	**Egress Memory Allocation Unit 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Egress Memory Allocation Unit (MAU) 2-Bit Soft Error* bit is masked/disabled	0, 8	RWS	Yes	1

Register 11-50. 1D0h Error Handler 32-Bit Error Mask *(*Only Port 0, *Factory Test Only)*

Bit(s)	Description	Bit Exists Only on Port(s)	Type	Serial EEPROM	Default
8	**Ingress RAM Uncorrectable ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM Uncorrectable ECC Error* bit is masked/disabled	0, 8	RWS	Yes	1
9	**Ingress LLIST 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM 1-Bit ECC Error* bit is masked/disabled	0, 8	RWS	Yes	1
10	**Ingress LLIST Uncorrectable ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress LLIST Uncorrectable ECC Error* bit is masked/disabled	0, 8	RWS	Yes	1
11	**Credit Update Timeout Status Mask** 0 = No effect on reporting activity 1 = *Credit Update Timeout Status* bit is masked/disabled	0, 1, 8, 9, 10, 11	RWS	Yes	1
12	**INCH Underrun Error Mask** 0 = No effect on reporting activity 1 = *INCH Underrun Error* bit is masked/disabled	0, 1, 8, 9, 10, 11	RWS	Yes	1
13	**Ingress Memory Allocation Unit 1-Bit Soft Error Counter Overflow Mask** Mask for *Ingress Memory Allocation Unit 1-Bit Soft Error Counter Overflow* bit. 0 = No effect on reporting activity 1 = 1-bit Soft Error Counter Overflow is masked/disabled	0, 8	RWS	Yes	1
14	**Ingress Memory Allocation Unit 2-Bit Soft Error Mask** Mask for *Ingress Memory Allocation Unit 2-Bit Soft Error* bit. 0 = Error reporting enabled using interrupts 1 = 2-Bit soft error reporting is masked/disabled	0, 8	RWS	Yes	1
31:15	***Reserved***				0-0h

Note: *For register offset 1DCh, if Port 0 is the NT Port:*

- *This register is loaded from the NT Port Virtual Interface register offset 1DCh location in the serial EEPROM*
- *The serial EEPROM must be programmed such that both the Port 0 and NT Port Virtual Interface register offset 1DCh locations contain the same value for this register*

Register 11-51. 1DCh Debug Control (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	***Factory Test Only***			0-0h
11:8	**Upstream Port Number** When *Hardware/Software Configuration Mode Control* bit = 0, Upstream Port Number – Reads External strap value on the STRAP_UPSTRM_PORTSEL[3:0] balls. Software is not allowed to change this value.	HwInit	Yes	Set by Strapping ball levels
	When *Hardware/Software Configuration Mode Control* bit = 1, Upstream Port Number is set by software. 0h = Port 0 1h = Port 1 2h to 7h = ***Reserved*** 8h = Port 8 9h = Port 9 Ah = Port 10 Bh = Port 11 Ch to Fh = ***Reserved***	RW[a]	Yes	
14:12	***Reserved***			000b
15	**Hardware/Software Configuration Mode Control** 0 = Upstream and NT Port selection by the STRAP_UPSTRM_PORTSEL[3:0] and the STRAP_NT_UPSTRM_PORTSEL[3:0] balls, which are overridden by the serial EEPROM, cannot be changed by software at runtime. 1 = Upstream and NT Port assignment can be changed by software writing new values to the *Upstream Port Number*[11:8] and *NT Port Number*[27:24] fields, followed by issuance of a Hot Reset to the upstream port. The bit 20 (Upstream Port Hot Reset and Link Down Reset Propagation Disable bit) value must be 0.	RW	Yes	0

Register 11-51. 1DCh Debug Control (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
16	**Upstream Hot Reset Severity Control** 0 = Reset NT Port data path when the upstream port receives a Hot Reset or DL_Down condition 1 = Do not reset NT Port data path when the upstream port receives a Hot Reset or DL_Down condition ***Note:*** *In NT mode, a value of 1 is automatically set as default.*	RW	Yes	0
17	**Hot Reset Serial EEPROM Load Disable** Serial EEPROM load disable only for a Hot Reset or DL_Down condition; does not affect Fundamental Reset. 0 = Serial EEPROM load enabled upon a Hot Reset 1 = Serial EEPROM load disabled upon a Hot Reset	RW	Yes	0
19:18	**Mode Select** Mode is selected by STRAP_MODE_SEL[1:0] Strapping balls, and overridden by the serial EEPROM. Software is not allowed to change this value. 00b = ***Reserved*** 01b = NT Intelligent Adapter mode 10b = NT Dual-Host mode 11b = Transparent mode	HwInit R/W[a]	Yes Yes	Set by Strapping ball levels
20	**Upstream Port Hot Reset and Link Down Reset Propagation Disable** 0 = Internal Reset and Hot Reset propagation are enabled 1 = Internal Reset and Hot Reset propagation are disabled Set to 1 for NT Dual-Host mode.	RW	Yes	0
23:21	***Reserved***			000b
27:24	**NT Port Number** When bits [19:18] (*Mode Select* field) are set to 01b or 10b and bit 15 (*Hardware/Software Configuration Mode Control* bit) is cleared to 0, the NT Port number is set by the STRAP_NT_UPSTRM_PORTSEL[3:0] Strapping balls. This field is "don't care" for T mode. Software is not allowed to change this value.	HwInit	Yes	Set by Strapping ball levels
	When bits [19:18] (*Mode Select* field) are set to 01b or 10b and bit 15 (*Hardware/Software Configuration Mode Control* bit) is set to 1, the NT Port number is selected by this field set by software: 0h = Port 0 1h = Port 1 2h to 7h = ***Reserved*** 8h = Port 8 9h = Port 9 Ah = Port 10 Bh = Port 11 Ch to Fh = ***Reserved***	R/W[a]	Yes	

Register 11-51. 1DCh Debug Control (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
28	**Virtual Interface Access Enable** Used only in NT mode. When the serial EEPROM is not present, the default value is 1; otherwise, the default value is 0. 0 = Retries Type 0 Configuration TLP received on NT Port Virtual Interface 1 = Accepts Type 0 Configuration TLP on NT Port Virtual Interface ***Notes:*** *This bit does not affect the PEX 8524 in Transparent mode.* *Set this bit to enable Configuration access to the NT Port Virtual Interface.*	RW	Yes	1
29	**Link Interface Access Enable** Used only in NT mode. Default value is 1 when bits [19:18] (*Mode Select* field) are set to 10b (Dual Host mode). Otherwise, the default value is 0. 0 = Retries Type 0 Configuration TLP received on NT Port Link Interface 1 = Accepts Type 0 Configuration TLP on NT Port Link Interface ***Notes:*** *This bit does not affect the PEX 8524 in Transparent mode.* *Set this bit to enable Configuration access to the NT Port Link Interface.*	RW	Yes	0
30	**On-Board SerDes Lane Status Control** 0 = Physical Layer Lane up status controls on-board PEX_LANE_GOOD[7:0]# and PEX_LANE_GOOD[31:16]# outputs 1 = Software-driven value to offset 1F4h controls the on-board SerDes Lane-Good output	RW	Yes	0
31	**Power-Up RAM BIST Status** Reports the power-up RAM BIST result. 0 = No power-up RAM BIST error 1 = **Non-recoverable Fatal error detected, must replace PEX 8524 device**	RO	No	0

a. Although these bits are RW, do not change by software.

Register 11-52. 1E0h Power Management Hot Plug User Configuration (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**L0s Entry Idle Count** Time to meet to enter L0s. 0 = Idle condition lasts for 1 µs 1 = Idle condition lasts for 4 µs	RW	Yes	0
1	**L1 Upstream Port Receiver Idle Count** For active L1 entry. 0 = Upstream port receiver idle for 2 µs 1 = Upstream port receiver idle for 3 µs	RW	Yes	0
2	**HPC PME Turn-Off Enable** 1 = PME Turn-off message is transmitted before the port is turned Off on a downstream port	RW	Yes	0
4:3	**HPC T_{pepv} Delay** Slot power-applied to power-valid delay time. 00b = 16 ms 01b = 32 ms 10b = 64 ms 11b = 128 ms	RO	Yes	00b
5	**HPC Inband Presence Detect Enable** 0 = HP_PRSNT[1:0]# or HP_PRSNT[11:8]# Input balls are used to detect a board present in the slot 1 = SerDes Receiver Detect mechanism is used to detect a board present in the slot	RO	Yes	0
6	**HPC T_{pvperl} Delay** Downstream port power-valid to reset signal release time. 0 = 20 ms 1 = 100 ms (default)	RO	Yes	1
12:7	**HPC Test Bits** ***Factory Test Only.*** Testing bits – must be 000_000b.	RW	Yes	0_0000_0b
31:13	***Reserved***			0-0h

Register 11-53. 1E4h Egress Control and Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM	Default
0	**Egress Credit Update Timer Enable** In this mode, when the port is not receiving credits to make forward progress and the Egress Timeout timer times out, the downstream link is brought down. 0 = Egress Credit update timer disabled 1 = Egress Credit update timer enabled	0, 1, 8, 9, 10, 11	RW	Yes	0
1	**Egress Timeout Value** 0 = Minimum 512 ms (Maximum 768 ms) 1 = Minimum 1,024 ms (Maximum 1,280 ms)	0, 1, 8, 9, 10, 11	RW	Yes	0
2	**DL_Down Handling** 0 = Reports Unsupported Request error for all TLP requests received in DL_Down state 1 = Reports Unsupported Request for first Posted/ Non-Posted TLP request in DL_Down state – silently drops subsequent TLP requests	0, 1, 8, 9, 10, 11	RW	Yes	0
7:3	***Reserved***				0-0h
15:8	**Link-List RAM Soft Error Count** Link-List RAM 8-bit Soft Error Counter value. Counter shared by: • Packet Link-List RAM • Packet Link-List De-allocation RAM • Scheduler Data RAM Counter increments for 1-bit soft errors detected in the RAM.	0, 8	RO	No	00h
19:16	**VC&T Encountered Timeout** 0h = VC0 Posted 1h = VC0 Non-Posted 2h = VC0 Completion 3h = VC1 Posted 4h = VC1 Non-Posted 5h = VC1 Completion	0, 1, 8, 9, 10, 11	RO	Yes	0h
23:20	***Reserved***				0h
31:24	**Packet RAM Soft Error Count** Counter increments for each 1-bit soft error detected in the RAM.	0, 8	RO	No	00h

Register 11-54. 1E8h Bad TLP Count (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Bad TLP Count** Counts the number of TLPs with bad LCRC, or number of TLPs with a sequence number mismatch error. The maximum value is FFh. The Counter saturates at FFh and does not roll over to 00h.	RW	Yes	00h
31:8	***Reserved***			0000_00h

Register 11-55. 1ECh Bad DLLP Count (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Bad DLLP Count** Counts the number of DLLPs with bad LCRC, or number of DLLPs with a sequence number mismatch error. The maximum value is FFh. The Counter saturates at FFh and does not roll over to 00h.	RW	Yes	00h
31:8	***Reserved***			0000_00h

Register 11-56. 1F0h PLX-Specific Relaxed Ordering Enable (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
19:0	***Reserved***			0h
20	**PLX-Specific Relaxed Ordering Enable** **Silicon Revision AA** ***Reserved***			0
	Silicon Revisions BB/BC Enables VC0 Completions to pass VC0 Posted packets. 0 = VC0 completion TLP blocked by older VC0 Posted TLP 1 = VC0 Completion TLP bypasses the older VC0 Posted TLP	RW	Yes	0
31:21	***Reserved***			0h

Note: *For register offset 1F4h, if the following conditions are met:*

- *Serial EEPROM programs Port 0 to be the NT Port*
- ***On-Board SerDes Lane Status Control*** *is set (1DCh[30]=1) to enable software or serial EEPROM control of the PEX_LANE_GOOD[31:16, 7:0]# outputs*

the serial EEPROM must be programmed such that both Port 0 and the NT Port Virtual Interface register offset 1F4h locations contain the same value for this register.

Register 11-57. 1F4h Software-Controlled Lane Status (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Software-Controlled Lane Status** Echoes the state of the PEX_LANE_GOOD[7:0]# balls when the **Debug Control** register *On-Board SerDes Lane Status Control* bit (offset 1DCh[30]) is cleared to 0; otherwise, these bits are Read-Write when the *On-Board SerDes Lane Status Control* bit is set to 1. These bits control the SerDes lanes, as follows: **Bit** **SerDes Lane** 0 0 … 6 6 7 7	RO	Yes	0-0h
		RW	Yes	0-0h
15:8	***Reserved***			0-0h
31:16	**Software-Controlled Lane Status** Echoes the state of the PEX_LANE_GOOD[31:16]# balls when the **Debug Control** register *On-Board SerDes Lane Status Control* bit (offset 1DCh[30]) is cleared to 0; otherwise, these bits are Read-Write when the *On-Board SerDes Lane Status Control* bit is set to 1. These bits control the SerDes lanes, as follows: **Bit** **SerDes Lane** 16 16 … 30 30 31 31	RO	Yes	0-0h
		RW	Yes	0-0h

Register 11-58. 1F8h ACK Transmission Latency Limit (All Ports)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM</th><th>Default</th></tr>
<tr><td>7:0</td><td>ACK Transmission Latency Limit
If the serial EEPROM is not present, the value of this register changes based upon the negotiated link width after the link is up. This value assumes that Maximum Payload Size is 256 bytes.
If the serial EEPROM is present, program the serial EEPROM to load the value based upon the programmed port width and Device Control register Maximum Payload Size field value (offset 70h[7:5]):
<table><tr><th rowspan="2">Maximum Payload Size</th><th colspan="5">Port Width</th></tr><tr><th>x1</th><th>x2</th><th>x4</th><th>x8</th><th>x16[a]</th></tr><tr><td>128B</td><td>FAh</td><td>80h</td><td>49h</td><td>43h</td><td>37h</td></tr><tr><td>256B</td><td>FFh</td><td>D9h</td><td>76h</td><td>6Bh</td><td>64h</td></tr></table>a. x16 is valid only for Station 1.
Note: The value of this field is valid after link negotiation completes.</td><td>RW</td><td>Yes</td><td>FFh</td></tr>
<tr><td>15:8</td><td>HPC Test Bits
Factory Test Only. Testing bits – must be 00h.</td><td>RW</td><td>Yes</td><td>00h</td></tr>
<tr><td>31:16</td><td>Reserved</td><td></td><td></td><td>0000h</td></tr>
</table>

11.13.2 Physical Layer Registers

Notes: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes lanes into groups of four contiguous lanes for testing purposes. For Port 0, the quads are SerDes[0-3] and SerDes[4-7]. For Port 8, the quads are SerDes[16-19], SerDes[20-23], SerDes[24-27], and SerDes[28-31].*

Port 0 bits in these registers affect Station 0 ports and SerDes. Port 8 bits in these registers affect Station 1 ports and SerDes.

Table 11-14. PLX-Specific Physical Layer Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved		200h – 20Ch
Phy User Test Pattern 0		210h
Phy User Test Pattern 4		214h
Phy User Test Pattern 8		218h
Phy User Test Pattern 12		21Ch
Physical Layer Status	Physical Layer Command	220h
Port Configuration		224h
Physical Layer Test		228h
Physical Layer		22Ch
Physical Layer Port Command		230h
SKIP Ordered-Set Interval		234h
Quad 0 SerDes Diagnostic Data		238h
Quad 1 SerDes Diagnostic Data		23Ch
Quad 2 SerDes Diagnostic Data		240h
Quad 3 SerDes Diagnostic Data		244h
SerDes Nominal Drive Current Select		248h
SerDes Drive Current Level Select 1		24Ch
SerDes Drive Current Level Select 2		250h
SerDes Drive Equalization Level Select 1		254h
SerDes Drive Equalization Level Select 2		258h
Reserved		25Ch
Status Data from Serial EEPROM	Serial EEPROM Status / Serial EEPROM Control	260h
Serial EEPROM Buffer		264h
Reserved		268h – 2C4h

Register 11-59. 210h Phy User Test Pattern 0 (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern 0** Test pattern bytes 0-3. Used for Digital Far-End Loop-Back testing.	RW	Yes	0-0h

Register 11-60. 214h Phy User Test Pattern 4 (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern 4** Test pattern bytes 4-7. Used for Digital Far-End Loop-Back testing.	RW	Yes	0-0h

Register 11-61. 218h Phy User Test Pattern 8 (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern 8** Test pattern bytes 8-11. Used for Digital Far-End Loop-Back testing.	RW	Yes	0-0h

Register 11-62. 21Ch Phy User Test Pattern 12 (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern 12** Test pattern bytes 12-15. Used for Digital Far-End Loop-Back testing.	RW	Yes	0-0h

Register 11-63. 220h Physical Layer Command and Status (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
Physical Layer Command				
0	**Port Enumerator Enable** 0 = Enumerate not enabled 1 = Enumerate enabled	HwInit	Yes	0
1	**TDM Enable** 0 = TDM not enabled 1 = TDM enabled	HwInit	Yes	0
2	***Reserved***			0
3	**Upstream Port as Configuration Master Enable** 0 = Upstream Port Cross-link not supported 1 = Upstream Port Cross-link supported	RW	Yes	0
4	**Downstream Port as Configuration Slave Enable** 0 = Downstream Port Cross-link not supported 1 = Downstream Port Cross-link supported	RW	Yes	0
5	**Lane Reversal Disable** 0 = Lane reversal supported 1 = Lane reversal not supported	RW	Yes	0
6	***Reserved***			0
7	**FC-Init Triplet Enable** **Silicon Revision AA** 0 = FC-Init1 Triplet (P, NP, Cpl) can be interrupted by idles 1 = FC-Init1 Triplet (P, NP, Cpl) must be back-to-back ***Note: Logic in Silicon Revisions BB/BC is inverted from Silicon Revision AA.***	RW	Yes	1
	FC-Init Triplet Disable **Silicon Revisions BB/BC** 0 = FC-Init1 Triplet (P, NP, Cpl) must be back-to-back 1 = FC-Init1 Triplet (P, NP, Cpl) can be interrupted by idles ***Note: Logic in Silicon Revisions BB/BC is inverted from Silicon Revision AA.***	RW	Yes	1
15:8	**N_FTS Value** Number of Fast Training Sets (N_FTS) value to transmit in training sets.	RW	Yes	40h

Register 11-63. 220h Physical Layer Command and Status (Only Ports 0, 8, and NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Physical Layer Status			
19:16	***Reserved***			0h
22:20	**Number of Ports Enumerated** Number of ports in current configuration.	HwInit	Yes	000b
23	***Reserved***			0
24	**Port 0 or 8 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow	RW1C	Yes	0
25	**Port 1 or 9 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow	RW1C	Yes	0
26	**Port 10 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow ***Reserved*** for Station 0.	RW1C	Yes	0
27	**Port 11 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow ***Reserved*** for Station 0.	RW1C	Yes	0
31:28	***Reserved***			0h

Register 11-64. 224h Port Configuration (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**Port Configuration** The serial EEPROM bit values always override the values of the STRAP_STN0_PORTCFG[4:0] and STRAP_STN1_PORTCFG[3:0] Strapping signals (assuming the serial EEPROM values are loaded; refer to Table 11-15). Bits [4:3] must always be programmed to 00b. This register is reset only by a Fundamental Reset (PEX_PERST# assertion). The serial EEPROM is used to optionally re-configure the ports from the value set by the STRAP_STN0_PORTCFG[4:0] and STRAP_STN1_PORTCFG[3:0] inputs, using the values defined in Table 11-15. ***Note:*** *All other configurations default to option 0h.*	HwInit	Yes	0_0000b
31:5	***Reserved***			0-0h

Table 11-15. PEX 8524 Port Configurations

Configuration Value (Port 0 or 8, Offset 224h[4:0])	Lane Width Per Port					
	Station 0		Station 1			
	0	1	8	9	10	11
0h	x4	x4	x4	x4	x4	x4
1h			x16[a]	–	–	–
2h	x8		x8	x8	–	–
3h			x8	x4	x4	–
4h			x8	x4	x2	x2
5h			x8	x2	x2	x4
6h			x8	x2	x4	x2

a. Ports 8 and 9 can be combined to create a 16-lane (x16) port.

Register 11-65. 228h Physical Layer Test (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Timer Test Mode Enable** 0 = Normal Physical Layer Timer parameters used 1 = Shortens Timer scale from milliseconds to microseconds	RW	Yes	0
1	**SKIP-Timer Test Mode Enable** 0 = Disables SKIP-Timer Test mode 1 = Enables SKIP-Timer Test mode	RW	Yes	0
2	**Port_0_x1** 1 = Ports 0 and/or 8 are configured as x1 only	RW	Yes	0
3	**TCB Capture Disable** 0 = Training Control Bit (TCB) Capture is enabled 1 = Disables TCB Capture	RW	Yes	0
4	**Analog Loop-Back Enable** 0 = PEX 8524 enters Digital Loop-Back Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loop-Back* bit exclusively set in the TS1 Training Control symbol. PEX 8524 then loops back data through the elastic buffer, 8b/10b decoder, and 8b/10b encoder. 1 = PEX 8524 enters Analog Loop-Back Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loop-Back* bit exclusively set in the TS1 Training Control symbol. PEX 8524 then loops back the symbol stream from the 10-bit Receive interface (before the elastic buffer) to the 10-bit Transmit interface.	RW	Yes	0
5	**Port/SerDes Test Pattern Enable Select** 1 = Bits [31:28] (*User Test Pattern Enable* bits) select ports rather than SerDes quads	RW	Yes	0
6	***Reserved***			0
7	**SerDes BIST Enable** When programmed to 1 by serial EEPROM, enables SerDes internal loop-back Pseudo-Random Bit Sequence (PRBS) test for 512 µs before starting link initialization.	RO	Yes	0
9:8	**PRBS Diagnostic Data Select** Selects the SerDes within the quad for PRBS generation/checking. **Value** / **Port 0 Station 0 SerDes** / **Port 8 Station 1 SerDes** 00b = [0, 4] / [16, 20, 24, 28] 01b = [1, 5] / [17, 21, 25, 29] 10b = [2, 6] / [18, 22, 26, 30] 11b = [3, 7] / [19, 23, 27, 31]	RW	Yes	00b
15:10	***Reserved***			0-0h

Register 11-65. 228h Physical Layer Test (Only Ports 0, 8, and NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
19:16	**PRBS Enable** When set to 1, enables PRBS sequence generation/checking on the SerDes quads, by Station. **Bit** / **Port 0 Station 0 SerDes** / **Port 8 Station 1 SerDes** 16 / [0-3] / [16-19] 17 / [4-7] / [20-23] 18 / ***Reserved*** / [24-27] 19 / ***Reserved*** / [28-31] ***Note: PRBS Enable and User Test Pattern Enable (bits [31:28]) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each station register (Ports 0 and 8), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.***	RW	Yes	0000b
23:20	**PRBS External Loop-Back** 0 = SerDes quad establishes Internal Analog Loop-Back mode when the corresponding *PRBS Enable* bit (bit 19, 18, 17, or 16) is set to 1 1 = SerDes quad establishes Analog Loop-Back Master mode when the corresponding *PRBS Enable* bit (bit 19, 18, 17, or 16) is set to 1 The following bit commands are valid when the **Physical Layer Port Command** register *Port x Loop-Back Command* bit (Port 0 or 8, offset 230h[0, 4, 8, and/or 12]) is set for the associated port. **Bit** / **Port 0 Station 0 SerDes** / **Port 8 Station 1 SerDes** 20 / [0-3] / [16-19] 21 / [4-7] / [20-23] 22 / ***Reserved*** / [24-27] 23 / ***Reserved*** / [28-31]	RW	Yes	0000b

Register 11-65. 228h Physical Layer Test (Only Ports 0, 8, and NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
27:24	**PRBS Error Count Reset** When set to 1, resets the PRBS Error Counter (**Quad SerDes *x* Diagnostic Data** register *PRBS Error Count* field). The bits in this field are self-clearing. **Bit** / **Port 0 Station 0** / **Port 8 Station 1** 24: Offset 238h[31:24] / Offset 238h[31:24] 25: Offset 23Ch[31:24] / Offset 23Ch[31:24] 26: ***Reserved*** / Offset 240h[31:24] 27: ***Reserved*** / Offset 244h[31:24]	RO	Yes	0000b
31:28	**User Test Pattern Enable** 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit Phy User Test Pattern [**Phy User Test Pattern *x*** registers (Ports 0 and 8, offsets 210h through 21Ch)] on the SerDes quads in Digital Far-End Loop-Back Master mode. **Bit** / **Port 0 Station 0 SerDes** / **Port 8 Station 1 SerDes** 28: [0-3] / [16-19] 29: [4-7] / [20-23] 30: ***Reserved*** / [24-27] 31: ***Reserved*** / [28-31] ***Note: User Test Pattern Enable and PRBS Enable (bits [19:16]) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each station register (Ports 0 and 8), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.***	RW	Yes	0000b

Note: *Port 0 parameters apply to SerDes[0-3] and SerDes[4-7]. Port 8 parameters apply to SerDes[16-19], SerDes[20-23], SerDes[24-27], and SerDes[28-31].*

Register 11-66. 22Ch Physical Layer (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
5:0	***Factory Test Only***	RW1S	Yes	00_0000b
7:6	***Reserved***	RW1S	Yes	00b
9:8	**SerDes Quad 0 TxTermAdjust** SerDes Quad 0 TxTermAdj[1:0]. Control bus to adjust Transmit termination values above or below the nominal 50 Ohms for physical lanes [0-3]/[16-19]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b
11:10	**SerDes Quad 1 TxTermAdjust** SerDes Quad 1 TxTermAdj[1:0]. Control bus to adjust Transmit termination values above or below the nominal 50 Ohms for physical lanes [4-7]/[20-23]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b
13:12	**SerDes Quad 2 TxTermAdjust** SerDes Quad 2 TxTermAdj[1:0]. Control bus to adjust Transmit termination values above or below the nominal 50 Ohms for physical lanes [24-27]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b
15:14	**SerDes Quad 3 TxTermAdjust** SerDes Quad 3 TxTermAdj[1:0]. Control bus to adjust Transmit termination values above or below the nominal 50 Ohms for physical lanes [28-31]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b

Register 11-66. 22Ch Physical Layer (Only Ports 0, 8, and NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
17:16	**SerDes Quad 0 RxTermAdjust** SerDes Quad 0 RxTermAdj[1:0]. Control bus to adjust Receive termination values above or below the nominal 50 Ohms for physical lanes [0-3]/[16-19]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b
19:18	**SerDes Quad 1 RxTermAdjust** SerDes Quad 1 RxTermAdj[1:0]. Control bus to adjust Receive termination values above or below the nominal 50 Ohms for physical lanes [4-7]/[20-23]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b
21:20	**SerDes Quad 2 RxTermAdjust** SerDes Quad 2 RxTermAdj[1:0]. Control bus to adjust Receive termination values above or below the nominal 50 Ohms for physical lanes [24-27]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b
23:22	**SerDes Quad 3 RxTermAdjust** SerDes Quad 3 RxTermAdj[1:0]. Control bus to adjust Receive termination values above or below the nominal 50 Ohms for physical lanes [28-31]. This allows precise matching to compensate for package or board impedance mismatch. 00b = Sets Tx termination to nominal (approximately 50 Ohms) 01b = Sets Tx termination to (nominal -17%) 10b = Sets Tx termination to (nominal +10%) 11b = Sets Tx termination to (nominal -15%)	RW1S	Yes	00b

Register 11-66. 22Ch Physical Layer (Only Ports 0, 8, and NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
25:24	**SerDes Quad 0 RxEqCtl** SerDes Quad 0 RxEqCtl[1:0]. Control bus to adjust the Receiver equalization, globally for physical lanes [0-3]/[16-19]. For further details, refer to the expanded description that follows this register table. Field decode is defined in Table 11-16.	RW1S	Yes	00b
27:26	**SerDes Quad 1 RxEqCtl** SerDes Quad 1 RxEqCtl[1:0]. Control bus to adjust the Receiver equalization, globally for physical lanes [4-7]/[20-23]. For further details, refer to the expanded description that follows this register table. Field decode is defined in Table 11-16.	RW1S	Yes	00b
29:28	**SerDes Quad 2 RxEqCtl** SerDes Quad 2 RxEqCtl[1:0].Control bus to adjust the Receiver equalization, globally for physical lanes [24-27]. For further details, refer to the expanded description that follows this register table. Field decode is defined in Table 11-16.	RW1S	Yes	00b
31:30	**SerDes Quad 3 RxEqCtl** SerDes Quad 3 RxEqCtl[1:0].Control bus to adjust the Receiver equalization, globally for physical lanes [28-31]. For further details, refer to the expanded description that follows this register table. Field decode is defined in Table 11-16.	RW1S	Yes	00b

Note: *Port 0 parameters apply to SerDes[0-3] and SerDes[4-7]. Port 8 parameters apply to SerDes[16-19], SerDes[20-23], SerDes[24-27], and SerDes[28-31].*

SerDes Quad *x* RxEqCtl Expanded Description. At high speeds, the channel between a PCI Express Transmitter and Receiver exhibits frequency-dependent losses (*such as* due to PCB dielectric and conductor skin-effect). The channel acts as a low-pass filter, attenuating the high-frequency components of a signal passing through it. This distortion results in Inter Symbol Interference (ISI). ISI is a form of deterministic jitter that can easily close the received data "eye," reducing the ability to reliably recover a data stream across the channel. To mitigate the effects of ISI, the receiver at each lane includes a receive equalizer. The receive equalizer is implemented as a selectable, high-pass filter at the receiver input pad and is capable of removing as much as 0.4 UI of ISI-related jitter. SerDes Quad *x* RxEqCtl decodes as defined in Table 11-16.

The Channel Length assumes standard FR4 material. The Rx Equalizer settings should be chosen based on the amount of deterministic jitter induced by the channel. The channel lengths listed in the table above are included as a general guideline, not as an absolute reference. Deterministic jitter as a function of channel length can vary with PCB layer stackup, PCB material, and the type of connector(s) used.

Table 11-16. RxEqCtl[1:0] Decode for Register Offset 224h[31:24]

RxEqCtl[1:0]	RX Eq Setting	Input Jitter	Channel Length
00b	Maximum Rx Eq	0.25 UI	50.8 cm (20 inches) and two or more connectors
01b	Minimum Rx Eq	Between 0.1 and 0.25 UI	Between 20.32 and 50.8 cm (8 and 20 inches) and up to two connectors
10b, 11b	Rx Eq OFF	< 0.1 UI	20.32 cm (8 inches) or less, up to one connector

Register 11-67. 230h Physical Layer Port Command (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Port 0 or 8 Loop-Back Command** 0 = Port 0 or 8 is not enabled to go to Loop-Back Master state 1 = Port 0 or 8 is enabled to go to Loop-Back Master state	RW	Yes	0
1	**Port 0 or 8 Scrambler Disable** If serial EEPROM load sets this bit, scrambler is disabled in Configuration-Complete state. If software sets this bit when the Link is in the up state, hardware immediately disables its scrambler without executing Link Training protocol. The upstream/downstream device scrambler will not be disabled. 0 = Port 0 or 8 scrambler is enabled 1 = Port 0 or 8 scrambler is disabled	RW	Yes	0
2	**Port 0 or 8 Rx L1 Only** Port 0 or 8 Receiver enters to ASPM L1. 0 = Port 0 or 8 receiver is allowed to go to ASPM L0s or L1 state when it detects Electrical Idle Ordered-Set in L0 state 1 = Port 0 or 8 receiver is allowed to go to ASPM L1 only when it detects Electrical Idle Ordered-Set in L0 state	RW	Yes	0
3	**Port 0 or 8 Ready as Loop-Back Master** Port 0 or 8 LTSSM established Loop-Back as a Master. 0 = Port 0 or 8 is not in Loop-Back Master mode 1 = Port 0 or 8 is in Loop-Back Master mode	RO	No	0
4	**Port 1 or 9 Loop-Back Command** 0 = Port 1 or 9 is not enabled to go to Loop-Back Master state 1 = Port 1 or 9 is enabled to go to Loop-Back Master state	RW	Yes	0
5	**Port 1 or 9 Scrambler Disable** If serial EEPROM load sets this bit, scrambler is disabled in Configuration-Complete state. If software sets this bit when the Link is in the up state, hardware immediately disables its scrambler without executing Link Training protocol. The upstream/downstream device scrambler is not disabled. 0 = Port 1 or 9 scrambler is enabled 1 = Port 1 or 9 scrambler is disabled	RW	Yes	0
6	**Port 1 or 9 Rx L1 Only** Port 1 or 9 Receiver enters to ASPM L1. 0 = Port 1 or 9 receiver is allowed to go to ASPM L0s or L1 state when it detects Electrical Idle Ordered-Set in L0 state 1 = Port 1 or 9 receiver is allowed to go to ASPM L1 only when it detects Electrical Idle Ordered-Set in L0 state	RW	Yes	0
7	**Port 1 or 9 Ready as Loop-Back Master** Port 1 or 9 LTSSM established Loop-Back as a Master. 0 = Port 1 or 9 is not in Loop-Back Master mode 1 = Port 1 or 9 is in Loop-Back Master mode	RO	No	0

Register 11-67. 230h Physical Layer Port Command (Only Ports 0, 8, and NT Port Link Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
8	**Port 10 Loop-Back Command** 0 = Port 10 is not enabled to go to Loop-Back Master state 1 = Port 10 is enabled to go to Loop-Back Master state ***Reserved*** for Station 0.	RW	Yes	0
9	**Port 10 Scramble Disable** If serial EEPROM load sets this bit, scrambler is disabled in Configuration-Complete state. ***Reserved*** for Station 0. If software sets this bit when the Link is in the up state, hardware immediately disables its scrambler without executing Link Training protocol. The upstream/downstream device scrambler is not disabled. 0 = Port 10 scrambler is enabled 1 = Port 10 scrambler is disabled	RW	Yes	0
10	**Port 10 Rx L1 Only** Port 10 Receiver enters to ASPM L1. ***Reserved*** for Station 0. 0 = Port 10 receiver is allowed to go to ASPM L0s or L1 state when it detects Electrical Idle Ordered-Set in L0 state 1 = Port 10 receiver is allowed to go to ASPM L1 only when it detects Electrical Idle Ordered-Set in L0 state	RW	Yes	0
11	**Port 10 Ready as Loop-Back Master** Port 10 LTSSM established Loop-Back as a Master. ***Reserved*** for Station 0. 0 = Port 10 is not in Loop-Back Master mode 1 = Port 10 is in Loop-Back Master mode	RO	No	0
12	**Port 11 Loop-Back Command** 0 = Port 11 is not enabled to go to Loop-Back Master state 1 = Port 11 is enabled to go to Loop-Back Master state ***Reserved*** for Station 0.	RW	Yes	0
13	**Port 11 Scramble Disable** If serial EEPROM load sets this bit, scrambler is disabled in Configuration-Complete state. ***Reserved*** for Station 0. If software sets this bit when the Link is in the up state, hardware immediately disables its scrambler without executing Link Training protocol. The upstream/downstream device scrambler is not disabled. 0 = Port 11 scrambler is enabled 1 = Port 11 scrambler is disabled	RW	Yes	0
14	**Port 11 Rx L1 Only** Port 11 Receiver enters to ASPM L1. ***Reserved*** for Station 0. 0 = Port 11 receiver is allowed to go to ASPM L0s or L1 state when it detects Electrical Idle Ordered-Set in L0 state 1 = Port 11 receiver is allowed to go to ASPM L1 only when it detects Electrical Idle Ordered-Set in L0 state	RW	Yes	0
15	**Port 11 Ready as Loop-Back Master** Port 11 LTSSM established Loop-Back as a Master. ***Reserved*** for Station 0. 0 = Port 11 is not in Loop-Back Master mode 1 = Port 11 is in Loop-Back Master mode	RO	No	0
31:16	***Reserved***			0-0h

Register 11-68. 234h SKIP Ordered-Set Interval (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	**SKIP Ordered-Set Interval** SKIP Ordered-Set interval, in symbol times. 49Ch = Minimum interval (1,180 symbol times) 602h = Maximum interval (1,538 symbol times)	RWS	Yes	49Ch
31:12	***Reserved***			0000_0h

Register 11-69. 238h Quad 0 SerDes Diagnostic Data (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
9:0	**Expected PRBS Data** Expected PRBS SerDes[0-3]/[16-19] Diagnostic data.	RO	Yes	00h
19:10	**Received PRBS Data** Received PRBS SerDes[0-3]/[16-19] Diagnostic data.	RO	Yes	00h
23:20	***Reserved***			0h
31:24	**PRBS Error Count** PRBS SerDes[0-3]/[16-19] Error count (0 to 255).	RO	Yes	00h

Note: *Port 0 parameters apply to SerDes[0-3]. Port 8 parameters apply to SerDes[16-19].*

Register 11-70. 23Ch Quad 1 SerDes Diagnostic Data Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
9:0	**Expected PRBS Data** Expected PRBS SerDes[4-7]/[20-23] Diagnostic data.	RO	Yes	00h
19:10	**Received PRBS Data** Received PRBS SerDes[4-7]/[20-23] Diagnostic data.	RO	Yes	00h
23:20	***Reserved***			0h
31:24	**PRBS Error Count** PRBS SerDes[4-7]/[20-23] Error count (0 to 255).	RO	Yes	00h

Note: *Port 0 parameters apply to SerDes[4-7]. Port 8 parameters apply to SerDes[20-23].*

Register 11-71. 240h Quad 2 SerDes Diagnostic Data (Only Port 8 and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
9:0	**Expected PRBS Data** Expected PRBS SerDes[24-27] Diagnostic data.	RO	Yes	00h
19:10	**Received PRBS Data** Received PRBS SerDes[24-27] Diagnostic data.	RO	Yes	00h
23:20	***Reserved***			0h
31:24	**PRBS Error Count** PRBS SerDes[24-27] Error count (0-255).	RO	Yes	00h

Note: *This register is **reserved** for Port 0. Port 8 parameters apply to SerDes[24-27].*

Register 11-72. 244h Quad 3 SerDes Diagnostic Data (Only Port 8 and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
9:0	**Expected PRBS Data** Expected PRBS SerDes[28-31] Diagnostic data.	RO	Yes	00h
19:10	**Received PRBS Data** Received PRBS SerDes[28-31] Diagnostic data.	RO	Yes	00h
23:20	***Reserved***			0h
31:24	**PRBS Error Count** PRBS SerDes[28-31] Error count (0 to 255).	RO	Yes	00h

Note: *This register is **reserved** for Port 0. Port 8 parameters apply to SerDes[28-31].*

Register 11-73. 248h SerDes Nominal Drive Current Select (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description		Type	Serial EEPROM	Default
1:0	**SerDes_0/SerDes_16 Nominal Drive Current**	The following values for Nominal Current apply to each drive: • 00b = 20 mA • 01b = 10 mA • 10b = 28 mA • 11b = 20 mA	RWS	Yes	00b
3:2	**SerDes_1/SerDes_17 Nominal Drive Current**		RWS	Yes	00b
5:4	**SerDes_2/SerDes_18 Nominal Drive Current**		RWS	Yes	00b
7:6	**SerDes_3/SerDes_19 Nominal Drive Current**		RWS	Yes	00b
9:8	**SerDes_4/SerDes_20 Nominal Drive Current**		RWS	Yes	00b
11:10	**SerDes_5/SerDes_21 Nominal Drive Current**		RWS	Yes	00b
13:12	**SerDes_6/SerDes_22 Nominal Drive Current**		RWS	Yes	00b
15:14	**SerDes_7/SerDes_23 Nominal Drive Current**		RWS	Yes	00b
17:16	**SerDes_24 Nominal Drive Current**		RWS	Yes	00b
19:18	**SerDes_25 Nominal Drive Current**		RWS	Yes	00b
21:20	**SerDes_26 Nominal Drive Current**		RWS	Yes	00b
23:22	**SerDes_27 Nominal Drive Current**		RWS	Yes	00b
25:24	**SerDes_28 Nominal Drive Current**		RWS	Yes	00b
27:26	**SerDes_29 Nominal Drive Current**		RWS	Yes	00b
29:28	**SerDes_30 Nominal Drive Current**		RWS	Yes	00b
31:30	**SerDes_31 Nominal Drive Current**		RWS	Yes	00b

Note: *Port 0 parameters apply to SerDes[0-3] (bits [7:0]) and SerDes[4-7] (bits [15:8]); bits [31:16] are* ***reserved****. Port 8 parameters apply to SerDes[16-19], SerDes[20-23], SerDes[24-27], and SerDes[28-31].*

Register 11-74. 24Ch SerDes Drive Current Level Select 1 (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description		Type	Serial EEPROM	Default
3:0	**SerDes_0/SerDes_16 Drive Current Level**	The following values represent the ratio of Actual Current/ Nominal Current (selected in the **SerDes Nominal Drive Current Select** register) and apply to each drive: 0h = 1.00 8h = 0.60 1h = 1.05 9h = 0.65 2h = 1.10 Ah = 0.70 3h = 1.15 Bh = 0.75 4h = 1.20 Ch = 0.80 5h = 1.25 Dh = 0.85 6h = 1.30 Eh = 0.90 7h = 1.35 Fh = 0.95	RWS	Yes	0h
7:4	**SerDes_1/SerDes_17 Drive Current Level**		RWS	Yes	0h
11:8	**SerDes_2/SerDes_18 Drive Current Level**		RWS	Yes	0h
15:12	**SerDes_3/SerDes_19 Drive Current Level**		RWS	Yes	0h
19:16	**SerDes_4/SerDes_20 Drive Current Level**		RWS	Yes	0h
23:20	**SerDes_5/SerDes_21 Drive Current Level**		RWS	Yes	0h
27:24	**SerDes_6/SerDes_22 Drive Current Level**		RWS	Yes	0h
31:28	**SerDes_7/SerDes_23 Drive Current Level**		RWS	Yes	0h

Note: *Port 0 parameters apply to SerDes[0-7]. Port 8 parameters apply to SerDes[16-23].*

Register 11-75. 250h SerDes Drive Current Level Select 2 (Only Port 8 and NT Port Link Interface)

Bit(s)	Description		Type	Serial EEPROM	Default
3:0	**SerDes_24 Drive Current Level**	The following values represent the ratio of Actual Current/Nominal Current (selected in **SerDes Nominal Drive Current Select** register) and apply to each drive: 0h = 1.00 8h = 0.60 1h = 1.05 9h = 0.65 2h = 1.10 Ah = 0.70 3h = 1.15 Bh = 0.75 4h = 1.20 Ch = 0.80 5h = 1.25 Dh = 0.85 6h = 1.30 Eh = 0.90 7h = 1.35 Fh = 0.95	RWS	Yes	0h
7:4	**SerDes_25 Drive Current Level**		RWS	Yes	0h
11:8	**SerDes_26 Drive Current Level**		RWS	Yes	0h
15:12	**SerDes_27 Drive Current Level**		RWS	Yes	0h
19:16	**SerDes_28 Drive Current Level**		RWS	Yes	0h
23:20	**SerDes_29 Drive Current Level**		RWS	Yes	0h
27:24	**SerDes_30 Drive Current Level**		RWS	Yes	0h
31:28	**SerDes_31 Drive Current Level**		RWS	Yes	0h

Note: *This register is **reserved** for Port 0. Port 8 parameters apply to SerDes[24-31].*

Register 11-76. 254h SerDes Drive Equalization Level Select 1 (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description		Type	Serial EEPROM	Default
3:0	**SerDes_0/SerDes_16 Drive Equalization Level**	The following values represent the percentage of Drive Current attributable to Equalization Current and apply to each drive: I_{EQ} / I_{DR} — De-Emphasis (dB) 0h = 0.00 — 0.00 1h = 0.04 — -0.35 2h = 0.08 — -0.72 3h = 0.12 — -1.11 4h = 0.16 — -1.51 5h = 0.20 — -1.94 6h = 0.24 — -2.38 7h = 0.28 — -2.85 8h = 0.32 — -3.35 9h = 0.36 — -3.88 Ah = 0.40 — -4.44 Bh = 0.44 — -5.04 Ch = 0.48 — -5.68 Dh = 0.52 — -6.38 Eh = 0.56 — -7.13 Fh = 0.60 — -7.96	RWS	Yes	8h
7:4	**SerDes_1/SerDes_17 Drive Equalization Level**		RWS	Yes	8h
11:8	**SerDes_2/SerDes_18 Drive Equalization Level**		RWS	Yes	8h
15:12	**SerDes_3/SerDes_19 Drive Equalization Level**		RWS	Yes	8h
19:16	**SerDes_4/SerDes_20 Drive Equalization Level**		RWS	Yes	8h
23:20	**SerDes_5/SerDes_21 Drive Equalization Level**		RWS	Yes	8h
27:24	**SerDes_6/SerDes_22 Drive Equalization Level**		RWS	Yes	8h
31:28	**SerDes_7/SerDes_23 Drive Equalization Level**		RWS	Yes	8h

Note: *Port 0 parameters apply to SerDes[0-7]. Port 8 parameters apply to SerDes[16-23].*

Register 11-77. 258h SerDes Drive Equalization Level Select 2 (Only Port 8 and NT Port Link Interface)

Bit(s)	Description		Type	Serial EEPROM	Default
3:0	**SerDes_24 Drive Equalization Level**	The following values represent the percentage of Drive Current attributable to Equalization Current and apply to each drive:	RWS	Yes	8h
7:4	**SerDes_25 Drive Equalization Level**		RWS	Yes	8h
11:8	**SerDes_26 Drive Equalization Level**		RWS	Yes	8h
15:12	**SerDes_27 Drive Equalization Level**		RWS	Yes	8h
19:16	**SerDes_28 Drive Equalization Level**		RWS	Yes	8h
23:20	**SerDes_29 Drive Equalization Level**		RWS	Yes	8h
27:24	**SerDes_30 Drive Equalization Level**		RWS	Yes	8h
31:28	**SerDes_31 Drive Equalization Level**		RWS	Yes	8h

I_{EQ} / I_{DR}	De-Emphasis (dB)
0h = 0.00	0.00
1h = 0.04	-0.35
2h = 0.08	-0.72
3h = 0.12	-1.11
4h = 0.16	-1.51
5h = 0.20	-1.94
6h = 0.24	-2.38
7h = 0.28	-2.85
8h = 0.32	-3.35
9h = 0.36	-3.88
Ah = 0.40	-4.44
Bh = 0.44	-5.04
Ch = 0.48	-5.68
Dh = 0.52	-6.38
Eh = 0.56	-7.13
Fh = 0.60	-7.96

Note: *This register is **reserved** for Port 0. Port 8 parameters apply to SerDes[24-31].*

Register 11-78. 260h Serial EEPROM Status and Control (Only Port 0)

Bit(s)	Description	Type	Serial EEPROM	Default
	Serial EEPROM Control			
12:0	**Serial EEPROM Block Address** Serial EEPROM Block Address for 32 KB.	RW	Yes	0000h
15:13	**Serial EEPROM Command** Commands to the Serial EEPROM Controller. 001b = Data from Serial EEPROM Status[31:24] bits written to the Serial EEPROM internal **Status** register 010b = Write four bytes of data from the *Serial EEPROM Buffer* into the memory location pointed to by the *Serial EEPROM Block Address* field 011b = Read four bytes of data from the memory location pointed to by the *Serial EEPROM Block Address* field into the *Serial EEPROM Buffer* 100b = Reset Write Enable latch 101b = Data from Serial EEPROM internal status register written to the Serial EEPROM Status[31:24] bits 110b = Set Write Enable latch All other values are ***reserved***. ***Note:*** *For value of 001b, only bits [31, 27:26] can be written into the serial EEPROM's internal* ***Status*** *register.*	RW	Yes	000b
	Serial EEPROM Status			
17:16	**Serial EEPROM Present** Serial EEPROM Present status, unless bit 21 (CRC Disable bit) is set to ignore CRC checking ***(not recommended)***. 00b = Not present 01b = Serial EEPROM Present – no CRC error 10b = ***Reserved*** 11b = Serial EEPROM Present, but with CRC error – unless bit 21 (*CRC Disable* bit) is set to ignore CRC checking ***(not recommended)***	RO	Yes	00b
19:18	**Serial EEPROM Command Status** 00b = Serial EEPROM Command complete 01b = Serial EEPROM Command not complete 10b = Serial EEPROM Command complete with CRC error 11b = ***Reserved***	RO	Yes	00b
20	**Serial EEPROM Block Address Upper Bit** *Serial EEPROM Block Address* upper bit 13. Extends serial EEPROM to 64 KB.	RW	Yes	0
21	**CRC Disable** 0 = Serial EEPROM input data uses CRC 1 = Serial EEPROM input data CRC disabled ***(not recommended)***	RW	Yes	0
23:22	***Reserved***			00b

Register 11-78. 260h Serial EEPROM Status and Control (Only Port 0) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM</th><th>Default</th></tr>
<tr><td colspan="5">Status Data from Serial EEPROM</td></tr>
<tr><td>24</td><td>Serial EEPROM_RDY#
0 = Serial EEPROM ready to transmit data
1 = Write cycle in progress</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>25</td><td>Serial EEPROM_WEN
0 = Serial EEPROM Write disabled
1 = Serial EEPROM Write enabled</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>27:26</td><td>Serial EEPROM_BP[1:0]
Serial EEPROM Block-Write Protect bits.
<table>
<tr><th rowspan="2">BP[1:0]</th><th rowspan="2">Level</th><th colspan="3">Array Addresses Protected</th></tr>
<tr><th>16-KB Device</th><th>32-KB Device</th><th>64-KB Device</th></tr>
<tr><td>00b</td><td>0</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td>01b</td><td>1
(top 1/4)</td><td>3000h - 3FFFh</td><td>6000h - 7FFFh</td><td>–</td></tr>
<tr><td>10b</td><td>2
(top 1/2)</td><td>2000h - 3FFFh</td><td>4000h - 7FFFh</td><td>–</td></tr>
<tr><td>11b</td><td>3
(All)</td><td>0000h - 3FFFh</td><td>0000h - 7FFFh</td><td>–</td></tr>
</table></td><td>RW</td><td>Yes</td><td>00b</td></tr>
<tr><td>30:28</td><td>Serial EEPROM Write Status
Value is 000b when serial EEPROM is not in an internal Write cycle.
Note: Definition of this field varies among serial EEPROM manufacturers. Reads of the Serial EEPROM internal Status register can return 000b or 111b, depending on the serial EEPROM that is used.</td><td>RO</td><td>Yes</td><td>000b</td></tr>
<tr><td>31</td><td>Serial EEPROM_WPEN
Serial EEPROM Write Protect Enable. When:
= 0 and Serial EEPROM_WEN = 1, the Serial EEPROM Status register is writable.
= 1, Serial EEPROM Status register is protected.
Note: This bit is not implemented in certain serial EEPROMs. Refer to the serial EEPROM manufacturer's data sheet.</td><td>RW</td><td>Yes</td><td>0</td></tr>
</table>

Note: *Within the serial EEPROM's **Status** register, only bits [31, 27:26] can be written.*

Register 11-79. 264h Serial EEPROM Buffer (Only Port 0)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Serial EEPROM Buffer**	RW	Yes	0-0h

11.13.3 CAM Routing Registers

The CAM Routing registers contain mirror copies of the registers used for:

- **Bus Number CAM (Content-Addressable Memory)** – Used to determine Configuration TLP completion route

  These registers contain mirror copies of the **Primary Bus Number**, **Secondary Bus Number** and **Subordinate Bus Number** registers of each PEX 8524 port.

- **I/O CAM** – Used to determine I/O request routing

  These registers contain mirror copies of the **I/O Base** and **I/O Limit** registers of each PEX 8524 port.

- **AMCAM (Address-Mapping CAM)** – Used to determine Memory request route

  These registers contain mirror copies of the **Memory Base and Limit Address**. **Prefetchable Memory Base and Limit Address**, **Prefetchable Memory Upper Base Address[63:32]**, and **Prefetchable Memory Upper Limit Address[63:32]** register of each PEX 8524 port.

Note: These registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 11-17. PLX-Specific CAM Routing Register Map (Only Ports 0 and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	Bus Number CAM 0			2C8h
Reserved	Bus Number CAM 1			2CCh
Reserved			2D0h –	2E4h
Reserved	Bus Number CAM 8			2E8h
Reserved	Bus Number CAM 9			2ECh
Reserved	Bus Number CAM 10			2F0h
Reserved	Bus Number CAM 11			2F4h
Reserved			2F8h –	304h
I/O CAM_1		I/O CAM_0		308h
Reserved			30Ch –	314h
I/O CAM_9		I/O CAM_8		318h
I/O CAM_11		I/O CAM_10		31Ch
Reserved			320h –	344h
AMCAM_0 Memory Limit and Base				348h
AMCAM_0 Prefetchable Memory Limit and Base[31:0]				34Ch
AMCAM_0 Prefetchable Memory Base[63:32]				350h
AMCAM_0 Prefetchable Memory Limit[63:32]				354h
AMCAM_1 Memory Limit and Base				358h
AMCAM_1 Prefetchable Memory Limit and Base[31:0]				35Ch
AMCAM_1 Prefetchable Memory Base[63:32]				360h
AMCAM_1 Prefetchable Memory Limit[63:32]				364h
Reserved			368h –	3C4h

Table 11-17. PLX-Specific CAM Routing Register Map (Only Ports 0 and 8) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
AMCAM_8 Memory Limit and Base	3C8h
AMCAM_8 Prefetchable Memory Limit and Base[31:0]	3CCh
AMCAM_8 Prefetchable Memory Base[63:32]	3D0h
AMCAM_8 Prefetchable Memory Limit[63:32]	3D4h
AMCAM_9 Memory Limit and Base	3D8h
AMCAM_9 Prefetchable Memory Limit and Base[31:0]	3DCh
AMCAM_9 Prefetchable Memory Base[63:32]	3E0h
AMCAM_9 Prefetchable Memory Limit[63:32]	3E4h
AMCAM_10 Memory Limit and Base	3E8h
AMCAM_10 Prefetchable Limit and Memory Base[31:0]	3ECh
AMCAM_10 Prefetchable Memory Base[63:32]	3F0h
AMCAM_10 Prefetchable Memory Limit[63:32]	3F4h
AMCAM_11 Memory Limit and Base	3F8h
AMCAM_11 Prefetchable Limit and Memory Base[31:0]	3FCh
AMCAM_11 Prefetchable Memory Base[63:32]	400h
AMCAM_11 Prefetchable Memory Limit[63:32]	404h
Reserved	408h – 65Ch
Ingress Control	660h
Reserved	664h
Ingress Port Enable	668h
Reserved	66Ch – 67Ch
I/OCAM_0 Upper Port 0	680h
I/OCAM_1 Upper Port 1	684h
Reserved	688h – 69Ch
I/OCAM_8 Upper Port 8	6A0h
I/OCAM_9 Upper Port 9	6A4h
I/OCAM_10 Upper Port 10	6A8h
I/OCAM_11 Upper Port 11	6ACh
Reserved	6B0h – 6BCh

11.13.3.1 Bus Number CAM Registers

Register 11-80. 2C8h Bus Number CAM 0 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of Port 0 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 0 Secondary Bus Number.	RW	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of Port 0 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***			00h

Register 11-81. 2CCh Bus Number CAM 1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of Port 1 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 1 Secondary Bus Number.	RW	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of Port 1 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***			00h

Register 11-82. 2E8h Bus Number CAM 8 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of Port 8 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 8 Secondary Bus Number.	RW	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of Port 8 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***			00h

Register 11-83. 2ECh Bus Number CAM 9 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of Port 9 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 9 Secondary Bus Number.	RW	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of Port 9 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***			00h

Register 11-84. 2F0h Bus Number CAM 10 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of Port 10 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 10 Secondary Bus Number.	RW	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of Port 10 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***			00h

Register 11-85. 2F4h Bus Number CAM 11 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of Port 11 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 11 Secondary Bus Number.	RW	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of Port 11 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***			00h

11.13.3.2 I/O CAM Registers

Register 11-86. 308h I/O CAM_0 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 0 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 0 I/O Limit value.	RW	Yes	0h

Register 11-87. 30Ah I/O CAM_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 1 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 1 I/O Limit value.	RW	Yes	0h

Register 11-88. 318h I/O CAM_8 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 8 I/O Base value.	RW	Yes	0h
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 8 I/O Limit value.	RW	Yes	0h

Register 11-89. 31Ah I/O CAM_9 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 9 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 9 I/O Limit value.	RW	Yes	0h

Register 11-90. 31Ch I/O CAM_10 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 10 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 10 I/O Limit value.	RW	Yes	0h

Register 11-91. 31Eh I/O CAM_11 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 11 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 11 I/O Limit value.	RW	Yes	0h

11.13.3.3 AMCAM (Address-Mapping CAM) Registers

AMCAM registers contain mirror copies of the **Memory Base and Limit Address**. **Prefetchable Memory Base and Limit Address**, **Prefetchable Memory Upper Base Address[63:32]**, and **Prefetchable Memory Upper Limit Address[63:32]** registers of each PEX 8524 port.

Register 11-92. 348h AMCAM_0 Memory Limit and Base (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Port 0 Memory Base value.	RW	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Port 0 Memory Limit value.	RW	Yes	000h

Register 11-93. 34Ch AMCAM_0 Prefetchable Memory Limit and Base[31:0] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_0 Port 0 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_0 Port 0 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 11-94. 350h AMCAM_0 Prefetchable Memory Base[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_0 Port 0 Prefetchable Memory Base[63:32].	RW	Yes	FFFF_FFFFh

Register 11-95. 354h AMCAM_0 Prefetchable Memory Limit[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_0 Port 0 Prefetchable Memory Limit[63:32].	RW	Yes	0-0h

Register 11-96. 358h AMCAM_1 Memory Limit and Base (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Port 1 Memory Base value.	RW	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Port 1 Memory Limit value.	RW	Yes	000h

Register 11-97. 35Ch AMCAM_1 Prefetchable Memory Limit and Base[31:0] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_1 Port 1 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_1 Port 1 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 11-98. 360h AMCAM_1 Prefetchable Memory Base[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_1 Port 1 Prefetchable Memory Base[63:32].	RW	Yes	FFFF_FFFFh

Register 11-99. 364h AMCAM_1 Prefetchable Memory Limit[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_1 Port 1 Prefetchable Memory Limit[63:32].	RW	Yes	0-0h

Register 11-100. 3C8h AMCAM_8 Memory Limit and Base (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Port 8 Memory Base value.	RW	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Port 8 Memory Limit value.	RW	Yes	000h

Register 11-101. 3CCh AMCAM_8 Prefetchable Memory Limit and Base[31:0] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_8 Port 8 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_8 Port 8 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 11-102. 3D0h AMCAM_8 Prefetchable Memory Base[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_8 Port 8 Prefetchable Memory Base[63:32].	RW	Yes	FFFF_FFFFh

Register 11-103. 3D4h AMCAM_8 Prefetchable Memory Limit[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_8 Port 8 Prefetchable Memory Limit[63:32].	RW	Yes	0-0h

Register 11-104. 3D8h AMCAM_9 Memory Limit and Base (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Port 9 Memory Base value.	RW	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Port 9 Memory Limit value.	RW	Yes	000h

Register 11-105. 3DCh AMCAM_9 Prefetchable Memory Limit and Base[31:0] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_9 Port 9 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_9 Port 9 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 11-106. 3E0h AMCAM_9 Prefetchable Memory Base[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_9 Port 9 Prefetchable Memory Base[63:32].	RW	Yes	FFFF_FFFFh

Register 11-107. 3E4h AMCAM_9 Prefetchable Memory Limit[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_9 Port 9 Prefetchable Memory Limit[63:32].	RW	Yes	0-0h

Register 11-108. 3E8h AMCAM_10 Memory Limit and Base (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Port 10 Memory Base value.	RW	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Port 10 Memory Limit value.	RW	Yes	000h

Register 11-109. 3ECh AMCAM_10 Prefetchable Limit and Memory Base[31:0] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_10 Port 10 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_10 Port 10 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 11-110. 3F0h AMCAM_10 Prefetchable Memory Base[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_10 Port 10 Prefetchable Memory Base[63:32].	RW	Yes	FFFF_FFFFh

Register 11-111. 3F4h AMCAM_10 Prefetchable Memory Limit[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_10 Port 10 Prefetchable Memory Limit[63:32].	RW	Yes	0-0h

Register 11-112. 3F8h AMCAM_11 Memory Limit and Base (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Port 11 Memory Base value.	RW	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Port 11 Memory Limit value.	RW	Yes	000h

Register 11-113. 3FCh AMCAM_11 Prefetchable Limit and Memory Base[31:0] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_11 Port 11 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_11 Port 11 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 11-114. 400h AMCAM_11 Prefetchable Memory Base[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_11 Port 11 Prefetchable Memory Base[63:32].	RW	Yes	FFFF_FFFFh

Register 11-115. 404h AMCAM_11 Prefetchable Memory Limit[63:32] (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_11 Port 11 Prefetchable Memory Limit[63:32].	RW	Yes	0-0h

11.13.4 Ingress Control Registers

Table 11-18. PLX-Specific Ingress Control Register Map (Only Ports 0 and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Reserved				664h
Ingress Port Enable				668h

Register 11-116. 660h Ingress Control (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Enable CSR Access by Downstream Devices** **Silicon Revision AA** Enables acceptance of Configuration requests from a Requester that is downstream from a Transparent port, targeting any downstream Transparent port's Type 1 Header registers or NT Port Virtual Interface Type 0 Header registers (*such as* for Peer Configuration access). 0 = Configuration requests from a downstream device that are targeting PEX 8524 registers are ***not supported***; the downstream port flags an Uncorrectable Error, and, returns a Completion with Unsupported Request (UR) specified in the *Completion Status* field, to the downstream Requester. Only this mode is *PCI Express Base r1.0a*-compliant. 1 = The following types of Configuration requests from downstream Requesters are allowed: • Type 0 requests targeting the Type 1 Header registers in that downstream port • Type 1 requests targeting the Type 1 Header registers in other downstream Transparent ports, and • Type 1 requests targeting the Type 0 Header registers in the NT Port Virtual Interface The upstream port registers are not accessible from the downstream port. **Silicon Revisions BB/BC** Enables acceptance of both Configuration and Memory requests from a Requester that is downstream from a Transparent port, targeting any PEX 8524 registers. 0 = Configuration requests from a downstream device are ***not supported***; the downstream port flags an Uncorrectable Error, and, returns a Completion with Unsupported Request (UR) specified in the *Completion Status* field, to the downstream Requester. Only this mode is *PCI Express Base r1.0a*-compliant. 1 = Configuration and Memory requests from downstream Requesters, targeting any PEX 8524 registers in any port, are allowed. ***Note:*** *This bit can be initially set only through the upstream port, the NT Port Link Interface, or serial EEPROM, to enable register access through the downstream Transparent ports; a Requester downstream from a Transparent port cannot set the bit to grant itself (or peers) access to PEX 8524 registers. Configuration requests can access those registers that are defined by PCI-SIG specifications, and generally cannot access device-specific registers other than the NT Port* ***Cursor Mechanism*** *registers. Memory requests can access all PEX 8524 registers.*	RW	Yes	0
1	**Disable Unsupported Request Response for *Reserved* Configuration Registers** 1 = Disables completions with an Unsupported Request (UR) status from being returned when Configuration Writes are attempted on PLX-specific registers	RW	Yes	0

Register 11-116. 660h Ingress Control (Only Ports 0 and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
24:2	***Factory Test Only***	RW	Yes	0-0h
25	***Factory Test Only*** **Silicon Revision AA**	RW	Yes	0
	Disable Upstream Port BAR0 and BAR1 Registers **Silicon Revisions BB/BC** 0 = Enables upstream **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively) 1 = Disables upstream **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively)	RW	Yes	0
26	***Factory Test Only***	RW	Yes	0
27	***Reserved*** **Silicon Revision AA**			0
	BIOS Enumeration Fix Disable **Silicon Revisions BB/BC** For NT Failover in Silicon Revisions BB/BC, this bit must be set.	RW	Yes	0
31:28	***Factory Test Only***	RW	Yes	0h

Register 11-117. 668h Ingress Port Enable (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Ingress Port Enable** The value of this register depends on the number of ports used, which is dependent on the **Port Configuration** register *Port Configuration* field (offset 224h[4:0]) value or STRAP_STN0_PORTCFG[4:0] and STRAP_STN1_PORTCFG[3:0] balls. Set the upper 16 bits to FFFFh. For the lower 16 bits, set each bit position that corresponds to an enabled port. When a port is enabled in the corresponding station configuration, the bit is set to 1; otherwise, the bit is cleared to 0. *For example*: • If Station 0 is configured as x8x4x4, bits [3:0]=0111b • If Station 0 is configured as x16, bits [3:0]=0001b • If Station 0 is configured as x8x8, bits [3:0]=0011b • If Station 0 is configured as x4x4x4x4, bits [3:0]=1111b Table 11-19 provides a sample mapping, based on the Port Configuration value. ***Note:*** *This register in both stations (Ports 0 and 8) must be programmed to the same value, to reflect the configuration of all ports.*	RW	Yes	FFFF_0F0Fh

Table 11-19. PEX 8524 Ingress Port Configurations

Port Configuration Register Value (Port 0 or 8, Offset 224h[4:0])	Lane Width Per Port						Ingress Port Enable Register Value (Port 0 or 8, Offset 668h)
	Station 0		Station 1				
	0	1	8	9	10	11	
0h	x4	x4	x4	x4	x4	x4	FFFF_0F03h
1h			x16[a]				FFFF_0103h
2h	x8		x8	x8			FFFF_0303h
3h			x8	x4	x4		FFFF_0703h
4h			x8	x4	x2	x2	FFFF_0F03h
5h			x8	x2	x2	x4	FFFF_0F03h
6h			x8	x2	x4	x2	FFFF_0F03h

a. Ports 8 and 9 can be combined to create a 16-lane (x16) port.

11.13.5 I/O CAM Base and Limit Upper 16 Bits Registers

Table 11-20. PLX-Specific I/O CAM Base and Limit Upper 16 Bits Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
I/O CAM_0 Limit[31:16] Upper Port 0	I/O CAM_0 Base[31:16] Upper Port 0	680h
I/O CAM_1 Limit[31:16] Upper Port 1	I/O CAM_1 Base[31:16] Upper Port 1	684h
Reserved		688h – 69Ch
I/O CAM_8 Limit[31:16] Upper Port 8	I/O CAM_8 Base[31:16] Upper Port 8	6A0h
I/O CAM_9 Limit[31:16] Upper Port 9	I/O CAM_9 Base[31:16] Upper Port 9	6A4h
I/O CAM_10 Limit[31:16] Upper Port 10	I/O CAM_10 Base[31:16] Upper Port 10	6A8h
I/O CAM_11 Limit[31:16] Upper Port 11	I/O CAM_11 Base[31:16] Upper Port 11	6ACh
Reserved		6B0h – 6BCh

Register 11-118. 680h I/OCAM_0 Upper Port 0 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/OCAM Base[31:16]** I/O Base Upper 16 bits.	RW	Yes	FFFFh
31:16	**I/OCAM Limit[31:16]** I/O Limit Upper 16 bits.	RW	Yes	0000h

Register 11-119. 684h I/OCAM_1 Upper Port 1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/OCAM Base[31:16]** I/O Base Upper 16 bits.	RW	Yes	FFFFh
31:16	**I/OCAM Limit[31:16]** I/O Limit Upper 16 bits.	RW	Yes	0000h

Register 11-120. 6A0h I/OCAM_8 Upper Port 8 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/OCAM Base[31:16]** I/O Base Upper 16 bits.	RW	Yes	FFFFh
31:16	**I/OCAM Limit[31:16]** I/O Limit Upper 16 bits.	RW	Yes	0000h

Register 11-121. 6A4h I/OCAM_9 Upper Port 9 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/OCAM Base[31:16]** I/O Base Upper 16 bits.	RW	Yes	FFFFh
31:16	**I/OCAM Limit[31:16]** I/O Limit Upper 16 bits.	RW	Yes	0000h

Register 11-122. 6A8h I/OCAM_10 Upper Port 10 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/OCAM Base[31:16]** I/O Base Upper 16 bits.	RW	Yes	FFFFh
31:16	**I/OCAM Limit[31:16]** I/O Limit Upper 16 bits.	RW	Yes	0000h

Register 11-123. 6ACh I/OCAM_11 Upper Port 11 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/OCAM Base[31:16]** I/O Base Upper 16 bits.	RW	Yes	FFFFh
31:16	**I/OCAM Limit[31:16]** I/O Limit Upper 16 bits.	RW	Yes	0000h

11.13.6 Base Address Registers (BARs)

The registers defined in Table 11-21 contain a shadow copy of the two Type 1 Configuration Base Address registers for each PEX 8524 port.

Table 11-21. PLX-Specific Base Address Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
BAR0 for Port 0		6C0h
BAR1 for Port 0		6C4h
BAR0 for Port 1		6C8h
BAR1 for Port 1		6CCh
Reserved		6D0h – 6FCh
BAR0 for Port 8		700h
BAR1 for Port 8		704h
BAR0 for Port 9		708h
BAR1 for Port 9		70Ch
BAR0 for Port 10		710h
BAR1 for Port 10		714h
BAR0 for Port 11		718h
BAR1 for Port 11		71Ch
Reserved		720h – 73Ch

Register 11-124. 6C0h BAR0 for Port 0 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping_0 Range** Memory Mapping for Port 0. 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	RW	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores writes.	RO	Yes	0
15:4	***Reserved***			000h
31:16	**Base Address_0** Shadow copy of Base Address 0 for Port 0. Where **BAR0**[15:4] = ***Reserved***.	RW	Yes	0000h

Register 11-125. 6C4h BAR1 for Port 0 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When Port 0 **BAR0**[2:1] = 10b, becomes a Shadow copy of Port 0 **Base Address_1**[63:32].	RW	Yes	0000_0000h

Register 11-126. 6C8h BAR0 for Port 1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping_1 Range** Memory Mapping for Port 1. 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	RW	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores writes.	RO	Yes	0
15:4	***Reserved***			000h
31:16	Shadow copy of Base Address 0 for Port 1. Where **BAR0**[15:4] = ***Reserved***.	RW	Yes	0000h

Register 11-127. 6CCh BAR1 for Port 1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When Port 1 **BAR0**[2:1] = 10b, becomes a Shadow copy of Port 1 **Base Address_1**[63:32].	RW	Yes	0000_0000h

Register 11-128. 700h BAR0 for Port 8 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping_8 Range** Memory Mapping for Port 8. 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	RW	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores writes.	RO	Yes	0
15:4	***Reserved***			000h
31:16	**Base Address_0** Shadow copy of Base Address 0 for Port 8. Where **BAR0**[15:4] = ***Reserved***.	RW	Yes	0000h

Register 11-129. 704h BAR1 for Port 8 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When Port 8 **BAR0**[2:1] = 10b, becomes a Shadow copy of Port 8 **Base Address_1**[63:32].	RW	Yes	0000_0000h

Register 11-130. 708h BAR0 for Port 9 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping_9 Range** Memory Mapping for Port 9. 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	RW	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores writes.	RO	Yes	0
15:4	***Reserved***			000h
31:16	**Base Address_0** Shadow copy of Base Address 0 for Port 9. Where **BAR0**[15:4] = ***Reserved***.	RW	Yes	0000h

Register 11-131. 70Ch BAR1 for Port 9 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When Port 9 **BAR0**[2:1] = 10b, becomes a Shadow copy of Port 9 **Base Address_1**[63:32].	RW	Yes	0-0h

Register 11-132. 710h BAR0 for Port 10 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping_10 Range** Memory Mapping for Port 10. 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	RW	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores writes.	RO	Yes	0
15:4	***Reserved***			000h
31:16	**Base Address_0** Shadow copy of Base Address 0 for Port 10. Where **BAR0**[15:4] = ***Reserved***.	RW	Yes	0000h

Register 11-133. 714h BAR1 for Port 10 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When Port 10 **BAR0**[2:1] = 10b, becomes a Shadow copy of Port 10 **Base Address_1**[63:32].	RW	Yes	0-0h

Register 11-134. 718h BAR0 for Port 11 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping_11 Range** Memory Mapping for Port 11. 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	RW	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores writes.	RO	Yes	0
15:4	***Reserved***			000h
31:16	**Base Address_0** Shadow copy of Base Address 0 for Port 11. Where **BAR0**[15:4] = ***Reserved***.	RW	Yes	0000h

Register 11-135. 71Ch BAR1 for Port 11 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When Port 11 **BAR0**[2:1] = 10b, becomes a Shadow copy of Port 11 **Base Address_1**[63:32].	RW	Yes	0-0h

11.13.7 Shadow Virtual Channel (VC) Capability Registers

Table 11-22. PLX-Specific Shadow Virtual Channel (VC) Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
VC0 Port 0 Capability				740h
VC1 Port 0 Capability				744h
VC0 Port 1 Capability				748h
VC1 Port 1 Capability				74Ch
Reserved				750h – 77Ch
VC0 Port 8 Capability				780h
VC1 Port 8 Capability				784h
VC0 Port 9 Capability				788h
VC1 Port 9 Capability				78Ch
VC0 Port 10 Capability				790h
VC1 Port 10 Capability				794h
VC0 Port 11 Capability				798h
VC1 Port 11 Capability				79Ch
Reserved				7A0h – 83Ch
Port 0 VC Capability_1				840h
Port 1 VC Capability_1				844h
Reserved				848h – 85Ch
Port 8 VC Capability_1				860h
Port 9 VC Capability_1				864h
Port 10 VC Capability_1				868h
Port 11 VC Capability_1				86Ch
Reserved				870h – 9ECh

Register 11-136. 740h VC0 Port 0 Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC_VC0_0 Map[0]** Always mapped to Virtual Channel 0. Reads 1, and ignores writes.	RO	Yes	1
7:1	**TC_VC0_0 Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when assigning traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			000h
24	**VC0_0 ID** Port 0 Virtual Channel 0 ID.	RO	Yes	0
30:25	***Reserved***			00h
31	**VC0_0 Enable** Port 0 Virtual Channel 0 Enable.	RO	Yes	1

Register 11-137. 744h VC1 Port 0 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
7:1	**TC_VC1_0 Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***			000h
24	**VC1_0 ID** Port 0 Virtual Channel 1 ID.	RW	Yes	1
30:25	***Reserved***			000h
31	**VC1_0 Enable** Port 0 Virtual Channel 1 Enable.	RW	Yes	0

Register 11-138. 748h VC0 Port 1 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC_VC0_1 Map[0]** Always mapped to Virtual Channel 0. Reads 1, and ignores writes.	RO	Yes	1
7:1	**TC_VC0_1 Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			000h
24	**VC0_1 ID** Port 1 Virtual Channel 0 ID.	RO	Yes	0
30:25	***Reserved***			000h
31	**VC0_1 Enable** Port 1 Virtual Channel 0 Enable.	RO	Yes	1

Register 11-139. 74Ch VC1 Port 1 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
7:1	**TC_VC1_1 Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***			000h
24	**VC1_1 ID** Port 1 Virtual Channel 1 ID.	RW	Yes	1
30:25	***Reserved***			000h
31	**VC1_1 Enable** Port 1 Virtual Channel 1 Enable.	RW	Yes	0

Register 11-140. 780h VC0 Port 8 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC_VC0_8 Map[0]** Always mapped to Virtual Channel 0. Reads 1, and ignores writes.	RO	Yes	1
7:1	**TC_VC0_8 Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			000h
24	**VC0_8 ID** Port 8 Virtual Channel 0 ID.	RO	Yes	0
30:25	***Reserved***			000h
31	**VC0_8 Enable** Port 8 Virtual Channel 0 Enable.	RO	Yes	1

Register 11-141. 784h VC1 Port 8 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
7:1	**TC_VC1_8 Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***			000h
24	**VC1_8 ID** Port 8 Virtual Channel 1 ID.	RW	Yes	1
30:25	***Reserved***			000h
31	**VC1_8 Enable** Port 8 Virtual Channel 1 Enable.	RW	Yes	0

Register 11-142. 788h VC0 Port 9 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC_VC0_9 Map[0]** Always mapped to Virtual Channel 0. Reads 1, and ignores writes.	RO	Yes	1
7:1	**TC_VC0_9 Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			000h
24	**VC0_9 ID** Port 9 Virtual Channel 0 ID.	RO	Yes	0
30:25	***Reserved***			000h
31	**VC0_9 Enable** Port 9 Virtual Channel 0 Enable.	RO	Yes	1

Register 11-143. 78Ch VC1 Port 9 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
7:1	**TC_VC1_9 Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***			000h
24	**VC1_9 ID** Port 9 Virtual Channel 1 ID.	RW	Yes	1
30:25	***Reserved***			000h
31	**VC1_9 Enable** Port 9 Virtual Channel 1 Enable.	RW	Yes	0

Register 11-144. 790h VC0 Port 10 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC_VC0_10 Map[0]** Always mapped to Virtual Channel 0. Reads 1, and ignores writes.	RO	Yes	1
7:1	**TC_VC0_10 Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			000h
24	**VC0_10 ID** Port 10 Virtual Channel 0 ID.	RO	Yes	0
30:25	***Reserved***			000h
31	**VC0_10 Enable** Port 10 Virtual Channel 0 Enable.	RO	Yes	1

Register 11-145. 794h VC1 Port 10 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
7:1	**TC_VC1_10 Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***			000h
24	**VC1_10 ID** Port 10 Virtual Channel 1 ID.	RW	Yes	1
30:25	***Reserved***			000h
31	**VC1_10 Enable** Port 10 Virtual Channel 1 Enable.	RW	Yes	0

Register 11-146. 798h VC0 Port 11 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC_VC0_11 Map[0]** Always mapped to Virtual Channel 0. Reads 1, and ignores writes.	RO	Yes	1
7:1	**TC_VC0_11 Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			000h
24	**VC0_11 ID** Port 11 Virtual Channel 0 ID.	RO	Yes	0
30:25	***Reserved***			000h
31	**VC0_11 Enable** Port 11 Virtual Channel 0 Enable.	RO	Yes	1

Register 11-147. 79Ch VC1 Port 11 Capability (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
7:1	**TC_VC1_11 Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***			000h
24	**VC1_11 ID** Port 11 Virtual Channel 1 ID.	RW	Yes	1
30:25	***Reserved***			000h
31	**VC1_11 Enable** Port 11 Virtual Channel 1 Enable.	RW	Yes	0

Register 11-148. 840h Port 0 VC Capability_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
4	**Low-Priority Extended VC Count** Low-priority Virtual Channel count.	RW	Yes	0
31:5	***Reserved***			0-0h

Register 11-149. 844h Port 1 VC Capability_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
4	**Low-Priority Extended VC Count** Low-priority Virtual Channel count.	RW	Yes	0
31:5	***Reserved***			0-0h

Register 11-150. 860h Port 8 VC Capability_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
4	**Low-Priority Extended VC Count** Low-priority Virtual Channel count.	RW	Yes	0
31:5	***Reserved***			0-0h

Register 11-151. 864h Port 9 VC Capability_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
4	**Low-Priority Extended VC Count** Low-priority Virtual Channel count.	RW	Yes	0
31:5	***Reserved***			0-0h

Register 11-152. 868h Port 10 VC Capability_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
4	**Low-Priority Extended VC Count** Low-priority Virtual Channel count.	RW	Yes	0
31:5	***Reserved***			0-0h

Register 11-153. 86Ch Port 11 VC Capability_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
4	**Low-Priority Extended VC Count** Low-priority Virtual Channel count.	RW	Yes	0
31:5	***Reserved***			0-0h

11.13.8 Ingress Credit Handler (INCH) Registers

Changing credits values from default register values must be done carefully. Credits must be programmed properly, otherwise the device will not function as expected. Also, there are minimal required Header credits for all the flows, which are required to achieve reasonable performance. (Refer to *the PEX 85XX EEPROM – PEX 8532/8524/8516 Design Note*, Section 6.9, "Internal Credit Handler VCnT Threshold Registers," for details.) The minimum initial Payload credits for Posted and Completions must exceed the required credits for a Maximum Payload Size TLP by 8.

Table 11-23. PLX-Specific Ingress Credit Handler (INCH) Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				9F0h
INCH FC Update Pending Timer				9F4h
Reserved				9F8h
Reserved		INCH Mode		9FCh
INCH Threshold Port 0 or 8 VC0 Posted				A00h
INCH Threshold Port 0 or 8 VC0 Non-Posted				A04h
INCH Threshold Port 0 or 8 VC0 Completion				A08h
INCH Threshold Port 0 or 8 VC1 Posted				A0Ch
INCH Threshold Port 0 or 8 VC1 Non-Posted				A10h
INCH Threshold Port 0 or 8 VC1 Completion				A14h
INCH Threshold Port 1 or 9 VC0 Posted				A18h
INCH Threshold Port 1 or 9 VC0 Non-Posted				A1Ch
INCH Threshold Port 1 or 9 VC0 Completion				A20h
INCH Threshold Port 1 or 9 VC1 Posted				A24h
INCH Threshold Port 1 or 9 VC1 Non-Posted				A28h
INCH Threshold Port 1 or 9 VC1 Completion				A2Ch
INCH Threshold Port 10 VC0 Posted				A30h
INCH Threshold Port 10 VC0 Non-Posted				A34h
INCH Threshold Port 10 VC0 Completion				A38h
INCH Threshold Port 10 VC1 Posted				A3Ch
INCH Threshold Port 10 VC1 Non-Posted				A40h
INCH Threshold Port 10 VC1 Completion				A44h
INCH Threshold Port 11 VC0 Posted				A48h
INCH Threshold Port 11 VC0 Non-Posted				A4Ch
INCH Threshold Port 11 VC0 Completion				A50h
INCH Threshold Port 11 VC1 Posted				A54h
INCH Threshold Port 11 VC1 Non-Posted				A58h
INCH Threshold Port 11 VC1 Completion				A5Ch
Reserved				AC0h – B7Ch

Register 11-154. 9F4h INCH FC Update Pending Timer (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Port 0 or 8 Update Timer** Update Pending Timer for Port 0 or 8. Port 0 copy controls Port 0, and Port 8 copy controls Port 8. (Refer to Table 11-24.) For implementation, a value of 01h or 00h into the CSR results in waiting 255 symbol times. Values are automatically set at reset according to the **Device Control** register Maximum Payload Size (offset 70h[7:5]) and **Link Status** register Negotiated Link Width (offset 78h[25:20]) fields. Programmable by serial EEPROM if the associated **INCH Mode** register *Pending Timer Source* bit (offset 9FCh[20]) is set.	RW	Yes	00h
15:8	**Port 1 or 9 Update Timer** Update Pending Timer for Port 1 or 9. Port 1 copy controls Port 1, and Port 9 copy controls Port 9. (Refer to Table 11-24.) For implementation, a value of 01h or 00h into the CSR results in waiting 255 symbol times. Values are automatically set at reset according to the **Device Control** register *Maximum Payload Size* (offset 70h[7:5]) and **Link Status** register *Negotiated Link Width* (offset 78h[25:20]) fields. Programmable by serial EEPROM if the associated **INCH Mode** register *Pending Timer Source* bit (offset 9FCh[21]) is set.	RW	Yes	00h
23:16	**Port 10 Update Timer** Update Pending Timer for Port 10. ***Reserved*** for Station 0. (Refer to Table 11-24.) For implementation, a value of 01h or 00h into the CSR results in waiting 255 symbol times. Values are automatically set at reset according to the **Device Control** register *Maximum Payload Size* (offset 70h[7:5]) and **Link Status** register *Negotiated Link Width* (offset 78h[25:20]) fields. Programmable by serial EEPROM if the associated **INCH Mode** register *Pending Timer Source* bit (offset 9FCh[22]) is set.	RW	Yes	00h
31:24	**Port 11 Update Timer** Update Pending Timer for Port 11. ***Reserved*** for Station 0. (Refer to Table 11-24.) For implementation, a value of 01h or 00h into the CSR results in waiting 255 symbol times. Values are automatically set at reset according to the **Device Control** register *Maximum Payload Size* (offset 70h[7:5]) and **Link Status** register *Negotiated Link Width* (offset 78h[25:20]) fields. Programmable by serial EEPROM if the associated **INCH Mode** register *Pending Timer Source* bit (offset 9FCh[23]) is set.	RW	Yes	00h

Table 11-24. FC Update Pending Timer Guidelines

Maximum Packet Size	Link Width	Recommended Timer Count
128 bytes	x1	76h
	x2	40h
	x4	24h
	x8	21h
	x16 (Station 1 only)	18h
256 bytes	x1	D0h
	x2	6Ch
	x4	3Bh
	x8	36h
	x16 (Station 1 only)	24h

Register 11-155. 9FCh INCH Mode (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Maximum Mode Enable** ***Factory Test Only***	RO	Yes	FFh
15:8	***Reserved***			0h
19:16	***Factory Test Only***	RW	Yes	0h
23:20	**Pending Timer Source** 0 = **INCH FC Update Pending Timer** register (offset 9F4h) uses default value 1 = **INCH FC Update Pending Timer** register (offset 9F4h) uses serial EEPROM value **Bit** / **Port 0** / **Port 8** 20 / Port 0 Pending Timer Source / Port 8 Pending Timer Source 21 / Port 1 Pending Timer Source / Port 9 Pending Timer Source 22 / ***Reserved*** / Port 10 Pending Timer Source 23 / ***Reserved*** / Port 11 Pending Timer Source	RW	Yes	0-0h
31:24	***Reserved***			00h

11.13.8.1 INCH Threshold Port Virtual Channel Registers

There are six Ingress Credit Handler (INCH) Threshold Port VC registers, which are duplicated for each port. These registers represent the maximum number of headers or payload credits allocated per port, virtual channel, and type. The register names and address/location are defined in Table 11-23. The following registers describe the data that applies to these registers.

Register 11-156. A00h, A18h, A30h, A48h INCH Threshold Port *n* VC0 Posted (Only Ports 0 and 8, where *n* = 0 through 1 for Station 0 ports, and *n* = 8 through 11 for Station 1 ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Posted credits are used for Virtual Channel 0 (VC0) Memory Write and Message transactions.				
2:0	***Reserved***			AA – 0A58h BB/BC – 1890h
8:3	**Payload** ***Reserved*** bits [2:0] force the Payload Credits to be a multiple of 8. Minimum value = Maximum Payload Size (MPS; encoded in offset 70h[7:5]) divided by 16, rounded up to a multiple of 8. Minimum value for 256 MPS is 0_0001_0b; otherwise, the minimum value is 0_0000_1b. **Silicon Revision AA** Payload = 0_0101_1b = Bh, shifted left 3 bits is 58h = 88 Payload Credits (1,408 bytes). **Silicon Revisions BB/BC** Payload = 0_1001_0b = 12h, shifted left 3 bits is 90h = 144 Payload Credits (2,304 bytes).	RW	Yes	
13:9	**Header** Minimum value = 00_001b. **Silicon Revision AA** Header = 00_101b = 5h = 5 Header Credits. **Silicon Revisions BB/BC** Header = 01_100b = Ch = 12 Header Credits.			
31:14	***Reserved***			0-0h

Register 11-157. A04h, A1Ch, A34h, A4Ch INCH Threshold Port *n* VC0 Non-Posted (Only Ports 0 and 8, where *n* = 0 through 1 for Station 0 ports, and *n* = 8 through 11 for Station 1 ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Non-Posted credits are used for Virtual Channel 0 (VC0) Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions.				
8:0	**Payload** Minimum value = 0_0000_0001b. **Silicon Revision AA** Payload = 0_0000_1001b = 9 Payload Credits (144 bytes). **Silicon Revisions BB/BC** Payload = 0_0000_0111b = 7 Payload Credits (112 bytes).	RW	Yes	AA – 1209h BB/BC – 0E07h
13:9	**Header** Minimum value = 00_001b. **Silicon Revision AA** Header = 01_001b = 9 Header Credits. **Silicon Revisions BB/BC** Header = 00_111b = 7 Header Credits.			
31:14	***Reserved***			0-0h

Register 11-158. A08h, A20h, A38h, A50h INCH Threshold Port *n* VC0 Completion (Only Ports 0 and 8, where *n* = 0 through 1 for Station 0 ports, and *n* = 8 through 11 for Station 1 ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Completion credits are used for Virtual Channel 0 (VC0) Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions.				
2:0	***Reserved***			AA – 0A58h BB/BC – 1480h
8:3	**Payload** ***Reserved*** bits [2:0] force the Payload Credits to be a multiple of 8. Minimum value = Maximum Payload Size (MPS; encoded in offset 70h[7:5]) or size of largest Read request (whichever is smaller), divided by 16, rounded up to a multiple of 8. Minimum value for MPS or largest Read request greater than 128 bytes is 0_0001_0b; otherwise, the minimum value is 0_0000_1b. **Silicon Revision AA** Payload = 0_0101_1b = Bh, shifted left 3 bits is 58h = 88 Payload Credits (1,408 bytes). **Silicon Revisions BB/BC** Payload = 0_1000_0b = 10h, shifted left 3 bits is 00h = 128 Payload Credits (2,048 bytes).	RW	Yes	
13:9	**Header** Minimum value = 00_001b. **Silicon Revision AA** Header = 00_101b = 5h = 5 Header Credits. **Silicon Revisions BB/BC** Header = 01_010b = Ah = 10 Header Credits.			
31:14	***Reserved***			0-0h

Register 11-159. A0Ch, A24h, A3Ch, A54h INCH Threshold Port *n* VC1 Posted (Only Ports 0 and 8, where *n* = 0 through 1 for Station 0 ports, and *n* = 8 through 11 for Station 1 ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Posted credits are used for Virtual Channel 1 (VC1) Memory Write and Message transactions. A port does not advertise VC1 credits unless its VC1 is enabled, by setting the port's **VC1 Resource Control** register *VC1 Enable* bit (offset 168h[31]=1).				
2:0	***Reserved***			210h
8:3	**Payload** Payload = 0_0001_0b = 2h, shifted left 3 bits to be a multiple of 8, for 10h = 16 Payload Credits (256 bytes).	RW	Yes	
13:9	**Header** Header = 00_001b = 1 Header Credit.			
31:14	***Reserved***			0-0h

Register 11-160. A10h, A28h, A40h, A58h INCH Threshold Port *n* VC1 Non-Posted (Only Ports 0 and 8, where *n* = 0 through 1 for Station 0 ports, and *n* = 8 through 11 for Station 1 ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Non-Posted credits are used for Virtual Channel 1 (VC1) Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions. A port does not advertise VC1 credits unless its VC1 is enabled, by setting the port's **VC1 Resource Control** register *VC1 Enable* bit (offset 168h[31]=1).				
8:0	**Payload** Payload = 0_0000_0001b = 1 Payload Credit (112 bytes).	RW	Yes	0201h
13:9	**Header** Header = 00_001b = 1 Header Credit.			
31:14	***Reserved***			0-0h

Register 11-161. A14h, A2Ch, A44h, A5Ch INCH Threshold Port *n* VC1 Completion (Only Ports 0 and 8, where *n* = 0 through 1 for Station 0 ports, and *n* = 8 through 11 for Station 1 ports)

Bit(s)	Description	Type	Serial EEPROM	Default
Completion credits are used for Virtual Channel 1 (VC1) Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions. A port does not advertise VC1 credits unless its VC1 is enabled, by setting the port's **VC1 Resource Control** register *VC1 Enable* bit (offset 168h[31]=1).				
2:0	***Reserved***			210h
8:3	**Payload** Payload = 0_0001_0b = 2h, shifted left 3 bits to be a multiple of 8, for 10h = 16 Payload Credits (256 bytes).	RW	Yes	
13:9	**Header** Header = 00_001b = 1 Header Credit.			
31:14	***Reserved***			0-0h

11.13.9 Ingress One-Bit ECC Error Count Register

Table 11-25. PLX-Specific Ingress One-Bit ECC Error Count Register Map (Only Ports 0 and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress One-Bit ECC Error Count		***Reserved***		BE8h

Register 11-162. BE8h Ingress One-Bit ECC Error Count (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	***Reserved***			0000h
23:16	**Ingress Packet RAM 1-Bit ECC Count** Record number of 1-bit Correctable errors that occurred in Ingress RAM. Counter increments for each 1-bit Soft error detected in RAM.	RO	No	00h
31:24	**Ingress Pointer Linked List RAM 1-Bit ECC Count** Record number of 1-bit Correctable errors that occurred in the Ingress Pointer Linked List RAM. Counter increments for each 1-bit Soft error detected in RAM.	RO	No	00h

11.13.10 Relaxed Completion Ordering (Ingress) Register – Silicon Revisions BB/BC Only

Table 11-26. PLX-Specific Relaxed Completion Ordering (Ingress) Register Map (Only Ports 0 and 8, Silicon Revisions BB/BC Only)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PLX-Specific Relaxed Completion Ordering (Ingress)				BECh

Register 11-163. BECh PLX-Specific Relaxed Completion Ordering (Ingress) (Only Ports 0 and 8, Silicon Revisions BB/BC Only)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Enable PLX-Specific Relaxed Completion Ordering** **Silicon Revision AA** ***Not supported*** **Silicon Revisions BB/BC** Enables PLX-Specific Relaxed Completion Ordering on ingress ports identified by the **PLX-Specific Relaxed Ordering Mode (Ingress)** register (offset BFCh).	RW	Yes	0
31:1	***Reserved***			0-0h

11.13.11 Relaxed Ordering Mode (Ingress) Register

Table 11-27. PLX-Specific Relaxed Ordering Mode (Ingress) Register Map (Only Ports 0 and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				BF0h – BF8h
PLX-Specific Relaxed Ordering Mode (Ingress)				BFCh

Register 11-164. BFCh PLX-Specific Relaxed Ordering Mode (Ingress) (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Enable_RLX_Ordering Port 0 or 8** When any of these bits are set, the corresponding Traffic Class for this port allows PLX-Specific Relaxed Ordering on Port 0 or 8.	RW	Yes	00h
15:8	**Enable_RLX_Ordering Port 1 or 9** When any of these bits are set, the corresponding Traffic Class for this port allows PLX-Specific Relaxed Ordering on Port 1 or 9.	RW	Yes	00h
23:16	**Enable_RLX_Ordering Port 10** When any of these bits are set, the corresponding Traffic Class for this port allows PLX-Specific Relaxed Ordering on Port 10. ***Reserved*** for Station 0.	RW	Yes	00h
31:24	**Enable_RLX_Ordering Port 11** When any of these bits are set, the corresponding Traffic Class for this port allows PLX-Specific Relaxed Ordering on Port 11. ***Reserved*** for Station 0.	RW	Yes	00h

11.13.12 Internal Credit Handler (ITCH) VC&T Threshold Registers

The ITCH Virtual Channel (VC) and Type [P (Posted), NP (Non-Posted), and Cpl (Completion)] (VC&T) Threshold registers in each station define internal credits and mechanisms that are used to prevent Egress Packet RAM (containing outgoing packets to be transmitted by ports in a station) from being overflowed by packets from the Ingress Packet RAM (containing incoming packets received by ports in a station). The Egress Packet RAM can become filled due to lack of ingress credits from the external device, or insufficient bandwidth to transmit packets as fast as they arrive. The internal mechanisms prevent overflow by applying backpressure from the Egress RAM to the Ingress ports (and ultimately to external devices by withholding additional Ingress Credits).

Table 11-28 defines the ITCH VC&T (Virtual Channel Threshold register map.

Table 11-28. PEX 8524 PLX-Specific Internal Credit Handler (ITCH) VC&T Threshold Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
ITCH VC&T Threshold_1				C00h
ITCH VC&T Threshold_2				C04h
ITCH VC&T Threshold_3				C08h

The PEX 8524 uses one of two backpressure mechanisms, depending on the ITCH VC&T register values:

- **Deadlock Avoidance mode** (Silicon Revisions AA, BB, and BC) – Enabled as the default backpressure mode, when the ITCH VC&T values are the default register values (in which the Threshold values do not correspond to physical locations within the Egress Packet RAM). In Deadlock Avoidance mode, once the switch port's Egress queue fills to 75% of capacity, the switch gives priority to Posted traffic, to avoid deadlock.

  PEX 8524 Silicon Revisions AA, BA and BB should operate in Deadlock Avoidance mode, with the ITCH VC&T registers programmed only to default register values, unless Threshold mode is needed to resolve a Requester Completion Timeout issue in applications where Completions are delayed when Deadlock Avoidance mode activates (due to the Egress Packet RAM becoming more than 75% full).

- **Threshold mode** (Silicon Revision BC only) – Enabled when the ITCH VC&T registers are programmed to non-default Packet Count values. The non-default register values effectively partition the Egress RAM into separate sections for Posted, Non-Posted and/or Completion packets.

  In Threshold mode, if the Egress Packet RAM fills with packets of a particular VC&T beyond the programmed Upper Packet Count value for that VC&T, internal forwarding of additional packets of that VC&T from Ingress Packet RAM to Egress Packet RAM is halted. When sufficient packets of that same VC&T are emptied from the Egress Packet RAM (by the Egress ports in the Station) such that the Egress Packet RAM contains fewer packets of that VC&T than the programmed Lower Packet Count for that VC&T, internal forwarding of packets (of that same VC&T) to Egress Packet RAM from Ingress Packet RAM resumes.

Note: *Previously scheduled packets arrive in their entirety, completely unaffected by the cut-off signal.*

All ports in a station share the Egress Packet RAM, as well as the same **ITCH VC&T Threshold** register values; therefore, the **ITCH VC&T Threshold** register values allocate the RAM equally among all enabled ports within the station.

While Deadlock Avoidance mode can allow blocking of Completion packets if the Egress Packet RAM fills to 75% of capacity, recommended register values for Threshold mode allow Completion packets to potentially make comparatively further forward progress (than in Deadlock Avoidance mode). Therefore, for applications that can potentially experience congestion within the Egress Packet RAM, Threshold mode is recommended for PEX 8524 Silicon Revision BC, to reduce the possibility of Completion Timeout (by a Requester of Read requests).

Generally, it is sufficient to program only the Posted Packet Counts, and leave the Non-Posted and Completion Packet Counts at default values. Programming only the Posted Packet Counts prevents clogging of the Egress RAM for any combination of packets, allowing Non-Posted and Completion transactions to make forward progress from the Ingress Packet RAM into the Egress Packet RAM, regardless of whether the Egress Packet RAM is filled with Posted packets.

For calculating **ITCH VC&T Threshold** register values, each station contains 40,960 bytes of Egress Packet RAM, structured as 2,048, 20-byte beats, and each unit in the **ITCH VC&T Threshold** register values corresponds to eight, 20-byte beats. Therefore, a programmed value of 1 represents 160 bytes, 2 is 320 bytes, and so forth. The entire TLP (Header, Payload, and ECRC, if any) is used to determine a total byte size, and the total byte size is divided by 20 and rounded up to the nearest integer to ascertain the number of beats.

Recommended register values for Threshold mode are based upon the number of ports enabled in a station (as configured in the **Port Configuration** register, offset 224h). A port is considered enabled, regardless of whether it is used. The number of enabled ports is usually the same as the **Physical Layer Status** register *Number of Ports Enumerated* field (offset 220h[22:20]), which the PEX 8524 automatically updates after a reset.

Table 11-29 lists the recommended Posted Upper Packet Count values (for offset C00h[7:0] for VC0, and offset C04h[23:16] for VC1).

The Posted Lower Packet Count values must be at least 5 or 6 less than the Posted Upper Packet Count. Table 11-30 lists the recommended Posted Lower Packet Count values (for offset C00h[15:8] for VC0, and offset C04h[31:24] for VC1), which are 12 less than the Posted Upper Packet Count.

Table 11-29. ITCH VC&T Posted Upper Packet Count

Number of Enabled Ports	Port Configuration Register Value (Port 0 or 8, Offset 224h[4:0])	VC0 Value (Offset C00h[7:0]) VC1 Value (Offset C04h[23:16])
1	1h	EEh
2	2h	6Eh
3	3h	43h
4	0h, 4h, 5h, 6h	2Eh

Table 11-30. ITCH VC&T Posted Lower Packet Count

Number of Enabled Ports	Port Configuration Register Value (Port 0 or 8, Offset 224h[4:0])	VC0 Value (Offset C00h[15:8]) VC1 Value (Offset C04h[31:24])
1	1h	E2h
2	2h	62h
3	3h	37h
4	0h, 4h, 5h, 6h	22h

Register 11-165. C00h ITCH VC&T Threshold_1 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**VC0 Posted Upper Packet Count** VC0 posted upper packet beat limit.	RW	Yes	FFh
15:8	**VC0 Posted Lower Packet Count** VC0 posted lower packet beat limit.	RW	Yes	7Fh
23:16	**VC0 Non-Posted Upper Packet Count** VC0 non-posted upper packet beat limit.	RW	Yes	FFh
31:24	**VC0 Non-Posted Lower Packet Count** VC0 non-posted lower packet beat limit.	RW	Yes	7Fh

Register 11-166. C04h ITCH VC&T Threshold_2 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**VC0 Completion Upper Packet Count** VC0 completion upper packet beat limit.	RW	Yes	FFh
15:8	**VC0 Completion Lower Packet Count** VC0 completion lower packet beat limit.	RW	Yes	7Fh
23:16	**VC1 Posted Upper Packet Count** VC1 posted upper packet beat limit.	RW	Yes	FFh
31:24	**VC1 Posted Lower Packet Count** VC1 posted lower packet beat limit.	RW	Yes	7Fh

Register 11-167. C08h ITCH VC&T Threshold_3 (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**VC1 Non-Posted Upper Packet Count** VC1 non-posted upper packet beat limit.	RW	Yes	FFh
15:8	**VC1 Non-Posted Lower Packet Count** VC1 non-posted lower packet beat limit.	RW	Yes	7Fh
23:16	**VC1 Completion Upper Packet Count** VC1 completion upper packet beat limit.	RW	Yes	FFh
31:24	**VC1 Completion Lower Packet Count** VC1 completion lower packet beat limit.	RW	Yes	7Fh

11.14 Advanced Error Reporting Capability Registers

Table 11-31. Advanced Error Reporting Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log_0		FD0h
Header Log_1		FD4h
Header Log_2		FD8h
Header Log_3		FDCh
Reserved		FE0h – FFCh

Register 11-168. FB4h PCI Express Enhanced Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**PCI Express Extended Capability ID**	RO	Yes	0001h
19:16	**Capability Version**	RO	Yes	1h
31:20	**Next Capability Offset**	RO	Yes	138h

Register 11-169. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Training Error Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
3:1	***Reserved***			000b
4	**Data Link Protocol Error Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
11:5	***Reserved***			0000_000b
12	**Poisoned TLP Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
13	***Reserved***	RW1CS	Yes	0
14	***Reserved*** ***Note:*** *Bit 14 is not applicable to switches; therefore, the PCI Express Base r1.0a provides exemption from supporting this bit.*			0
15	**Completer Abort Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
16	***Reserved***	RW1CS	Yes	0
17	**Receiver Overflow Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
18	**Malformed TLP Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
19	**ECRC Error Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
20	**Unsupported Request Error Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
31:21	***Reserved***			0-0h

Register 11-170. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Training Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
3:1	***Reserved***			000b
4	**Data Link Protocol Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
11:5	***Reserved***			0000_000b
12	**Poisoned TLP Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
13	***Reserved***	RWS	Yes	0
14	***Reserved*** ***Note:*** *Bit 14 is not applicable to switches; therefore, the PCI Express Base r1.0a provides exemption from supporting this bit.*			0
15	**Completer Abort Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
16	***Reserved***	RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
19	**ECRC Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and header logging are masked for this error	RWS	Yes	0
31:21	***Reserved***			0-0h

Register 11-171. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Training Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	1
3:1	***Reserved***			000b
4	**Data Link Protocol Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	1
11:5	***Reserved***			0-0h
12	**Poisoned TLP Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	0
13	***Reserved***	RWS	Yes	1
14	***Reserved*** ***Note:*** *Bit 14 is not applicable to switches; therefore, the PCI Express Base r1.0a provides exemption from supporting this bit.*			0
15	**Completer Abort Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	0
16	***Reserved***	RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	1
19	**ECRC Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	0
20	**Unsupported Request Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	RWS	Yes	0
31:21	***Reserved***			0-0h

Register 11-172. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Receiver Error Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
5:1	***Reserved***			0-0h
6	**Bad TLP Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
7	**Bad DLLP Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
8	**Replay Number Rollover Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
11:9	***Reserved***			000b
12	**Replay Timer Timeout Status** 0 = No error detected 1 = Error detected	RW1CS	Yes	0
31:13	***Reserved***			0-0h

Register 11-173. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Receiver Error Mask** 0 = Error reporting not masked 1 = Error reporting masked	RWS	Yes	0
5:1	***Reserved***			0-0h
6	**Bad TLP Mask** 0 = Error reporting not masked 1 = Error reporting masked	RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting not masked 1 = Error reporting masked	RWS	Yes	0
8	**Replay Number Rollover Mask** 0 = Error reporting not masked 1 = Error reporting masked	RWS	Yes	0
11:9	***Reserved***			000b
12	**Replay Timer Timeout Mask** 0 = Error reporting not masked 1 = Error reporting masked	RWS	Yes	0
31:13	***Reserved***			0-0h

Register 11-174. FCCh Advanced Error Capabilities and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register.	ROS	Yes	1_1111b
5	**ECRC Generation Capable** 0 = ECRC generation ***not supported*** 1 = ECRC generation supported, but must be enabled	RO	Yes	1
6	**ECRC Generation Enable** 0 = ECRC generation disabled 1 = ECRC generation enabled	RWS	Yes	0
7	**ECRC Checking Capable** 0 = ECRC checking ***not supported*** 1 = ECRC checking supported, but must be enabled	RO	Yes	1
8	**ECRC Checking Enable** 0 = ECRC checking disabled 1 = ECRC checking enabled	RWS	Yes	0
31:9	***Reserved***			0-0h

Register 11-175. FD0h Header Log_0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_0** First DWord header. TLP header associated with error.	ROS	Yes	0-0h

Register 11-176. FD4h Header Log_1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_1** Second DWord header. TLP header associated with error.	ROS	Yes	0-0h

Register 11-177. FD8h Header Log_2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_2** Third DWord header. TLP header associated with error.	ROS	Yes	0-0h

Register 11-178. FDCh Header Log_3 (All Ports)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_3** Fourth DWord header. TLP header associated with error.	ROS	Yes	0-0h

Chapter 12 Non-Transparent (NT) Bridging

12.1 Introduction

The following are key elements of PEX 8524 NT bridging (NTB):

- Device Type Identification
- Non-Transparent Port (NT Port) Reset
- Scratchpad Registers
- Doorbell Registers
- BAR Setup Registers
- Address Translation

12.1.1 Device Type Identification

Devices identify themselves by way of the Conventional PCI CSR header **Class Code** register. A Transparent PCI-to-PCI bridge identifies itself as a Class Code 060400h. An NT bridge identifies itself as "other," 068000h, with a Type 0 Header. This identification is consistent with the use of other Non-Transparent bridges available in the industry.

The **PCI Express Capability List and Capabilities** register includes a *Device/Port Type* field. In this register, a Transparent bridge/switch port identifies itself as an upstream or downstream port, while an NT bridge/switch NT Port identifies itself as a PCI Express endpoint.

12.1.2 Non-Transparent Port (NT Port) Reset

The section discusses Non-Transparent mode exceptions and enhancements to Transparent mode PCI Express (standard) reset behavior.

12.1.2.1 Fundamental Reset (PEX_PERST#)

PEX_PERST# resets all PEX 8524 states, including NT Port states. All Sticky bits and Configuration registers in Virtual and Link spaces are initialized to default values by this reset.

12.1.2.2 Intelligent Adapter Mode NT Port Reset

In Intelligent Adapter mode, when a Hot Reset is received by the transparent-side upstream port, the PEX 8524 propagates the reset to all transparent downstream ports to reset them, resets the internal fabric and NT Port Virtual Interface states. There is no reset propagation to the NT Port and its link-side remains intact. The PEX 8524 supports an option that allows these Hot Reset conditions at its Transparent upstream port to be masked (disabled), by setting the Port 0 **Debug Control** register *Upstream Port Hot Reset and Link Down Reset Propagation Disable* bit (offset 1DCh[20]).

When the NT Port Link Interface receives a Hot Reset, the NT Port Link Interface registers are reset. This reset type does not reset the Transparent ports nor NT Port Virtual Interface. Instead, when the NT Port Link Interface receives a Hot Reset (or enters the DL_Down condition), the PEX_NT_RESET# signal is asserted Low for 1 µs. The system can use this signal to trigger a reset of the entire Local subsystem (Transparent side).

When software writes to the PEX 8524 transparent side upstream port **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]), the resulting secondary bus reset is (as above) propagated to all PEX 8524 Transparent downstream ports, and the port states and NT Port Virtual Interface states are reset.

12.1.2.3 Dual-Host Mode NT Port Reset

Dual-Host mode reset behavior is the same as in Intelligent Adapter mode, with the following exception – in Dual-Host mode, a Hot Reset received from the Active host as seen at the PEX 8524 Transparent upstream port (or DL_Down condition) does ***not*** reset the Transparent ports, the internal switch-fabric nor the NT Port Virtual Interface. The queues' internal operation and downstream ports remain intact, allowing the Backup Host to take over (as described in Section 4.4.2, "Dual-Host Mode").

There is no reset propagation onto the NT Port.

12.1.2.4 Reset Propagation

Reset propagation, during a Hot Reset or by way of the **Bridge Control** register *Secondary Bus Reset* mechanism is limited to transparent downstream ports. In an NT bridge, this reset cannot be propagated across the bridge (across the NT Port). (Refer to Chapter 5, "Reset and Initialization," for details regarding PEX 8524 Transparent mode reset behavior.)

12.1.3 Scratchpad Registers

Scratchpad registers are readable and writable from both sides of the NT bridge, providing a generic means for inter-host communications. A block of eight registers are provided, accessible in Memory or I/O space from the NT Port Virtual and Link Interfaces. These registers pass control and status information between Virtual and Link Interface devices or they can be generic R/W registers. Reading or writing Scratchpad registers does not cause interrupt assertion – **Doorbell** registers are used for this purpose.

12.1.4 Doorbell Registers

Doorbell registers are used to transmit interrupts from one side of the NT bridge to the other. This section describes a typical set of Doorbell Control registers.

A 16-bit software-controlled Interrupt Request register and associated 16-bit Mask register are implemented for the NT Port Virtual and Link Interfaces. These registers can be accessed from the NT Port Virtual and Link Interfaces, in Memory or I/O space. The Doorbell mechanisms consist of the following registers:

- **Set Virtual Interface IRQ**
- **Clear Virtual Interface IRQ**
- **Set Virtual Interface IRQ Mask**
- **Clear Virtual Interface IRQ Mask**
- **Set Link Interface IRQ**
- **Clear Link Interface IRQ**
- **Set Link Interface IRQ Mask**
- **Clear Link Interface IRQ Mask**

An interrupt is asserted on the NT Port Virtual Interface when one or more of the **IRQ Set/Clear** register bits are set to 1 and their corresponding **Mask** register bits are cleared to 0. The Link Interface works identically. The interrupt is de-asserted when all set bits are masked or cleared.

In a PCI Express switch, interrupt state transitions (from setting to clearing, or vice versa) result in packets being transmitted upstream on the appropriate side of the bridge when INT*x* is enabled. Standard PCI Express Capability structures allow these interrupts to be configured as MSI or INT*x*. When MSI is enabled, packets are transmitted only when interrupts transition from Clear IRQ to Set IRQ.

Internally, the **Set IRQ** and **Clear IRQ** registers are the same register. One location is used to set bits and the other is used to clear bits. The status can be read from either register.

The PEX 8524 Virtual interrupts are also disabled/removed when the link to the other device is down.

12.1.5 BAR Setup Registers

All NT Port Virtual and Link Interface BARs include programmable window sizes, with the exception of BAR0 and BAR1 (on both interfaces), which provide Memory and/or I/O-Mapped access to the CSRs. The BAR Setup registers are used to program the window size of each BAR. A detailed description of the NT Port Virtual and Link Interface BARs follows.

12.1.5.1 NT Port Virtual Interface BARs

Table 12-1 defines the NT Port Virtual Interface BARs.

Table 12-1. NT Port Virtual Interface BARs

Register	Description
BAR0	***Reserved***. All PEX 8524 Port Configuration registers are mapped into Memory space using Transparent upstream port Type 1 space BAR0 and BAR1 registers. The Local Host, connected to the Transparent ports, can use the Transparent upstream port BARs to access the PEX 8524 Port Configuration registers.
BAR1	BAR1 is ***reserved***.
BAR2	Configured by the **NT Port Virtual Interface BAR2 Setup** register. BAR2 is always a 32-bit BAR and uses Direct Address Translation.
BAR3	Configured by the **NT Port Virtual Interface BAR3 Setup** register. BAR3 is always a 32-bit BAR and uses Lookup Table-based Address Translation described in Section 12.1.6.2, "Lookup Table-Based Address Translation."
BAR4	Configured by the **NT Port Virtual Interface BAR4/5 Setup** register. BAR4 can be implemented as a 32-bit BAR or lower half of a 64-bit BAR by combining it with BAR5. BAR4 uses Direct Address Translation.
BAR5	Enabled only when BAR4 is configured as a 64-bit BAR. Holds the upper 32-bit Base address of the 64-bit Memory Address range. The **NT Port Virtual Interface BAR4/5 Setup** register defines the size. BAR5 is not implemented as a 32-bit only BAR. BAR5 uses Direct Address Translation.

12.1.5.2 NT Port Link Interface BARs

Table 12-2 defines the NT Port Link Interface BARs.

Table 12-2. NT Port Link Interface BARs

Register	Description
BAR0	Maps all PEX 8524 Port Configuration registers into System Host Memory Space. BAR0 is always enabled.
BAR1	Maps only NT Port Virtual Interface and Link Interface Configuration registers into System Host I/O space. BARs can be disabled (enabled by default) by the **NT Port Link Interface BAR0/BAR1 Setup** register.
BAR2	Configured by the **NT Port Link Interface BAR2/3 Setup** register. BAR2 can be implemented as a 32-bit BAR or lower half of a 64-bit BAR by combining it with BAR3. BAR2 uses Direct Address Translation.
BAR3	Enabled only when BAR2 is configured as a 64-bit BAR. Holds the upper 32-bit Base address of the 64-bit Memory Address range. The **NT Port Link Interface BAR3 Setup** register defines the size. BAR3 is not implemented as a 32-bit only BAR. BAR3 uses Direct Address Translation.
BAR4	Configured by the **NT Port Link Interface BAR4/5 Setup** register. BAR4 can be implemented as a 32-bit BAR or lower half of a 64-bit BAR by combining it with BAR5. BAR4 uses Direct Address Translation.
BAR5	Enabled only when BAR4 is configured as a 64-bit BAR. Holds the upper 32-bit Base address of the 64-bit Memory Address range. The **NT Port Link Interface BAR5 Setup** register defines the size. BAR5 is not implemented as a 32-bit only BAR. BAR5 uses Direct Address Translation.

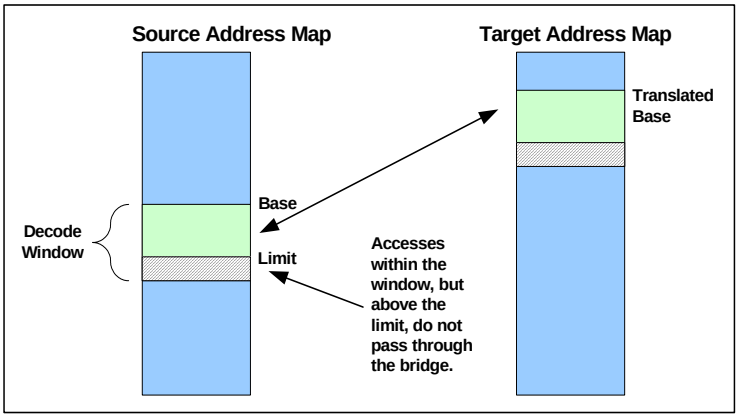
12.1.5.3 BAR Limit Registers

The Base Address register (BAR) Address Range size is a power of two (BARs can be assigned only Memory resources in “power of two” granularity).

A Limit register is used to reduce the Address Range size. When a Limit register is implemented, the address range extends from the Base register to the Limit register, instead of to the Base register plus an offset of $2^N - 1$, where N is the number of bits in the offset (as defined by the **Setup** register).

The NT Port forwards the transaction when the transaction address falls within the range of the BAR lower address limit value to the BAR Limit register value. If the transaction address is outside this range, the NT Port reports an “Unsupported Request” and discards the transaction.

Figure 12-1. Limit Register Application



12.1.6 Address Translation

The Transparent bridge uses Base and Limit registers in I/O space, Non-Prefetchable Memory space, and Prefetchable Memory space to map transactions in the downstream direction across the bridge. All downstream devices must be mapped in contiguous address regions, such that a single Address range in each space is sufficient. Upstream mapping is done by way of inverse decode, relative to the same registers. A Transparent bridge does not translate the addresses of forwarded transactions/packets.

Address domain is unique per host. If a transaction originates in one host domain and targets a device in another host domain, it must travel through the NT Port. If the NT Port does not process address translation, the transaction travels to a non-targeted device on a second host domain, or is rejected by the NT Port upstream bridge. Transactions crossing the address domain must be address-translated by the NT Port before transmitting the transaction to the target host domain.

The NT bridge uses the Conventional PCI set of BARs in its Type 0 CSR header to define Address ranges into the Memory space on the other side of the bridge. BARs define resource Address ranges that allow transaction forwarding to the opposite (other side) interface.

There are two sets of BARs – one each for the Virtual and Link Interfaces. BARs contain a Setup and Address Translation register:

- BAR Setup registers enable/disable the BAR and define the Address range size and type. Certain BARs contain a Limit register, which is used to restrict its Address range size to less than a power of two. BAR Setup registers must be programmed prior to allowing configuration software to assign a resource for these BARs.
- BAR Address Translation registers must be programmed before generating traffic across the NT Port. This programming is typically done by information downloaded from the serial EEPROM or by software.

The PEX 8524 NT Port Virtual Interface supports two types of address translation:

- Direct Address Translation
- Lookup Table-Based Address Translation

The PEX 8524 NT Port Link Interface supports only Direct Address Translation.

12.1.6.1 Direct Address Translation

The BAR Setup registers define a mask that splits the address into an upper *base* field and a lower *offset* field. Translation then consists of replacing, under the maskable portion of the Setup register, the Address Base bits with the corresponding Address Translation register bits. Figure 12-2 illustrates Direct Address Translation.

The device(s) on the originating-host domain can communicate to a single device or multiple devices mapped to consecutive Memory Address space on the Target Host domain, by using the Direct Address Translation mechanism. Figure 12-3 illustrates the entire address map, claimed by the NT Port, mapped into the single target device. Figure 12-4 illustrates the entire address map claimed by the NT Port, mapped into multiple target devices. Multiple devices must be in contiguous Memory ranges.

Figure 12-2. Direct Address Translation

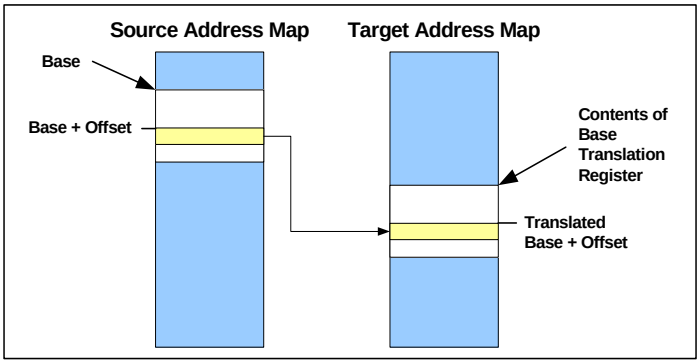


Figure 12-3. NT Port Mapped into Single Target Device

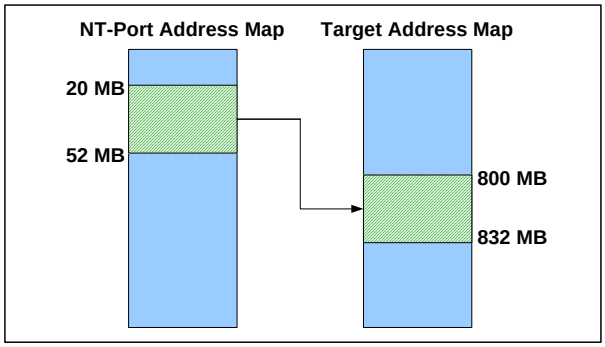
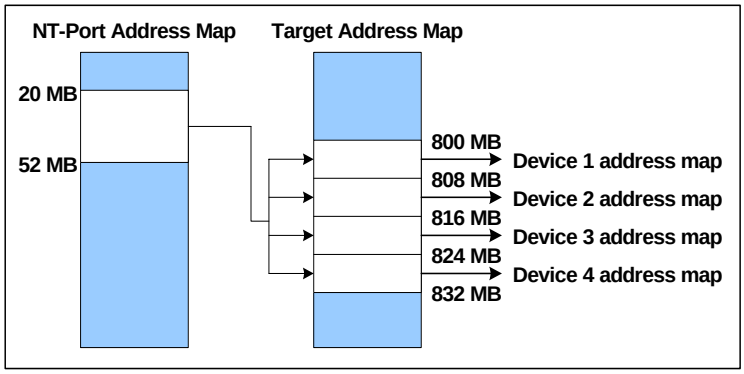


Figure 12-4. NT Port Mapped into Multiple Target Devices



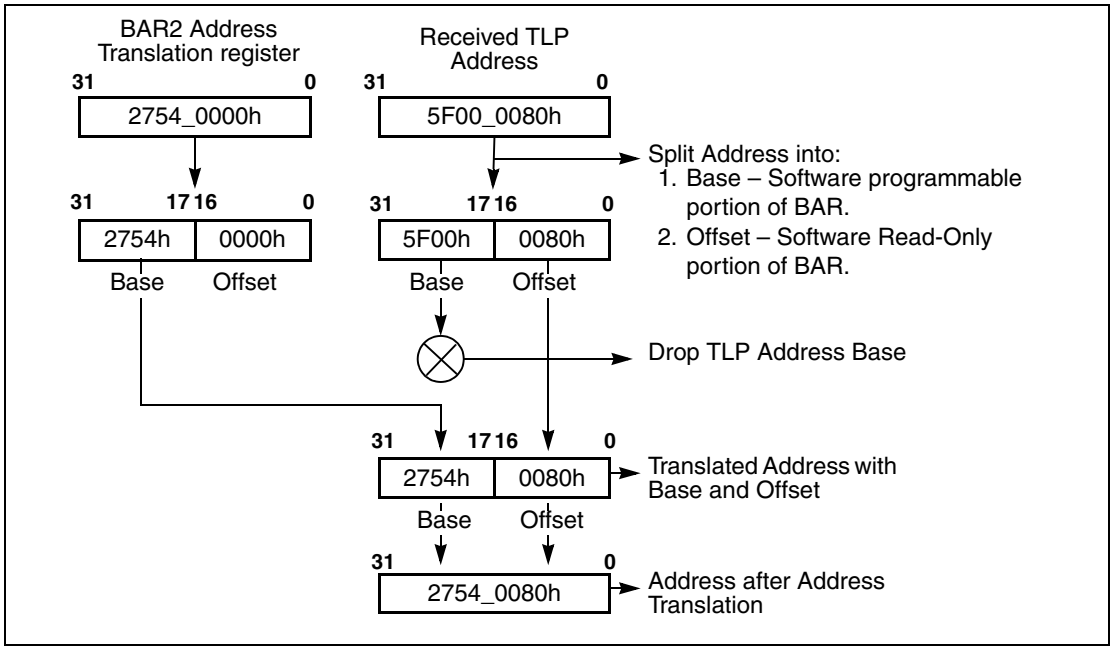
Address Translation Example

Assume the following:

1. NT Port Virtual Interface BAR2 claims 128 KB Memory space.
2. Configuration software assigns the 5F00_0000h address value to NT Port Virtual Interface BAR2 and it is within the transparent upstream port Memory window.
3. Device driver software programs the BAR2 address translation register to 2754_0000h.

The PEX 8524 receives a transaction to the NT Port Virtual Interface with address 5F00_0080h. The received transaction address is attaining the NT Port Virtual Interface BAR2. The PEX 8524 claims the transaction and executes the address translation described in Figure 12-5.

Figure 12-5. Address Translation Example



Note: *Nibble boundary-aligned hex address, bar_addr_xlation_reg[31:16], is 0010_0111_0101_0100b (2754h).*

12.1.6.2 Lookup Table-Based Address Translation

On the NT Port Virtual Interface, BAR3 uses a special lookup table-based address translation for transactions that fall within its window.

The **NT Port Virtual Interface BAR3 Setup** register defines the lookup table (LUT) entry/page size. The **NT Port Virtual Interface BAR3** size is determined by multiplying the page size by 64.

This **BAR3 Setup** register defines a mask that splits the transaction address into upper and lower/offset fields. The upper field is further divided into two portions – the upper portion is termed "Base Address" and lower portion is termed "Lookup Table Index." The index field location of the received TLP address varies, based on the page size selection. Table 12-3 defines the LUT entry/page size, corresponding BAR size, and bit position of individual fields in the received transaction address.

Figure 12-6 describes the Lookup Table-Based Address Translation scheme. The received transaction address is divided into three parts, based on the **BAR Setup** register. The *Base Address* and *LUT Index* fields are compared against the BAR. If the transaction address attains the BAR, the PEX 8524 uses the LUT Index to select the LUT Entry. The PEX 8524 replaces the Base address and LUT Index with the selected Lookup Table Entry value, if the entry is valid. Otherwise, the NT Port Virtual Interface returns an *Unsupported Request* (UR) error condition. The PEX 8524 passes the received transaction address offset into translated address offset without modification.

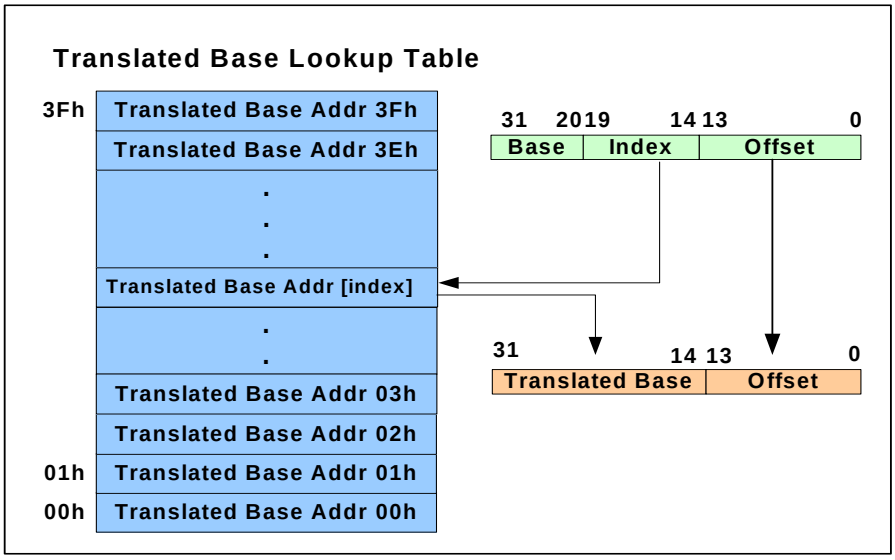
Applications can use the Lookup Table-Based Address translation when the target device's address range is scattered over 32-bit Memory space.

The NT Port Lookup table descriptions are discussed in Section 15.13.2, "NT Port Virtual Interface Lookup Table-Based Address Translation Registers."

Table 12-3. Received Transaction-Address Breakdown

Page Size (Bytes)	Window Size (Bytes)	Base Address (Bits)	LUT Index (Bits)	Offset (Bits)
4K	256K	[31:18]	[17:12]	[11:0]
8K	512K	[31:19]	[18:13]	[12:0]
16K	1M	[31:20]	[19:14]	[13:0]
32K	2M	[31:21]	[20:15]	[14:0]
64K	4M	[31:22]	[21:16]	[15:0]
128K	8M	[31:23]	[22:17]	[16:0]
256K	16M	[31:24]	[23:18]	[17:0]
512K	32M	[31:25]	[24:19]	[18:0]
1M	64M	[31:26]	[25:20]	[19:0]
2M	128M	[31:27]	[26:21]	[20:0]
4M	256M	[31:28]	[27:22]	[21:0]
8M	12M	[31:29]	[28:23]	[22:0]
16M	1G	[31:30]	[29:24]	[23:0]
32M	2G	31	[30:25]	[24:0]

Figure 12-6. Lookup Table-Based Address Translation



12.2 Requester ID Translation

Configuration, Message, and Completion transactions are ID-routed instead of address-routed. Of these, the NT Port forwards only the completion transaction between the two host domains. PCI Express switches and bridges use the Requester ID [defined in completion Transaction Layer Packet (TLP) header] to route these packets.

The Requester ID consists of the following:

- Requester's PCI Bus Number
- Device Number
- Function Number

The Completer ID consists of the following:

- Completer's PCI Bus Number
- Device Number
- Function Number

Note: *The PCI Bus Number is unique for each host domain.*

Figure 12-7 illustrates the Memory Request TLP header format. Figure 12-8 illustrates the Completion TLP Header format.

Figure 12-7. Memory Request TLP Header Format

	Byte 0								Byte 1								Byte 2								Byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bytes 0-3	R	Fmtx1		Type					R	TC			R				TD	EP	Attr		R				Length							
Bytes 4-7	Requester ID																Tag								Last DW BE				1st DW BE			
Bytes 8-11	Address[63:32]																															
Bytes 12-15	Address[31:0]																								R							

Figure 12-8. Completion TLP Header Format

	Byte 0								Byte 1								Byte 2								Byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bytes 0-3	R	Fmt		Type					R	TC			R				TD	EP	Attr		R				Length							
Bytes 4-7	Completer ID																Completer			BCM	Byte Count											
Bytes 8-11	Requester ID																Tag								R	Lower Address						

12.2.1 Transaction Sequence

To implement a transaction sequence:

1. Requester inserts ID information into the Memory Read TLP that it generates on the initiating Host domain.
2. Switches and bridges between the transaction initiator and PEX 8524 NT Port route this Memory Read TLP based on the address.
3. NT Port replaces the Memory Read TLP Requester ID with its ID, and conducts the address translation before it forwards this Requester ID-translated TLP to the Target Host domain, because the NT Port is the transaction initiator in the target host domain.
4. Switches and bridges between the PEX 8524 NT Port and target device route this Memory Read TLP, based on the address.
5. When the target device generates the completion TLP, it copies the Memory Read TLP Requester ID into the corresponding completion *TLP Requester ID* field and inserts its ID into the *TLP Completer ID* field.
6. Switches and bridges between the target device and PEX 8524 NT Port route the completion TLP, based on Requester ID information.
7. NT Port restores the original Requester ID value from the Configuration register and implements another Requester ID and Completer ID translation for the completion TLP before it forwards the completion TLP to the requester-host domain.
8. Switches and bridges between the PEX 8524 NT Port and requester route the Completion TLP, based on the Requester ID.
9. Requester accepts the Completion TLP and processes it.

12.2.2 Transaction Originating in Local Host Domain

The translation of outgoing requests from the NT Port Virtual Interface to the NT Port Link Interface uses an 8-entry LUT, as discussed in Section 15.13.5, "NT Port Virtual Interface Send Lookup Table Entry Registers." Each LUT entry supports all outgoing requests and any number of outstanding requests made by a single device or function. If a device uses Phantom Function Numbers to increase the maximum number of outstanding transactions, then each phantom function consumes a LUT entry. The LUT must be configured, by a serial EEPROM or local firmware, before it is possible to transmit requests to the system domain, which provides a measure of security and protection.

When a Memory request arrives at the NT Port Virtual Interface, the packet Requester ID is associated with this LUT. If it attains one of the enabled LUT entries, the corresponding entry address (TxIndex) is inserted into the *Function Number* field of the packet's Requester ID. Conversely, if it does not attain one of the enabled LUT entries, an Unsupported Request completion is returned.

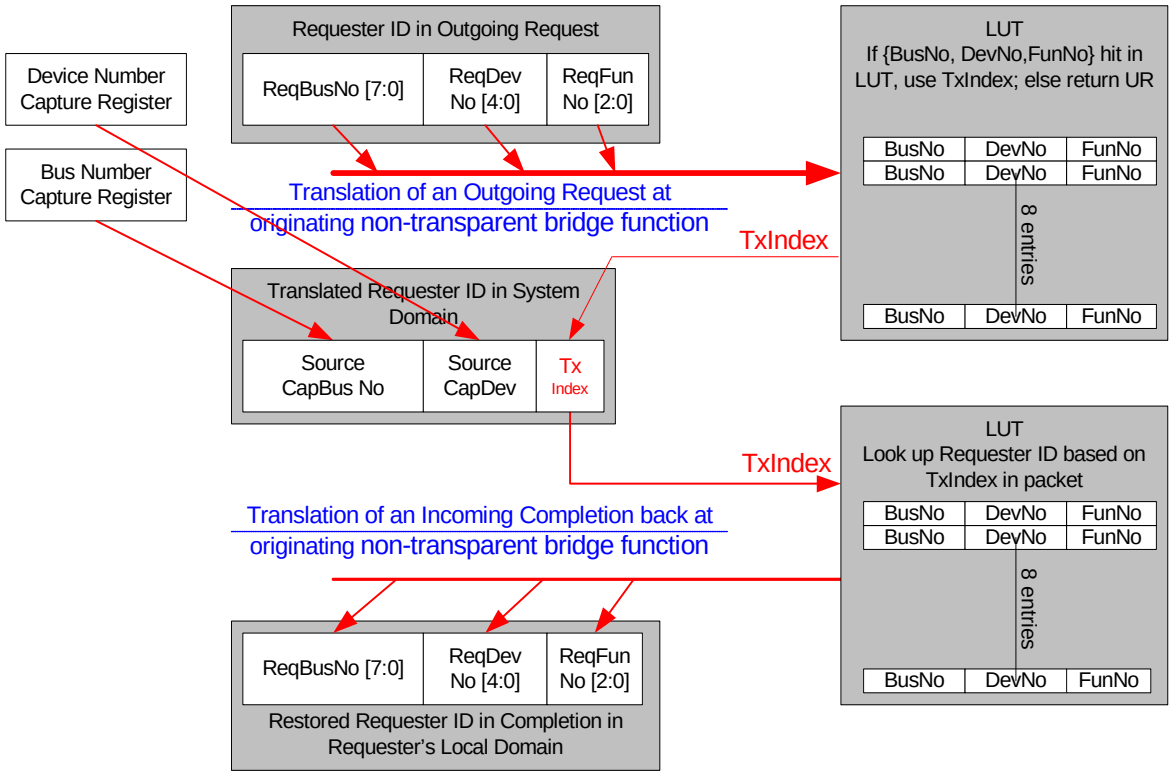
At the same time, the contents of the **NT Port Link Interface Bus Number** and **Device Number Capture** registers (the values used during the last CSR Write to the port) are copied into the packet *Requester ID Bus Number* and *Device Number* fields.

A completion, with translated Requester ID, returned from the system domain to the PEX 8524, is recognized when its Requester ID Bus and Device Numbers match the NT Port Link Interface Captured Bus and Device Numbers. (Refer to Figure 12-9.)

When the original Requester ID is restored, the following occurs:

1. TxIndex is retrieved from the *Function Number* field of the completion TLP Requester ID.
2. TxIndex is used to look up the same 8-entry LUT, to restore the original Requester ID.
3. If the selected entry is valid, the restored Requester ID is placed into the completion *TLP Requester* field; otherwise, an Unexpected Completion is returned.
4. *Completion TLP Completer ID* field is replaced by the NT Port Virtual Interface Captured Bus, Device, and Function Numbers.
5. Translated Completion TLP is forwarded to the original requester in the local domain.

Figure 12-9. Requester ID Translation for Request Originating in Local Domain



12.2.3 System Host Domain Transaction Originating

Transactions originating in System Host domain use a second LUT, with 32 entries, as illustrated in Figure 12-10. This data structure supports up to 32 devices (elsewhere in the system domain) that are transmitting requests through the associated NT Port. Because the Function Number is not used in the LUT association, a separate LUT entry is not required for each requesting or phantom function device. The LUT must be configured before transmitting requests through the NT Port. This requester registration process, which cannot be accomplished by a peer, is an effective security and protection mechanism.

When a request is received from the system domain and routed to the NT Port, its Requester ID is again translated – Bus and Device Numbers, but not Function Number. The received Memory request TLP Requester ID is associated with this LUT, and the address (RxIndex) of the corresponding matching entry is substituted into the *Device Number* field of the Memory request's *TLP Requester ID* field.

If no match is found, or the matched entry is not enabled, the request receives a UR response.

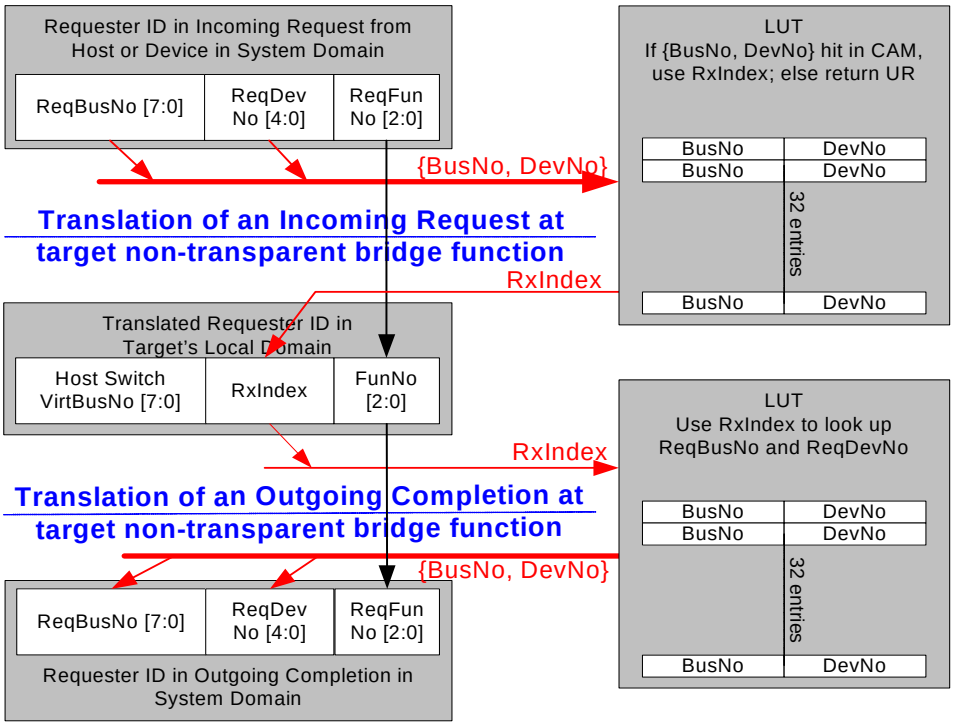
If a match is found, and matched entry is enabled, the PEX 8524 internal virtual PCI Bus Number is copied into the packet Requester ID's *Bus Number* field. The translated Memory request TLP is address-translated and forwarded into the Local domain.

The PEX 8524 internal virtual PCI Bus Number is sufficient to route the completion from the completer back to the NT Port in the completer's domain, because the NT Port is the only possible requester on the switch internal virtual bus. Elsewhere in the PCI Express hierarchy, the Bus Number is sufficient to route the completion back into the switch containing the NT Port.

The inverse translation occurs when a completion passes through the NT bridge from the local domain to the system domain. The RxIndex is retrieved from the *Device Number* field of the received completion *TLP Requester ID* header field, and used to look up the 32-entry LUT. The Completion TLP *Requester ID*, *Bus Number* and *Device Number* fields are replaced by the decoded LUT-entry Bus Number and Device Number values if the entry is valid; otherwise, an Unexpected Completion is returned.

The Completion TLP Completer ID is replaced by the NT Port Link Interface Captured Bus Number, Captured Device Number and Function Number values before forwarding the Completion TLP to the system domain.

Figure 12-10. Requester ID Translation for Request Originating in System Domain



12.3 NT Port Power Management Handling

12.3.1 Active-State Power Management (ASPM)

When NT mode is enabled (Intelligent Adapter or Dual-Host mode), the PEX 8524 does not enter into active Power Management states L0s and L1 on any of its ports, although the PEX 8524 NT Link Interface Type 0 Endpoint, NT Virtual Interface Type 0 Endpoint, and Transparent Type 1 ports are enabled for ASPM by programming the **Link Control** register *Active State Power Management (ASPM) Control* field. The PEX 8524 NT Link Interface Type 0 Endpoint and Transparent upstream port do not enter L0s nor request an ASPM L1 entry on its transmit direction. Similarly, the PEX 8524 Transparent downstream ports do not enter L0s on their transmit direction. If an ASPM L1 request is received on a PEX 8524 Transparent downstream port, a PM_Active_State_Nak message is transmitted downstream, irrespective of the **Link Control** register *Active State Power Management (ASPM) Control* field value. The PEX 8524 allows all ports to receive a lane entry to the L0s state.

12.3.2 PCI-PM and PME Turn Off Support

When NT mode is enabled, the NT Port Link Interface Type 0 Endpoint behaves as other endpoints in the D3hot PCI-PM power states. Once in the D3hot state, the PEX 8524 NT Port Link Interface Type 0 Endpoint requests PCI_PM L1 entry and finally settles in the L1 link state. Only Configuration accesses and messages to the NT Port Link Interface Type 0 Endpoint are supported in the D3hot state. NT host software can transmit PME_Turn_Off messages when the NT host decides to turn off the main power and main reference clock. The PEX 8524 NT Link Interface Type 0 Endpoint indicates its readiness to lose power by transmitting a PME_To_Ack message toward the upstream device. The PME_To_Ack message is transmitted when there is no pending TLP waiting to be transmitted in the PEX 8524 NT Port Link Interface upstream direction. The port requests the L2/L3 Ready state, by transmitting PM_Enter_L23 DLLP to the upstream device after transmitting PME_To_Ack TLP. The port settles into the L3 link state when the power controller removes the main power and Reference Clock.

When the PME_Turn_Off message is received on the PEX 8524 transparent upstream port, the port broadcasts this message to all PEX 8524 downstream devices, including the NT Port Virtual Interface Type 0 Endpoint. After the PME_To_Ack message is received from all downstream devices and from the PEX 8524 NT Port Virtual Interface Type 0 Endpoint, the PEX 8524 transparent upstream port transmits an aggregated PME_To_Ack message to the upstream component after it finishes transmitting all pending TLPs to the upstream component. When NT mode is enabled, the PEX 8524 transparent downstream ports allow the attached devices to enter the PCI-PM-compatible L1 state. The PEX 8524 NT Port Virtual Interface Type 0 Endpoint never enters the PCI-PM L1 state.

12.3.3 Message Generation

The PEX 8524 NT Port Link Interface Type 0 Endpoint never generates PM_PME messages. The PEX 8524 NT Port Virtual Interface Type 0 Endpoint never receives Set_Slot_Power_Limit messages and never generates PM_PME messages.

12.4 NT Hot Plug Support

The PEX 8524 Transparent downstream ports, with NT mode enabled, behave in the same way when NT mode is disabled. The PEX 8524 NT Port Virtual Interface Type 0 Endpoint never receives nor generates Hot Plug messages. The PEX 8524 NT Port Link Interface Type 0 Endpoint generates and receives Hot Plug messages that an Endpoint (or switch upstream port) receives/generates. The PEX 8524 NT Port Link Interface Type 0 Endpoint and transparent upstream port implements Hot Plug client features. Attention Button Present Device, Attention Indicator Present Device, and Power Indicator Present Device registers and their functionality are implemented on the PEX 8524 NT Port Link Interface Type 0 Endpoint and PEX 8524 downstream ports. The PEX 8524 NT Port Virtual Interface Type 0 Endpoint does not implement Hot Plug Control nor Hot Plug Client functionality, because it is an Endpoint device not connected to a Physical Link.

Figure 12-11. Sample Intelligent Adapter Mode Hot Plug View

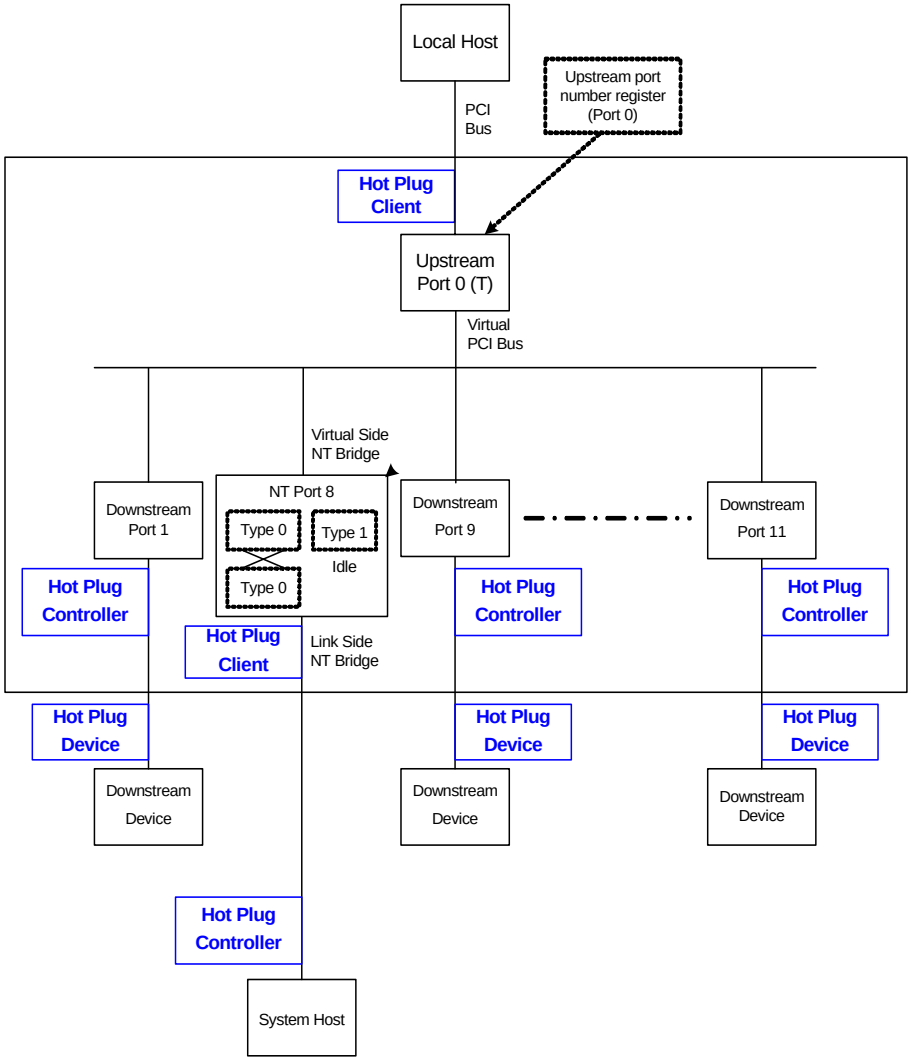
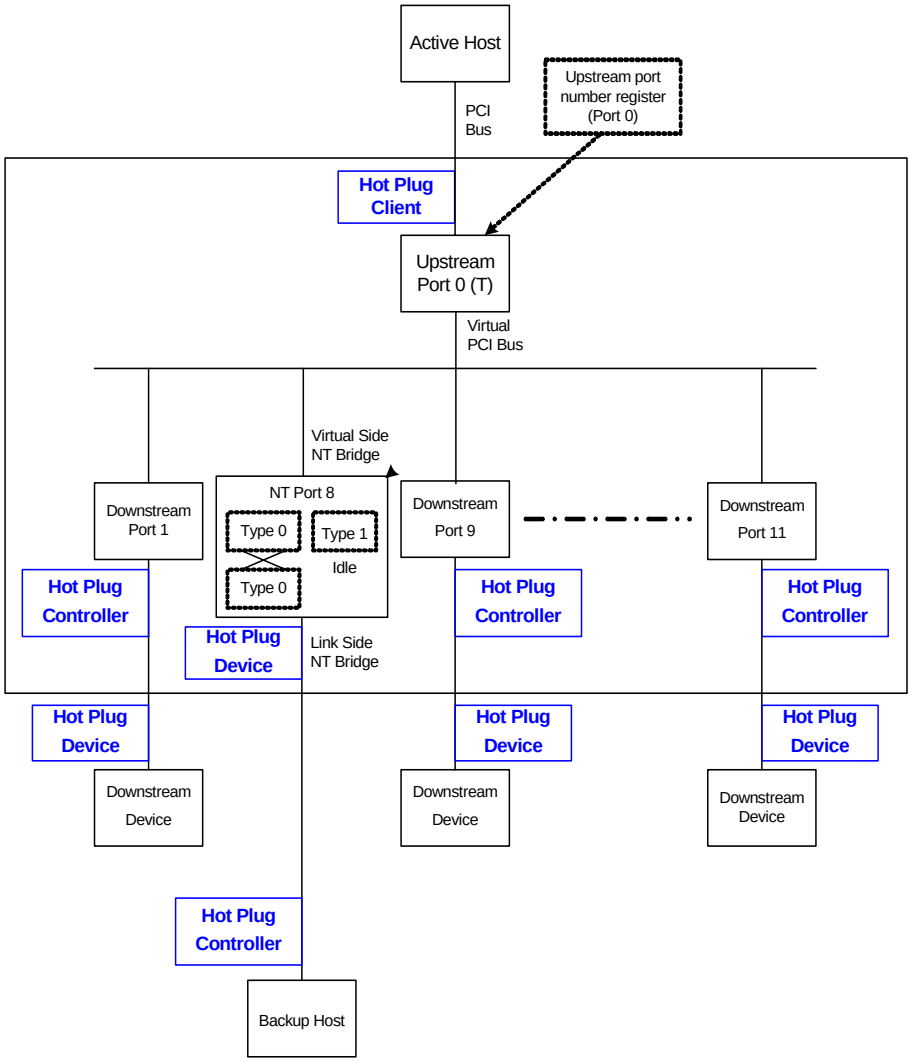


Figure 12-12. Sample Dual-Host Mode Hot Plug View



12.4.1 Hot Plug Sequence during Host-Failover

Hot Plugging the complete Active Host domain into the Backup Host is similar to Hot Plugging the endpoint device into the downstream port of a Switch or Root Port. If the Backup Host is dead, it is not a problem. If the Active Host is dead, the Backup Host first completes the Hot Plug insertion sequence before it starts the failover sequence.

The Active Host can service none or a portion of the Hot Plug sequence on a Transparent downstream port and dies before servicing the remaining sequence. The downstream port Hot Plug Controller module previously transmitted an interrupt for the next Hot Plug sequence to the failed transparent upstream port and it did not receive service from failed active host. The Backup Host disables "MSI and INT*x* interrupt generation" before it starts the failover sequence. After the Backup Host finishes the failover sequence, it enables "MSI and/or INT*x* interrupt generation" for the Transparent downstream port. This interrupt generation re-enabling generates Interrupt Assertion messages (or MSI) to the self-promoted Backup (Active) Host. The self-promoted Backup (Active) Host continues the remaining Hot Plug insertion/removal sequence from the failed Active Host.

Chapter 13 NT Port Interrupts

13.1 Introduction

NT Port Virtual and Link sides can generate MSI or INT*x* interrupts, which are enabled by the **Command** register *Interrupt Disable* or **Message Control** register *MSI Enable* bits (offsets 04h[10] or 48h[16], respectively). Because they are endpoints, the NT Port Virtual and Link sides cannot receive Interrupt messages; therefore, if an interrupt message is received, it is reported as an error condition.

The NT Port Virtual side generates interrupts to the Local Host/Active Host for device-specific errors reported by NT Port Egress modules or Doorbell interrupts.

The NT Port Link side generates interrupts to the System/Inactive Secondary Host when device-specific errors are reported by NT Port Ingress modules.

13.2 Doorbell Interrupts

By default, all interrupt sources are masked. If software processes an interrupt, it first clears the Interrupt Mask register for the interrupt source.

The asserted INT*x* virtual wires are de-asserted, when the software clears the Event Status bit that caused the assertion.

The Interrupt handler has two set of registers – one set for Virtual Side Type 0 Configuration Space and another set for Link Side Type 0 Configuration Space of the NT Port.

Further details regarding MSI and INTx interrupts are provided in Chapter 6, "Interrupts."

13.3 Doorbell Registers

A 16-bit software-controlled **Interrupt Request** register and associated 16-bit **Mask** register are implemented for the NT Port Virtual and Link Interfaces. These registers can be accessed from the NT Port Virtual or Link Interface, in Memory or I/O space. The Doorbell mechanisms consist of the following registers:

- **Set Virtual Interface IRQ**
- **Clear Virtual Interface IRQ**
- **Set Virtual Interface IRQ Mask**
- **Clear Virtual Interface IRQ Mask**
- **Set Link Interface IRQ**
- **Clear Link Interface IRQ**
- **Set Link Interface IRQ Mask**
- **Clear Link Interface IRQ Mask**

An interrupt is asserted on the NT Port Virtual Interface when one or more of the **IRQ Set/Clear** register bits are set to 1 and their corresponding **Mask** register bits are cleared to 0. The NT Port Link Interface works identically. The interrupt is de-asserted when all set bits are masked or cleared.

The **IRQ Set/Clear** registers are internally the same physical **Interrupt Request** register, which includes two separate DWords – one DWord is used to set bits, the other is used to clear bits. The status can be read from either register.

The **IRQ Set/Clear Mask** registers are also internally the same register – one interface is used to set a **Mask** register bit, the other is used to clear a **Mask** register bit.

Chapter 14 Non-Transparent Bridging Software Architecture

14.1 Introduction

This chapter focuses on system configuration and data transfer through the NT Port. The PEX 8524 supports two types of NT modes:

- Intelligent Adapter
- Dual-Host

The NT Port and NT-mode type are described in Chapter 12, "Non-Transparent (NT) Bridging."

The PEX 8524 NT feature and mode (Intelligent Adapter or Dual-Host) are enabled using board-level Strapping balls. The PEX 8524 requires software support for the following:

- System Configuration
- Data transfer through NT Port
- Quality of Service (QoS) management in a switch
- Performance tuning in a switch
- Interrupt Service routine
- Hot Plug routine
- Power Management routine
- Error Handling routine

14.2 System Configuration

The PCI Express Configuration model supports two Configuration mechanisms:

- PCI-compatible configuration
- PCI Express-enhanced configuration

The PCI-compatible mechanism supports 100% binary compatibility with the *PCI r2.3* or later operating systems and corresponding bus enumeration and configuration software.

The PCI Express-enhanced mechanism is provided to increase the size of available Configuration space and optimize Configuration mechanisms.

14.2.1 PEX 8524 Intelligent Adapter Mode

Figure 14-1 describes a sample system view with PEX 8524 NT Intelligent Adapter mode enabled.

The PEX 8524 Transparent ports are PCI-to-PCI bridges, and the PEX 8524 NT Port is two Type 0 Endpoint devices connected back-to-back. PCI Express devices must include an assigned unique ID (Bus, Device, and Function Numbers).

Each PEX 8524 Transparent port has its own 4-KB PCI Express Configuration registers and the NT Port includes an 8-KB Configuration space – 4 KB for the NT Port Virtual Interface Type 0 Endpoint and another 4 KB for the NT Port Link Interface Type 0 Endpoint.

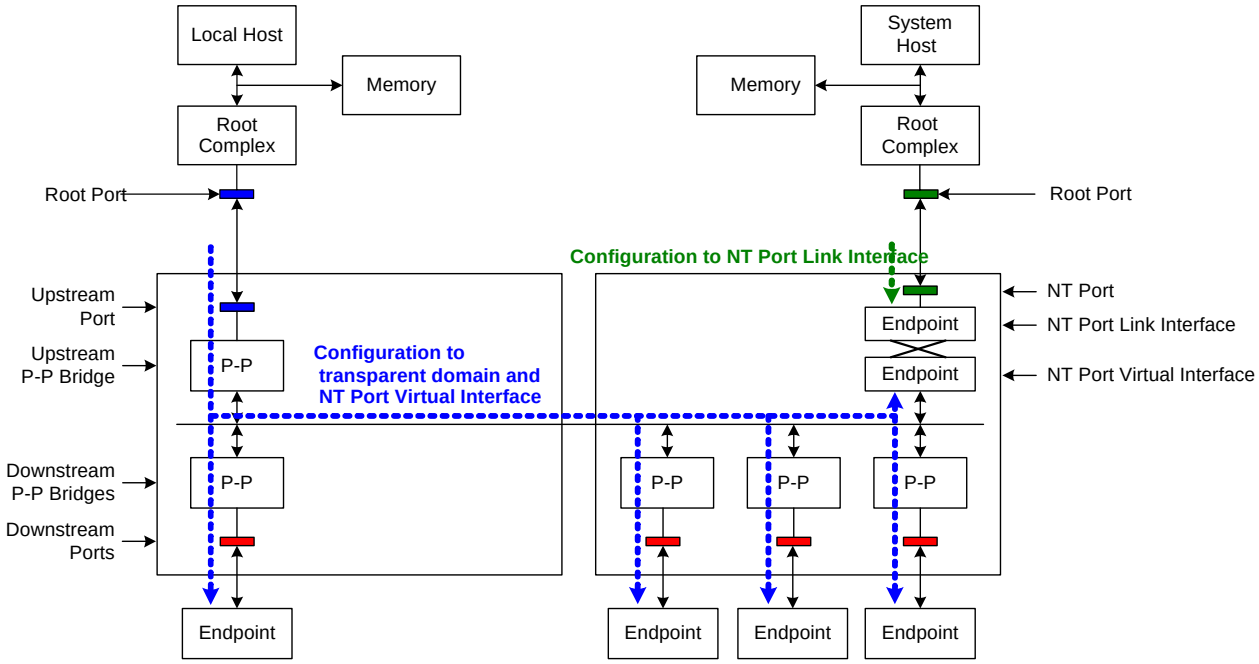
At power-up, one of PEX 8524 ports is selected as the upstream port and one of PEX 8524 downstream ports is selected as the NT Port, using board-level Strapping balls or a serial EEPROM.

The BIOS running in the Local Host configures the PEX 8524 upstream port, downstream ports, and NT Port Virtual Interface Type 0 Endpoint. The BIOS running in the System Host configures the NT Port Link Interface Type 0 Endpoint.

The Local Host-connected Root Complex initiates a Type 0 Configuration request to configure only the PEX 8524 upstream port and initiates Type 1 Configuration requests to configure the PCI Express hierarchy behind the PEX 8524 upstream port, including the PEX 8524 NT Port Virtual Interface Type 0 Endpoint. The Local Host is not allowed to configure the NT Port Link Interface Type 0 Endpoint using Type 0/Type 1 Configuration requests.

The System Host-connected Root Complex initiates a Type 0 Configuration request to configure only the PEX 8524 NT Port Link Interface Type 0 Endpoint. If this Root Complex initiates Type 1 Configuration requests, the NT Port Link Interface Type 0 Endpoint rejects the cycles as Unsupported Request (UR) errors.

Figure 14-1. Sample System Configuration with Non-Transparent PEX 8524



NT Port Virtual and Link Interface Type 0 Endpoint BAR2 through BAR5 are disabled, by default. Each BAR includes a corresponding BAR Setup register. This BAR Setup register controls the corresponding BAR, in the following manner:

1. Enables/disables BAR.
2. Programs BAR size.
3. Maps BAR group into 32- or 64-bit Address space.
4. Maps BAR into Prefetchable or Non-Prefetchable Memory space.

Refer Section 12.1.5, "BAR Setup Registers," for a detailed description of BARs and BAR Setup registers.

Use a serial EEPROM to enable the necessary BARs for inter-host-domain traffic by default; otherwise, System software/BIOS and Device Driver software must work together to enable the NT Port Type 0 Endpoint BARs before assigning resources to the BARs.

The PEX 8524 implements the following two Configuration register bits to take advantage of software layer resource assignment for the NT Port. The NT Port includes **Debug Control** register *Link Interface Access Enable* and *Virtual Interface Access Enable* device-specific Configuration register bits, mapped to PEX 8524 Port 0, at offset 1DCh[29:28], respectively.

By default, the *Virtual Interface Access Enable* configuration bit is set to 1, and the *Link Interface Access Enable* configuration bit is cleared to 0. The serial EEPROM overrides these default values.

If the *Virtual Interface Access Enable* configuration bit is cleared to 0, the NT Port Virtual Interface Type 0 Endpoint returns a "Configuration Retry Status (CRS)" response (completion with CRS status) for the received Configuration request from the Local Host. Otherwise, it accesses the corresponding Configuration registers.

If the *Link Interface Access Enable* configuration bit is cleared to 0, the NT Port Link Interface Type 0 Endpoint returns a "Configuration Retry Status (CRS)" response (completion with CRS status) for the received Configuration request from the System Host. Otherwise, it accesses the corresponding Configuration registers.

14.2.2 Sample PEX 8524 Configuration Steps

The PEX 8524 can be configured using a serial EEPROM or software.

To configure the PEX 8524:

1. Select PEX 8524 operating mode:
   a. Use STRAP_MODE_SEL[1:0] balls to select PEX 8524 operating mode. (Refer to Table 3-7, "PEX 8524VAA/BB/BC Strapping Signals, 680-Ball PBGA – 24 Balls," or Table 3-14, "PEX 8524BB/BC Strapping Signals, 644-Ball PBGA – 24 Balls," for the operating mode encoding values.)
   b. Serial EEPROM is used to override the Strapping ball selection.
2. Select port configuration:
   a. Select STRAP_STN0_PORTCFG[4:0] for PEX 8524 Station 0 port configuration, and STRAP_STN1_PORTCFG[3:0] for PEX 8524 Station 1 port configuration. (Refer to Table 4-1, "PEX 8524 Port Configurations," for the Strapping ball encoded values.)
   b. Serial EEPROM is used to override the Strapping ball selection.
3. Select upstream port:
   a. STRAP_UPSTRM_PORTSEL[3:0] selects one of PEX 8524 ports as an upstream port.
   b. Serial EEPROM is used to override the Strapping ball selection.
4. NT Port selection:
   a. STRAP_NT_UPSTRM_PORTSEL[3:0] selects one of the PEX 8524 downstream ports as an NT port.
   b. Serial EEPROM is used to override the Strapping ball selection.
5. Power-up the system.
6. Software enumeration directives:
   a. Locating Root Port devices and Root Complex integrated Endpoint devices within a Root Complex are implementation-specific.
   b. Root Complex is allowed more than one Root Port.
   c. PCI Express hierarchy starts from Root Complex Root Port.
   d. Local Host BIOS and System Host BIOS scans the device presence behind Root Port, using Type 0 Configuration request.
   e. BIOS reads key configuration registers (*for example*, *Header Type*, *Class Code*, *PCI Express Device/Port Type* field, and so forth) to locate the Device and Header Types.
   f. PEX 8524 NT Port Link Interface Type 0 Endpoint responds to the Configuration access with CRS, as its "Link Interface Access Enable," is disabled by default.
   g. System Host connected Root Complex later Retries this Configuration request to the PEX 8524 NT Port Link Interface Type 0 Endpoint.
   h. PEX 8524 NT Port Link Interface Type 0 Endpoint continues to Retry the Configuration request until it comprehends that "Link Interface Access Enable" is enabled.
   i. PEX 8524 upstream port accesses the corresponding Configuration registers and returns a successful completion.
   j. BIOS detects a PCI-to-PCI bridge device behind Local Host connected Root Complex and programs the PEX 8524 upstream port **Primary Bus Number**, **Secondary Bus Number**, and **Subordinate Bus Number** registers.
   k. BIOS commences scanning devices behind the PEX 8524 upstream port, using a Type 1 Configuration request.

l. If the received Type 1 Configuration request Bus Number is equal to the PEX 8524 upstream port Secondary Bus Number register value, and the Type 1 Configuration request Device Number is equal to the downstream port number or NT Port number, PEX 8524 accesses the corresponding port configuration register. (Downstream ports "port number" and NT Port "port number" are equal to Device Number on the PEX 8524 internal PCI Bus. NT Port Virtual Interface Type 0 Endpoint Device Number is the NT Port "port number" and NT Port Link Interface Type 0 Endpoint Device Number is the Device Number assigned by the upstream device.)

m. If BIOS locates a PCI-to-PCI device (downstream port) on the PEX 8524 internal PCI Bus, it commences the depth-first device scan behind the PEX 8524 downstream port, by programming PEX 8524 downstream port's **Primary Bus Number**, **Secondary Bus Number**, and **Subordinate Bus Number** registers.

n. PEX 8524 upstream port routes received Type 1 Configuration request to a PEX 8524 downstream port, if the received Type 1 Configuration request Bus Number is greater than the PEX 8524 upstream port Secondary Bus Number and less than or equal to PEX 8524 upstream port Subordinate Bus Number, as well as within the PEX 8524 downstream port Secondary Bus Number and Subordinate Bus Number window.

o. If the received Type 1 Configuration request Bus Number is equal to PEX 8524 downstream port Secondary Bus Number, the PEX 8524 downstream converts this Type 1 Configuration access to a Type 0 Configuration access, if the Type 1 Configuration request Device Number is 0. If the Type 1 Configuration request Device Number is non-zero, the PEX 8524 downstream port returns an Unsupported Request (UR) error.

p. If the received Type 1 Configuration request Bus Number is greater than the PEX 8524 downstream port Secondary Bus Number and less than or equal to the PEX 8524 downstream port Subordinate Bus Number, the PEX 8524 downstream port forwards this Type 1 Configuration request to the downstream device, unmodified.

q. If BIOS locates an NT Port Virtual Interface Type 0 Endpoint of the PEX 8524 internal PCI Bus, it stops scanning behind the NT Port, because it is an Endpoint and the PCI Express hierarchy ends in an Endpoint.

r. After locating all devices within the PCI Express hierarchy, BIOS commences resource assignment (*for example*, Memory, I/O, and/or Interrupt resource).

s. If the application is not using a serial EEPROM, system software/BIOS requires modification to implement the following:

- Assign a Memory, I/O, and/or Interrupt resource to the PEX 8524 upstream port BAR0 (Memory BAR) or PEX 8524 NT Port Virtual Interface BAR1 (I/O BAR) before assigning Memory resources to PEX 8524 NT Port Virtual Interface Type 0 Endpoint BAR2 to BAR5
- Use Memory/I/O-Mapped cycle (refer to Section 15.2, "Register Access," for details) to program the PEX 8524 NT Port Virtual Interface Type 0 Endpoint BAR Setup register
- Assign a resource to the PEX 8524 NT Port Virtual Interface Type 0 Endpoint

t. Use Memory/I/O-Mapped cycle to program the NT Port Link Interface Type 0 Endpoint BAR Setup register.

u. Use Memory-Mapped cycle to enable *Link Interface Access Enable* configuration bit.

v. After enabling the PEX 8524 NT Port Link Interface Type 0 Endpoint, System Host BIOS is allowed to enumerate and assign a resource to the PEX 8524 NT Port Link Interface Type 0 Endpoint.

w. Use a Memory/I/O-Mapped cycle to program the PEX 8524 NT Port Type 0 Endpoint Address Translation registers. (Refer to Chapter 15, "NT Port Virtual Interface Registers," and Chapter 16, "NT Port Link Interface Registers," for details.)

x. Use Memory/I/O-Mapped cycle to program the PEX 8524 NT Port Type 0 Endpoint BAR Limit registers if application is to efficiently use the memory resource. (Refer to Chapter 15, "NT Port Virtual Interface Registers," and Chapter 16, "NT Port Link Interface Registers," for details.)

y. Use Memory/I/O-Mapped cycle to program the PEX 8524 NT Port Type 0 Endpoint "Send LUT Entry" and "Receive LUT Entry" registers. (Refer to Chapter 15, "NT Port Virtual Interface Registers," and Chapter 16, "NT Port Link Interface Registers," for details.)

14.2.3 PEX 8524 Dual-Host Mode

PEX 8524 NT Dual-Host mode is similar to the PEX 8524 NT Intelligent Adapter mode, except the default values of the NT Port *Link Interface Access Enable* and *Virtual Interface Access Enable* bits (offset 1DCh[29:28], respectively) are set to 1. Both hosts connected to the PEX 8524 upstream port and NT Port Link Interface Type 0 Endpoint can concurrently enumerate the devices. The PEX 8524 does not generate a CRS response in NT Dual-Host mode.

14.2.4 Host-Failover Application

The Host-Failover application is based on the basic Dual-Host configuration, and dynamic swapping of the upstream and NT Ports is supported on Ports 0 and 8. The Active Host periodically transmits heartbeat messages, by way of the PEX 8524 to the Backup Host, to indicate that it remains active. When the Backup Host fails to receive heartbeat messages before its Fail Detect Timer expires, it starts the Failover process. The Backup Host halts cross-domain traffic before it starts the failover. The Backup Host uses the Memory-Mapped access to the **PCI Express Capabilities** register (offset 68h) to execute the failover. The Backup Host follows the ensuing procedure to take control:

1. Failover Detected:
   a. Backup Host detects the Active Host's failure condition, then starts the Failover process (*such as*, Heartbeat Message Reception timeout).
   b. Upstream port remains active in this state.

2. Upstream Port Demotion:
   a. PEX 8524 is not in Reset when the Failover process starts.
   b. **Debug Control** register Upstream Port Hot Reset and Link Down Reset Propagation Disable bit (Port 0, offset 1DCh[20]) can disable Reset generation due to a Hot Reset and the upstream port DL_Down condition. The bit is asserted, by default, for Dual-Host mode.
   c. **Silicon Revisions BB/BC only** – The serial EEPROM must be programmed with the Port 0, offset 1DCh, value in Port 0 and the NT Port Virtual Interface, and the **Ingress Control** register *BIOS Enumeration Fix Disable* bit (660h[27]) must be set to 1.
   d. As one of the first steps in the Failover process, the Backup Host demotes the upstream port by writing 0000b into the **PCI Express Capabilities** register (PCI Express Endpoint) *Device/Port Type* field (offset 68h[23:20]).
   e. Transaction Layer Ingress snoops this access and informs Event *d* detection to the TLP-destined Transparent upstream port.
   f. Event *e* causes the upstream port Physical Layer to bring down its upstream link, which generates the upstream port DL_Down condition.
   g. Event *e* also causes the upstream port to change its *Device/Port Type* field to "PCI Express Endpoint", and changes the *PCI Class Code* to "other bridged devices". The Transparent upstream port becomes a PCI Express endpoint.
   h. Upstream port Transaction Layer Egress module drops all outgoing packets to the upstream device when it comprehends the upstream port DL_Down condition.
   i. **Debug Control** register *Upstream Port Number* and *NT Port Number* fields (offset 1DCh[11:8 and 27:24], respectively) remain unchanged in this state.

j. Downstream port internal modules forward/generate the packet for the upstream device, which is transmitted to the previous upstream port, and the packets are dropped by the demoted upstream port Transaction Layer Egress module due to this DL_Down condition.

k. When a Transaction Layer Ingress module receives TLPs from the demoted upstream connected device, the module processes the normal upstream port type of address decoding and forwards the packet to the destination port, based on AMCAM, IOCAM, or BusNoCAM lookup.

3. NT Port (Self) Promotion as a New Upstream Port:

a. Software can disable the *I/O Access Enable*, *Memory Access Enable*, *Bus Master Enable*, Interrupt generation on the NT Port Virtual Interface, and *Error Message Generation Enable* CSR bits, if it does not want to receive spurious traffic immediately after self-promotion.

Refer to the *PCI-to-PCI Bridge r1.1* **Command** register for these CSR descriptions and the **Device Control** register for *Error Message Generation Enable* CSR bits.

b. Backup Host promotes itself as an Active Host by writing 0101b into the NT Port Virtual Interface Type 0 Configuration **PCI Express Capabilities** register (Transparent upstream port) *Device/Port Type* field (offset 68h[23:20]).

c. PEX 8524 swaps the **Debug Control** register *Upstream Port Number* and *NT Port Number* fields (offset 1DCh[11:8 and 27:24], respectively) values when a Transaction Layer ingress informs Event *b* of this condition.

d. PEX 8524 processes the port transition. PEX 8524 converts the demoted Transparent upstream port to the NT Port, and the previous NT Port to the Transparent upstream port.

e. New upstream port retrieves previously programmed NT Port Virtual Interface Type 0 CSR values.

f. PEX 8524 does not swap the Configuration space value from previous upstream port to new upstream port by itself after failover. Software running in Promoted Active Host should follow the ensuing procedure to bring the system into a communicating state:

– Copy the previous upstream port Configuration space value to a new upstream port Configuration space value.

– Copy the previous NT Port Virtual Interface Type 0 endpoint Configuration space value to a new NT Port Virtual Interface Type 0 Endpoint Configuration space value.

– If possible, reset the entire hierarchy and restart the system, using full software re-enumeration.

14.3 Data Transfer through NT Port

The following discusses the Configuration registers mainly programmed for Data transfer through the NT Port.

To transfer data from NT Port Virtual Interface to NT Port Link Interface direction:

1. Assign memory space to NT Port Virtual Interface Type 0 Endpoint BARs.
2. Enable NT Port Virtual Interface Type 0 Endpoint *Memory Access Enable* bit (offset 04h[1]).
3. Enable NT Port Link Interface Type 0 Endpoint *Bus Master Enable* bit (offset 04h[2]).
4. Program NT Port Virtual Interface Type 0 Endpoint Address Translation registers with transaction completer (target) BAR value. If the application is using Lookup Table-based Address translation, it must enable the corresponding LUT Entry as well. Address Translation register values can be dynamically changed by a device driver, depending on where the requester is located. Before changing the Address Translation register values, the device driver must ensure an outstanding request is not pending to the NT Port.
5. Enable and program NT Port Virtual Interface "Send LUT Entry" registers with Requester ID (Bus, Device, and Function Numbers). "Send LUT Entry" register values can be dynamically changed by a device driver, depending on the request enabled to communicate through the PEX 8524 NT Port. Before changing the "Send LUT Entry," the device driver must ensure an outstanding request is not pending for that requester.

To transfer data from NT Port Link Interface to NT Port Virtual Interface direction:

1. Assign memory space to NT Port Link Interface Type 0 Endpoint BARs.
2. Enable NT Port Link Interface Type 0 Endpoint *Memory Access Enable* bit (offset 04h[1]).
3. Enable NT Port Virtual Interface Type 0 Endpoint *Bus Master Enable* bit (offset 04h[2]).
4. Program NT Port Link Interface Type 0 Endpoint Address Translation registers with transaction completer (target) BAR value. Address translation register values can be dynamically changed by a device driver, depending on where the requester located the Virtual Link side. Before changing the Address translation register values, the device driver must ensure an outstanding request is not pending to the NT Port.
5. Enable and program NT Port Link Interface "Receive LUT Entry" registers with Requester Bus Number and Device Number values. "Receive LUT Entry" register values can be dynamically changed by a device driver, depending on the request enabled to communicate through the PEX 8524 NT Port. Before changing the "Receive LUT Entry," the device driver must ensure an outstanding request is not pending for that requester.

Chapter 15 NT Port Virtual Interface Registers

15.1 Introduction

This chapter defines the registers for the PEX 8524 Non-Transparent (NT) Port Virtual Interface (interface) registers. The NT Port includes two sets of Configuration, Capability, Control, and Status registers to support the Virtual and Link Interfaces. NT Port Virtual Interface register mapping is defined in Table 15-1.

NT Port Link Interface registers are defined in Chapter 16, "NT Port Link Interface Registers." Transparent mode registers are defined in Chapter 11, "PEX 8524 Transparent Mode Port Registers."

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r2.3*
- *PCI Power Mgmt. r1.1*
- *PCI Express Base r1.0a*

Table 15-1. NT Port Virtual Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Configuration Header Registers			New Capability Pointer (40h)	00h … 34h … 3Ch
	Next Capability Pointer (48h)		Capability ID (01h)	40h
Power Management Capability Registers				44h
	Next Capability Pointer (68h)		Capability ID (05h)	48h
Message Signaled Interrupt Capability Registers				… 64h
	Next Capability Pointer (00h)		Capability ID (10h)	68h
PCI Express Capability Registers				… 80h
Reserved				84h – 8Ch
NT Port Registers				90h … FFh
Next Capability Offset (FB4h)	1h		Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers				104h 108h
Reserved				10Ch – 134h
Next Capability Offset (148h)	1h		Extended Capability ID (0004h)	138h
Power Budgeting Extended Capability Registers				… 144h
Next Capability Offset (000h)	1h		Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers				… 1C4h
PLX-Specific Registers				1C8h … C08h
PEX 8524 Non-Transparent Bridging-Specific Registers				C3Ch … FB0h
Next Capability Offset (138h)	1h		PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Capability Registers				… FFCh

15.2 Register Access

The PEX 8524 NT Port Virtual Interface implements a 4-KB Configuration space. The lower 256 bytes (offsets 00h through FFh) is the PCI-compatible Configuration space, and the upper 960 Dwords (offsets 100h through FFFh) is the PCI Express Extended Configuration space. The PEX 8524 supports four mechanisms for accessing NT Port Virtual Interface registers:

- PCI Express Base r1.0a Configuration Mechanism
- PLX-Specific Memory-Mapped Configuration Mechanism
- PLX-Specific I/O-Mapped Configuration Mechanism
- PLX-Specific Cursor Mechanism

15.2.1 *PCI Express Base r1.0a* Configuration Mechanism

The PCI Express Configuration mechanism is divided into two mechanisms:

- *PCI r2.3*-Compatible Configuration
- PCI Express Enhanced Configuration

The *PCI r2.3*-compatible Configuration mechanism provides standard access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Virtual Interface Configuration register space. The PCI Express Enhanced Configuration mechanism provides access to the remaining 4 KB (offsets 100h through FFFh).

15.2.1.1 *PCI r2.3*-Compatible Configuration Mechanism

The *PCI r2.3*-Compatible Configuration mechanism provides standard access to the PEX 8524 NT Port Virtual Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration space. (Refer to Figure 15-1.) This mechanism is used to access the PEX 8524 NT Port Virtual Interface Type 0 (PCI endpoint) registers:

- Configuration Header Registers
- Power Management Capability Registers
- Message Signaled Interrupt Capability Registers
- PCI Express Capability Registers

The *PCI r2.3*-Compatible Configuration mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8524 Configuration registers. The PEX 8524 upstream port captures the Bus and Device Numbers assigned by the upstream device on the PCI Express link attached to thePEX 8524 upstream port, as required by the *PCI Express Base r1.0a*.

The PEX 8524 decodes all Type 1 Configuration accesses received on its upstream port, when any of the following conditions exist:

- If the Bus Number specified in the Configuration access is the number of the PEX 8524 internal virtual PCI Bus, the PEX 8524 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the NT Port Virtual Interface (or to the PCI-to-PCI bridge in one of the PEX 8524 downstream Transparent ports), the PEX 8524 processes the Read or Write request to the downstream port register specified in the original Type 1 Configuration access.
  - If the specified Device Number does not correspond to any of the PEX 8524 downstream port Device Numbers, the PEX 8524 responds with an *Unsupported Request* (UR).

Because the *PCI r2.3*-Compatible Configuration Mechanism is limited to the first 256 bytes of the NT Port Virtual Interface Configuration register space, one of the following must be used to access beyond byte FFh:

- PCI Express Enhanced Configuration Mechanism
- PLX-Specific Memory-Mapped Configuration Mechanism
- PLX-Specific Cursor Mechanism

The *PCI r2.3*-Compatible Configuration mechanism uses the same Request format as the PCI Express Enhanced Configuration Mechanism. For PCI-compatible Configuration Requests, the Extended Register Address field must be all zeros (0).

Do not use this mechanism to access the PEX 8524 Device-Specific Configuration registers.

15.2.1.2 PCI Express Enhanced Configuration Mechanism

The PCI Express Enhanced Configuration Mechanism uses a flat, Root Complex Memory-Mapped Address space to access device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and the Memory data returns the addressed register's contents. The Root Complex converts the Memory transaction into a Configuration transaction. This mechanism is used to access the NT Port Virtual Interface Type 0 registers:

- Configuration Header Registers
- Power Management Capability Registers
- Message Signaled Interrupt Capability Registers
- PCI Express Capability Registers
- Device Serial Number Extended Capability Registers
- Power Budgeting Extended Capability Registers
- Virtual Channel Extended Capability Registers
- Advanced Error Reporting Capability Registers

Do not use this mechanism to access the PEX 8524 Device-Specific Configuration registers.

15.2.2 PLX-Specific Memory-Mapped Configuration Mechanism

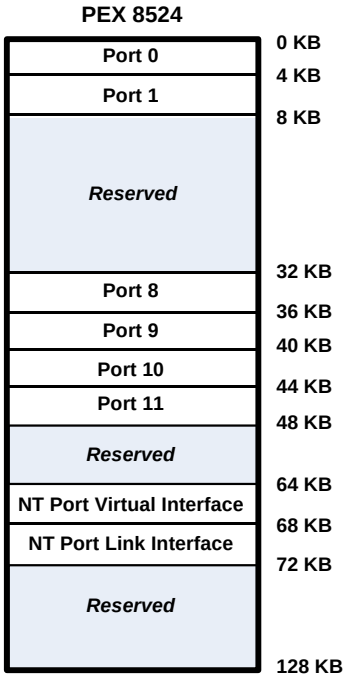
The PLX-Specific Memory-Mapped Configuration mechanism provides a method to access the PEX 8524 port Configuration registers of all ports in a single Memory map, as illustrated in Figure 15-1. The registers of each port are contained within a 4-KB range.

When the NT Port is enabled at Fundamental reset, the NT Port Virtual Interface and Link Interface Configuration registers are used in place of the Type 1 Configuration registers for that port.

To utilize the PLX-Specific Memory-Mapped Configuration mechanism, use the *PCI r2.3*-Compatible Configuration Mechanism to program the PEX 8524 upstream port **Base Address 0** and **Base Address 1** registers. After the PEX 8524 upstream port Memory-Mapped register Base address is set, the upstream port register is accessed with memory reads from and writes to the configuration space registers. The NT Port registers are accessed with Memory reads from and writes to the 4-KB range, starting at offset 64 KB for the Virtual Interface registers and offset 68 KB for the Link Interface registers.

This mechanism is used to access all PEX 8524 Configuration registers.

Figure 15-1. PEX 8524 Register Offset from Upstream Port BAR0/1 Base Address (Non-Transparent Mode)

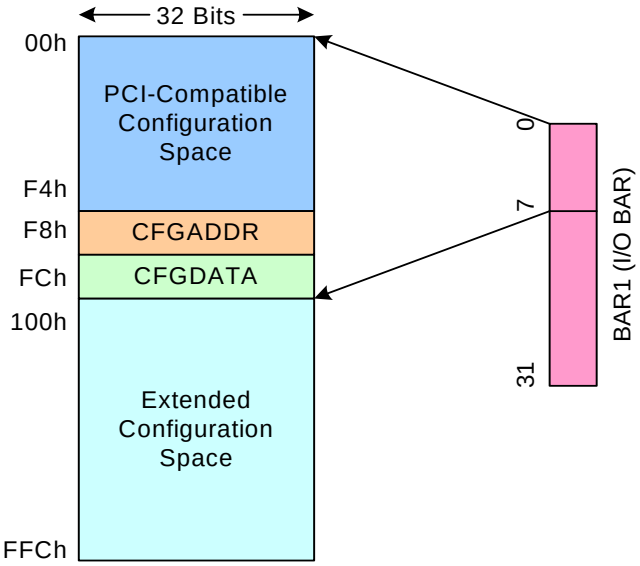


15.2.3 PLX-Specific I/O-Mapped Configuration Mechanism

The first 256 bytes of NT Port Virtual Interface Configuration Space registers are directly accessible by I/O transaction. The NT Port Virtual Interface BAR1 register is used for I/O-mapped access. (Refer to Figure 15-2.)

Extended Configuration Space registers are accessed by using the Cursor mechanism in I/O space.

Figure 15-2. I/O-Mapped Configuration Space View



15.2.4 PLX-Specific Cursor Mechanism

In Figure 15-2, the software uses the **Configuration Address Window** (CFGADDR) register to point to the NT Port Virtual or Link Interface Configuration Space registers, including the Extended Space register.

Software uses the **Configuration Data Window** (CFGDATA) register to write to or read from the selected Configuration Space registers.

Refer to Section 15.8.4, "NT Port Cursor Mechanism Control Registers," for the register descriptions.

15.3 Register Descriptions

The remainder of this chapter details the PEX 8524 NT Port Virtual Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8524 NT Port Virtual and Link Interfaces
- Type (*such as* RW or HwInit; refer to Table 11-3, "Register Types, Grouped by User Accessibility." for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8524 serial EEPROM initialization feature
- Default power-on/reset value

15.4 Configuration Header Registers

Table 15-2. Type 0 Configuration Space Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST *(Not Supported)*	Configuration Layout Type and Function Type	Master Latency Timer	Cache Line Size	0Ch
Reserved				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Reserved			New Capability Pointer (40h)	34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch

Register 15-1. 00h Product Identification

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Vendor ID** Unless overwritten by the serial EEPROM, returns the PLX PCI-SIG-assigned Vendor ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Vendor ID with another Vendor ID.	HwInit	Yes	10B5h
31:16	**Device ID** Unless overwritten by the serial EEPROM, 8532h is returned by the PEX 8524V and 8524h is returned by the PEX 8524, the PLX-assigned Device ID. The Serial EEPROM register initialization capability is used to replace the PLX-assigned Device ID with another Device ID.	HwInit	Yes	8532h (PEX 8524V) 8524h (PEX 8524)

Register 15-2. 04h Status/Command

Bit(s)	Description	Type	Serial EEPROM	Default
	Command			
0	**I/O Access Enable** 0 = PEX 8524 ignores I/O requests on the NT Port Virtual Interface 1 = PEX 8524 accepts I/O requests received on the NT Port Virtual Interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8524 ignores Memory requests on the NT Port Virtual Interface 1 = PEX 8524 accepts Memory requests received on the NT Port Virtual Interface	RW	Yes	0
2	**Bus Master Enable** Controls Memory request forwarding in the upstream direction. Does not affect message forwarding nor Completions in the upstream direction. 0 = PEX 8524 handles Memory requests received on the NT Port's Link Interface as Unsupported Requests (UR); for Non-Posted Requests, PEX 8524 returns a Completion with UR completion status 1 = PEX 8524 forwards Memory requests in the upstream direction	RW	Yes	0
3	**Special Cycle Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
4	**Memory Write and Invalidate** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
5	**VGA Palette Snoop** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
6	**Parity Error Response Enable** Controls the *Master Data Parity Error*.	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
8	**SERR# Enable** Controls the *Signaled System Error* bit. When 1, enables reporting of Fatal and Non-Fatal errors detected by the NT Port Virtual Interface to the Root Complex.	RW	Yes	0
9	**Fast Back-to-Back Transactions Enabled** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
10	**Interrupt Disable** 0 = NT Port Virtual Interface enabled to generate INT*x* Interrupt messages 1 = NT Port Virtual Interface prevented from generating INT*x* Interrupt messages	RW	Yes	0
15:11	***Reserved***			00h

Register 15-2. 04h Status/Command *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Status			
18:16	***Reserved***			000b
19	**Interrupt Status** 0 = No INT*x* Interrupt pending 1 = INT*x* Interrupt pending internally to NT Port Virtual Interface	RO	Yes	0
20	**Capabilities List** Set to 1, as required by the *PCI Express Base r1.0a*.	RO	Yes	1
21	**66 MHz Capable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
22	***Reserved***			0
23	**Fast Back-to-Back Transactions Capable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
24	**Master Data Parity Error** If the *Parity Error Response Enable* bit is set to 1, the NT Port Virtual Interface sets this bit to 1 when the NT Port: • Forwards the poisoned TLP Write request from the Link Interface to the Virtual Interface, **or** • Receives a Completion marked as poisoned on the Virtual Interface If the *Parity Error Response Enable* bit is cleared to 0, the PEX 8524 never sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL Timing** ***Not supported*** Always cleared to 00b.	RO	No	00b
27	**Signaled Target Abort** Set to 1, when the NT Port forwards a Completion with Completer Abort (CA) status from the Link Interface to the Virtual Interface. ***Note:*** *When set during a forwarded Completion, the **Uncorrectable Error Status** register Completer Abort Status bit (offset FB8h[15]) is not updated, because the NT Port does not log the requests that it forwards.*	RW1C	Yes	0

Register 15-2. 04h Status/Command *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
28	**Received Target Abort** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
29	**Received Master Abort** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
30	**Signaled System Error** When the *SERR# Enable* bit is set to 1, the NT Port Virtual Interface sets Signaled System Error to 1 when it transmits an ERR_FATAL or ERR_NONFATAL message to its upstream port. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** The NT Port Virtual Interface sets this bit to 1 when it receives a Poisoned TLP, regardless of the *Parity Error Response Enable* bit state. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 15-3. 08h Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the silicon revision (AAh, BBh, or BCh for PEX 8524V; BBh or BCh for PEX 8524), the PLX-assigned Revision ID for this version of the PEX 8524. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Revision ID with another Revision ID. ***Note:*** ***Silicon Revision BB only*** *– Bit 0 is hardwired to 1 and is not programmable by serial EEPROM.* ***Silicon Revision BC only*** *– Bits [2:0] are hardwired to 100b and are not programmable by serial EEPROM.*	RO	Yes (Refer to Note)	AAh, BBh, or BCh (PEX 8524V) or BBh or BCh (PEX 8524)
Class Code				**068000h**
15:8	**Programming Interface** ***Reserved***, as required by the *PCI r2.3*.	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 15-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Cache Line Size** Implemented as a Read-Write field for Conventional PCI compatibility purposes and does not impact PEX 8524 functionality.	RW	Yes	00h
15:8	**Master Latency Timer** ***Not supported*** Cleared to 00h.	RO	No	00h
22:16	**Configuration Layout Type** Type 0 Configuration Header for NT Port.	RO	Yes	00h
23	**Function Type** 0 = PEX 8524 is a single-function device	RO	Yes	0
31:24	**BIST** ***Not supported***	RO	No	00h

Register 15-5. 14h Base Address 1

Bit(s)	Description	Type	Serial EEPROM	Default
0	**I/O Space Indicator** I/O BAR when offset D0h[1:0] = 11b; otherwise, ***reserved***.	RO	Yes	1
7:1	***Reserved***			0h
31:8	**I/O Base Address** 256-byte I/O Space Base address when offset D0h[1:0] = 11b; otherwise, ***reserved***.	RW	Yes	0000_00h

Note: *When software writes to the NT Port Virtual Interface **Base Address 1** (**BAR1**) register, the value is automatically copied to the **NT Port Virtual Interface BAR1 Shadow** register (offset D6Ch).*

*Software (device driver) must copy the **BAR1** register value to the **BAR1 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 14h or D6Ch, and write the value to Port 8, offset D6Ch*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 14h or D6Ch, and write the value to Port 0, offset D6Ch*

Register 15-6. 18h Base Address 2

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	Yes	0
2:1	**Memory Map Type** 00b = Mappable anywhere in 32-bit Memory space 01b, 10b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
11:4	***Reserved***			00h
31:12	**Base Address 2** Contains the software-assigned Memory Space Base address: • Enabled and sized by the **NT Port Virtual Interface BAR2 Setup** register • Used for Memory transactions crossing the NT Port • Minimum Address range requested is 4 KB • Uses direct address translation • Includes a **Limit** register	RW	Yes	0000_0h

Note: *When software writes to the NT Port Virtual Interface **Base Address 2** (**BAR2**) register, the value is automatically copied to the **NT Port Virtual Interface BAR2 Shadow** register (offset D70h).*

*Software (device driver) must copy the **BAR2** register value to the **BAR2 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 18h or D70h, and write the value to Port 8, offset D70h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 18h or D70h, and write the value to Port 0, offset D70h*

Register 15-7. 1Ch Base Address 3 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	Yes	0
2:1	**Memory Map Type** 00b = Mappable anywhere in 32-bit Memory Address space 01b, 10b, 11b = ***Not allowed***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
17:4	***Reserved***			0000h
31:18	**Base Address 3** Contains the software-assigned Memory Space Base address: • Enabled and sized by the **NT Port Virtual Interface BAR3 Setup** register • No **Limit** register • Used for Memory transactions crossing the NT Port • Minimum Address range requested is 256 KB • Uses LUT address translation	RW	Yes	0000h

Note: *When software writes to the NT Port Virtual Interface **Base Address 3** (**BAR3**) register, the value is automatically copied to the **NT Port Virtual Interface BAR3 Shadow** register (offset D74h).*

*Software (device driver) must copy the **BAR3** register value to the **BAR3 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 1Ch or D74h, and write the value to Port 8, offset D74h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 1Ch or D74h, and write the value to Port 0, offset D74h*

Register 15-8. 20h Base Address 4

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	Yes	0
2:1	**Memory Map Type** 00b = BAR is mapped anywhere in 32-bit Memory space 10b = BAR is mapped anywhere in 64-bit Memory space 01b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
11:4	***Reserved***			00h
31:12	**Base Address 4** Contains the software-assigned Memory Space Base address: • Enabled and sized by the **NT Port Virtual Interface BAR4/5 Setup** register • Used for Memory transactions crossing the NT Port • Minimum address range requested is 4 KB • Uses direct address translation	RW	Yes	0000_0h

Note: *When software writes to the NT Port Virtual Interface **Base Address 4** (**BAR4**) register, the value is automatically copied to the **NT Port Virtual Interface BAR4 Shadow** register (offset D78h).*

*Software (device driver) must copy the **BAR4** register value to the **BAR4 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 20h or D78h, and write the value to Port 8, offset D78h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 20h or D78h, and write the value to Port 0, offset D78h*

Register 15-9. 24h Base Address 5

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address 5** NT Port Virtual Interface upper 32-bit address if BAR4/5 is implemented as a 64-bit BAR; otherwise, ***reserved***. RW, based on the **NT Port Virtual Interface BAR5 Setup** register. The BAR4/5 group uses direct address translation. Contains a **Limit** register.	RW	Yes	0-0h

Note: *When software writes to the NT Port Virtual Interface **Base Address 5** (**BAR5**) register, the value is automatically copied to the **NT Port Virtual Interface BAR5 Shadow** register (offset D7Ch).*

*Software (device driver) must copy the **BAR5** register value to the **BAR5 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 24h or D7Ch, and write the value to Port 8, offset D7Ch*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 24h or D7Ch, and write the value to Port 0, offset D7Ch*

Register 15-10. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Subsystem Vendor ID** Unless overwritten by the serial EEPROM, returns the PLX PCI-SIG-assigned Vendor ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Vendor ID with another Vendor ID.	HwInit	Yes	10B5h
31:16	**Subsystem ID** Unless overwritten by the serial EEPROM, the PEX 8524 returns 8532h (PEX 8524V) or 8524h (PEX 8524), the PLX-assigned Device ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX-assigned Device ID with another Device ID.	HwInit	Yes	8532h (PEX 8524V) 8524h (PEX 8524)

Register 15-11. 34h New Capabilities Pointer

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**New Capability Pointer** Default 40h points to the **Power Management Capabilities** register.	RO	Yes	40h
31:8	***Reserved***			0000_00h

Register 15-12. 3Ch Interrupt

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Interrupt Line** Interrupt Line Routing value communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
15:8	**Interrupt Pin** Identifies the Conventional PCI interrupt message(s) that the device (or device function) uses. When values = 01h, 02h, 03h, and 04h, maps to Conventional PCI interrupt messages for INTA#, INTB#, INTC#, and INTD#, respectively. When 00h, indicates that the device does not use Conventional PCI interrupt message(s). Only values 00h or 01h are allowed in the PEX 8524.	RO	Yes	01h
31:16	***Reserved***			0000h

15.5 Power Management Capability Registers

This section details the NT Port Virtual Interface Power Management registers. The register map is defined in Table 15-3.

Table 15-3. Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Power Management Capabilities		Next Capability Pointer (48h)	Capability ID (01h)	40h
Data	Power Management Control/ Status Bridge Extensions	Power Management Status and Control		44h

Register 15-13. 40h Power Management Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Capability ID** Default = 01h – only value allowed. Indicates that the data structure currently being pointed to is the PCI Power Management data structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **Message Signaled Interrupt Capability** register.	RO	Yes	48h
18:16	**Version** Default = 010b – only value allowed.	RO	Yes	010b
19	**PME Clock** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
20	***Reserved***			0
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** ***Not supported*** Default 000b indicates that the PEX 8524 does ***not support*** Auxiliary Current requirements.	RO	Yes	000b
25	**D1 Support** ***Not supported*** Default 0 indicates that the PEX 8524 does ***not support*** the D1 Power state.	RO	No	0
26	**D2 Support** ***Not supported*** Default 0 indicates that the PEX 8524 does ***not support*** the D2 Power state.	RO	No	0
31:27	**PME Support** Default 0000_0b indicates that the NT Port does ***not*** forward PME messages.	RO	Yes	0000_0b

Register 15-14. 44h Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
Power Management Status and Control				
1:0	**Power State** This field is used to determine the current power state of the port, and to set the port into a new power state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
7:2	***Reserved***	RO	No	0h
8	**PME Enable** 0 = Disables PME generation	RO	No	0[a]
12:9	**Data Select** RW by Serial EEPROM mode only[b]. Bits [12:9] select the **Data** and **Data Scale** registers. 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	RO	Yes	0h
14:13	**Data Scale** RW by Serial EEPROM mode only[b]. There are four internal **Data Scale** registers per port. Bits [12:9], *Data Select*, select the **Data Scale** register.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port	RO	No	0[a]
Power Management Control/Status Bridge Extensions				
21:16	***Reserved***			0-0h
22	**B2/B3 Support** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
23	**Bus Power/Clock Control Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
Power Management Data				
31:24	**Data** RW by Serial EEPROM mode only[b]. There are four internal **Data** registers per port. Bits [12:9], *Data Select*, select the **Data** register.	RO	Yes	00h

a. Because the PEX 8524 does not support auxiliary power, this bit is not sticky, and is always cleared to 0 at power-on reset.

*b. With no serial EEPROM, reads return 0h for the **Data Scale** and **Data** registers (for all Data Selects).*

15.6 Message Signaled Interrupt Capability Registers

The Message Signaled Interrupt (MSI) Capability registers are defined in Section 11.8, "Message Signaled Interrupt Capability Registers." Table 15-4 defines the register map used by the NT Port Virtual Interface.

Table 15-4. Message Signaled Interrupt Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Message Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
Message Address[31:0]				4Ch
Message Upper Address[63:32]				50h
Reserved		Message Data		54h
Reserved				58h – 64h

15.7 PCI Express Capability Registers

This section details the PEX 8524 PCI Express Capability registers. The Hot Plug capabilities, command, status, and events are included in these registers. The register map is defined in Table 15-5.

Table 15-5. PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capabilities		Next Capability Pointer (00h)	Capability ID (10h)	68h
Device Capabilities				6Ch
Device Status		Device Control		70h
Link Capabilities				74h
Link Status		Link Control		78h
Reserved				7Ch – 8Ch

Register 15-15. 68h PCI Express Capability List and Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
PCI Express Capability List				
7:0	**Capability ID** Set to 10h by default, as required by the *PCI Express Base r1.0a*.	RO	Yes	10h
15:8	**Next Capability Pointer** 00h = PCI Express Capability is the last capability in the first 256-byte Configuration space of the PEX 8524 NT Port Virtual Interface capability list The PEX 8524 NT Port Virtual Interface Extended Capabilities list starts at 100h.	RO	Yes	00h
PCI Express Capabilities				
19:16	**Capability Version** Set to 1h.	RO	Yes	1h
23:20	**Device/Port Type** PCI Express Endpoint device.	RO	Yes	0h
24	**Slot Implemented** ***Not valid for PCI Express Endpoint devices.***	RO	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 0000_0b, because the Base message and MSI messages are the same.	RO	Yes	0000_0b
31:30	***Reserved***			00b

Register 15-16. 6Ch Device Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Maximum Payload Size Supported** 000b = NT Port Virtual Interface supports 128-byte maximum payload 001b = NT Port Virtual Interface supports 256-byte maximum payload No other values are supported. ***Note:*** *Serial EEPROM must not load greater than 256 bytes Maximum Payload Size.*	RO	Yes	001b
4:3	**Phantom Functions Supported** ***Not supported*** Cleared to 00b.	RO	Yes	00b
5	**Extended Tag Field Supported** ***Not supported*** 0 = Maximum Tag field is 5 bits 1 = Maximum Tag field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency**	RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency**	RO	Yes	000b
12	**Attention Button Present** No Attention button present for NT Virtual Interface.	RO	No	0
13	**Attention Indicator Present** No Attention indicator present for NT Virtual Interface.	RO	No	0
14	**Power Indicator Present** No Power indicator present for NT Virtual Interface.	RO	No	0
17:15	***Reserved***			000b
25:18	**Captured Slot Power Limit Value** For the NT Port Virtual Interface register, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Scale* field.	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Virtual Interface register, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Value* field. 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***			0h

Register 15-17. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables NT Port Virtual Interface to report Correctable errors to local host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables NT Port Virtual Interface to report Non-Fatal errors to local host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables NT Port Virtual Interface to report Fatal errors to local host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables NT Port Virtual Interface to report Unsupported Request errors to local host	RW	Yes	0
4	**Relaxed Ordering Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
7:5	**Maximum Payload Size** The NT Port Virtual Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Virtual Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capabilities** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]). for the Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = Indicates that initially the PEX 8524 port is configured to support a Maximum Payload Size of 128 bytes 001b = Indicates that initially the PEX 8524 port is configured to support a Maximum Payload Size of 256 bytes No other values are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b

Register 15-17. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
8	**Extended Tag Field Enable** ***Not supported*** Cleared to 0.	RO	No	0
9	**Phantom Functions Enable** ***Not supported*** Cleared to 0.	RO	No	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported*** Cleared to 0.	RO	No	0
11	**No Snoop Enable** ***Not supported*** Cleared to 0.	RO	No	0
14:12	**Maximum Read Request Size** ***Not supported*** Cleared to 000b.	RO	No	000b
15	***Reserved***			0
	Device Status			
16	**Correctable Error Detected** 1 = NT Port detected a Correctable Error Set when the NT Port Virtual Interface detects a Correctable Error, regardless of the bit 0 (*Correctable Error Reporting Enable* bit) state.	RW1C	Yes	0
17	**Non-Fatal Error Detected** 1 = NT Port Virtual Interface detected a Non-Fatal Error Set when the NT Port Virtual Interface detects a Non-Fatal Error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable* bit) state.	RW1C	Yes	0
18	**Fatal Error Detected** 1 = NT Port Virtual Interface detected a Fatal Error Set when the NT Port Virtual Interface detects a Fatal Error, regardless of the bit 2 (*Fatal Error Reporting Enable* bit) state.	RW1C	Yes	0
19	**Unsupported Request Detected** 1 = NT Port Virtual Interface detected an Unsupported Request Set when the NT Port Virtual Interface detects an Unsupported Request, regardless of the bit 3 (*Unsupported Request Reporting Enable* bit) state.	RW1C	Yes	0
20	**Auxiliary (AUX) Power Detected** ***Not supported*** Cleared to 0.	RO	No	0
21	**Transactions Pending** Because the PEX 8524 NT Port is a bridging device, it does not track completion for the corresponding non-posted transactions. Therefore, the NT Port Virtual Interface does not implement Transactions Pending.	RO	No	0
31:22	***Reserved***			000h

Register 15-18. 74h Link Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Maximum Link Speed** Set to 0001b for 2.5 Gbps.	RO	Yes	0001b
9:4	**Maximum Link Width** Actual link width is set by signal ball strapping options. The PEX 8524 Maximum Link Width is x8 = 00_1000b (Station 0), or x16 = 01_0000b (Station 1).	RO	No	Strap levels
11:10	**Active State Power Management (ASPM) Support** Indicates the level of ASPM supported by the port. 01b = L0s link power state entry is supported All other values are ***reserved***.	RO	Yes	01b
14:12	**L0s Exit Latency** 101b = NT Port Virtual Interface L0s Exit Latency is between 1 and 2 µs	RO	No	101b
17:15	**L1 Exit Latency** 101b = NT Port Virtual Interface L1 Exit Latency is between 16 and 32 µs	RO	Yes	101b
23:18	***Reserved***			0-0h
31:24	**Port Number** The NT Port Number is selected by signal ball strapping options. Refer to STRAP_NT_UPSTRM_PORTSEL[3:0] for details.	HwInit	No	Set by strap levels

Register 15-19. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** Not applicable to the NT Port Virtual Interface, because no external port connection exists.	RW	Yes	00b
2	***Reserved***			0
3	**Read Completion Boundary (RCB)** ***Not supported*** Cleared to 0.	RO	Yes	0
4	**Link Disable** For NT Port – ***Reserved.***	RO	No	0
5	**Retrain Link** For NT Port – ***Reserved.***	RO	No	0
6	**Common Clock Configuration** Not applicable to the NT Port Virtual Interface, because no external port connection exists.	RW	Yes	0
7	**Extended SYNC** Not applicable to the NT Port Virtual Interface, because no external port connection exists.	RW	Yes	0
15:8	***Reserved***			00h
	Link Status			
19:16	**Link Speed** The NT Port Virtual Interface is set to 1h for 2.5 Gbps.	RO	Yes	1h
25:20	**Negotiated Link Width** Not applicable to the NT Port Virtual Interface, because no external port connection exists.	RO	Yes	00_0001b
26	**Training Error** For endpoint devices – ***Reserved.***	RO	No	0
27	**Link Training** For endpoint devices – ***Reserved.***	RO	No	0
28	**Slot Clock Configuration** Because there is no external connection to the NT Port Virtual Interface, Slot Clock Configuration is always 0, which indicates that the PEX 8524 uses an independent clock.	HwInit	Yes	0
31:29	***Reserved***			000b

15.8 NT Port Registers

15.8.1 NT Port Virtual Interface IRQ Doorbell Registers

This section details the PEX 8524 NT Port Virtual Interface Interrupt Request (IRQ) Doorbell registers. The register map is defined in Table 15-6.

Table 15-6. NT Port Virtual Interface Interrupt Request (IRQ) Doorbell Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Set Virtual Interface IRQ	90h
Reserved	Clear Virtual Interface IRQ	94h
Reserved	Set Virtual Interface IRQ Mask	98h
Reserved	Clear Virtual Interface IRQ Mask	9Ch
Reserved	Set Link Interface IRQ	A0h
Reserved	Clear Link Interface IRQ	A4h
Reserved	Set Link Interface IRQ Mask	A8h
Reserved	Clear Link Interface IRQ Mask	ACh

Register 15-20. 90h Set Virtual Interface IRQ

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Set Virtual IRQ** Controls the state of the Virtual Interface Doorbell Interrupt request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register sets the corresponding Interrupt request. The Virtual Interface interrupt is asserted if the following conditions exist: • This register (offset 90h or 94h) value is non-zero, and, • The corresponding mask bit in the **Set Virtual Interface IRQ Mask** or **Clear Virtual Interface IRQ Mask** register (offset 98h or 9Ch, respectively) is not set, and, • Interrupts (either INT*x* or MSI) are enabled	RW1S	Yes	0000h
31:16	***Reserved***			0000h

Register 15-21. 94h Clear Virtual Interface IRQ

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Clear Virtual IRQ** Controls the state of the Virtual Interface Doorbell Interrupt request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register clears the corresponding Interrupt request. The Virtual Interface interrupt is asserted if the following conditions exist: • This register (offset 94h or 90h) value is non-zero, and, • The corresponding mask bit in the **Set Virtual Interface IRQ Mask** or **Clear Virtual Interface IRQ Mask** register (offset 98h or 9Ch, respectively) is not set, and, • Interrupts (either INT*x* or MSI) are enabled	RW1C	Yes	0000h
31:16	***Reserved***			0000h

Register 15-22. 98h Set Virtual Interface IRQ Mask

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Set Virtual IRQ Mask** Virtual Interface interrupt IRQ Mask Set. Reading returns the state of the mask bits. 0 = Corresponding interrupt request bit in the **Set Virtual Interface IRQ** register (offset 90h) is unmasked 1 = Corresponding interrupt request bit in the **Set Virtual Interface IRQ** register (offset 90h) is masked/disabled Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register clears the corresponding interrupt mask bit.	RW1S	Yes	FFFFh
31:16	***Reserved***			0000h

Register 15-23. 9Ch Clear Virtual Interface IRQ Mask

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Clear Virtual IRQ Mask** Controls the state of the Virtual Interface Interrupt Request bits. Reading returns the status of the bits. 0 = Corresponding interrupt request bit in the **Clear Virtual Interface IRQ** register (offset 94h) is unmasked 1 = Corresponding interrupt request bit in the **Clear Virtual Interface IRQ** register (offset 94h) is masked/disabled Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register clears the corresponding interrupt mask bit.	RW1C	Yes	FFFFh
31:16	***Reserved***			0000h

Register 15-24. A0h Set Link Interface IRQ

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Set Link IRQ** Controls the state of the Link Interface Doorbell Interrupt request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register sets the corresponding Interrupt request. The Link Interface interrupt is asserted if the following conditions exist: • This register (offset A0h or A4h) value is non-zero, and, • The corresponding mask bit in the **Set Link Interface IRQ Mask** or **Clear Link Interface IRQ Mask** register (offset A8h or ACh, respectively) is not set, and, • Interrupts (either INT*x* or MSI) are enabled	RW1S	Yes	0000h
31:16	***Reserved***			0000h

Register 15-25. A4h Clear Link Interface IRQ

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Clear Link IRQ** Controls the state of the Link Interface Doorbell Interrupt request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register clears the corresponding Interrupt request. The Link Interface interrupt is asserted if the following conditions exist: • This register (offset A4h or A0h) value is non-zero, and, • The corresponding mask bit in the **Set Link Interface IRQ Mask** or **Clear Link Interface IRQ Mask** register (offset A8h or ACh, respectively) is not set, and, • Interrupts (either INT*x* or MSI) are enabled	RW1C	Yes	0000h
31:16	***Reserved***			0000h

Register 15-26. A8h Set Link Interface IRQ Mask

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Set Link IRQ Mask** Link Interface Interrupt IRQ Mask Set. Reading returns the state of the IRQ mask. 0 = Corresponding interrupt request bit in the **Set Link Interface IRQ** register (offset A0h) is unmasked 1 = Corresponding interrupt request bit in the **Set Link Interface IRQ** register (offset A0h) is masked/disabled Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register sets the corresponding interrupt mask bit.	RW1S	Yes	FFFFh
31:16	***Reserved***			0000h

Register 15-27. ACh Clear Link Interface IRQ Mask

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Clear Link IRQ Mask** Link Interface Interrupt IRQ Mask Clear. Reading returns the state of the IRQ mask. 0 = Corresponding interrupt request bit in the **Clear Link Interface IRQ** register (offset A4h) is unmasked 1 = Corresponding interrupt request bit in the **Clear Link Interface IRQ** register (offset A4h) is masked/disabled Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register clears the corresponding interrupt mask bit.	RW1C	Yes	FFFFh
31:16	***Reserved***			0000h

15.8.2 NT Port Scratchpad (Mailbox) Registers

The PEX 8524 NT Port Scratchpad (Mailbox) registers are defined in Section 16.8.2, "NT Port Scratchpad (Mailbox) Registers." Table 15-7 defines the register map used by the NT Port Virtual Interface.

Table 15-7. PEX 8524 NT Port Scratchpad (Mailbox) Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Scratchpad_0				B0h
NT Port Scratchpad_1				B4h
NT Port Scratchpad_2				B8h
NT Port Scratchpad_3				BCh
NT Port Scratchpad_4				C0h
NT Port Scratchpad_5				C4h
NT Port Scratchpad_6				C8h
NT Port Scratchpad_7				CCh

15.8.3 NT Port Virtual Interface BAR Setup Registers

This section details the **NT Port Virtual Interface BAR Setup** registers. The register map is defined in Table 15-8.

The **NT Port Virtual Interface BAR*x* Setup** (offsets D0h through E0h) register values are shadowed in the corresponding **NT Port Virtual Interface BAR*x* Setup Shadow** registers (offsets D80h through D90h, respectively). When software writes to an **NT Port Virtual Interface BAR*x* Setup** register, the value is automatically copied to the corresponding **NT Port Virtual Interface BAR*x* Setup Shadow** register. If the **NT Port Virtual Interface BAR*x* Setup** registers are programmed by serial EEPROM, the **NT Port Virtual Interface BAR*x* Setup Shadow** registers must also be programmed by serial EEPROM, to the same respective register values.

Table 15-8. PEX 8524 NT Port Virtual Interface BAR Setup Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Virtual Interface BAR1 Setup				D0h
NT Port Virtual Interface BAR2 Setup				D4h
NT Port Virtual Interface BAR3 Setup				D8h
NT Port Virtual Interface BAR4/5 Setup				DCh
NT Port Virtual Interface BAR5 Setup				E0h
Reserved			E4h –	F4h

Register 15-28. D0h NT Port Virtual Interface BAR1 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	**I/O BAR1 Enable** 11b = Enables Virtual Interface **BAR1** as an I/O BAR. All other values disable **BAR1**.	RW	Yes	11b
31:2	***Reserved***			0-0h

Note: *Software must copy the **BAR1 Setup** register value to the **BAR1 Setup Shadow** register (D80h) in the non-NT Station:*

- *If the NT Port is one of Ports 0 through 3, software must read the value in NT Port Virtual Interface, offset D0h or D80h, and write the value to Port 8, offset D80h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset D0h or D80h, and write the value to Port 0, offset D80h*

Register 15-29. D4h NT Port Virtual Interface BAR2 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
2:1	**BAR2 Type** 00b = Selects 32-bit Memory BAR No other values are allowed.	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
30:12	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding bits in **BAR2** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR2** are RW bits	RW	Yes	0000_0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all bits in **BAR2** read 0 1 = **BAR2** is enabled, Size and Type specified in this register	RW	Yes	0

Note: *Software must copy the **BAR2 Setup** register value to the **BAR2 Setup Shadow** register (D84h) in the non-NT Station:*

- *If the NT Port is one of Ports 0 through 3, software must read the value in NT Port Virtual Interface, offset D4h or D84h, and write the value to Port 8, offset D84h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset D4h or D84h, and write the value to Port 0, offset D84h*

Register 15-30. D8h NT Port Virtual Interface BAR3 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
15:1	***Reserved***			0-0h
19:16	**BAR3 LUT Page Size** Selects the page size of the Virtual Interface **BAR3** Address range. The total size of this range is dependent on the page size. When the *BAR3 LUT Page Size Extension* bit value is 0, the encodings are as follows: 0h = Disables BAR3 1h to 4h = ***Reserved*** 5h = 4 KB 6h = 8 KB 7h = 16 KB 8h = 32 KB 9h = 64 KB Ah = 128 KB Bh = 256 KB Ch = 512 KB Dh = 1 MB Eh = 2 MB Fh = 4 MB When the *BAR3 LUT Page Size Extension* bit value is 1, the encodings are as follows: 0h = 8 MB 1h = 16 MB 2h = 32 MB 3h to Fh = ***Reserved***	RW	Yes	0h
20	**BAR3 LUT Page Size Extension** Allows selection of larger page sizes when programming Page Size[19:16]. 0 = Page sizes 4 KB through 4 MB are available in the Page Size[19:16] 1 = Page sizes 8 through 32 MB are available in the Page Size[19:16]	RW	Yes	0
31:21	***Reserved***			000h

Note: *Software must copy the **BAR3 Setup** register value to the **BAR3 Setup Shadow** register (D88h) in the non-NT Station:*

- *If the NT Port is one of Ports 0 through 3, software must read the value in NT Port Virtual Interface, offset D8h or D88h, and write the value to Port 8, offset D88h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset D8h or D88h, and write the value to Port 0, offset D88h*

Register 15-31. DCh NT Port Virtual Interface BAR4/5 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR 10b = **BAR4/5** is implemented as a 64-bit Memory BAR ***Note:*** *It is illegal to program 10b and clear the* ***NT Port Virtual Interface BAR5 Setup*** *register BAR5 Enable bit (offset E0h[31]).*	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
30:12	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding bits in **BAR4** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR4** are RW bits	RW	Yes	0000_0h
31	**BAR4 Enable** When bits [2:1] = 00b, enables **BAR4**; otherwise, belongs to the *BAR4 Size*[30:12] field. 0 = **BAR4** is disabled, all bits in **BAR4** read 0 1 = **BAR4** is enabled, Size and Type specified in this register	RW	Yes	0

Note: *Software must copy the* ***BAR4 Setup*** *register value to the* ***BAR4 Setup Shadow*** *register (D8Ch) in the non-NT Station:*

- *If the NT Port is one of Ports 0 through 3, software must read the value in NT Port Virtual Interface, offset DCh or D8Ch, and write the value to Port 8, offset D8Ch*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset DCh or D8Ch, and write the value to Port 0, offset D8Ch*

Register 15-32. E0h NT Port Virtual Interface BAR5 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
30:0	**BAR5 Size** Together with the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Size* field (offset DCh[31:12]), specifies the Address Range size requested by **BAR4/5** in 64-bit mode when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* field (offset DCh[2:1]) is set to 10b. 0 = Corresponding bits in **BAR5** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR5** are RW bits	RW	Yes	0-0h
	Reserved when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* field (offset DCh[2:1]) is cleared to 00b.			0-0h
31	**BAR5 Enable** 0 = **BAR5** is disabled 1 = **BAR5** is enabled when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* field (offset DCh[2:1]) is set to 10b ***Note:*** *It is illegal to program the **NT Port Virtual Interface BAR4/5 Setup** register BAR4 Type = 10b and clear this bit.*	RW	Yes	0
	Reserved when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* field (offset DCh[2:1]) is cleared to 00b.			0

Note: *Software must copy the **BAR5 Setup** register value to the **BAR5 Setup Shadow** register (D90h) in the non-NT Station:*

- *If the NT Port is one of Ports 0 through 3, software must read the value in NT Port Virtual Interface, offset E0h or D90h, and write the value to Port 8, offset D90h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset E0h or D90h, and write the value to Port 0, offset D90h*

15.8.4 NT Port Cursor Mechanism Control Registers

This section details the NT Port Cursor Mechanism Control registers. The register map for the Virtual and Link Interfaces is defined in Table 15-9.

The Cursor Mechanism registers at offsets F8h/FCh provide a means for accessing PCI Express Extended Configuration Space registers (100h through FFFh) within the NT Port Virtual and Link Interfaces, when only standard PCI Configuration transactions (that do not support Extended Register Number), and/or I/O Request transactions (using the NT Port **BAR1** address, if enabled) are available. The Cursor Mechanism can generally access only those registers that are defined by the *PCI Express Base r1.0a*, and not the device-specific registers. However if Port 0 is the NT Port, the Cursor Mechanism in the NT Port Virtual Interface registers can also access the Device-Specific registers.

Table 15-9. NT Port Cursor Mechanism Control Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Configuration Address Window		***Reserved***		F8h
Configuration Data Window				FCh

Register 15-33. F8h Configuration Address Window

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	***Reserved***			0000h
25:16	**Offset** Register Offset.	RW	Yes	000h
30:26	***Reserved***			0h
31	**Interface Select** 0 = Access to NT Port Virtual Interface Type 0 Configuration Space register 1 = Access to NT Port Link Interface Type 0 Configuration Space register	RW	Yes	0

Register 15-34. FCh Configuration Data Window

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Data Window** Software selects a register by writing into the NT Port Configuration Address window, then reads or writes to that register using this register.	RW	Yes	0-0h

15.9 Device Serial Number Extended Capability Registers

The NT Port Device Serial Number Extended Capability registers are the same as the PEX 8524 Transparent port registers, as defined in Section 11.10, "Device Serial Number Extended Capability Registers." The register map is defined in Table 15-10 and applies to the Virtual and Link Interfaces.

Table 15-10. PEX 8524 Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h) / Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Higher DW)		108h

15.10 Power Budgeting Extended Capability Registers

The NT Port Power Budgeting Extended Capability registers are the same as the PEX 8524 Transparent port registers, as defined in Section 11.11, "Power Budgeting Extended Capability Registers." The register map is defined in Table 15-11 and applies to the Virtual and Link Interfaces.

Table 15-11. PEX 8524 Power Budgeting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h) / Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budgeting Data		140h
Reserved	Power Budget Capability	144h

15.11 Virtual Channel Extended Capability Registers

The NT Port Virtual Channel Extended Capability registers are the same as the PEX 8524 Transparent port registers, as defined in Section 11.12, "Virtual Channel Extended Capability Registers." The register map is defined in Table 15-12 and applies to the Virtual and Link Interfaces.

Table 15-12. PEX 8524 Virtual Channel Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (000h) / Capability Version (1h)	Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
VC1 Resource Capability		164h
VC1 Resource Control		168h
VC1 Resource Status	***Reserved***	16Ch
Reserved		170h – 1B4h
Virtual Channel Arbitration Table		1B8h … 1C4h

15.12 PLX-Specific Registers

The PEX 8524 NT mode Virtual Interface PLX-Specific registers are defined in Section 11.13, "PLX-Specific Registers," except as defined in Table 15-13 through Table 15-16 and/or their respective register tables. The entire register map is defined in Table 15-13.

Note: *This register group is accessed using a Memory-Mapped cycle. It is recommended that these register values* ***not*** *be changed.*

Table 15-13. NT Port Virtual Interface PLX-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Error Checking and Debug Registers	1C8h … 1FCh
Physical Layer Registers	200h … 2C4h
CAM Routing Registers	2C8h … 344h
NT Port Virtual Interface Ingress Control Register	660h … 668h
I/O CAM Base and Limit Upper 16 Bits Registers	680h … 6ACh
Base Address Registers (BARs)	6C0h … 73Ch
Shadow Virtual Channel (VC) Capability Registers	740h … 9ECh
Ingress Credit Handler (INCH) Registers	9F0h … B7Ch
Reserved	B80h – BFCh
Internal Credit Handler (ITCH) VC&T Threshold Registers	C00h … C08h

15.12.1 Error Checking and Debug Registers

The NT mode Virtual Interface Error Checking and Debug registers are defined in Section 11.13.1, "Error Checking and Debug Registers," except as defined in Table 15-14 (offsets 1D4h through 1D8h and 1E0h are ***reserved***) and the register tables that follow.

Table 15-14. PLX-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				1C8h
Error Handler 32-Bit Error Status ***(Factory Test Only)***				1CCh
Error Handler 32-Bit Error Mask ***(Factory Test Only)***				1D0h
Reserved				1D4h – 1D8h
Debug Control				1DCh
Reserved				1E0h
Egress NT Port Virtual Interface Control and Status				1E4h
Reserved				1E8h – 1ECh
PLX-Specific Relaxed Ordering Enable				1F0h
Software-Controlled Lane Status				1F4h
Reserved		ACK Transmission Latency Limit		1F8h
Reserved				1FCh

a. Some registers are port-specific, some are station-specific, and some are device-specific.

Note: *All errors in register offset 1CCh generate MSI/INTx interrupts, when enabled.*

Register 15-35. 1CCh Error Handler 32-Bit Error Status *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Error Handler Completion FIFO Overflow Status** 0 = No overflow detected 1 = Completion FIFO Overflow detected when 4-deep completion FIFO for ingress, or 2-deep completion FIFO for egress, overflows	RW1CS	Yes	0
10:1	***Reserved***		No	0h
11	**Credit Update Timeout Status** No useful credit update to make forward progress for 512 ms or 1s (disabled by default). 0 = No Credit Update Timeout detected 1 = Credit Update Timeout completed	RW1CS	Yes	0
12	**INCH Underrun Error** Ingress Credit Underrun. 0 = No error detected 1 = Credit underrun error detected	RW1CS	Yes	0
31:13	***Reserved***		No	0h

Note: *Error logging is enabled in register offset 1D0h, by default.*

Register 15-36. 1D0h Error Handler 32-Bit Error Mask *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Error Handler Completion FIFO Overflow Status Masked** 0 = No effect on reporting activity 1 = Error Handler Completion FIFO Overflow Status bit is masked/disabled	RWS	Yes	1
10:1	***Reserved***		No	0h
11	**Credit Update Timeout Status Masked** 0 = No effect on reporting activity 1 = *Credit Update Timeout Status* bit is masked/disabled	RWS	Yes	1
12	**INCH Underrun Error Masked** 0 = No effect on reporting activity 1 = *INCH Underrun Error* bit is masked/disabled	RWS	Yes	1
31:13	***Reserved***		No	0h

Register 15-37. 1E4h Egress NT Port Virtual Interface Control and Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Egress Credit Update Timer Enable** 0 = Disables Egress Credit Update Timer 1 = Enables Egress Credit Update Timer	RW	Yes	0
1	**Egress Credit Timeout Value** 0 = Minimum 512 ms (Maximum 768 ms) 1 = Minimum 1,024 ms (Maximum 1,280 ms)	RW	Yes	0
2	**Egress Debug** ***Factory Test Only***	RW	Yes	0
15:3	***Reserved***			0-0h
19:16	**VC&T Encountered Timeout** 0h = VC0 Posted 1h = VC0 Non-Posted 2h = VC0 Completion 3h = VC1 Posted 4h = VC1 Non-Posted 5h = VC1 Completion	RO	Yes	0h
31:20	***Reserved***			000h

Register 15-38. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**ACK Transmission Latency Limit** If the serial EEPROM is not present, the value of this register changes based upon the negotiated link width after the link is up. The value of this register changes, based upon the negotiated link width of the NT Port Link Interface. If the serial EEPROM is present, program the serial EEPROM to load the value based upon the programmed link width of the NT Port Link Interface.	RW	Yes	FFh
15:8	**HPC Test Bits** ***Factory Test Only.*** Testing bits – must be 00h.	RW	Yes	00h
31:16	***Reserved***			0000h

15.12.2 NT Port Virtual Interface Physical Layer Registers

The NT Port Virtual Interface Physical Layer registers are defined in Section 11.13.2, "Physical Layer Registers," except as defined in Table 15-15.

Table 15-15. PLX-Specific NT Port Virtual Interface Physical Layer Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				200h – 20Ch
Phy User Test Pattern 0				210h
Phy User Test Pattern 4				214h
Phy User Test Pattern 8				218h
Phy User Test Pattern 12				21Ch
Physical Layer Status		Physical Layer Command		220h
Port Configuration				224h
Physical Layer Test				228h
Reserved				22Ch
Physical Layer Port Command				230h
SKIP Ordered-Set Interval				234h
Quad 0 SerDes Diagnostic Data				238h
Quad 1 SerDes Diagnostic Data				23Ch
Quad 2 SerDes Diagnostic Data				240h
Quad 3 SerDes Diagnostic Data				244h
SerDes Nominal Drive Current Select				248h
SerDes Drive Current Level Select 1				24Ch
SerDes Drive Current Level Select 2				250h
SerDes Drive Equalization Level Select 1				254h
SerDes Drive Equalization Level Select 2				258h
Reserved				25Ch – 2C4h

15.12.3 NT Port Virtual Interface Ingress Control Register

The NT Port Virtual Interface Ingress Control register is defined in Section 11.13.4, "Ingress Control Registers," with the addition of the **Ingress Control** register *No Snoop Disable* bit (bit 24) and bit 25 is changed to ***Factory Test Only***. The register map is defined in Table 15-16.

Table 15-16. PLX-Specific NT Port Virtual Interface Ingress Control Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Reserved				664h – 668h

Register 15-39. 660h Ingress Control (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Enable CSR Access by Downstream Devices** **Silicon Revision AA** Enables acceptance of Configuration requests from a Requester that is downstream from a Transparent port, targeting any downstream Transparent port's Type 1 Header registers or NT Port Virtual Interface Type 0 Header registers (*such as* for Peer Configuration access). 0 = Configuration requests from a downstream device are ***not supported***; the downstream port flags an Uncorrectable Error, and, returns a Completion with Unsupported Request (UR) specified in the *Completion Status* field, to the downstream Requester. Only this mode is *PCI Express Base r1.0a*-compliant. 1 = The following types of Configuration requests from downstream Requesters are allowed: • Type 0 requests targeting the Type 1 Header registers in that downstream port • Type 1 requests targeting the Type 1 Header registers in other downstream Transparent ports, and • Type 1 requests targeting the Type 0 Header registers in the NT Port Virtual Interface The upstream port registers are not accessible from the downstream port. **Silicon Revisions BB/BC** Enables acceptance of both Configuration and Memory requests from a Requester that is downstream from a Transparent port, targeting any PEX 8524 registers. 0 = Configuration requests from a downstream device are ***not supported***; the downstream port flags an Uncorrectable Error, and, returns a Completion with Unsupported Request (UR) specified in the *Completion Status* field, to the downstream Requester. Only this mode is *PCI Express Base r1.0a*-compliant. 1 = Configuration and Memory requests from downstream Requesters, targeting any PEX 8524 registers in any port, are allowed. ***Notes:*** *This bit can be initially set only through the upstream port, the NT Port Link Interface, or serial EEPROM, to enable register access through downstream Transparent ports; a Requester downstream from a Transparent port cannot set the bit to grant itself (or peers) access to PEX 8524 registers. Configuration requests can access those registers that are defined by PCI-SIG specifications, and generally cannot access device-specific registers other than the NT Port* ***Cursor Mechanism*** *registers. Memory requests can access all PEX 8524 registers.* *Configuration requests can access the NT Port* ***Cursor Mechanism*** *registers (offsets F8h/FCh) to provide indirect access to NT Port offsets above 100h, for Conventional PCI Requesters such as a PCI Master connected to a PCI Express-to-PCI bridge, that cannot generate Configuration requests containing an Extended Register Number. The NT Port Virtual Interface Cursor Mechanism (but not the NT Port Link Interface Cursor Mechanism) can access device-specific registers that exist in the NT Port; if Port 0 is the NT Port, the NT Port Virtual Interface Cursor Mechanism can access the device-specific registers (which exist only in Port 0) and the Station 0 registers (which exist in Port 0 for all enabled ports in Station 0).*	RW	Yes	0
1	**Disable Unsupported Request Response for *Reserved* Configuration Registers**	RW	Yes	0
23:2	***Factory Test Only***	RW	Yes	0-0h

Register 15-39. 660h Ingress Control (Only Ports 0 and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
24	**No Snoop Disable** **Silicon Revision AA** ***Not supported*** **Silicon Revisions BB/BC** Forces the packet header No Snoop attribute bit to 0, for all packets transferred between the NT Link and Virtual Interfaces (across the NT boundary, in both directions). Can be used to handle cache coherency-related issues in a system. 0 = Disables No Snoop Disable feature 1 = Enables No Snoop Disable feature	RW	Yes	0
26:25	***Factory Test Only***	RW	Yes	00b
27	***Reserved*** **Silicon Revision AA**			0
	BIOS Enumeration Fix Disable **Silicon Revisions BB/BC** For NT Failover in Silicon Revisions BB/BC, this bit must be set.	RW	Yes	0
31:28	***Factory Test Only***	RW	Yes	0h

15.13 PEX 8524 Non-Transparent Bridging-Specific Registers

Table 15-17 defines the register map of the registers implemented to support the PEX 8524 Non-Transparent Bridging function. The NT station contains the main copy of these registers, and the Transparent station contains the shadow copy of these registers. These registers are accessed by Memory-Mapped access to Port 0, Port 8, or NT Port.

Table 15-17. NT Port Virtual Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
NT Port Virtual Interface Memory Address Translation and BAR Limit Registers	C3Ch … C58h	
NT Port Virtual Interface Lookup Table-Based Address Translation Registers	C5Ch … D58h	
NT Port Link Interface VC Registers (Shadow Copy)	D5Ch … D64h	
NT Port Virtual Interface Base Address Registers (BARs) and BAR Setup Registers (Shadow Copy)	D68h … D90h	
NT Port Virtual Interface Send Lookup Table Entry Registers	D94h … DB0h	
Reserved	DB4h –	DF0h
NT Port Link Interface Capture and Virtual Interface Control Registers (Shadow Copy)	DF4h DF8h	
Reserved	DFCh –	FB0h

15.13.1 NT Port Virtual Interface Memory Address Translation and BAR Limit Registers

The NT station contains the main copy of these registers, and the Transparent station contains the shadow copies of these registers. Program **only** the main copy. The Shadow register is automatically updated. The reverse is not true. The register map is defined in Table 15-18.

*Note: The **NT Port Virtual Interface Memory BAR Address Translation** (offsets C3Ch, C44h and C48h) and **Memory BAR Limit** (offsets C4Ch, C54h and C58h) register values are shadowed to both Stations. If software writes to these registers, the Shadow registers are automatically updated; however, if the serial EEPROM programs these registers, the Shadow registers are **not** updated. Therefore, if the serial EEPROM is used to program initial values into these registers, software must read the registers and write back the values, to automatically update the Shadow registers.*

Table 15-18. NT Port Virtual Interface Memory Address Translation (BAR Limit) Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Memory BAR2 Address Translation[31:0]				C3Ch
Reserved				C40h
Memory BAR4/5 Address Translation[31:0]				C44h
Memory BAR4/5 Address Translation[63:32]				C48h
Memory BAR2 Limit[31:0]				C4Ch
Reserved				C50h
Memory BAR4/5 Limit[31:0]				C54h
Memory BAR5 Limit[63:32]				C58h

Register 15-40. C3Ch Memory BAR2 Address Translation[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR2 Base Translation Address[31:12]** NT Port Virtual Interface Base Translation address when the **NT Port Virtual Interface BAR2 Setup** register *BAR2 Enable* bit (offset D4h[31]) is set to 1.	RW	Yes	0-0h

Register 15-41. C44h Memory BAR4/5 Address Translation[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR4 Base Translation Address[31:12]** NT Port Virtual Interface Base Translation address when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Enable* bit (offset DCh[31]) is set to 1.	RW	Yes	0-0h

Register 15-42. C48h Memory BAR4/5 Address Translation[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**BAR4/5 Base Translation Address[63:32]** NT Port Virtual Interface Base Translation upper address when **BAR4/5** is enabled as a 64-bit BAR [**NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* (offset DCh[2:1]) and **BAR4 Setup** Shadow register BAR4 Type (offset D8Ch[2:1]) fields are both set to 10b].	RW	Yes	0-0h
	Read-Only when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* (offset DCh[2:1]) and **BAR4 Setup** Shadow register *BAR4 Type* (offset D8Ch[2:1]) fields are both cleared to 00b.	RO	No	0-0h

Register 15-43. C4Ch Memory BAR2 Limit[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR2 Limit[31:0]** Contains the address of the memory window upper limit defined in the **BAR2 Setup** register (offset D84h). 1 MB granularity. When the limit is greater than the window size, the limit is ignored.	RW	Yes	000h

Register 15-44. C54h Memory BAR4/5 Limit[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR4/5 Limit[31:0]** Contains the address of the memory window lower limit defined in the **BAR4 Setup** register (offset D8Ch). 1 MB granularity. When the limit is greater than the window size, the limit is ignored.	RW	Yes	0-0h

Register 15-45. C58h Memory BAR5 Limit[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**BAR5 Limit[63:32]** Contains the address of the memory window upper limit defined in the **BAR5 Setup** register (offset D90h) when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* (offset DCh[2:1]) and **BAR4 Setup** Shadow register BAR4 Type (offset D8Ch[2:1]) fields are both set to 10b]. 1 MB granularity. When the limit is greater than the window size, the limit is ignored.	RW	Yes	0-0h
	Read-Only when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* (offset DCh[2:1]) and **BAR4 Setup** Shadow register *BAR4 Type* (offset D8Ch[2:1]) fields are both cleared to 00b.	RO	No	0-0h

15.13.2 NT Port Virtual Interface Lookup Table-Based Address Translation Registers

There are 64 Base-Translation Lookup Table (LUT) Entry registers to support the LUT-based address translation. These registers are accessed using Port 0, Port 8, and the NT Port Virtual Interface Memory-Mapped or Cursor mechanism. Table 15-19 defines the register and address locations. The register description that follows defines the bit definitions that apply to all 64 registers.

The NT station contains the main copy of these registers, and the Transparent station contains the shadow copies of these registers. Program **only** the main copy. The Shadow register is automatically updated. The reverse is not true.

Note: *The **NT Port Virtual Interface Lookup Table-Based Address Translation** (offsets C5Ch through D58h) register values are shadowed to both Stations. If software writes to these registers, the Shadow registers are automatically updated; however, if the serial EEPROM programs these registers, the Shadow registers are **not** updated. Therefore, if the serial EEPROM is used to program initial values into these registers, software must read the registers and write back the values, to automatically update the Shadow registers.*

Table 15-19. Base-Translation Lookup Table Entry_*n* Register Locations

ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n*
C5Ch	0	C60h	1	C64h	2	C68h	3
C6Ch	4	C70h	5	C74h	6	C78h	7
C7Ch	8	C80h	9	C84h	10	C88h	11
C8Ch	12	C90h	13	C94h	14	C98h	15
C9Ch	17	CA0h	17	CA4h	18	CA8h	19
CACh	20	CB0h	21	CB4h	22	CB8h	23
CBCh	24	CC0h	25	CC4h	26	CC8h	27
CCCh	28	CD0h	29	CD4h	30	CD8h	31
CDCh	32	CE0h	33	CE4h	34	CE8h	35
CECh	36	CF0h	37	CF4h	38	CF8h	39
CFCh	40	D00h	41	D04h	42	D08h	43
D0Ch	44	D10h	45	D14h	46	D18h	47
D1Ch	48	D20h	49	D24h	50	D28h	51
D2Ch	52	D30h	53	D34h	54	D38h	55
D3Ch	56	D40h	57	D44h	58	D48h	59
D4Ch	60	D50h	61	D54h	62	D58h	63

Register 15-46. C5Ch - D58h Base-Translation Lookup Table Entry_*n* (where *n* = 0 through 63)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Entry Status** 0 = Invalid 1 = Valid	RWS	Yes	0
2:1	***Reserved***			00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
31:12	**Base Translation** Base Translation address value.	RW	Yes	0-0h

15.13.3 NT Port Link Interface VC Registers

The registers in this section are shadow copies and valid only for Port 0 and Port 8. If Port 0 or Port 8 is an NT Port, the register is in Virtual Interface Configuration space. Modifying these registers is ***not recommended***. Table 15-20 defines the register map.

Table 15-20. NT Port Link Interface VC Shadow Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Link Interface VC0 Resource Control (Shadow Copy)				D5Ch
NT Link Interface VC1 Resource Control (Shadow Copy)				D60h
NT Link Interface VC Capability 1 (Shadow Copy)				D64h

Register 15-47. D5Ch NT Link Interface VC0 Resource Control (Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TCVC_Map[0]** Always mapped to Virtual Channel 0.	RO	Yes	1
7:1	**TCVC_Map[7:1]** Mapped to Virtual Channel 0 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	7Fh
23:8	***Reserved***			0000h
24	**VC_ID** Virtual Channel identification number.	RO	Yes	0
30:25	***Reserved***			00h
31	**VC_Enable** Virtual Channel 0 enable.	RO	Yes	1

Register 15-48. D60h NT Link Interface VC1 Resource Control (Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***		No	0
7:1	**TCVC_Map[7:1]** Mapped to Virtual Channel 1 by default. Software can change this field during enumeration or when quiescing the traffic to the traffic class.	RW	Yes	00h
23:8	***Reserved***		Yes	0000h
24	**VC_ID** Virtual Channel identification number.	RW	Yes	1
30:25	***Reserved***		Yes	00h
31	**VC_Enable** Virtual Channel 1 enable.	RW	Yes	0

Register 15-49. D64h NT Link Interface VC Capability 1 (Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***		No	0h
6:4	**Low-Priority Virtual Channel Count** Indicates the number of Virtual Channels mapped to the low-priority group.	RO	Yes	000b
31:7	***Reserved***		No	0000_00h

15.13.4 NT Port Virtual Interface Base Address Registers (BARs) and BAR Setup Registers

The registers in this section are shadow copies and valid only for Port 0 and Port 8. If Port 0 or Port 8 is an NT Port, the register is in Virtual Interface Configuration space. ***Modifying these registers is not recommended.*** Table 15-21 defines the register map.

Table 15-21. NT Port Virtual Interface Base Address Register (BAR) and BAR Setup Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
BAR0 = ***Reserved***				D68h
BAR1				D6Ch
BAR2				D70h
BAR3				D74h
BAR4				D78h
BAR5				D7Ch
BAR1 Setup				D80h
BAR2 Setup				D84h
BAR3 Setup				D88h
BAR4 Setup				D8Ch
BAR5 Setup				D90h

Register 15-50. D6Ch BAR1 (14h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**I/O Space Indicator** 256-byte I/O BAR when the **NT Port Virtual Interface BAR1 Setup** register *I/O BAR1 Enable* field (offset D0h[1:0]) is set to 11b.	RO	Yes	1
	Reserved when the **NT Port Virtual Interface BAR1 Setup** register *I/O BAR1 Enable* field (offset D0h[1:0]) is not set to 11b.			0
7:1	***Reserved***			0h
31:8	**I/O Base Address** 256-byte I/O Space Base address when the **NT Port Virtual Interface BAR1 Setup** register *I/O BAR1 Enable* field (offset D0h[1:0]) is set to 11b.	RW	Yes	0000_00h
	Reserved when the **NT Port Virtual Interface BAR1 Setup** register *I/O BAR1 Enable* field (offset D0h[1:0]) is not set to 11b.			00000_00h

Note: *Software (device driver) must copy the **BAR1** register value to the **BAR1 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 14h or D6Ch, and write the value to Port 8, offset D6Ch*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 14h or D6Ch, and write the value to Port 0, offset D6Ch*

Register 15-51. D70h BAR2 (18h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	Yes	0
2:1	**Memory Map Type** 00b = BAR is mapped anywhere in 32-bit Memory space 01b, 10b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
11:4	***Reserved***			00h
31:12	**Base Address 2** Contains the software-assigned Memory Space Base Address: • Enabled and sized by **BAR2 Setup** register (offset D84h) • Used for Memory transactions crossing the NT Port • Minimum address range requested is 4 KB • Uses direct address translation	RW	Yes	0000_0h

Note: *Software (device driver) must copy the **BAR2** register value to the **BAR2 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 18h or D70h, and write the value to Port 8, offset D70h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 18h or D70h, and write the value to Port 0, offset D70h*

Register 15-52. D74h BAR3 (1Ch Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	Yes	0
2:1	**Memory Map Type** 00b = BAR is mapped anywhere in 32-bit Memory Address space 01b, 10b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
17:4	***Reserved***			0000h
31:18	**Base Address 3** Contains the software-assigned Memory Space Base Address: • Enabled and sized by **BAR3 Setup** register (offset D88h) • No **Limit** register • Used for Memory transactions crossing the NT Port • Minimum address range requested is 256 KB • Uses LUT address translation	RW	Yes	0000h

Note: *Software (device driver) must copy the **BAR3** register value to the **BAR3 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 1Ch or D74h, and write the value to Port 8, offset D74h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 1Ch or D74h, and write the value to Port 0, offset D74h*

Register 15-53. D78h BAR4 (20h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	Yes	0
2:1	**Memory Map Type** 00b = Mappable anywhere in 32-bit Memory space 10b = Mappable anywhere in 64-bit Memory space 01b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
11:4	***Reserved***			00h
31:12	**Base Address 4** Contains the software-assigned Memory Space Base Address: • Enabled and sized by **BAR4 Setup** register (offset D8Ch) • Used for Memory transactions crossing the NT Port • Minimum address range requested is 4 KB • Uses direct address translation	RW	Yes	0000_0h

Note: *Software (device driver) must copy the **BAR4** register value to the **BAR4 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 20h or D78h, and write the value to Port 8, offset D78h*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 20h or D78h, and write the value to Port 0, offset D78h*

Register 15-54. D7Ch BAR5 (24h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address 5** NT Port Virtual Interface upper 32-bit address when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* field (offset DCh[2:1]) is set to 10b. RW, based on **BAR5 Setup** register. The **BAR4/5** group uses direct address translation.	RW	Yes	0-0h
	Reserved when the **NT Port Virtual Interface BAR4/5 Setup** register *BAR4 Type* field (offset DCh[2:1]) is cleared to 00b.			0-0h

Note: *Software (device driver) must copy the **BAR5** register value to the **BAR5 Shadow** register in the non-NT Station:*

- *If the NT port is one of Ports 0 through 3, software must read the value in the NT Port Virtual Interface, offset 24h or D7Ch, and write the value to Port 8, offset D7Ch*
- *If the NT port is one of Ports 8 through 11, software must read the value in the NT Port Virtual Interface, offset 24h or D7Ch, and write the value to Port 0, offset D7Ch*

Register 15-55. D80h BAR1 Setup (D0h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	**I/O BAR1 Enable** 11b = Enables Virtual Interface **BAR1** as an I/O BAR All other values disable **BAR1**.	RW	Yes	11b
31:2	***Reserved***			0-0h

Register 15-56. D84h BAR2 Setup (D4h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
2:1	**BAR2 Type** 00b = Selects 32-bit memory BAR No other values are allowed.	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
30:12	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding bits in **BAR2** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR2** are RW bits	RW	Yes	0000_0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all bits in **BAR2** read 0 1 = **BAR2** is enabled, Size and Type specified in this register	RW	Yes	0

Note: *Register offset D84h must be programmed with the same value as the **NT Port Virtual Interface BAR2 Setup** register (offset D4h). This requirement applies only to the NT Virtual Interface.*

Register 15-57. D88h BAR3 Setup (D8h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
15:1	***Reserved***			0-0h
19:16	**LUT Page Size** Virtual **BAR3** Address range. The total size of this range is dependent on the page size. When the *BAR3 LUT Page Size Extension* bit value is 0, the encodings are as follows: 0h = Disables BAR3 1h to 4h = ***Reserved*** 5h = 4 KB 6h = 8 KB 7h = 16 KB 8h = 32 KB 9h = 64 KB Ah = 128 KB Bh = 256 KB Ch = 512 KB Dh = 1 MB Eh = 2 MB Fh = 4 MB When the *BAR3 LUT Page Size Extension* bit value is 1, the encodings are as follows: 0h = 8 MB 1h = 16 MB 2h = 32 MB 3h to Fh = ***Reserved***	RW	Yes	0h
20	**LUT Page Size Extension** Allows selection of larger page sizes when programming Page Size[19:16]. 0 = Page sizes 4 KB through 4 MB are available in Page Size[19:16] 1 = Page sizes 8 through 32 MB are available in Page Size[19:16]	RW	Yes	0
31:21	***Reserved***			000h

Note: *Register offset D88h must be programmed with the same value as the **NT Port Virtual Interface BAR3 Setup** register (offset D8h). This requirement applies only to the NT Virtual Interface.*

Register 15-58. D8Ch BAR4 Setup (DCh Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	***Reserved***			0
2:1	**BAR4 Type** 00b = Selects 32-bit memory BAR 10b = Selects 64-bit Memory BAR ***Note:*** *It is illegal to program 10b and clear the* **BAR5 Setup** *register* BAR5 Enable *bit (offset D90h[31]).*	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
30:12	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding bits in **BAR4** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR4** are RW bits	RW	Yes	0000_0h
31	**BAR4 Enable** When bits [2:1] = 00b, enables **BAR4**; otherwise, belongs to the BAR4 Size[30:12] field. 0 = **BAR4** is disabled, all bits in **BAR4** read 0 1 = **BAR4** is enabled, Size and Type specified in this register	RW	Yes	0

Note: *Register offset D8Ch must be programmed with the same value as the* ***NT Port Virtual Interface BAR4/5 Setup*** *register (offset DCh). This requirement applies only to the NT Virtual Interface.*

Register 15-59. D90h BAR5 Setup (E0h Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
30:0	**BAR5 Size** Together with the **BAR4 Setup** register *BAR4 Size* field (offset D8Ch[31:12]), specifies the Address Range size requested by **BAR4/5** in 64-bit mode when the **BAR4 Setup** register *BAR4 Type* field (offset D8Ch[2:1]) is set to 10b. 0 = Corresponding bits in **BAR5** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR5** are RW bits	RW	Yes	0-0h
	Reserved when the **BAR4 Setup** register *BAR4 Type* field (offset D8Ch[2:1]) is cleared to 00b.			0-0h
31	**BAR5 Enable** 0 = **BAR5** is disabled 1 = **BAR5** is enabled when the **BAR4 Setup** register *BAR4 Type* field (offset D8Ch[2:1]) is set to 10b ***Note:*** *It is illegal to program 10b and clear the* **BAR5 Setup** *register BAR5 Enable bit (offset D90h[31]).*	RW	Yes	0
	Reserved when the **BAR4 Setup** register *BAR4 Type* field (offset D8Ch[2:1]) is cleared to 00b.			0

Note: *Register offset D90h must be programmed with the same value as the* ***NT Port Virtual Interface BAR5 Setup*** *register (offset E0h). This requirement applies only to the NT Virtual Interface.*

15.13.5 NT Port Virtual Interface Send Lookup Table Entry Registers

This section describes the NT Port Virtual Interface Send (Requester ID Translation) Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory requests from NT Port Virtual Interface to the NT Port Link Interface, or
- Completion TLP from NT Port Link Interface to the NT Port Virtual Interface

The NT station contains the main copy of these registers, and the Transparent station contains the shadow copies of these registers. Program **only** the main copy. The Shadow register is automatically updated. The reverse is not true.

Table 15-22 defines the register and address locations. The register descriptions that follow the table define the bit definitions that apply to the two register types.

Note: *Software must copy the values to the same offsets in the non-NT Station (Port 0 or Port 8). If the NT Port is one of Ports 8 through 11, software must read the value(s) in the NT Port Virtual Interface and write the value(s) to the same offsets (D94h through DB0h, respectively) in Port 0; if the NT Port is one of Ports 0 through 3, software must read the value(s) in the NT Port Virtual Interface and write the value(s) to the same offsets (D94h through DB0h) in Port 8.*

Table 15-22. NT Port Virtual Interface Send Lookup Table Entry_*n* Register Locations

ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n*
D94h	0	DA4h	4
D98h	1	DA8h	5
D9Ch	2	DACh	6
DA0h	3	DB0h	7

Register 15-60. D94h - DB0h Virtual Interface Send Lookup Table Entry_*n* (where *n* = 0 through 7)

Bit(s)	Description		Type	Serial EEPROM	Default
2:0	**Requester ID**	**Function Number** LUT Entry_*n* Requester Function Number.	RW	Yes	000b
7:3		**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
30:16	***Reserved***				0-0h
31	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0

15.13.6 NT Port Link Interface Capture and Virtual Interface Control Registers

Table 15-23. NT Port Link Interface Capture and Virtual Interface Control Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Link Interface Capture Bus and Device Number				DF4h
NT Port Virtual Interface Control (Shadow Copy)				DF8h

Register 15-61. DF4h NT Port Link Interface Capture Bus and Device Number

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Captured Bus Number**	RW	Yes	00h
12:8	**Captured Device Number**	RW	Yes	0000_0b
31:13	***Reserved***			0-0h

Note: *The **NT Port Link Interface Capture Bus and Device Number** register (offset DF4h) exists only in the non-NT Station (Port 0 or Port 8), and must be programmed by software:*

- *If the NT Port is one of Ports 0 through 3, software must program the NT Port Link Interface Bus and Device Numbers into Port 8, offset DF4h*
- *If the NT port is one of Ports 8 through 11, software must program the NT Port Link Interface Bus and Device Numbers into Port 0, offset DF4h*

The Device Number should normally be 0000_0b; therefore, software should only need to program the Bus Number, if the Bus Number is not 00h (default).

Register 15-62. DF8h NT Port Virtual Interface Control (04h[2:0] Shadow Copy)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**I/O Access Enable** 0 = Disables 1 = Enables	RW	Yes	0
1	**Memory Access Enable** 0 = Disables 1 = Enables	RW	Yes	0
2	**Bus Master Enable** 0 = Disables 1 = Enables	RW	Yes	0
31:3	***Reserved***			0-0h

Note: *The **NT Port Virtual Interface Control** register (offset DF8h) exists in only in the non-NT Station (Port 0 or Port 8), and must be programmed by software indirectly by programming the NT Port Virtual Interface **Status/Command** register (offset 04h, normally programmed by system software):*

- *If the NT Port is one of Ports 0 through 3, this Shadow register exists only in Port 8*
- *If the NT Port is one of Ports 8 through 11, this Shadow register exists only in Port 0 (offset DF8h)*

15.14 Advanced Error Reporting Capability Registers

The Advanced Error Reporting Capability registers for the NT Port Virtual Interface are equivalent to those defined in Section 11.14, "Advanced Error Reporting Capability Registers." The registers are duplicated for the NT Port Virtual Interface, and Table 15-24 defines the register map.

Table 15-24. Advanced Error Reporting Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log_0		FD0h
Header Log_1		FD4h
Header Log_2		FD8h
Header Log_3		FDCh
Reserved	FE0h –	FFCh

Chapter 16 NT Port Link Interface Registers

16.1 Introduction

This chapter defines the PEX 8524 Non-Transparent (NT) Port Link Interface (interface) registers. The NT Port includes two sets of Configuration, Capability, Control, and Status registers to support the Virtual and Link Interfaces. The NT Port Link Interface register mapping is defined in Table 16-1.

NT Port Virtual Interface registers are defined in Chapter 15, "NT Port Virtual Interface Registers." Transparent mode registers are defined in Chapter 11, "PEX 8524 Transparent Mode Port Registers."

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r2.3*
- *PCI Power Mgmt. r1.1*
- *PCI Express Base r1.0a*

Table 16-1. NT Port Link Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Configuration Header Registers			New Capability Pointer (40h)	00h … 34h … 3Ch
		Next Capability Pointer (48h)	Capability ID (01h)	40h
Power Management Capability Registers				44h
		Next Capability Pointer (68h)	Capability ID (05h)	48h
Message Signaled Interrupt Capability Registers				… 64h
		Next Capability Pointer (00h)	Capability ID (10h)	68h
PCI Express Capability Registers				… 8Ch
NT Port Registers				90h … FCh
Next Capability Offset (FB4h)	1h		Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers				104h 108h
Reserved				10Ch – 134h
Next Capability Offset (148h)	1h		Extended Capability ID (0004h)	138h
Power Budgeting Extended Capability Registers				… 144h
Next Capability Offset (000h)	1h		Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers				… 1C4h
PLX-Specific Registers				1C8h … C08h
PEX 8524 Non-Transparent Bridging-Specific Registers				C3Ch … FB0h
Next Capability Offset (138h)	1h		PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Capability Registers				… FFCh

16.2 Register Access

The PEX 8524 NT Port Link Interface implements a 4-KB Configuration space. The lower 256 bytes (offsets 00h through FFh) is the PCI-compatible Configuration space, and the upper 960 Dwords (offsets 100h through FFFh) is the PCI Express Extended Configuration space. The PEX 8524 supports four mechanisms for accessing NT Port Link Interface registers:

- PCI Express Base r1.0a Configuration Mechanism
- PLX-Specific Memory-Mapped Configuration Mechanism
- PLX-Specific I/O-Mapped Configuration Mechanism
- PLX-Specific Cursor Mechanism

16.2.1 *PCI Express Base r1.0a* Configuration Mechanism

The PCI Express Configuration mechanism is divided into two mechanisms:

- *PCI r2.3*-Compatible Configuration
- PCI Express Enhanced Configuration

The PCI r2.3-Compatible Configuration Mechanism provides standard access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Link Interface Configuration Register space. The PCI Express Enhanced Configuration Mechanism provides access to the remaining 4 KB (offsets 100h through FFFh).

The PEX 8524 decodes Type 0 Configuration transactions received on its NT Port Link Interface. The PEX 8524 reads or writes to the NT Port Link Interface register, as specified in the original Type 0 Configuration access.

16.2.1.1 *PCI r2.3*-Compatible Configuration Mechanism

The *PCI r2.3*-Compatible Configuration space consists of the first 256 bytes of the NT Port Link Interface Configuration space. (Refer to Figure 16-1.) The *PCI r2.3*-Compatible Configuration mechanism provides standard access to the PEX 8524 NT Port Link Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration space. This mechanism is used to access the PEX 8524 NT Port Link Interface Type 0 (PCI endpoint) registers:

- Configuration Header Registers
- Power Management Capability Registers
- Message Signaled Interrupt Capability Registers
- PCI Express Capability Registers

Because the *PCI r2.3*-Compatible Configuration mechanism is limited to the first 256 bytes of the NT Port Link Interface Configuration Register space, one of the following must be used to access beyond byte FFh:

- PCI Express Enhanced Configuration Mechanism
- PLX-Specific Memory-Mapped Configuration Mechanism
- PLX-Specific Cursor Mechanism

The *PCI r2.3*-Compatible Configuration mechanism uses the same request format as the Extended PCI Express Mechanism. For PCI-compatible Configuration requests, the Extended Register Address field must be all zeros (0).

Do not use this mechanism to access the PEX 8524 Device-Specific Configuration registers.

16.2.1.2 PCI Express Enhanced Configuration Mechanism

The PCI Express Enhanced Configuration mechanism uses a flat, Root Complex Memory-Mapped address space to access Device Configuration registers. In this case, the memory address determines the configuration register accessed, and memory data returns the addressed register contents. The Root Complex converts the Memory transaction into a Configuration transaction before transmitting this access to the downstream devices. This mechanism is used to access the NT Port Link Interface Type 0 registers:

- Configuration Header Registers
- Power Management Capability Registers
- Message Signaled Interrupt Capability Registers
- PCI Express Capability Registers
- Device Serial Number Extended Capability Registers
- Power Budgeting Extended Capability Registers
- Virtual Channel Extended Capability Registers
- Advanced Error Reporting Capability Registers

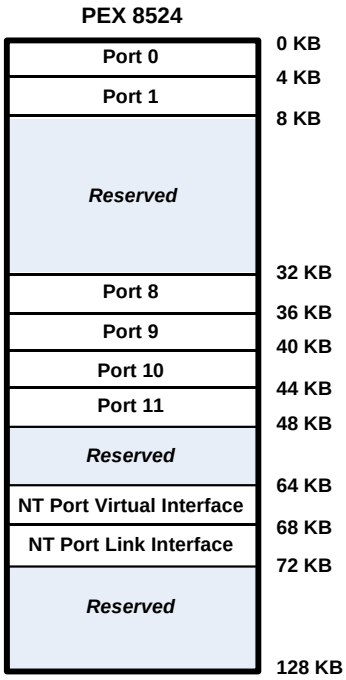
16.2.2 PLX-Specific Memory-Mapped Configuration Mechanism

The PLX-Specific Memory-Mapped Configuration mechanism provides a method to access the PEX 8524 port Configuration registers of all ports in a single Memory map, as illustrated in Figure 16-1. The registers of each port are contained within a 4-KB range.

When the NT Port is enabled at Fundamental reset, the NT Port Virtual and Link Interface Configuration registers are used in place of the Type 1 Configuration registers for that port.

To utilize the PLX-Specific Memory-Mapped Configuration mechanism, use the *PCI r2.3*-Compatible Configuration mechanism to program the PEX 8524 NT Port Link Interface **Base Address 0** register. After the NT Port Link Interface Memory-Mapped Base Address register is set, the NT Port registers are accessed with Memory reads from and writes to Configuration Space registers. The NT Port registers are accessed with Memory reads from and writes to the 4-KB range, starting at offset 64 KB for the Virtual Interface registers and offset 68 KB for Link Interface registers.

Figure 16-1. PEX 8524 Register Offset from Upstream Port BAR0/1 Base Address (Non-Transparent Mode)

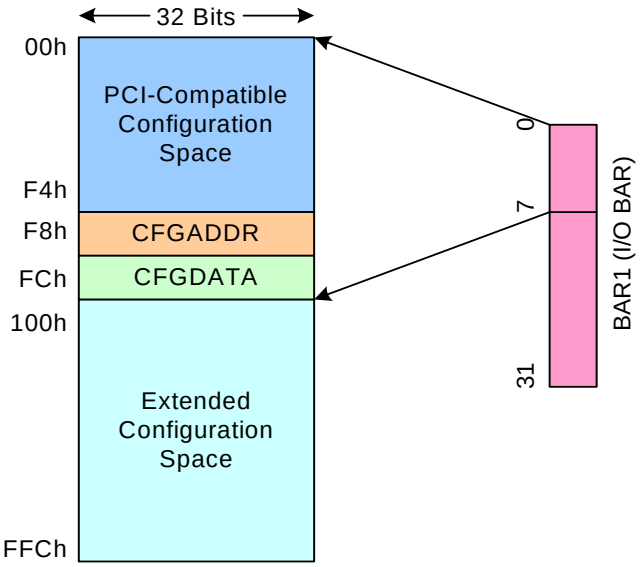


16.2.3 PLX-Specific I/O-Mapped Configuration Mechanism

The first 256 bytes of NT Port Link Interface Configuration Space registers are directly accessed by an I/O transaction. The NT Port Link Interface BAR1 register is used for I/O-Mapped access. (Refer to Figure 16-2.)

Extended Configuration Space registers are accessed by using the Cursor mechanism in I/O space.

Figure 16-2. I/O-Mapped Configuration Space View



16.2.4 PLX-Specific Cursor Mechanism

In Figure 16-2, the software uses the **Configuration Address Window** (CFGADDR) register to select the NT Port Virtual or Link Interface Configuration Space registers, including the Extended Configuration Space register.

Software uses the **Configuration Data Window** (CFGDATA) register to write to or read from the selected Configuration Space registers.

Refer to Section 16.8.4, "NT Port Cursor Mechanism Control Registers," for the register descriptions.

16.3 Register Descriptions

The remainder of this chapter details the PEX 8524 NT Port Link Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8524 NT Port Link and Virtual Interfaces
- Type (*such as* RW or HwInit; refer to Table 11-3, "Register Types, Grouped by User Accessibility." for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8524 serial EEPROM initialization feature
- Default power-on/reset value

16.4 Configuration Header Registers

Table 16-2. Type 0 Configuration Space Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST *(Not Supported)*	Configuration Layout Type and Function Type	Master Latency Timer	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			New Capability Pointer (40h)	34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch

Register 16-1. 00h Product Identification

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Vendor ID** Unless overwritten by the serial EEPROM, returns the PLX PCI-SIG-assigned Vendor ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Vendor ID with another Vendor ID.	HwInit	Yes	10B5h
31:16	**Device ID** Unless overwritten by the serial EEPROM, the PEX 8524 returns 8532h (680-ball package) or 8524h (644-ball package), the PLX-assigned Device ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX-assigned Device ID with another Device ID.	HwInit	Yes	8532h (680-ball package) 8524h (644-ball package)

Register 16-2. 04h Status/Command

Bit(s)	Description	Type	Serial EEPROM	Default
	Command			
0	**I/O Access Enable** 0 = PEX 8524 ignores I/O requests received on the NT Port Link Interface 1 = PEX 8524 accepts I/O requests received on the NT Port Link Interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8524 ignores Memory requests received on the NT Port Link Interface 1 = PEX 8524 accepts Memory requests received on the NT Port Link Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8524 Memory request forwarding in the upstream direction. Does not affect message forwarding and Completions in the upstream direction. 0 = PEX 8524 handles Memory requests received on the NT Port Virtual Interface as Unsupported Requests (UR); for Non-Posted requests, PEX 8524 returns a Completion with UR completion status 1 = PEX 8524 forwards Memory requests from the NT Port Virtual Interface to the Link Interface in the upstream direction	RW	Yes	0
3	**Special Cycle Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
4	**Memory Write and Invalidate** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
5	**VGA Palette Snoop** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
6	**Parity Error Response Enable** Controls the *Master Data Parity Error*.	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
8	**SERR# Enable** Controls the *Signaled System Error* bit. When 1, enables reporting of Fatal and Non-Fatal errors detected by the NT Port Link Interface to the Root Complex.	RW	Yes	0
9	**Fast Back-to-Back Transactions Enabled** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
10	**Interrupt Disable** 0 = NT Port Link Interface is enabled to generate INT*x* Interrupt messages 1 = NT Port Link Interface is prevented from generating INT*x* Interrupt messages	RW	Yes	0
15:11	***Reserved***			00h

Register 16-2. 04h Status/Command *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Status			
18:16	***Reserved***			000b
19	**Interrupt Status** 0 = No INT*x* Interrupt pending 1 = INT*x* Interrupt pending internally to NT Port Link Interface	RO	Yes	0
20	**Capabilities List** Set to 1, as required by the *PCI Express Base r1.0a*.	RO	Yes	1
21	**66 MHz Capable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
22	***Reserved***			0
23	**Fast Back-to-Back Transactions Capable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
24	**Master Data Parity Error** If the *Parity Error Response Enable* bit is set to 1, the NT Port Link Interface sets this bit to 1 when the NT Port: • Forwards the poisoned TLP Write request from the Virtual Interface to the Link Interface, **or** • Receives a Completion marked as poisoned on the Link Interface If the *Parity Error Response Enable* bit is cleared to 0, the PEX 8524 never sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL Timing** ***Not supported*** Always cleared to 00b.	RO	No	00b
27	**Signaled Target Abort** When a Memory-Mapped access payload length is greater than one DWord, the NT Port Link Interface sets this bit to 1. This bit is also set to 1 when the NT Port forwards a Completion with Completer Abort (CA) status from the Virtual Interface to the Link Interface. ***Note:*** *When set during a forwarded Completion, the **Uncorrectable Error Status** register Completer Abort Status bit (offset FB8h[15]) is not updated, because the NT Port does not log the requests that it forwards.*	RW1C	Yes	0

Register 16-2. 04h Status/Command *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
28	**Received Target Abort** Cleared to 0. Never set to 1.	RO	No	0
29	**Received Master Abort** Cleared to 0. Never set to 1.	RO	No	0
30	**Signaled System Error** When the *SERR# Enable* bit is set to 1, the NT Port Link Interface sets this bit to 1 when it transmits an ERR_FATAL or ERR_NONFATAL message to its upstream device. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** The NT Port Link Interface sets this bit to 1 when it receives a Poisoned TLP, regardless of the *Parity Error Response Enable* bit state. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 16-3. 08h Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the silicon revision (AAh, BBh, or BCh for PEX 8524V; BBh or BCh for PEX 8524), PLX-assigned Revision ID for this version of the PEX 8524. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Revision ID with another Revision ID. ***Note:*** ***Silicon Revision BB only*** *– Bit 0 is hardwired to 1 and is not programmable by serial EEPROM.* ***Silicon Revision BC only*** *– Bits [2:0] are hardwired to 100b and are not programmable by serial EEPROM.*	RO	Yes (Refer to Note)	AAh, BBh, or BCh (PEX 8524V) or BBh or BCh (PEX 8524)
Class Code				**068000h**
15:8	**Programming Interface** Cleared to 00h, as required by the *PCI r2.3* for other bridge devices.	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 16-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Cache Line Size** Implemented as a Read-Write field for Conventional PCI compatibility purposes and does not impact PEX 8524 functionality.	RW	Yes	00h
15:8	**Master Latency Timer** Cleared to 00h, as required by the *PCI Express Base r1.0a*.	RO	No	00h
22:16	**Configuration Layout Type** Type 0 Configuration Header for NT Port.	RO	Yes	00h
23	**Function Type** 0 = PEX 8524 is a single-function device	RO	Yes	0
31:24	**BIST** ***Not supported***	RO	No	00h

Register 16-5. 10h Base Address 0 (for NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8524 port Configuration registers into Memory space. NT Port Link BAR0 is configured by the serial EEPROM and Local Host. By default, the BAR Setup register selects 32-bit Memory BAR0 and 32-bit I/O BAR1 for CSR mapping. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = PEX 8524 Configuration registers are mapped anywhere in 32-bit Memory Address space only	RO	Yes	00b
3	**Prefetchable** The Base Address register maps PEX 8524 Configuration registers into Non-Prefetchable Memory space by default. ***Note:*** *Hardwired to 0.*	RO	No	0
16:4	***Reserved***			0-0h
31:17	**Base Address 0** 128-KB Base address in which to map the PEX 8524 Configuration Space registers into Memory space.	RW	Yes	0000h

Register 16-6. 14h Base Address 1

Bit(s)	Description	Type	Serial EEPROM	Default
0	**I/O Space Indicator** 0 = ***Reserved*** 1 = Implemented as an I/O BAR	RO	Yes	1
7:1	***Reserved***			0000_000b
31:8	**I/O Base Address** 256-byte I/O Space Base address. For the NT Port Link Interface, when offset E4h[1:0]=11b, this BAR is enabled.	RW	Yes	0000_00h

Register 16-7. 18h Base Address 2

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR; otherwise, ***reserved***	RO	Yes	0
2:1	**Memory Map Type** 00b = Mappable anywhere in 32-bit Memory space 10b = Mappable anywhere in 64-bit Memory space 01b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
11:4	***Reserved***			00h
31:12	**Base Address 2** Base Address is enabled and sized by the **NT Port Link Interface BAR2/3 Setup** register. This BAR2/BAR3 group uses direct address translation. The minimum BAR size is programmed to 4 KB.	RW	Yes	0000_0h

Register 16-8. 1Ch Base Address 3

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Upper Base Address** NT Port Link Interface upper 32-bit address if BAR2/3 is implemented as a 64-bit BAR; otherwise, ***reserved***. These fields are RW, based on the **NT Port Link Interface BAR2/3 Setup** and **NT Port Link Interface BAR3 Setup** registers. The BAR2/3 group uses direct address translation.	RW	Yes	0-0h

Register 16-9. 20h Base Address 4

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR; otherwise, ***reserved***	RO	Yes	0
2:1	**Memory Map Type** 00b = Mappable anywhere in 32-bit Memory space 10b = Mappable anywhere in 64-bit Memory space 01b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
11:4	***Reserved***			00h
31:12	**Base Address 4** Base Address size is set, and enabled by the **NT Port Link Interface BAR4/5 Setup** register. The BAR4/5 group uses direct address translation. The minimum BAR size is programmed to 4 KB.	RW	Yes	0000_0h

Register 16-10. 24h Base Address 5

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address 5** NT Port Link Interface upper 32-bit address if BAR4/5 is implemented as a 64-bit BAR; otherwise, ***reserved***. These fields are RW, based on the **NT Port Link Interface BAR4/5 Setup** and **NT Port Link Interface BAR5 Setup** registers. The BAR4/5 group uses direct address translation.	RW	Yes	0-0h

Register 16-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Subsystem Vendor ID** Unless overwritten by the serial EEPROM, returns the PLX PCI-SIG-assigned Vendor ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX Vendor ID with another Vendor ID.	HwInit	Yes	10B5h
31:16	**Subsystem ID** Unless overwritten by the serial EEPROM, 8532h is returned by the PEX 8524V and 8524h is returned by the PEX 8524, the PLX-assigned Device ID. The PEX 8524 Serial EEPROM register initialization capability is used to replace the PLX-assigned Device ID with another Device ID.	HwInit	Yes	8532h (PEX 8524V) 8524h (PEX 8524)

Register 16-12. 30h Expansion ROM Base Address

Bit(s)	Description	Type	Serial EEPROM	Default
Silicon Revision AA				
0	**Expansion ROM Enable** 0 = Expansion ROM is disabled 1 = Expansion ROM is enabled	RW	Yes	1
10:1	***Reserved***			0-0h
31:11	**Expansion ROM Base Address** Expansion ROM = 2 KB size (program register initially to FFFF_F801h). ***Note: Expansion ROM size is limited to 2 KB.*** *If Expansion ROM is enabled in Silicon Revision AA, this register must be programmed to the value for 2 KB, FFFF_F801h.*	RW	Yes	0-0h
Silicon Revisions BB/BC				
0	**Expansion ROM Enable** 0 = Expansion ROM is disabled 1 = Expansion ROM is enabled	RW	Yes	1
14:1	***Reserved***			0-0h
31:15	**Expansion ROM Base Address** Expansion ROM = 32 KB maximum size (program register initially to FFFF_8001h). ***Note: This BAR must not be programmed to enable more than 32 KB.*** *Expansion ROM is limited to 32 KB, because the largest serial EEPROM that can be used is 64 KB (limit of 16-bit addressing) and the Expansion ROM image is stored in the serial EEPROM, beginning at address 32 KB.*	RW	Yes	0-0h

Register 16-13. 34h New Capabilities Pointer

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**New Capability Pointer** Default 40h points to the **Power Management Capabilities** register. Do not change this register value.	RO	Yes	40h
31:8	***Reserved***			0000_00h

Register 16-14. 3Ch Interrupt

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Interrupt Line** Interrupt Line Routing Value communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
15:8	**Interrupt Pin** Identifies the Conventional PCI interrupt message(s) the device (or device function) uses. When values = 01h, 02h, 03h, and 04h, maps to Conventional PCI Interrupt messages for INTA#, INTB#, INTC#, and INTD#, respectively. When 0, indicates that the device does not use Conventional PCI Interrupt message(s). Only values 00h or 01h are allowed in the PEX 8524.	RO	Yes	01h
31:16	***Reserved***			0000h

16.5 Power Management Capability Registers

This section details the NT Port Link Interface Power Management registers. The register map is defined in Table 16-3.

Table 16-3. Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Power Management Capabilities		Next Capability Pointer (48h)	Capability ID (01h)	40h
Data	Power Management Control/ Status Bridge Extensions	Power Management Status and Control		44h

Register 16-15. 40h Power Management Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Capability ID** Default = 01h – only value allowed. Indicates that the data structure currently being pointed to is the PCI Power Management data structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **Message Signaled Interrupt Capability** register.	RO	Yes	48h
18:16	**Version** Default = 010b – only value allowed.	RO	Yes	010b
19	**PME Clock** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
20	***Reserved***			0
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** ***Not supported*** Default 000b indicates that the PEX 8524 does ***not support*** Auxiliary Current requirements.	RO	Yes	000b
25	**D1 Support** ***Not supported*** Default 0 indicates that the PEX 8524 does ***not support*** the D1 Power state.	RO	No	0
26	**D2 Support** ***Not supported*** Default 0 indicates that the PEX 8524 does ***not support*** the D2 Power state.	RO	No	0
31:27	**PME Support** Default 0000_0b indicates that the NT Port Link Interface does ***not*** forward PME messages.	RO	Yes	0000_0b

Register 16-16. 44h Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
Power Management Status and Control				
1:0	**Power State** This field is used to determine the current power state of the port, and to set the port into a new power state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
7:2	***Reserved***	RO	No	0h
8	**PME Enable** 0 = Disables PME generation	RO	No	0[a]
12:9	**Data Select** RW by Serial EEPROM mode only[b]. Bits [12:9] select the **Data** and **Data Scale** registers. 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	RO	Yes	0h
14:13	**Data Scale** RW by Serial EEPROM mode only[b]. There are four internal **Data Scale** registers per port. Bits [12:9], *Data Select*, select the **Data Scale** register.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port	RO	No	0[a]
Power Management Control/Status Bridge Extensions				
21:16	***Reserved***			0-0h
22	**B2/B3 Support** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
23	**Bus Power/Clock Control Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
Power Management Data				
31:24	**Data** RW by Serial EEPROM mode only[b]. There are four internal **Data** registers per port. Bits [12:9], *Data Select*, select the **Data** register.	RO	Yes	00h

a. Because the PEX 8524 does not support auxiliary power, this bit is not sticky, and is always cleared to 0 at power-on reset.

*b. With no serial EEPROM, reads return 0h for the **Data Scale** and **Data** registers (for all Data Selects).*

16.6 Message Signaled Interrupt Capability Registers

The Message Signaled Interrupt (MSI) Capability registers are defined in Section 11.8, "Message Signaled Interrupt Capability Registers." Table 16-4 defines the register map used by the NT Port Link Interface.

Table 16-4. Message Signaled Interrupt Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Message Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
Message Address[31:0]				4Ch
Message Upper Address[63:32]				50h
Reserved		Message Data		54h
Reserved				58h – 64h

16.7 PCI Express Capability Registers

This section details the PEX 8524 PCI Express Capability registers. The register map is defined in Table 16-5.

Table 16-5. PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capabilities		Next Capability Pointer (00h)	Capability ID (10h)	68h
Device Capabilities				6Ch
Device Status		Device Control		70h
Link Capabilities				74h
Link Status		Link Control		78h
Reserved				7Ch – 8Ch

Register 16-17. 68h PCI Express Capability List and Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
PCI Express Capability List				
7:0	**Capability ID** Set to 10h by default.	RO	Yes	10h
15:8	**Next Capability Pointer** 00h = PCI Express Capability is the last capability in the first 256-byte Configuration space of the PEX 8524 NT Port Link Interface capability list The PEX 8524 NT Port Link Interface Capabilities list starts at 100h.	RO	Yes	00h
PCI Express Capabilities				
19:16	**Capability Version** The PEX 8524 NT Port Link Interface sets this field to 1h, as required by the *PCI Express Base r1.0a*.	RO	Yes	1h
23:20	**Device/Port Type** Default = PCI Express Endpoint device.	RO	Yes	0h
24	**Slot Implemented** ***Not implemented in the NT Port interface.***	RO	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 0000_0b, because the Base message and MSI messages are the same.	RO	Yes	0000_0b
31:30	***Reserved***			00b

Register 16-18. 6Ch Device Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Maximum Payload Size Supported** 000b = NT Port Link Interface supports 128-byte maximum payload 001b = NT Port Link Interface supports 256-byte maximum payload No other values are supported. ***Note:*** *Serial EEPROM must not load greater than 256 bytes Maximum Payload Size.*	RO	Yes	001b
4:3	**Phantom Functions Supported** ***Not supported*** Cleared to 00b.	RO	Yes	00b
5	**Extended Tag Field Supported** ***Not supported*** 0 = Maximum Tag field is 5 bits 1 = Maximum Tag field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency**	RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency**	RO	Yes	000b
12	**Attention Button Present** For the NT Port Link Interface, this bit, value of 1 indicates that an Attention Button is implemented on that adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Button is ***not*** present on an adapter board for which the PEX 8524 provides the system interface.	HwInit	Yes	1
13	**Attention Indicator Present** For the NT Port Link Interface, this bit, value of 1 indicates that an Attention Indicator is implemented on the adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating an Attention Indicator is ***not*** present on an adapter board for which the PEX 8524 provides the system interface.	HwInit	Yes	1
14	**Power Indicator Present** For the NT Port Link Interface, this bit, value of 1 indicates that a Power Indicator is implemented on the adapter board. The PEX 8524 Serial EEPROM register initialization capability is used to change this value to 0, indicating that a Power Indicator is ***not*** present on an adapter board for which the PEX 8524 provides the system interface.	HwInit	Yes	1
17:15	***Reserved***			000b
25:18	**Captured Slot Power Limit Value** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Scale* field.	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Value* field. 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***			0h

Register 16-19. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables NT Port Link Interface to report Correctable errors to the system host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables NT Port Link Interface to report Non-Fatal errors to the system host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables NT Port Link Interface to report Fatal errors to the system host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables NT Port Link Interface to report Unsupported Request errors as an error message with a programmed uncorrectable error severity	RW	Yes	0
4	**Relaxed Ordering Enable** Cleared to 0, as required by the *PCI Express Base r1.0a*.	RO	No	0
7:5	**Maximum Payload Size** The NT Port Link Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Link Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capabilities** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]). for the Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = Indicates that initially the PEX 8524 port is configured to support a Maximum Payload Size of 128 bytes 001b = Indicates that initially the PEX 8524 port is configured to support a Maximum Payload Size of 256 bytes No other values are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b

Register 16-19. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
8	**Extended Tag Field Enable** ***Not supported*** Cleared to 0.	RO	No	0
9	**Phantom Functions Enable** ***Not supported*** Cleared to 0.	RO	No	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported*** Cleared to 0.	RO	No	0
11	**No Snoop Enable** ***Not supported*** Cleared to 0.	RO	No	0
14:12	**Maximum Read Request Size** ***Not supported*** Cleared to 000b.	RO	No	000b
15	***Reserved***			0
	Device Status			
16	**Correctable Error Detected** 1 = NT Port Link Interface detected a Correctable Error Set when the NT Port Link Interface detects a Correctable Error, regardless of the bit 0 (*Correctable Error Reporting Enable* bit) state.	RW1C	Yes	0
17	**Non-Fatal Error Detected** 1 = NT Port Link Interface detected a Non-Fatal Error Set when the NT Port Link Interface detects a Non-Fatal Error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable* bit) state.	RW1C	Yes	0
18	**Fatal Error Detected** 1 = NT Port Link Interface detected a Fatal Error Set when the NT Port Link Interface detects a Fatal Error, regardless of the bit 2 (*Fatal Error Reporting Enable* bit) state.	RW1C	Yes	0
19	**Unsupported Request Detected** 1 = NT Port Link Interface detected an Unsupported Request Set when the NT Port Link Interface detects an Unsupported Request, regardless of the bit 3 (*Unsupported Request Reporting Enable* bit) state.	RW1C	Yes	0
20	**Auxiliary (AUX) Power Detected** ***Not supported*** Cleared to 0.	RO	No	0
21	**Transactions Pending** Because PEX 8524 NT ports are a bridging device, they do not track non-posted and Completion for the corresponding non-posted transactions. Therefore, the NT Port Link Interface does not implement this bit.	RO	No	0
31:22	***Reserved***			000h

Register 16-20. 74h Link Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Maximum Link Speed** Set to 0001b for 2.5 Gbps.	RO	Yes	0001b
9:4	**Maximum Link Width** Actual link width is set by signal ball strapping options. The PEX 8524 Maximum Link Width is x8 = 00_1000b (Station 0), or x16 = 01_0000b (Station 1).	RO	No	Strap levels
11:10	**Active State Power Management (ASPM) Support** Indicates the level of ASPM supported by the port. 01b = L0s link power state entry is supported All other values are ***reserved***.	RO	Yes	01b
14:12	**L0s Exit Latency** 101b = NT Port Link Interface L0s Exit Latency is between 1 and 2 µs	RO	No	101b
17:15	**L1 Exit Latency** 101b = NT Port Link Interface L1 Exit Latency is between 16 and 32 µs	RO	Yes	101b
23:18	***Reserved***			0-0h
31:24	**Port Number** The NT Port Number is selected by signal ball strapping options. Refer to STRAP_NT_UPSTRM_PORTSEL[3:0] for details.	HwInit	No	Set by strap levels

Register 16-21. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** 00b = Disables L0s Link Interface Entry for NT Port 01b = Enables L0s Entry 10b and 11b are ***not allowed***.	RW	Yes	00b
2	***Reserved***			0
3	**Read Completion Boundary (RCB)** ***Not supported*** Cleared to 0.	RO	Yes	0
4	**Link Disable** ***Reserved*** for NT Port Link Interface.	RO	No	0
5	**Retrain Link** ***Reserved*** for NT Port Link Interface.	RO	No	0
6	**Common Clock Configuration** 0 = NT Port Link Interface and the device at the other end of the PCI Express link are operating with an **asynchronous** reference clock 1 = NT Port Link Interface and the device at the other end of the PCI Express link are operating with a **distributed** common reference clock	RW	Yes	0
7	**Extended SYNC** Set to 1 causes the NT Port Link Interface to transmit: • 4,096 FTS Ordered-Sets in the L0s state, • Followed by a single SKIP Ordered-Set prior to entering the L0 state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the Recovery state.	RW	Yes	0
15:8	***Reserved***			00h

Register 16-21. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
Link Status				
19:16	**Link Speed** NT Port Link Interface set to 1h for 2.5 Gbps.	RO	Yes	1h
25:20	**Negotiated Link Width** Indicates the negotiated width of the PCI Express link. 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 (Station 1 only) All other values are ***not supported***. The value in this field is undefined when the link is not up.	RO	Yes	00_0001b
26	**Training Error** ***Reserved*** for NT Port Link Interface.	RO	No	0
27	**Link Training** ***Reserved*** for NT Port Link Interface.	RO	No	0
28	**Slot Clock Configuration** Upstream port or NT Port Link Interface is set, but not both. 0 = Indicates that the PEX 8524 uses an independent clock 1 = Indicates that the PEX 8524 uses the same physical reference clock that the platform provides on the connector	HwInit	Yes	0
31:29	***Reserved***			000b

16.8 NT Port Registers

16.8.1 NT Port Link Interface Interrupt Request (IRQ) Doorbell Registers

The PEX 8524 NT Port Interrupt Control (Doorbell) registers are defined in Section 15.8.1, "NT Port Virtual Interface IRQ Doorbell Registers." Table 16-6 defines the register map used by the NT Port Link Interface.

Table 16-6. NT Port Link Interface Interrupt Request (IRQ) Doorbell Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Set Virtual Interface IRQ	90h
Reserved	Clear Virtual Interface IRQ	94h
Reserved	Set Virtual Interface IRQ Mask	98h
Reserved	Clear Virtual Interface IRQ Mask	9Ch
Reserved	Set Link Interface IRQ	A0h
Reserved	Clear Link Interface IRQ	A4h
Reserved	Set Link Interface IRQ Mask	A8h
Reserved	Clear Link Interface IRQ Mask	ACh

16.8.2 NT Port Scratchpad (Mailbox) Registers

This section details the PEX 8524 NT Port Scratchpad (Mailbox) registers. The register map is defined in Table 16-7.

Table 16-7. PEX 8524 NT Port Scratchpad (Mailbox) Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Scratchpad_0	B0h
NT Port Scratchpad_1	B4h
NT Port Scratchpad_2	B8h
NT Port Scratchpad_3	BCh
NT Port Scratchpad_4	C0h
NT Port Scratchpad_5	C4h
NT Port Scratchpad_6	C8h
NT Port Scratchpad_7	CCh

Register 16-22. B0h NT Port Scratchpad_0

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_0** 32-bit Scratchpad_0 register.	RW	Yes	0-0h

Register 16-23. B4h NT Port Scratchpad_1

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_1** 32-bit Scratchpad_1 register.	RW	Yes	0-0h

Register 16-24. B8h NT Port Scratchpad_2

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_2** 32-bit Scratchpad_2 register.	RW	Yes	0-0h

Register 16-25. BCh NT Port Scratchpad_3

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_3** 32-bit Scratchpad_3 register.	RW	Yes	0-0h

Register 16-26. C0h NT Port Scratchpad_4

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_4** 32-bit Scratchpad_4 register.	RW	Yes	0-0h

Register 16-27. C4h NT Port Scratchpad_5

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_5** 32-bit Scratchpad_5 register.	RW	Yes	0-0h

Register 16-28. C8h NT Port Scratchpad_6

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_6** 32-bit Scratchpad_6 register.	RW	Yes	0-0h

Register 16-29. CCh NT Port Scratchpad_7

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Scratchpad_7** 32-bit Scratchpad_7 register.	RW	Yes	0-0h

16.8.3 NT Port Link Interface BAR Setup Registers

This section details the NT Port Link Interface BAR Setup registers. The register map is defined in Table 16-8.

Table 16-8. PEX 8524 NT Port Link Interface BAR Setup Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				D0h – E0h
NT Port Link Interface BAR0/BAR1 Setup				E4h
NT Port Link Interface BAR2/3 Setup				E8h
NT Port Link Interface BAR3 Setup				ECh
NT Port Link Interface BAR4/5 Setup				F0h
NT Port Link Interface BAR5 Setup				F4h

Register 16-30. E4h NT Port Link Interface BAR0/BAR1 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	**BAR0 Type** 00b = 32-bit memory **BAR0** 11b = Link Interface **BAR0** is a 32-bit Memory BAR and Link Interface **BAR1** is an I/O BAR All other codes disable **BAR1** implementation.	RW	Yes	11b
31:2	***Reserved***			0-0h

Register 16-31. E8h NT Port Link Interface BAR2/3 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Type**	RO	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit BAR 10b = **BAR2/3** is implemented as a 64-bit BAR ***Note:*** *It is illegal to program 10b and clear the* ***NT Port Link Interface BAR3 Setup*** *register BAR3 Enable bit (offset ECh[31]).*	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
30:12	**BAR2 Size** Specifies the Address Range size requested by BAR2. 0 = Corresponding bits in **BAR2** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR2** are RW bits	RW	Yes	0000_0h
31	**BAR2 Enable** 0 = **BAR2** is disabled (bits [2:1] = 00b), all bits in **BAR2** read 0 1 = **BAR2** is enabled, Size and Type specified in this register	RW	Yes	0

Register 16-32. ECh NT Port Link Interface BAR3 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
30:0	**BAR3 Size** Specifies the Address Range size requested by **BAR2/3** in 64-bit mode when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is set to 10b. 0 = Read-Only bits that always return 0, writes are ignored 1 = Corresponding bits are RW bits	RW	Yes	0-0h
	Reserved when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is cleared to 00b.			0
31	**BAR3 Enable** 0 = **BAR3** is disabled 1 = **BAR2/3** is enabled when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is set to 10b ***Note:*** *It is illegal to program the* ***NT Port Link Interface BAR2/3 Setup*** *register BAR2 Type field (offset E8h[2:1]) to 10b and clear this bit.*	RW	Yes	0
	Reserved when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is cleared to 00b.			0

Register 16-33. F0h NT Port Link Interface BAR4/5 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Type**	RO	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit BAR 10b = **BAR4/5** is implemented as a 64-bit Memory BAR ***Note:*** *It is illegal to program 10b and clear the* ***NT Port Link Interface BAR5 Setup*** *register BAR5 Enable bit (offset F4h[31]).*	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
11:4	***Reserved***			00h
30:12	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding bits in **BAR4** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR4** are RW bits	RW	Yes	0000_0h
31	**BAR4 Enable** When bits [2:1] = 00b, enables **BAR4**; otherwise, belongs to the *BAR4 Size*[30:12] field. 0 = **BAR4** is disabled, all bits in **BAR4** read 0 1 = **BAR4** is enabled, Size and Type specified in this register	RW	Yes	0

Register 16-34. F4h NT Port Link Interface BAR5 Setup

Bit(s)	Description	Type	Serial EEPROM	Default
30:0	**BAR5 Size** Together with the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Size* field (offset F0h[31:12]), specifies the Address Range size requested by **BAR4/5** in 64-bit mode when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is set to 10b. 0 = Corresponding bits in **BAR5** are Read-Only bits that always return 0, and Writes are ignored 1 = Corresponding bits in **BAR5** are RW bits	RW	Yes	0-0h
	Reserved when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is cleared to 00b.			0-0h
31	**BAR5 Enable** 0 = **BAR5** is disabled 1 = **BAR4/5** is enabled when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is set to 10b ***Note:*** *It is illegal to program the* ***NT Port Link Interface BAR4/5 Setup*** *register BAR4 Type field (offset F0h[2:1]) to 10b and clear this bit.*	RW	Yes	0
	Reserved when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is cleared to 00b.			0

16.8.4 NT Port Cursor Mechanism Control Registers

This section details the NT Port Cursor Mechanism Control registers. The register map for the Virtual and Link Interfaces is defined in Table 16-9.

The Cursor Mechanism registers at offsets F8h/FCh provide a means for accessing PCI Express Extended Configuration Space registers (100h through FFFh) within the NT Port Virtual and Link Interfaces, when only standard PCI Configuration transactions (that do not support Extended Register Number), and/or I/O Request transactions (using the NT Port **BAR1** address, if enabled) are available. The Cursor Mechanism can generally access only those registers that are defined by the *PCI Express Base r1.0a*, and not the device-specific registers.

Table 16-9. NT Port Cursor Mechanism Control Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Configuration Address Window		***Reserved***		F8h
Configuration Data Window				FCh

Register 16-35. F8h Configuration Address Window

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	***Reserved***			0000h
25:16	**Offset** Register Offset	RW	Yes	000h
30:26	***Reserved***			0h
31	**Interface Select** 0 = Access to NT Port Link Interface Type 0 Configuration Space register 1 = Access to NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 16-36. FCh Configuration Data Window

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Data Window** Software selects a register by writing into the NT Port Link Interface Configuration Address window, then reads or writes to that register using this register.	RW	Yes	0-0h

16.9 Device Serial Number Extended Capability Registers

The NT Port Link Interface Device Serial Number Extended Capability registers are the same as the PEX 8524 Transparent port registers defined in Section 11.10, "Device Serial Number Extended Capability Registers." The register map is defined in Table 16-10 and applies to the Virtual and Link Interfaces.

Table 16-10. PEX 8524 Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h) / Capability Version (1h)	Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Higher DW)		108h

16.10 Power Budgeting Extended Capability Registers

The NT Port Link Interface Power Budgeting Extended Capability registers are the same as the PEX 8524 Transparent port registers defined in Section 11.11, "Power Budgeting Extended Capability Registers." The register map is defined in Table 16-11 and applies to the Virtual and Link Interfaces.

Table 16-11. PEX 8524 Power Budgeting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h) / Capability Version (1h)	Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budgeting Data		140h
Reserved	Power Budget Capability	144h

16.11 Virtual Channel Extended Capability Registers

The Virtual Channel Capability registers defined in Section 11.12, "Virtual Channel Extended Capability Registers," are also applicable to the NT Port Link Interface. Table 16-12 defines the register map.

The **Port VC Capability 1**, **VC0 Resource Control**, and **VC1 Resource Control** (offsets 14Ch, 15Ch, and 16Ch, respectively) register values are shadowed in the **NT Link Interface VC Capability 1**, **NT Link Interface VC0 Resource Control**, and **NT Link Interface VC1 Resource Control Shadow** registers (offsets D64h, D5Ch, and D60h, respectively).

Note: *These registers are not automatically shadowed when programmed by serial EEPROM; therefore, if the serial EEPROM programs these registers to non-default values, software must write the values to the registers (such as by reading the register and writing back the value), to cause the corresponding Shadow registers in the NT Port Virtual Interface to update.*

Table 16-12. Link Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (000h) / Capability Version (1h)	Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
VC1 Resource Capability		164h
VC1 Resource Control		168h
VC1 Resource Status	***Reserved***	16Ch
Reserved		170h – 1B4h
Virtual Channel Arbitration Table		1B8h … 1C4h

16.12 PLX-Specific Registers

The PEX 8524 NT mode Link Interface PLX-Specific registers are defined in Section 11.13, "PLX-Specific Registers," except as defined in Table 16-13 through Table 16-16 and/or their respective register tables. The entire register map is defined in Table 16-13.

Note: *This register group is accessed using a Memory-Mapped cycle. It is recommended that these register values* ***not*** *be changed.*

Table 16-13. NT Port Link Interface PLX-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Error Checking and Debug Registers	1C8h … 1FCh
Physical Layer Registers	200h … 2C4h
CAM Routing Registers	2C8h … 344h
NT Port Link Interface Ingress Control Register	660h … 668h
I/O CAM Base and Limit Upper 16 Bits Registers	680h … 6ACh
Base Address Registers (BARs)	6C0h … 73Ch
Shadow Virtual Channel (VC) Capability Registers	740h … 9ECh
Ingress Credit Handler (INCH) Registers	9F0h … B7Ch
Reserved	B80h – BFCh
Internal Credit Handler (ITCH) VC&T Threshold Registers	C00h … C08h

16.12.1 Error Checking and Debug Registers

The NT mode Link Interface Error Checking and Debug registers are defined in Section 11.13.1, "Error Checking and Debug Registers," except as defined in Table 16-14 (offsets 1D4h through 1D8h are ***reserved***) and the register tables that follow.

Table 16-14. PLX-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				1C8h
Error Handler 32-Bit Error Status ***(Factory Test Only)***				1CCh
Error Handler 32-Bit Error Mask ***(Factory Test Only)***				1D0h
Reserved				1D4h – 1D8h
Debug Control				1DCh
Reserved				1E0h
Egress NT Port Link Interface Control and Status				1E4h
Reserved				1E8h – 1ECh
Silicon Revision AA – ***Reserved*** Silicon Revisions BB/BC – PLX-Specific Relaxed Ordering Enable				1F0h
Reserved				1F4h
Reserved		ACK Transmission Latency Limit		1F8h
Reserved				1FCh

a. Some registers are port-specific, some are station-specific, and some are device-specific.

Note: *All errors in register offset 1CCh generate MSI/INTx interrupts, when enabled.*

Register 16-37. 1CCh Error Handler 32-Bit Error Status *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Error Handler Completion FIFO Overflow Status** 0 = No overflow detected 1 = Completion FIFO Overflow detected when 4-deep completion FIFO for ingress, or 2-deep completion FIFO for egress, overflows	RW1CS	Yes	0
10:1	***Reserved***		No	0h
11	**Credit Update Timeout Status** No useful credit update to make forward progress for 512 ms or 1s (disabled by default). 0 = No Credit Update Timeout detected 1 = Credit Update Timeout completed	RW1CS	Yes	0
12	**INCH Underrun Error** Ingress Credit Underrun. 0 = No error detected 1 = Credit underrun error detected	RW1CS	Yes	0
31:13	***Reserved***		No	0h

Note: *Error logging is enabled in register offset 1D0h, by default.*

Register 16-38. 1D0h Error Handler 32-Bit Error Mask *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Error Handler Completion FIFO Overflow Status Masked** 0 = No effect on reporting activity 1 = *Error Handler Completion FIFO Overflow Status* bit is masked/disabled	RWS	Yes	1
10:1	***Reserved***		No	0h
11	**Credit Update Timeout Status Masked** 0 = No effect on reporting activity 1 = *Credit Update Timeout Status* bit is masked/disabled	RWS	Yes	1
12	**INCH Underrun Error Masked** 0 = No effect on reporting activity 1 = *INCH Underrun Error* bit is masked/disabled	RWS	Yes	1
31:13	***Reserved***		No	0h

Register 16-39. 1E4h Egress NT Port Link Interface Control and Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Egress Credit Update Timer Enable** 0 = Disables Egress Credit Update Timer 1 = Enables Egress Credit Update Timer	RW	Yes	0
1	**Egress Credit Timeout Value** 0 = Minimum 512 ms (Maximum 768 ms) 1 = Minimum 1,024 ms (Maximum 1,280 ms)	RW	Yes	0
2	**Egress Debug** ***Factory Test Only***	RW	Yes	0
15:3	***Reserved***			0-0h
19:16	**VC&T Encountered Timeout** 0h = VC0 Posted 1h = VC0 Non-Posted 2h = VC0 Completion 3h = VC1 Posted 4h = VC1 Non-Posted 5h = VC1 Completion	RO	Yes	0h
31:20	***Reserved***			000h

Register 16-40. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**ACK Transmission Latency Limit** The value of this register remains 00h.	RW	Yes	00h
15:8	**HPC Test Bits** ***Factory Test Only.*** Testing bits – must be 00h.	RW	Yes	00h
31:16	***Reserved***			0000h

16.12.2 NT Port Link Interface Physical Layer Registers

The NT Port Link Interface Physical Layer registers are defined in Section 11.13.2, "Physical Layer Registers," except as defined in Table 16-15 and the register table that follows.

Table 16-15. PLX-Specific NT Port Link Interface Physical Layer Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				200h – 20Ch
Phy User Test Pattern 0				210h
Phy User Test Pattern 4				214h
Phy User Test Pattern 8				218h
Phy User Test Pattern 12				21Ch
Physical Layer Status		Physical Layer Command		220h
Port Configuration				224h
Physical Layer Test				228h
Physical Layer				22Ch
Physical Layer Port Command				230h
SKIP Ordered-Set Interval				234h
Quad 0 SerDes Diagnostic Data				238h
Quad 1 SerDes Diagnostic Data				23Ch
Quad 2 SerDes Diagnostic Data				240h
Quad 3 SerDes Diagnostic Data				244h
SerDes Nominal Drive Current Select				248h
SerDes Drive Current Level Select 1				24Ch
SerDes Drive Current Level Select 2				250h
SerDes Drive Equalization Level Select 1				254h
SerDes Drive Equalization Level Select 2				258h
Reserved				25Ch – 2C4h

Register 16-41. 220h Physical Layer Command and Status (Only Ports 0, 8, and NT Port Link Interface)

Bit(s)	Description	Type	Serial EEPROM	Default
	Physical Layer Command			
0	**Port Enumerator Enable** 0 = Enumerate not enabled 1 = Enumerate enabled	HwInit	No	0
1	**TDM Enable** 0 = TDM not enabled 1 = TDM enabled	HwInit	No	0
2	***Reserved***			0
3	**Upstream Port as Configuration Master Enable** 0 = Upstream Port Cross-link not supported 1 = Upstream Port Cross-link supported	RW	No	0
4	**Downstream Port as Configuration Slave Enable** 0 = Downstream Port Cross-link not supported 1 = Downstream Port Cross-link supported	RW	No	0
5	**Lane Reversal Disable** 0 = Lane reversal supported 1 = Lane reversal not supported	RW	No	0
6	***Reserved***			0
7	**FC-Init Triplet Enable** Flow control Initialization. 0 = Init FL1 Triplet can be interrupted by SKIP Ordered-Set/Idle Data symbol 1 = Init FL1 Triplet not interrupted	RW	No	1
15:8	**N_FTS Value** N_FTS value to transmit in training sets.	RW	No	40h
	Physical Layer Status			
19:16	***Reserved***			0h
22:20	**Number of Ports Enumerated** Number of ports in current configuration.	HwInit	No	00b
23	***Reserved***			0
24	**Port 0 or 8 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow	RW1C	No	0
25	**Port 1 or 9 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow	RW1C	No	0
26	**Port 10 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow ***Reserved*** for Station 0.	RW1C	No	0
27	**Port 11 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow ***Reserved*** for Station 0.	RW1C	No	0
31:28	***Reserved***			0h

16.12.3 NT Port Link Interface Ingress Control Register

The NT Port Link Interface Ingress Control register is defined in Section 11.13.4, "Ingress Control Registers," with the addition of the **Ingress Control** register *No Snoop Disable* bit (bit 24) and bit 25 is changed to ***Factory Test Only***. The register map is defined in Table 16-16.

Table 16-16. PLX-Specific NT Port Link Interface Ingress Control Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Reserved				664h – 668h

Register 16-42. 660h Ingress Control (Only Ports 0 and 8)

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Enable CSR Access by Downstream Devices** **Silicon Revision AA** Enables acceptance of Configuration requests from a Requester that is downstream from a Transparent port, targeting any downstream Transparent port's Type 1 Header registers or NT Port Virtual Interface Type 0 Header registers (*such as* for Peer Configuration access). 0 = Configuration requests from a downstream device are ***not supported***; the downstream port flags an Uncorrectable Error, and, returns a Completion with Unsupported Request (UR) specified in the *Completion Status* field, to the downstream Requester. Only this mode is *PCI Express Base r1.0a*-compliant. 1 = The following types of Configuration requests from downstream Requesters are allowed: • Type 0 requests targeting the Type 1 Header registers in that downstream port • Type 1 requests targeting the Type 1 Header registers in other downstream Transparent ports, and • Type 1 requests targeting the Type 0 Header registers in the NT Port Virtual Interface The upstream port registers are not accessible from the downstream port. **Silicon Revisions BB/BC** Enables acceptance of both Configuration and Memory requests from a Requester that is downstream from a Transparent port, targeting any PEX 8524 registers. 0 = Configuration requests from a downstream device are ***not supported***; the downstream port flags an Uncorrectable Error, and, returns a Completion with Unsupported Request (UR) specified in the *Completion Status* field, to the downstream Requester. Only this mode is *PCI Express Base r1.0a*-compliant. 1 = Configuration and Memory requests from downstream Requesters, targeting any PEX 8524 registers in any port, are allowed. ***Notes:*** *This bit can be initially set only through the upstream port, the NT Port Link Interface, or serial EEPROM, to enable register access through downstream Transparent ports; a Requester downstream from a Transparent port cannot set the bit to grant itself (or peers) access to PEX 8524 registers. Configuration requests can access those registers that are defined by PCI-SIG specifications, and generally cannot access device-specific registers other than the NT Port* ***Cursor Mechanism*** *registers. Memory requests can access all PEX 8524 registers.* *Configuration requests can access the NT Port* ***Cursor Mechanism*** *registers (offsets F8h/FCh) to provide indirect access to NT Port offsets above 100h, for Conventional PCI Requesters such as a PCI Master connected to a PCI Express-to-PCI bridge, that cannot generate Configuration requests containing an Extended Register Number. The NT Port Virtual Interface Cursor Mechanism (but not the NT Port Link Interface Cursor Mechanism) can access device-specific registers that exist in the NT Port; if Port 0 is the NT Port, the NT Port Virtual Interface Cursor Mechanism can access the device-specific registers (which exist only in Port 0) and the Station 0 registers (which exist in Port 0 for all enabled ports in Station 0).*	RW	Yes	0
1	**Disable Unsupported Request Response for *Reserved* Configuration Registers**	RW	Yes	0
23:2	***Factory Test Only***	RW	Yes	0-0h

Register 16-42. 660h Ingress Control (Only Ports 0 and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
24	**No Snoop Disable** **Silicon Revision AA** ***Not supported*** **Silicon Revisions BB/BC** Forces the packet header No Snoop attribute bit to 0, for all packets transferred between the NT Link and Virtual Interfaces (across the NT boundary, in both directions). Can be used to handle cache coherency-related issues in a system. 0 = Disables No Snoop Disable feature 1 = Enables No Snoop Disable feature	RW	Yes	0
26:25	***Factory Test Only***	RW	Yes	00b
27	***Reserved*** **Silicon Revision AA**			0
	BIOS Enumeration Fix Disable **Silicon Revisions BB/BC** For NT Failover in Silicon Revisions BB/BC, this bit must be set.	RW	Yes	0
31:28	***Factory Test Only***	RW	Yes	0h

16.13 PEX 8524 Non-Transparent Bridging-Specific Registers

Table 16-17 defines the register map of the registers implemented to support the PEX 8524 Non-Transparent Bridging function. The NT station contains the main copy of these registers, and the Transparent station contains the shadow copy of these registers. These registers are accessed by Memory-Mapped access to Port 0, Port 8, or NT Port.

Table 16-17. NT Port Link Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Link Interface Memory Address Translation and Limit BAR Registers				C3Ch … C58h
Reserved				C5Ch – DB0h
NT Port Link Interface Receive Lookup Table Entry Registers				DB4h … DF0h
Reserved				DF4h – FB0h

16.13.1 NT Port Link Interface Memory Address Translation and Limit BAR Registers

The NT station contains the main copy of these registers, and the Transparent station contains the shadow copy of these registers. Program **only** the main copy. The Shadow register is automatically updated. The reverse is not true. The register map is defined in Table 16-18.

Table 16-18. NT Port Link Interface Memory Address Translation and Limit BAR Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Memory BAR2/3 Address Translation[31:0]	C3Ch
Memory BAR2/3 Address Translation[63:32]	C40h
Memory BAR4/5 Address Translation[31:0]	C44h
Memory BAR4/5 Address Translation[63:32]	C48h
Memory BAR2/3 Limit[31:0]	C4Ch
Memory BAR2/3 Limit[63:32]	C50h
Memory BAR4/5 Limit[31:0]	C54h
Memory BAR4/5 Limit[63:32]	C58h

Register 16-43. C3Ch Memory BAR2/3 Address Translation[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR2/3 Base Translation Address[31:12]** NT Port Link Interface Base Translation address when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Enable* bit (offset E8h[31]) is set to 1.	RW	Yes	0-0h

Register 16-44. C40h Memory BAR2/3 Address Translation[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**BAR2/3 Base Translation Address[63:32]** NT Port Link Interface Base Translation upper address when BAR2/3 is enabled as a 64-bit BAR [**NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is set to 10b].	RW	Yes	0-0h
	Read-Only when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is cleared to 00b.	RO	No	0-0h

Register 16-45. C44h Memory BAR4/5 Address Translation[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR4/5 Base Translation Address[31:12]** NT Port Link Interface Base Translation address when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Enable* bit (offset F0h[31]) is set to 1.	RW	Yes	0-0h

Register 16-46. C48h Memory BAR4/5 Address Translation[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**BAR4/5 Base Translation Address[63:32]** NT Port Link Interface Base Translation upper address BAR 4/5 is enabled as a 64-bit BAR [**NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is set to 10b].	RW	Yes	0-0h
	Read-Only when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is cleared to 00b.	RO	No	0-0h

Register 16-47. C4Ch Memory BAR2/3 Limit[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR2/3 Limit[31:0]** Contains the address of the memory window lower limit defined in the **NT Port Link Interface BAR2/3 Setup** register (offset E8h). 1 MB granularity. When the limit is greater than the window size, the limit is ignored.	RW	Yes	000h

Register 16-48. C50h Memory BAR2/3 Limit[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**BAR2/3 Limit[63:32]** Contains the address of the memory window upper limit defined in the **NT Port Link Interface BAR3 Setup** register (offset ECh), when the following conditions exist: • **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is set to 10b, and • **NT Port Link Interface BAR3 Setup** register *BAR3 Enable* bit (offset ECh[31]) is set to 1 When the limit is greater than the window size, the limit is ignored.	RW	Yes	0-0h
	Read-Only when the **NT Port Link Interface BAR2/3 Setup** register *BAR2 Type* field (offset E8h[2:1]) is cleared to 00b.	RO	No	0-0h

Register 16-49. C54h Memory BAR4/5 Limit[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	***Reserved***			0-0h
31:12	**BAR4/5 Limit[31:0]** Contains the address of the memory window lower limit defined in the **NT Port Link Interface BAR4/5 Setup** register (offset F0h). 1 MB granularity. When the limit is greater than the window size, the limit is ignored.	RW	Yes	0-0h

Register 16-50. C58h Memory BAR4/5 Limit[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**BAR4/5 Limit[63:32]** Contains the address of the memory window upper limit defined in the **NT Port Link Interface BAR4/5 Setup** register (offset F0h), when the following conditions exist: • **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is set to 10b, and • **NT Port Link Interface BAR5 Setup** register *BAR5 Enable* bit (offset F4h[31]) is set to 1 When the limit is greater than the window size, the limit is ignored.	RW	Yes	0-0h
	Read-Only when the **NT Port Link Interface BAR4/5 Setup** register *BAR4 Type* field (offset F0h[2:1]) is cleared to 00b.	RO	No	0-0h

16.13.2 NT Port Link Interface Receive Lookup Table Entry Registers

This section describes the NT Port Link Interface Receive (Requester ID Translation) Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- TLP request from NT Port Link Interface to the Virtual Interface, or
- Completion TLP from NT Port Virtual Interface to the Link Interface

The NT station contains the main copy of these registers, and the Transparent station contains the shadow copies of these registers. Program **only** the main copy. The Shadow register is automatically updated. The reverse is not true.

Table 16-19 defines the register and address locations. The register descriptions that follow the table define the bit definitions that apply to the registers.

Note: *Writes to NT Port **Link Interface Receive Lookup Table Entry** registers (offsets DB4h through DF0h) are automatically copied to the same offsets in the NT Port Virtual Interface. If these NT Port Link Interface registers are programmed by serial EEPROM, the same data values must be programmed into the same register offsets in the NT Port Virtual Interface (that is, the values in serial EEPROM DWord addresses A4Dh through A5Ch must also be programmed into serial EEPROM DWord addresses B45h through B54h, respectively).*

Additionally, software must copy the values to the same offsets in the non-NT Station (Port 0 or Port 8). If the NT Port is one of Ports 8 through 11, software must read the value(s) in the NT Port Link Interface and write the value(s) to the same offsets (DB4h through DF0h) in Port 0; if the NT Port is one of Ports 0 through 3, software must read the value(s) in the NT Port Link Interface and write the value(s) to the same offsets (DB4h through DF0h) in Port 8.

Table 16-19. Link Interface Receive Lookup Table Entry_*n_m* Register Locations

ADDR Location	Lookup Table Entry_*n_m*	ADDR Location	Lookup Table Entry_*n_m*
DB4h	0_1	DD4h	16_17
DB8h	2_3	DD8h	18_19
DBCh	4_5	DDCh	20_21
DC0h	6_7	DE0h	22_23
DC4h	8_9	DE4h	24_25
DC8h	10_11	DE8h	26_27
DCCh	12_13	DECh	28_29
DD0h	14_15	DF0h	30_31

Register 16-51. DB4h - DF0h Link Interface Receive Lookup Table Entry_*n_m* (where *n_m* = 0_1 through 30_31)

Bit(s)	Description		Type	Serial EEPROM	Default
0	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0
2:1	***Reserved***				00b
7:3	**Requester ID**	**LUT Entry_*n* Device Number**	RW	Yes	0000_0b
15:8		**LUT Entry_*n* Bus Number**	RW	Yes	00h
16	**LUT Entry_*m* Enable** 0 = Disables 1 = Enables		RW	Yes	0
18:17	***Reserved***				00b
23:19	**LUT Entry_*m* Device Number**		RW	Yes	0000_0b
31:24	**LUT Entry_*m* Bus Number**		RW	Yes	00h

16.14 Advanced Error Reporting Capability Registers

The Advanced Error Reporting Capability registers for the NT Port Link Interface are equivalent to those defined in Section 11.14, "Advanced Error Reporting Capability Registers." The registers are duplicated for the NT Port Link Interface, and Table 16-20 defines the register map.

Table 16-20. Advanced Error Reporting Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log_0		FD0h
Header Log_1		FD4h
Header Log_2		FD8h
Header Log_3		FDCh
Reserved	FE0h –	FFCh

Chapter 17 Test and Debug

17.1 Physical Layer Loop-Back Operation

17.1.1 Overview

Physical layer loop-back functions are used to test SerDes in the PEX 8524, connections between devices, SerDes of external devices, and certain PEX 8524 and external digital logic.

The PEX 8524 supports five types of loop-back operations:

- **Internal Loop-Back** – Connects SerDes serial Tx output to serial Rx input. The Pseudo-Random Bit Sequence (PRBS) generator is used to create a pseudo-random data pattern that is transmitted and returned to the PRBS checker.
- **Analog Loop-Back Master** – The PEX 8524 enters Analog Loop-Back Master mode when the **Physical Layer Port Command** register *Port x Loop-Back Command* bit (Port 0 or 8, offset 230h[0, 4, 8, and/or 12]) is set. This method depends on an external device or dumb connection (*such as* a cable) to loop back the transmitted data to the PEX 8524. The Slave device must not include its elastic buffer in the Loop-Back data path because no SKIP Ordered-Sets are transmitted. Use the PRBS generator and checker to create and check the data pattern.
- **Digital Loop-Back Master** – The PEX 8524 enters Digital Loop-Back Master mode when the **Physical Layer Port Command** register *Port x Loop-Back Command* bit (Port 0 or 8, offset 230h[0, 4, 8, and/or 12]) is set. As with Analog Loop-Back Master mode, this method depends upon an external Slave device to loop back the transmitted data. This method is best utilized with an external Slave device that includes at least its elastic buffer in the Loop-Back data path. The PEX 8524 provides programmable test pattern generators and checkers that insert the SKIP Ordered-Set at the proper intervals.
- **Analog Loop-Back Slave** – The PEX 8524 enters Analog Loop-Back Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively set in the TS1 Training Control symbol, and the **Physical Layer Test** register *Analog Loop-Back Enable* bit (Port 0 or 8, offset 228h[4]) is set. The received data is looped back from the SerDes 10-bit receive interface to the 10-bit transmit interface. All digital logic is excluded from the Loop-Back data path.
- **Digital Loop-Back Slave** – The PEX 8524 enters Digital Loop-Back Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively set in the TS1 Training Control symbol, and the **Physical Layer Test** register *Analog Loop-Back Enable* bit (Port 0 or 8, offset 228h[4]) is cleared. In this mode, the data is looped back at an 8-bit level, which includes the PEX 8524 elastic buffer, 8b/10b decoder, and 8b/10b encoder in the Loop-Back data path.

17.1.1.1 Loop-Back Test Modes

The PEX 8524 supports all Loop-Back modes described in the *PCI Express Base r1.0a*. To establish a PEX 8524 port as a Loop-Back Master, the serial EEPROM is used to write 1 to the appropriate **Physical Layer Port Command** register *Port x Loop-Back Command* bit (Port 0 or 8, offset 230h[0, 4, 8, and/or 12]). This enables the selected port to set the *Loopback* bit in the Training Control symbol of the TS1 Ordered-Set during the *Configuration.Linkwidth.Start* state.

After a port is established as a Loop-Back Master, the corresponding **Physical Layer Port Command** register *Port x Ready as Loop-Back Master* status bit (Port 0 or 8, offset 230h[3, 7, 11, and/or 15]) is set. Depending on the capability of the Loop-Back Slave, the PRBS generator or **Phy User Test Pattern *x*** registers (Port 0 or 8, offsets 210h through 21Ch) are used to create a bit stream that is checked by appropriate checking logic.

When the PEX 8524 is established as a Loop-Back Slave, it can operate as an Analog or Digital (default) Far-End device:

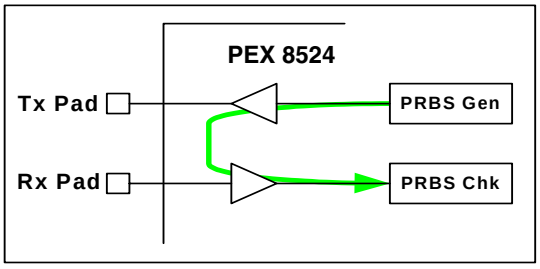
- Analog Loop-Back mode is selected by setting the **Physical Layer Test** register *Analog Loop-Back Enable* bit (Port 0 or 8, offset 228h[4]) to 1. In Analog Slave Loop-Back mode, the received data is looped back from the 10-bit received data, to the 10-bit transmit data.
- When Digital Loop-Back mode is selected (power-on default), the data is looped back from the 8-bit decoded received data to the 8-bit transmit data path. This loop-back point allows the elastic buffer 8b/10b decoder and 8b/10b encoder to be included in the test data path. Digital Loop-Back mode requires that the SKIP Ordered-Sets be included in the data stream.

17.1.2 Internal Loop-Back

Figure 17-1 illustrates the Loop-Back data path when Internal Loop-Back mode is enabled. The only items in the data path are the serializer and de-serializer. Loop-Back mode is used when the SerDes Built-In Self-Test (BIST) is enabled.

SerDes BIST is intended to overlap with the serial EEPROM load operation. To achieve this overlap, the **Physical Layer Test** register *SerDes BIST Enable* bit (Port 0 or 8, offset 228h[7]) is written early in the serial EEPROM load operation. After the *SerDes BIST Enable* bit is set, SerDes is placed in Loop-Back mode and the PRBS generator is started. The BIST is run for 512 µs; if an error is detected on a SerDes, the **Quad *x* SerDes Diagnostic Data** registers (Port 0 or 8, offsets 238h through 244h) log the number of PRBS errors generated for a group of SerDes lanes. While the SerDes BIST is in progress, the PRBS test data is present on the external TxP and TxN balls. The Tx Pad TxN signals must have an AC-coupled, 50-Ohm termination to ground. Reloading of the Serial EEPROM register load has no effect on the SerDes BIST.

Figure 17-1. Internal Loop-Back (Analog near End) Data Path



17.1.3 Analog Loop-Back Master

Analog Loop-Back mode is normally used for Analog Far-End testing; however, the mode can also be used to re-create the previously described BIST by looping back the data with a cable. (Refer to Figure 17-2.)

Looping back with a cable includes the internal bond, external balls, any board trace, and connectors in the test data path. (Refer to Figure 17-3.)

Figure 17-2. Analog Far-End Loop-Back

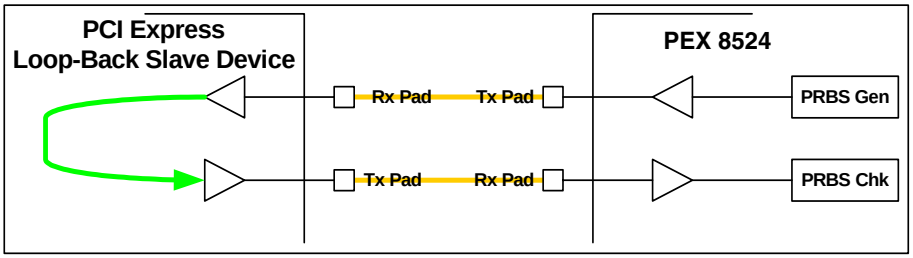
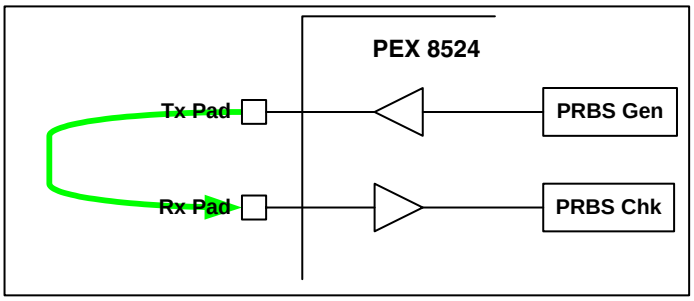


Figure 17-3. Cable Loop-Back



To cause a PEX 8524 port to request to become a Loop-Back Master:

1. After the link is up, set the appropriate **Physical Layer Port Command** register *Port x Loop-Back Command* bit (Port 0 or 8, offset 230h[0, 4, 8, and/or 12]), to cause the port to transition from the L0 state to Recovery, then to the Loop-Back state:
   - If a cable is used for a loop-back, the port transitions from the Configuration state to the Loop-Back state. Connect this cable only after the upstream link is up and Writes are possible.
   - If the cable is connected before the upstream device is able to set the appropriate **Physical Layer Test** register *PRBS External Loop-Back* and *PRBS Enable* bits (Port 0 or 8, offset 228h[23:20 and 19:16], respectively) associated with the SerDes assigned to the port being tested, the link with the cable can reach the L0 state and not go to the Loop-Back state.
   - Cable length is limited only by the PCI Express drivers and cable properties.
2. After the port is in the Loop-Back state, the corresponding **Physical Layer Port Command** register *Port x Ready as Loop-Back Master* status bit (Port 0 or 8, offset 230h[3, 7, 11, and/or 15]) is set:
   - At this time, the PRBS engine can be enabled by setting the **Physical Layer Test** register *PRBS Enable* bit (Port 0 or 8, offset 228h[19:16]) associated with the SerDes assigned to the port being tested.
   - The returned PRBS data is checked by the PRBS checker. Errors are logged in the **Quad *x* SerDes Diagnostic Data** registers (Port 0 or 8, offsets 238h through 244h) that correspond to the SerDes quad being tested.

Note: *The PRBS generator can be difficult to use because SKIP Ordered-Sets are not generated by the PRBS generator, and consequently the PEX 8524 can lose symbol lock unless the Slave device inserts the SKIP Ordered-Sets. However, if the Slave device is enabled to support digital loop-back, it inserts SKIP Ordered-Sets. If the **Phy User Test Pattern x** registers (Port 0 or 8, offsets 210h through 21Ch) are used (rather than PRBS), SKIP Ordered-Sets are automatically generated.*

17.1.4 Digital Loop-Back Master

The only difference between the Analog and Digital Loop-Back Master modes is that the external device is assumed to possess certain digital logic in the Loop-Back data path. Because this includes the elastic buffer, SKIP Ordered-Sets must be included in the test pattern. For the PEX 8524, this precludes PRBS engine use, because the PRBS generator does not generate SKIP Ordered-Sets.

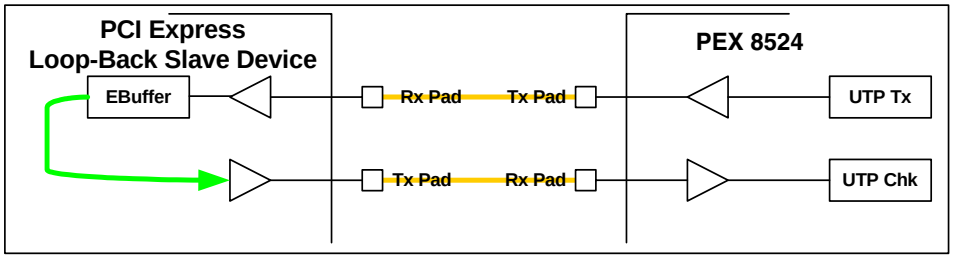
The PEX 8524 provides the programmable **Phy User Test Pattern *x*** (Port 0 or 8, offsets 210h through 21Ch) transmitter for Digital Far-End Loop-Back testing.

*To program the **Phy User Test Pattern x** transmitter:*

1. After Loop-Back Master mode is established, write the test pattern values to the **Phy User Test Pattern *x*** registers (Port 0 or 8, offsets 210h through 21Ch), in Port 0 for the Station 0 SerDes and in Port 8 for the Station 1 SerDes. To start transmitting the test pattern on specific SerDes quads, set the corresponding **Physical Layer Test** register *User Test Pattern Enable* bit(s) (Port 0 or 8, offset 228h[31:28]):
   - If the **Physical Layer Test** register *Port/SerDes Test Pattern Enable Select* bit (Port 0 or 8, offset 228h[5]) is also set, the test pattern is transmitted on all corresponding port lanes, regardless of width.
   - If the *Port/SerDes Test Pattern Enable Select* bit is cleared, the test pattern is transmitted only on the corresponding SerDes quad lanes.
   - The **Phy User Test Pattern *x*** registers can be written to change the test pattern during the test.
2. SKIP Ordered-Sets are inserted at the interval determined by the value in the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Port 0 or 8, offset 234h[11:0]) (default value is 1,180 symbol times) at the nearest data pattern boundary.

   The Test Pattern checker ignores SKIP Ordered-Sets returned by the Loop-Back Slave, because the number of SKIP symbols received differ from the number transmitted.
3. All other data is compared to the data transmitted and errors are logged in the **Quad *x* SerDes Diagnostic Data** registers.

Figure 17-4. Digital Far-End Loop-Back



The following example illustrates the necessary steps for running the Digital Loop-Back Master test, with Port 1 as a x4 port on SerDes[4:7]:

1. Write 0F00_0000h to the **Physical Layer Test** register (Port 0, offset 228h), to clear the **Quad *x* SerDes Diagnostic Data** register *PRBS Error Count* field (Port 0, offsets 238h through 244h[31:24]).
2. To generate a specific test pattern, write the 128-bit value into **Phy User Test Pattern *x*** registers (Port 0, offsets 210h through 21Ch).
3. Write 0000_0010h to the **Physical Layer Port Command** register (Port 0, offset 230h), to enable Digital Loop-Back Master mode on Port 1.
4. Read the **Physical Layer Port Command** register (Port 0, offset 230h), to confirm that Port 1 is in Digital Loop-Back Master mode. The value should be 0000_0090h.
5. Write 2000_0000h to the **Physical Layer Test** register (Port 0, offset 228h), to enable the Test Pattern on SerDes[4:7].
6. Read the **Quad 1 SerDes Diagnostic Data** register *PRBS Error Count* field (Port 0, offset 23Ch[31:24]), to check for errors on SerDes[4:7]. If there are no errors, the field has a value of 00h.
7. Exit Digital Loop-Back Master mode by clearing the **Physical Layer Port Command** register (Port 0, offset 230h), and then the **Physical Layer Test** register (Port 0, offset 228h).

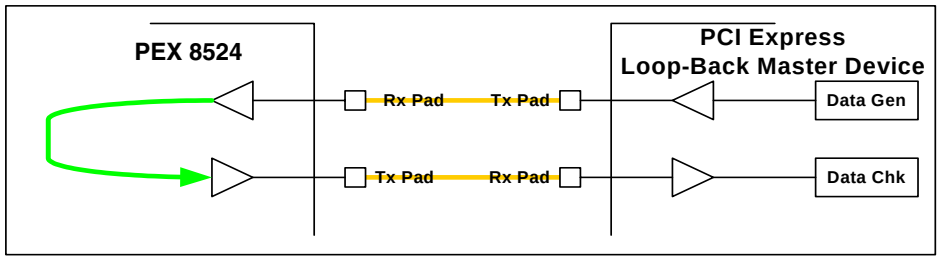
17.1.5 Analog Loop-Back Slave

The PEX 8524 becomes an Analog Loop-Back Slave if the following conditions exist (refer to Figure 17-5):

- At least two consecutive TS1 Ordered-Sets have the *Loopback* bit exclusively set in the TS1 Training Control symbol, and
- **Physical Layer Test** register *Analog Loop-Back Enable* bit (Port 0 or 8, offset 228h[4]) is set

While an Analog Loop-Back Slave, the PEX 8524 includes only the serializer and de-serializer in the Loop-Back data path. The Loop-Back Master must provide the test pattern and data pattern checking. It is unnecessary for the Loop-Back Master to include SKIP Ordered-Sets in the data pattern.

Figure 17-5. Analog Loop-Back Slave Mode



17.1.6 Digital Loop-Back Slave

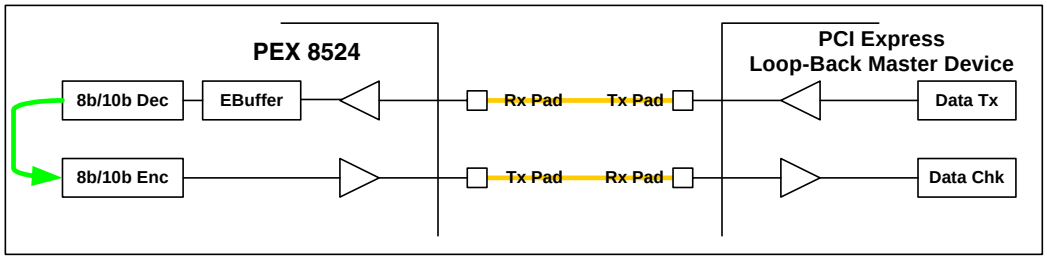
The PEX 8524 becomes a Digital Loop-Back Slave if the following conditions exist (refer to Figure 17-6):

- At least two consecutive TS1 Ordered-Sets have the *Loopback* bit exclusively set in the TS1 Training Control symbol, and
- **Physical Layer Test** register *Analog Loop-Back Enable* bit (Port 0 or 8, offset 228h[4]) is cleared

When a PEX 8524 port is a Digital Loop-Back Slave, it includes the elastic buffer and 8b/10b decoder and encoder in the Loop-Back data path. The Loop-Back Master must provide the test pattern and data pattern checker. Additionally, the Master must transmit valid 8b/10b symbols, for the Loop-Back data from the Slave to be valid.

The Loop-Back Master must also transmit SKIP Ordered-Sets with the data pattern. The data checker must make provisions for the PEX 8524 to return more or fewer SKIP symbols than it received.

Figure 17-6. Digital Loop-Back Slave Mode



17.1.7 Using the Diagnostic Registers

There are two diagnostic registers for Station 0, and four diagnostic registers for Station 1, one for each SerDes quad. Registers at offsets 240h and 244h are ***reserved*** for Station 0. The **Quad *x* SerDes Diagnostic Data** register (Port 0 or 8, offsets 238h through 244h) contents reflect the performance of the SerDes selected by the **Physical Layer Test** register *PRBS Diagnostic Data Select* SerDes Select field (Port 0 or 8, offset 228h[9:8]). *For example*, if the SerDes Select field is set to 10b, the information in the **Quad 0 SerDes Diagnostic Data** register (Port 0 or 8, offset 238h) is for SerDes 2 in quad 0 for Port 0, and SerDes 18 in quad 0 for Port 8. Table 17-1 further illustrates this example.

The *PRBS Diagnostic Data Select* SerDes Select field must be set up before the test is started.

Table 17-1. SerDes Register Contents When *PRBS Diagnostic Data Select* SerDes Select Field = 10b

Port 0 or 8, Register Offset	Register	Port 0	Port 8
238h	**Quad 0 SerDes Diagnostic Data**	SerDes 2	SerDes 18
23Ch	**Quad 1 SerDes Diagnostic Data**	SerDes 6	SerDes 22
240h	**Quad 2 SerDes Diagnostic Data**	–	SerDes 26
244h	**Quad 3 SerDes Diagnostic Data**	–	SerDes 30

17.2 Pseudo-Random and Bit-Pattern Generation

Each SerDes quad has an associated PRBS generator and checker. The PRBS generator is based on a 7-bit Linear Feedback Shift register (LFSR), which can generate up to (2^7 – 1) unique patterns. The PRBS logic is assigned to a SerDes in the quad by manipulating the **Physical Layer Test** register *PRBS Diagnostic Data Select* SerDes Select field (Port 0 or 8, offset 228h[9:8]) in each station. The PRBS bit stream is used for internal SerDes or Analog Far-End Loop-Back testing.

The PEX 8524 also provides a method of creating a repeating programmable bit pattern. Each of the four 32-bit **Phy User Test Pattern *x*** registers (Port 0 or 8, offsets 210h through 21Ch) are loaded with a 32-bit data pattern. After a port is established as a Loop-Back Master, set the **Physical Layer Test** register *User Test Pattern Enable* bit(s) (Port 0 or 8, offset 228h[31:28]) to 1, for the SerDes quad(s) associated with that port. The PEX 8524 proceeds to transmit the data pattern on all lanes, starting with Byte 0 of the **Phy User Test Pattern 0** register, and continuing, in sequence, through Byte 3 of the **Phy User Test Pattern 12** register. SKIP Ordered-Sets are inserted at the proper intervals, which makes this method appropriate for Digital Far-End Loop-Back testing. The received pattern is compared to the transmitted pattern. Any errors are logged and retrieved by reading the **Quad *x* SerDes Diagnostic Data** registers (Port 0 or 8, offsets 238h through 244h).

To produce a pseudo-clock bitstream in Analog Loop-Back mode, set the registers as follows:

1. In the Slave device, enable Analog Loop-Back by setting the **Physical Layer Test** register *Analog Loop-Back Enable* bit (Port 0 or 8, offset 228h[4] in PLX switches).
2. In the PEX 8524 Loop-Back Master device:
   a. Write the value 4A4A_4A4Ah into each of the **Phy User Test Pattern *x*** registers (Port 0 or 8, offsets 210h through 21Ch).
   b. Set the **Physical Layer Port Command** register *Port x Loop-Back Command* bit (Port 0 or 8, offset 230h[0, 4, 8, and/or 12]) for the specific port. To verify whether loop-back is successful, read the corresponding **Physical Layer Port Command** register *Port x Ready as Loop-Back Master* status bit (Port 0 or 8, offset 230h[3, 7, 11, and/or 15]) in the same Nibble that was set in step *a*. The Nibble value will be 9h if loop-back is successful.
   c. Set the **Physical Layer Test** register *User Test Pattern Enable* bit(s) (Port 0 or 8, offset 228h[31:28]) for the particular SerDes quad(s) used by the port selected step *b*, for the the **Physical Layer Port Command** register (Port 0 or 8, offset 230h).
   d. The interval between SKIP Ordered-Sets can be programmed in the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Port 0 or 8, offset 234h[11:0]).

   Note: *A high value for offset 234h[11:0] (such as FFFh) can cause the link to fail.*
3. Exit Analog Loop-Back mode by clearing the **Physical Layer Port Command** register (Port 0 or 8, offset 230h), and then the **Physical Layer Test** register (Port 0 or 8, offset 228h). The link will re-establish itself.

17.3 JTAG Interface

The PEX 8524 provides a JTAG Boundary Scan interface, which is utilized to debug board connectivity for each ball.

17.3.1 *IEEE 1149.1* and *1149.6* Test Access Port

The *IEEE 1149.1* Test Access Port (TAP), commonly called the JTAG (Joint Test Action Group) debug port, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to 1149.1 to support PCI Express SerDes testing. These standards describe methods for accessing internal chip facilities, using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with *IEEE Standard 1149.1-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals** – JTAG debug port implements the four required JTAG signals – JTAG_TCK, JTAG_TDI, JTAG_TDO, and JTAG_TMS – and optional JTAG_TRST# signal
- **Clock Requirements** – JTAG_TCK signal frequency ranges from DC to 10 MHz
- **JTAG Reset Requirements** – Section 17.3.4, "JTAG Reset Input Signal JTAG_TRST#"

17.3.2 JTAG Instructions

The JTAG debug port provides the *IEEE Standard 1149.1-1990* EXTEST, SAMPLE/PRELOAD, BYPASS, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. ***PRIVATE instructions are for PLX use only.*** Invalid instructions behave as BYPASS instructions. Table 17-2 lists the JTAG instructions, along with their input codes.

Table 17-2. JTAG Instructions

Instruction	Input Code	Comments
EXTEST	00000b	*IEEE Standard 1149.1-1990*
IDCODE	00001b	
SAMPLE/PRELOAD	00010b	
BYPASS	11111b	
EXTEST_PULSE	00011b	*IEEE Standard 1149.6-2003*
EXTEST_TRAIN	00100b	
PRIVATE[a]	00101b	
	00110b	
	00111b	
	01000b	
	01001b	
	01010b	
	01011b	
	01100b	
	01101b	
	01110b	
	01111b	

a. ***Warning:*** *Non-PLX use of PRIVATE instructions can cause a component to operate in a hazardous manner.*

Table 17-3 defines the JTAG IDCODE values returned by the PEX 8524V for Silicon Revisions AA, BB, and BC, and PEX 8524 for Silicon Revisions BB and BC.

Table 17-3. JTAG IDCODE Values

Device	Unit of Measure	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
PEX 8524VAA	Bits	0001b	0010_0001_0101_0100b	001_1100_1101b	1
	Hex	1h	2154h	1CDh	1h
	Decimal	1	8532	461	1
PEX 8524VBB	Bits	0100b	0010_0001_0101_0100b	001_1100_1101b	1
	Hex	4h	2154h	1CDh	1h
	Decimal	4	8532	461	1
PEX 8524VBC	Bits	1000b	0010_0001_0101_0100b	001_1100_1101b	1
	Hex	8h	2154h	1CDh	1h
	Decimal	8	8532	461	1
PEX 8524BB	Bits	0100b	0010_0001_0100_1100b	001_1100_1101b	1
	Hex	4h	214Ch	1CDh	1h
	Decimal	4	8524	461	1
PEX 8524BC	Bits	1000b	0010_0001_0100_1100b	001_1100_1101b	1
	Hex	8h	214Ch	1CDh	1h
	Decimal	8	8524	461	1

17.3.3 JTAG Boundary Scan

Scan Description Language (BSDL), IEEE 1149.1-1994, is a supplement to IEEE Standard *1149.1-1990* and *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, allows a rigorous description of testability features in components which comply with the standard. This standard is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical port description, physical ball map, instruction set, and Boundary register description.

The logical port description assigns symbolic names to the chip balls. Each ball includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical ball map correlates the chip logical ports to the physical balls of a specific package. A BSDL description can include several physical ball maps, and maps are provided with a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction register to place the chip in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the chip.

The Boundary register description lists each cell or shift stage of the Boundary register. Each cell contains a unique number, the cell numbered 0 is the closest to the Test Data Out (JTAG_TDO) ball and the cell with the highest number is closest to the Test Data In (JTAG_TDI) ball. Each cell contains additional information, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

17.3.4 JTAG Reset Input Signal JTAG_TRST#

The JTAG_TRST# Input ball is the asynchronous JTAG logic reset. When JTAG_TRST# is set Low, it causes the PEX 8524's JTAG TAP Controller to initialize. In addition, when the JTAG TAP Controller is initialized, it selects the PEX 8524 standard logic path (core-to-I/O). It is recommended to take the following into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, consider one of the following:
  - JTAG_TRST# Input signal to use a Low-to-High transition once during PEX 8524 boot-up, along with the system PEX_PERST# signal
  - Hold the JTAG_TMS ball High while clocking the JTAG_TCK ball five times
- If JTAG functionality is not required, the JTAG_TRST# signal must be directly connected to VSS to hold the JTAG TAP Controller inactive
- If the PEX 8524's JTAG TAP Controller is not intended to be used by the design, it is recommended that a 1.5K-Ohm pull-down resistor be connected to the JTAG_TRST# ball, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation

17.4 Lane Good Status LEDs

The PEX 8524 provides Lane Good outputs, PEX_LANE_GOOD[7:0]# and PEX_LANE_GOOD[31:16]#, that can directly drive external common anode LED modules to provide visual indication of the negotiated link width for each port. Each LED corresponds to one lane.

Software can determine:

- Which lanes have completed Physical Layer linkup, by performing a Memory Read of the **Software-Controlled Lane Status** register *Software-Controlled Lane Status* bits (Port 0, offset 1F4h). Bits [31:16, 7:0] correspond to Lanes [31:16, 7:0], respectively.
- Whether the link for each port has trained, by reading the **VC0 Resource Status** register *VC0 Negotiation Pending* and **VC1 Resource Status** register *VC1 Negotiation Pending* bits (offsets 160h[17] and 16Ch[17], respectively) in each port. If the bit value is 0, the link has completed Flow Control initialization. These registers can be read by either a PCI Express Configuration request or Memory Read.
- The negotiated link width of each port, by reading the **Link Status** register *Negotiated Link Width* field (offset 78h[25:20]) in each port. This register can be read by either a Configuration request or Memory Read.

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Chapter 18 Electrical Specifications

18.1 Introduction

This chapter contains the PEX 8524 power-up/power-down sequencing rules and electrical specifications.

18.2 Power-Up/Power-Down Sequence

For reliable operation, VDD10, VDD10S, and VDD10A should power-up first and power-down last. No specific sequence is required between the VTT_PEX, VDD33, and VDD33A supplies. All supply rails should power-up within 50 ms of one another.

18.3 Absolute Maximum Ratings

Warning: *Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the device at these limits is not recommended.*

Table 18-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
I/O Interface Supply Voltage	VDD33	-0.5 to +4.6	V
PLL Supply Voltage	VDD33A	-0.5 to +4.6	V
Core (Logic) Supply Voltage	VDD10	-0.3 to +1.65	V
SerDes Analog Supply Voltage	VDD10A	-0.3 to +1.65[a]	V
SerDes Digital Supply Voltage	VDD10S	-0.3 to +1.65[a]	V
SerDes Termination Supply Voltage	VTT_PEX	-0.3 to +2.5	V
Input Voltage (3.3V Interface)	V_I	-0.3 to +4.6	V
Operating Ambient Temperature PEX 8524VAA (Commercial) PEX 8524VBB/BC, PEX 8524BB/BC (Industrial)	T_A	 0 to +70 -40 to +85	 °C °C
Storage Temperature	T_{STG}	-55 to +150	°C

a. The SerDes Analog and Digital power supplies should track within 0.01V of one another.

18.4 Power Characteristics

Table 18-2. Operating Condition Power Supply Rails

Symbol	Parameter		Min	Typ	Max	Units
VDD33	I/O Supply	3.3V ±10%	3.0	3.3	3.6	V
VDD33A	PLL Supply	3.3V ±10%	3.0	3.3	3.6	V
VDD10	Digital Core Supply					
	PEX 8524VAA	1.15±3%	1.12	1.15	1.18	V
	PEX 8524VBB/BC, PEX 8524BB/BC	1.0V ±10%	0.9	1.0	1.1	V
VDD10A	Analog SerDes Supply					
	PEX 8524VAA	1.15±3%	1.12	1.15	1.18	V
	PEX 8524VBB/BC, PEX 8524BB/BC	1.0V ±10%	0.9	1.0	1.1	V
VDD10S	Digital SerDes Supply					
	PEX 8524VAA	1.15±3%	1.12	1.15	1.18	V
	PEX 8524VBB/BC, PEX 8524BB/BC	1.0V ±10%	0.9	1.0	1.1	V
VTT_PEX	SerDes Termination Supply Voltage		1.35	1.5	1.8	V

18.5 Power Consumption

Note: *The total power values listed in Table 18-3 are rounded to two digits.*

Table 18-3. PEX 8524VAA Power Dissipation (Watts) {4 to 24 Lanes}

Traffic Conditions	SerDes/Core VDD10		SerDes VTT		VDD33		Total	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max
A. Heavy	5.088	7.891	0.96	1.08	0.092	0.109	6.14	9.08
B. Medium	4.688	7.601	0.96	1.08	0.092	0.109	5.74	8.79
C. Light	4.288	6.891	0.96	1.08	0.092	0.109	5.34	8.08

A. Peer-to-peer traffic, all lanes active, 80 to 90% link utilization.

B. Host-Centric traffic, all lanes active, 50 to 70% link utilization.

C. Host-Centric traffic, 75% lanes active, 50% link utilization.

Typical Condition – Nominal process, room temperature and nominal voltage.
Maximum Condition – Fast/fast process, -40°C temperature and worst voltage.
Maximum Power/SerDes Quad – 325 mW.

Table 18-4. PEX 8524VBB/BC Power Dissipation (Watts) {4 to 24 Lanes}

Traffic Conditions	Core/ SerDes Digital (VDD10)		PCI Express Digital (VDD10S)		PCI Express Analog (VDD10A)		SerDes Termination (VTT_PEX)		PLL (VDD33A)		GPIO (VDD33)		Total	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
A. Heavy	3.42	3.88	1.52	1.72	0.42	0.48	1.04	1.26	0.02	0.03	0.02	0.03	**6.44**	**7.40**
B. Medium	3.15	3.57	1.28	1.45	0.36	0.40	0.88	1.06	0.02	0.03	0.02	0.03	**5.71**	**6.54**
C. Light	2.56	2.9.	1.28	1.45	0.36	0.40	0.88	1.06	0.02	0.03	0.02	0.03	**5.12**	**5.87**

A. 85% lane bandwidth utilization. All 24 lanes in L0 active state.

B. 35% lane bandwidth utilization. All 24 lanes in L0 active state.

C. 10% lane bandwidth utilization. All 24 lanes in L0 active state.

Typ Condition – Typical silicon process, 25°C, nominal supply voltage.
Max Condition – Fast silicon process, 0°C, +10% supply voltage.

Table 18-5. PEX 8524BB/BC Power Dissipation (Watts) {4 to 24 Lanes}

Traffic Conditions	Core/ SerDes Digital (VDD10)		PCI Express Digital (VDD10S)		PCI Express Analog (VDD10A)		SerDes Termination (VTT_PEX)		PLL (VDD33A)		GPIO (VDD33)		Total	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
A. Heavy	3.03	3.43	1.14	1.29	0.32	0.36	0.78	0.95	0.02	0.03	0.02	0.03	**5.31**	**6.09**
B. Medium	1.99	2.26	0.958	1.09	0.27	0.30	0.66	0.79	0.02	0.03	0.02	0.03	**3.92**	**4.50**
C. Light	1.44	1.63	0.958	1.09	0.27	0.30	0.66	0.79	0.02	0.03	0.02	0.03	**3.37**	**3.87**

A. 85% lane bandwidth utilization. All 24 lanes in L0 active state.

B. 35% lane bandwidth utilization. All 24 lanes in L0 active state.

C. 10% lane bandwidth utilization. All 24 lanes in L0 active state.

Typ Condition – Typical silicon process, 25°C, nominal supply voltage.
Max Condition – Fast silicon process, 0°C, +10% supply voltage.

18.6 I/O Interface Signal Groupings

Table 18-6. Signal Group PCI Express Analog Interface

Signal Group	Signal Type	Signals	Notes
(a)	PCI Express Output (Transmit)	PEX_PETn[31:16, 7:0], PEX_PETp[31:16, 7:0],	Refer to Table 18-9
(b)	PCI Express Input (Receive)	PEX_PERn[31:16, 7:0], PEX_PERp[31:16, 7:0],	Refer to Table 18-10
(c)	PCI Express Differential Clock Input	PEX_REFCLKn, PEX_REFCLKp	Refer to Table 18-11

Table 18-7. Signal Group Digital Interface

Signal Group	Signal Type	Signals	Notes
(d)	Digital Output	EE_CS#, EE_DI, EE_SK, HP_ATNLED[11:8, 1:0]#, HP_CLKEN[11:8, 1:0]#, HP_PERST[11:8, 1:0]#, HP_PWREN[11:8, 1:0]#, HP_PWRLED[11:8, 1:0]#, JTAG_TDO, PEX_LANE_GOOD[31:16, 7:0]#, PEX_NT_RESET#	Refer to Table 18-8
(e)	Digital Input[a]	EE_PR#, PEX_PERST#, STRAP_FACTORY_TEST1#, STRAP_MODE_SEL[1:0], STRAP_NT_UPSTRM_PORTSEL[3:0], STRAP_STN0_PORTCFG[4:0], STRAP_STN1_PORTCFG[3:0], STRAP_TESTMODE[3:0], STRAP_UPSTRM_PORTSEL[3:0]	
(f)	Digital Input with Internal Pull-up Resistor	EE_DO, HP_BUTTON[11:8, 1:0]#, HP_MRL[11:8, 1:0]#, HP_PRSNT[11:8, 1:0]#, HP_PWRFLT[11:8, 1:0]#, JTAG_TCK, JTAG_TDI, JTAG_TMS, JTAG_TRST#	

a. STRAP_ signals must be tied High to VDD33 or Low to VSS (GND),

Table 18-8. DC Electrical Characteristics – Digital Interface

Symbol	Signal Group	Parameter	Min	Typ	Max	Unit	Conditions
I_{OL}	(d)	Output Low Current	8			mA	V_{OL} = 0.4V
I_{OH}	(d)	Output High Current	8			mA	V_{OH} = 1.5V
V_{IL}	(e) (f)	Input Low Voltage			0.8	V	
V_{IH}	(e) (f)	Input High Voltage	2.0			V	
C_{PIN}	(a)	Ball Capacitance			***TBD***	pF	
	(b)	Ball Capacitance			***TBD***	pF	
	(c)	Ball Capacitance			5	pF	
	(d)	Ball Capacitance			6	pF	
	(e) (f)	Ball Capacitance			5	pF	
$I_{LEAKAGE}$	(d)	Three-state Leakage			±500	nA	
	(e)	Input Leakage			±50	nA	
	(f)	Pull-Up Leakage	+0.1/-8		+0.1/-20	µA	
R_{PU}	(f)	Pull-Up Impedance	200K			Ohm	

Table 18-9. PCI Express Transmit (Signal Group a) AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800		1.2	V	$V_{TX-DIFFp-p} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the 2nd and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the 1st bit after a transition. Refer to Note 1.
T_{TX-EYE}	Minimum Tx Eye Width	0.75			UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI This parameter is measured with the equivalent of a zero-jitter Reference Clock. Refer to Notes 1 and 2.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the Jitter Median and Maximum Deviation from the Median			0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFF}$ = 0V) in relation to recovered Tx UI. Refer to Notes 1 and 2.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- Tx Output Rise/Fall Time	0.125			UI	Refer to Notes 1 and 4.
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp} = RMS(\lvert V_{TX-D+} + V_{TX-D-} \rvert/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-} \rvert/2$ Refer to Note 1.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	0		100	mV	$\lvert V_{TX-CM-DC}$ [during L0] $- V_{TX-CM-Idle-DC}$ [during Electrical Idle]$\rvert \leq 100$mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-} \rvert/2$ [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-} \rvert/2$ [Electrical Idle] Refer to Note 1.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0		25	mV	$\lvert V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \rvert \leq 25$mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\lvert V_{TX-D+} \rvert$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\lvert V_{TX-D-} \rvert$ Refer to Note 1.
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp} = \lvert V_{TX-Idle-D+} - V_{TX-Idle-D-} \rvert \leq 20$mV Refer to Note 1.
$V_{TX-RCV-DETECT}$	Amount of Voltage Change Allowed during Receiver Detection			600	mV	The total amount of voltage change that a Transmitter can apply to sense whether a low-impedance Receiver is present.
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0		3.6	V	The allowed DC Common Mode voltage under any condition.

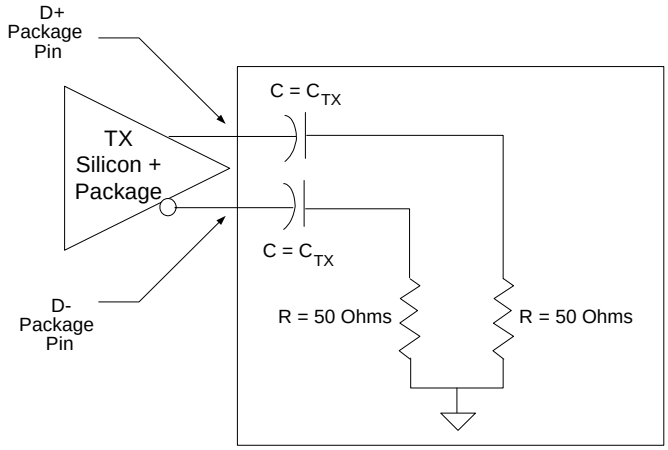
Table 18-9. PCI Express Transmit (Signal Group a) AC and DC Characteristics *(Cont.)*

Symbol	Parameter	Min	Typ	Max	Units	Comments
$I_{TX-SHORT}$	Tx Short Circuit Current Limit			90	mA	The total current the Transmitter can provide when shorted to its ground.
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle. Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle Ordered-Set.
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered-Set			20	UI	After sending an Electrical Idle Ordered-Set, the Transmitter must meet all Electrical Idle specifications within this time. A de-bounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$RL_{TX-DIFF}$	Differential Return Loss	10			dB	Measured over 50 MHz to 1.25 GHz.
RL_{TX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz.
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ohm	Tx DC Differential mode low impedance. Refer to Note 5.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500 + 2 UI	ps	Static skew between any two Transmitter lanes within a single link.

Notes:

1. *Specified at the measurement point into a timing and voltage compliance test load, as illustrated in Figure 18-1.*

Figure 18-1. Compliance Test/Measurement Load



2. *At T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the Transmitter. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half the total Tx jitter budget. (**Note:** The median is not the same as the mean.) The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. This parameter is measured with the equivalent of a zero-jitter Reference Clock. The T_{TX-EYE} measurement is to be met at the target bit error rate. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification is to be met using the compliance pattern at a sample size of 1,000,000 UI.*

3. *The Transmitter input impedance shall result in a differential return loss, greater than or equal to 10 dB, with a Differential Test Input signal no less than 200 mV (peak value, 400 mV differential peak-to-peak) swing around ground, applied to D+ and D- lines and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ohms to ground for both the D+ and D- lines. The series capacitance C_{TX} is optional for the return loss measurement.*

4. *Measured between 20 to 80% at Transmitter package balls into a test load, as illustrated in Figure 18-1, both V_{TX-D+} and V_{TX-D-}.*

5. *$Z_{TX-DIFF-DC}$ is the small signal resistance of the transmitter measured at a DC operating point that is equivalent to that established by connecting a 100 Ohm resistor from D+ and D- while the Tx is driving a static logic 1 or logic 0. Equivalently, this parameter can be derived by measuring the RMS voltage of the Tx while transmitting a test pattern into two different differential terminations that are near 100 Ohms.*

   Small signal resistance is measured by forcing a small change in differential voltage and dividing this by the corresponding change in current.

Table 18-10. PCI Express Receive (Signal Group b) AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	The UI is 400 ps ±300 ppm.
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as: $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6\ UI$ Refer to Notes 6, 7, and 8.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFF}$ = 0V) in relation to recovered Tx UI. Refer to Notes 6 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-ACp} = \|V_{RX-D+} + V_{RX-D-}\| /2 - V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}\ of\ \|V_{RX-D+}\|$ Refer to Note 6.
$RL_{RX-DIFF}$	Differential Return Loss	10			dB	Measured over 50 MHz to 1.25 GHz. Refer to Note 9.
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz. Refer to Note 9.
$Z_{RX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ohm	Rx DC Differential mode impedance.
Z_{RX-DC}	DC Input Impedance	40	50	60	Ohm	Required Rx D+ and D- DC impedance (50 Ohms ±20% tolerance). Refer to Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} + V_{RX-D-}\|$ Measured at the package balls of the Receiver.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Idle Detect Threshold Integration Time			10	ms	An un-expected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Skew			20	ns	Skew across all lanes in a link.

Notes:

6. *The test load in Figure 18-1 should be used as the Rx device when taking measurements.*
7. *The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half the total, 0.64. (**Note:** The median is not the same as the mean.) The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. The $T_{RX\text{-}EYE}$ measurement is to be met at the target bit error rate. The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification is to be met using the compliance pattern at the sample size of 1,000,000 UI.*
8. *Refer to the PCI Express Jitter and BER White Paper for details regarding the Rx-Eye measurement.*
9. *The Receiver input impedance shall result in a differential return loss, greater than or equal to 10 dB, with a Differential Test Input signal of no less than 200 mV (peak value, 400 mV differential peak-to-peak) swing around ground, applied to D+ and D- lines and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ohms to ground for both the D+ and D- lines. The series capacitance C_{TX} is optional for the return loss measurement.*

Table 18-11. PCI Express Differential Clock (Signal Group c) AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{REFCLK}	Reference Clock Frequency		100		MHz	
V_{CM}	Input Common Mode Voltage	0.6	0.65	0.7	V	1
V_{SW}	Differential Voltage Swing (0-to-peak)	125		800	mV	
	Differential Voltage Swing (peak-to-peak)	250		1,600	mV	
T_R/T_F	Clock Input Rise/Fall Time			1.5	ns	2
DC_{REFCLK}	Input Clock Duty Cycle	40	50	60	%	
R_{TERM}	Input Parallel Termination (Single-ended)		55		Ohm	
	Input Parallel Termination (Differential)		110		Ohm	
PPM	Reference Clock Tolerance	-300		+300	ppm	

Notes:

1. *PEX_REFCLKn/p must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.*
2. *Specified at 20 to 80% points at the package balls.*

18.7 Transmit Drive Characteristics

The drive current and the transmit equalization function is programmable, to allow for optimization of different backplane lengths and materials.

18.7.1 Drive Current

The nominal drive current is programmable (2-bit) within the range of 10 to 28 mA. [Refer to the **SerDes Nominal Drive Current Select** register (offset 248h) for details.]

The nominal drive current can be further programmed (4-bit) with finer granularity, within the range of 0.65X to 1.35X. [Refer to the **SerDes Drive Current Level Select 1** and **SerDes Drive Current Level Select 2** registers (offsets 24Ch and 250h, respectively) for details.]

18.7.2 Transmit Equalization

The Transmitter incorporates programmable (4-bit) first-order equalization, within the range of 0 to -7.96 dB. [Refer to the **SerDes Drive Equalization Level Select 1** and **SerDes Drive Equalization Level Select 2** registers (offsets 254h and 258h, respectively) for details.]

18.7.3 Transmit Termination Adjust

The *PCI Express Base r1.0a* specifies termination (50 Ohms nominal) at the Transmit side to VTT. The Transmit driver incorporates a 2-bit register (per SerDes quad), which allows for a ±20% termination adjustment to mitigate stub effects and other non-idealities in the PCB channel. Refer to the **Physical Layer** register *SerDes Quad x TxTermAdjust* fields (offset 22Ch[15:8]) for details.

18.8 Receive Characteristics

The following programmable bits control the electrical characteristics of the Receiver circuit, to mitigate the effects of signal loss and distortion across the PCB channel.

18.8.1 Receive Equalization

The Receiver incorporates a programmable 2-bit register (per SerDes quad) to modify the high-pass filter within the circuit, which serves to mitigate the effects of Inter Symbol Interference due to frequency-dependent losses across the PCB material. Refer to **Physical Layer** register *SerDes Quad x RxEqCtl* fields (offset 22Ch[31:24]) for details.

18.8.2 Receive Termination Adjust

The *PCI Express Base r1.0a* specifies termination (50 Ohms nominal) at the Receive side to ground. The Receiver input incorporates a 2-bit register (per SerDes quad), which allows for a ±20% termination adjustment to mitigate stub effects and other non-idealities in the PCB channel. Refer to the **Physical Layer** register *SerDes Quad x RxTermAdjust* fields (offset 22Ch[23:16]) for details.

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Chapter 19 Mechanical Specifications

19.1 PEX 8524 Package Specifications

The PEX 8524VAA/BB/BC is offered in a 35-mm square, 680-ball PBGA (Plastic BGA) package. Table 19-1 defines the package specifications.

The PEX 8524BB/BC is offered in a 31-mm square, 644-ball PBGA (Plastic BGA) package. Table 19-2 defines the package specifications.

Unpopulated BGA balls allow board design and placement of board-level de-coupling capacitors between VDD33, VDD10, VDD10A, VDD10S, and VSS/Ground.

Table 19-1. PEX 8524VAA/BB/BC Package Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array (PBGA)
Number of Balls	680
Package Dimensions	35 x 35 mm (approximately 2.23 mm high)
Ball matrix pattern	34 x 34 mm (10 x 10 center area reserved for Ground)
Ball pitch	1.00 mm
Ball diameter	0.60 ±0.15 mm
Ball spacing	0.40 mm

Table 19-2. PEX 8524BB/BC Package Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array (PBGA)
Number of Balls	644
Package Dimensions	31 x 31 mm (approximately 2.42 mm high)
Ball matrix pattern	30 x 30 mm (10 x 10 center area reserved for Ground)
Ball pitch	1.00 mm
Ball diameter	0.61 mm
Ball spacing	0.40 mm

19.2 PEX 8524 Mechanical Dimensions

Figure 19-1. PEX 8524VAA/BB/BC 680-Ball PBGA Mechanical Dimensions

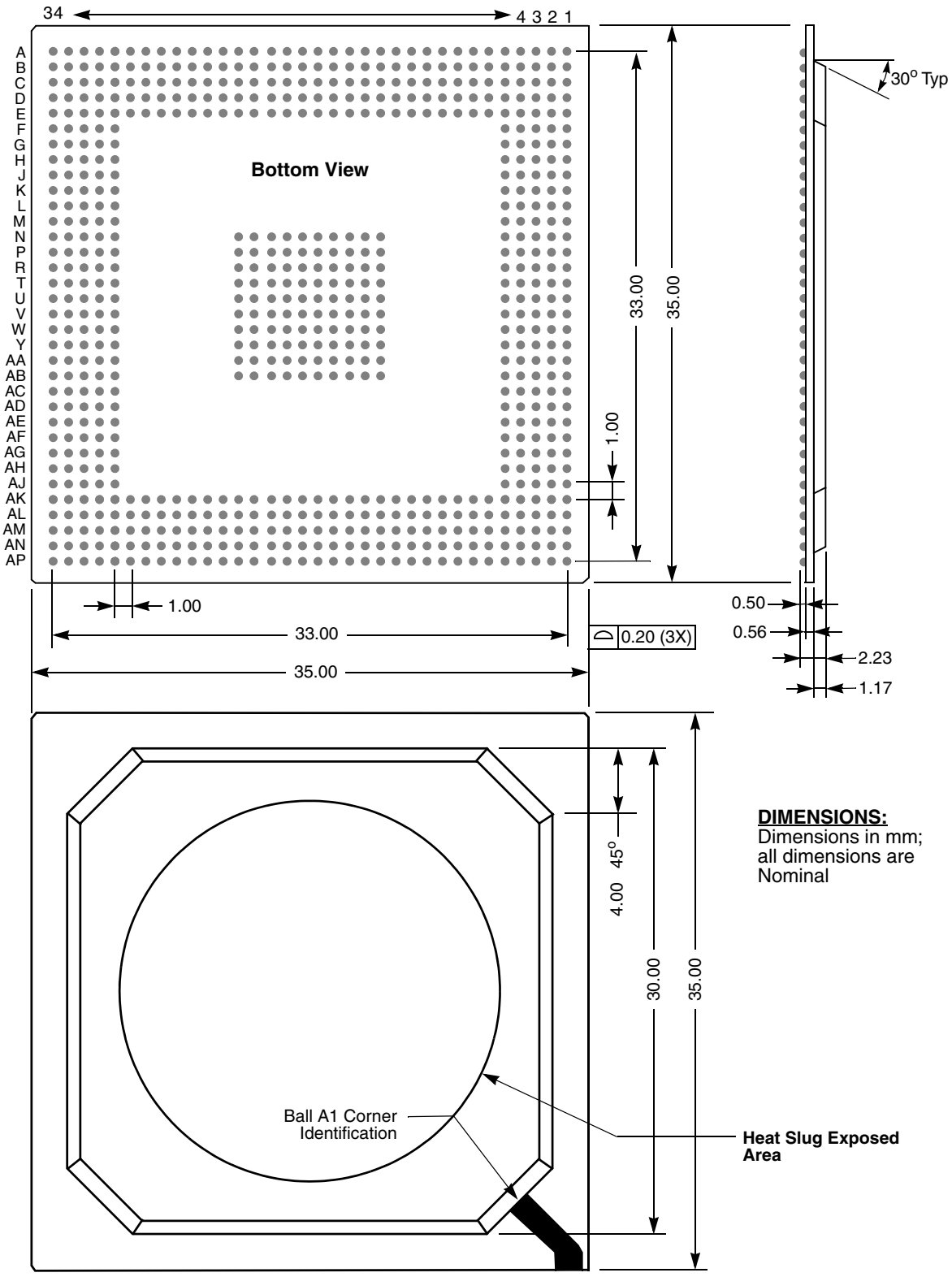
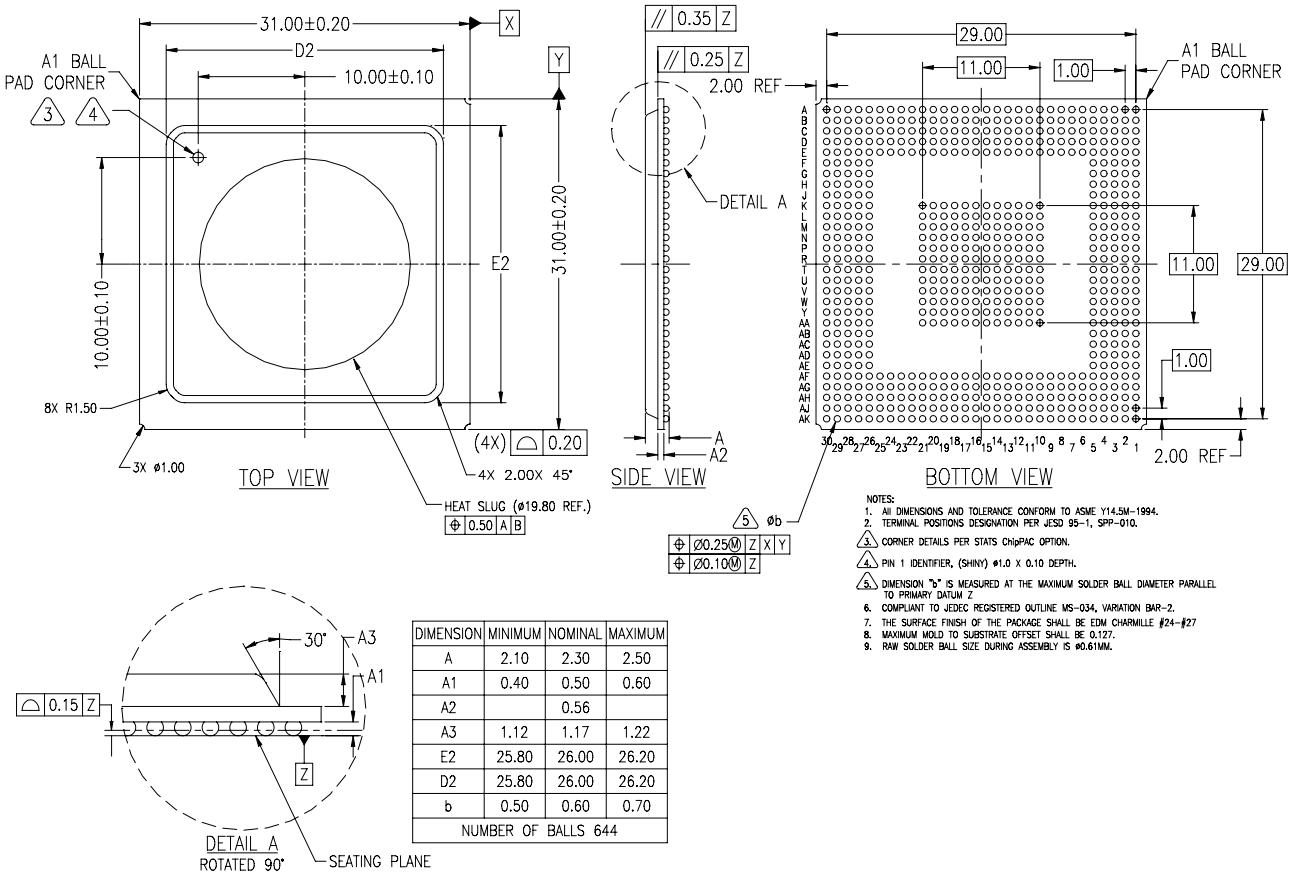


Figure 19-2. PEX 8524BB/BC 644-Ball PBGA Mechanical Dimensions



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.10	2.30	2.50
A1	0.40	0.50	0.60
A2		0.56	
A3	1.12	1.17	1.22
E2	25.80	26.00	26.20
D2	25.80	26.00	26.20
b	0.50	0.60	0.70
NUMBER OF BALLS 644			

19.3 Thermal Characteristics

Neither the PEX 8524V nor PEX 8524 includes a heat sink. The information described in this section is based on sample thermal performance when a heat sink is used with the PEX 8524V or PEX 8524, and is provided for reference only.

Table 19-3. Sample PEX 8524VAA Heat Sink and Airflow Requirements*

Traffic	Commercial	Commercial
	Heat Sink	Airflow
Light	Yes	2 m/s
Medium		
High		

Table 19-4. Sample PEX 8524VBB/BC and PEX 8524BB/BC Heat Sink and Airflow Requirements*

Traffic	Commercial		Industrial	
	Heat Sink	Airflow	Heat Sink	Airflow
Light	Yes	1 m/s	Yes	2 m/s
Medium				
High				

* Legend for Table 19-3 and Table 19-4:

Light Traffic	Host-Centric traffic, 75% lanes active, 50% link utilization
Medium Traffic	Host-Centric traffic, all lanes active, 50 to 70% link utilization
Heavy Traffic	Peer-to-peer traffic, all lanes active, 80 to 90% link utilization
Typical	Nominal process, room temperature and nominal voltage
Maximum	Fast/fast process, -40°C temperature and worst voltage
Maximum Power/SerDes Quad	325 mW

Table 19-5 defines the package thermal resistance, in **°C/W** ($\Theta_{j\text{-}a}$).

Table 19-5. Sample PEX 8524V and PEX 8524 Package Thermal Resistance

Device	Air Flow	No Heat Sink	Heat Sink
PEX 8524V	0 m/s	–	8.0
	1 m/s		6.5
	2 m/s		5.3
PEX 8524	0 m/s	–	11.1
	1 m/s		6.4
	2 m/s		5.5

Figure 19-3. Sample PEX 8524V Copper Fin Heat Sink (38 x 38 x 12.7 mm)

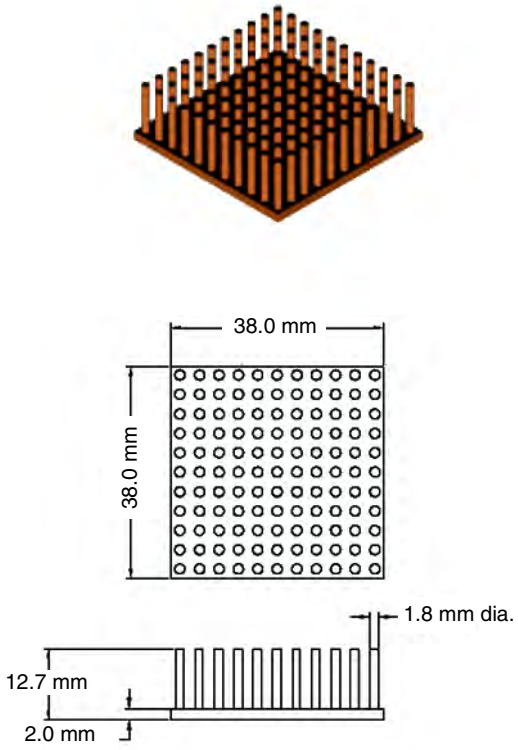
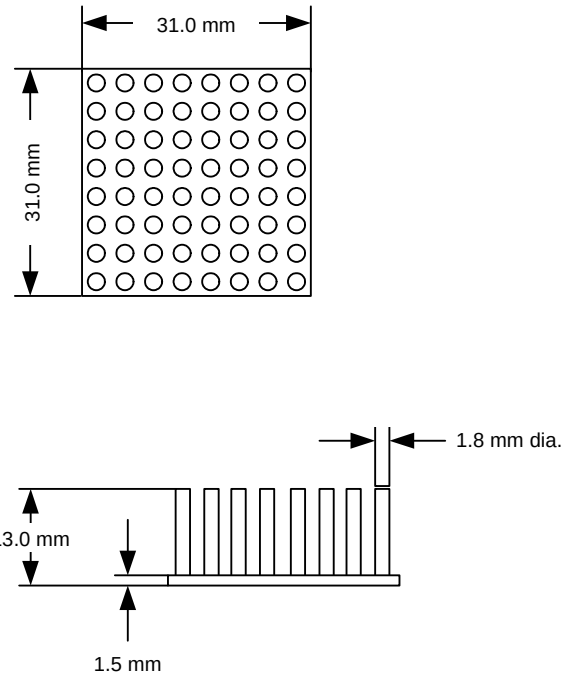


Figure 19-4. Sample PEX 8524 Copper Fin Heat Sink (31 x 31 x 13 mm)



Note: *The 3-D heat sink illustration for the PEX 8524 will be included in a future data book update.*

Appendix A Serial EEPROM Memory Map

A.1 Serial EEPROM Memory Map

In Table A-1, all register offsets are Byte addresses, and all serial EEPROM addresses are DWord addresses (Byte addresses shifted right 2 bits). The serial EEPROM DWord addresses are used directly for the **Serial EEPROM Control** register *Serial EEPROM Block Address* field (Port 0, offset 260h[12:0]).

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
000h	Product Identification	000h	31Ah	4B8h	7D2h	85Ch	8E6h	970h	A68h
004h	Command/Status	001h	31Bh	4B9h	7D3h	85Dh	8E7h	971h	A69h
008h	Class Code and Revision ID	002h	31Ch	4BAh	7D4h	85Eh	8E8h	972h	A6Ah
00Ch	Miscellaneous Control	003h	31Dh	4BBh	7D5h	85Fh	8E9h	973h	A6Bh
010h	Base Address 0	004h	31Eh	4BCh	7D6h	860h	8EAh	974h	A6Ch
014h	Base Address 1	005h	31Fh	4BDh	7D7h	861h	8EBh	975h	A6Dh
018h	Bus Number	006h	320h	4BEh	7D8h	862h	8ECh	976h	A6Eh
01Ch	Secondary Status, I/O Limit, and I/O Base	007h	321h	4BFh	7D9h	863h	8EDh	977h	A6Fh
020h	Memory Base and Limit Address	008h	322h	4C0h	7DAh	864h	8EEh	978h	A70h
024h	Prefetchable Memory Base and Limit Address	009h	323h	4C1h	7DBh	865h	8EFh	979h	A71h
028h	Prefetchable Memory Upper Base Address[63:32]	00Ah	324h	4C2h	7DCh	866h	8F0h	97Ah	A72h
02Ch	Prefetchable Memory Upper Limit Address[63:32]	00Bh	325h	4C3h	7DDh	867h	8F1h	97Bh	A73h
030h	I/O Base Address[31:16] and I/O Limit Address[31:16] (Transparent mode) Expansion ROM Base Address (NT Link Port) ***Reserved*** (NT Virtual Ports)	00Ch	326h	4C4h	7DEh	868h	8F2h	97Ch	A74h
034h	Capabilities Pointer	00Dh	327h	4C5h	7DFh	869h	8F3h	97Dh	A75h
038h	Expansion ROM Base Address	00Eh	328h	4C6h	7E0h	86Ah	8F4h	97Eh	A76h
03Ch	Bridge Control and Interrupt Signal	00Fh	329h	4C7h	7E1h	86Bh	8F5h	97Fh	A77h

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
040h	Power Management Capability	010h	32Ah	4C8h	7E2h	86Ch	8F6h	980h	A78h
044h	Power Management Status and Control	011h	32Bh	4C9h	7E3h	86Dh	8F7h	981h	A79h
	PM Data[31:24] and *Data Scale*[14:13], for *Data Select*[12:9] = 0h	B7Ch	B89h	BB0h	BBDh	BCAh	BD7h	B62h	B6Fh
	PM Data[31:24] and *Data Scale*[14:13], for *Data Select*[12:9] = 3h	B7Dh	B8Ah	BB1h	BBEh	BCBh	BD8h	B63h	B70h
	PM Data[31:24] and *Data Scale*[14:13], for *Data Select*[12:9] = 4h	B7Eh	B8Bh	BB2h	BBFh	BCCh	BD9h	B64h	B71h
	PM Data[31:24] and *Data Scale*[14:13], for *Data Select*[12:9] = 7h	B7Fh	B8Ch	BB3h	BC0h	BCDh	BDAh	B65h	B72h
048h	Message Signaled Interrupt Capability	012h	32Ch	4CAh	7E4h	86Eh	8F8h	982h	A7Ah
04Ch	Message Address[31:0]	013h	32Dh	4CBh	7E5h	86Fh	8F9h	983h	A7Bh
050h	Message Upper Address[63:32]	014h	32Eh	4CCh	7E6h	870h	8FAh	984h	A7Ch
054h	Message Data	015h	32Fh	4CDh	7E7h	871h	8FBh	985h	A7Dh
058h	***Reserved***	016h	330h	4CEh	7E8h	872h	8FCh	986h	A7Eh
05Ch	***Reserved***	017h	331h	4CFh	7E9h	873h	8FDh	987h	A7Fh
060h	***Reserved***	018h	332h	4D0h	7EAh	874h	8FEh	988h	A80h
064h	***Reserved***	019h	333h	4D1h	7EBh	875h	8FFh	989h	A81h
068h	PCI Express Capability List and Capabilities	01Ah	334h	4D2h	7ECh	876h	900h	98Ah	A82h
06Ch	Device Capabilities	01Bh	335h	4D3h	7EDh	877h	901h	98Bh	A83h
070h	Device Status and Control	01Ch	336h	4D4h	7EEh	878h	902h	98Ch	A84h
074h	Link Capabilities	01Dh	337h	4D5h	7EFh	879h	903h	98Dh	A85h
078h	Link Status and Control	01Eh	338h	4D6h	7F0h	87Ah	904h	98Eh	A86h
07Ch	Slot Capabilities	01Fh	339h	4D7h	7F1h	87Bh	905h	98Fh	A87h
080h	Slot Status and Control	020h	33Ah	4D8h	7F2h	87Ch	906h	990h	A88h
084h	***Reserved***	021h	33Bh	4D9h	7F3h	87Dh	907h	991h	A89h
088h	***Reserved***	022h	33Ch	4DAh	7F4h	87Eh	908h	992h	A8Ah
08Ch	***Reserved***	023h	33Dh	4DBh	7F5h	87Fh	909h	993h	A8Bh
090h	Set Virtual Interface IRQ (NT Virtual/Link Ports only)	–	–	–	–	–	–	994h	A8Ch
094h	Clear Virtual Interface IRQ (NT Virtual/Link Ports only)	–	–	–	–	–	–	995h	A8Dh
098h	Set Virtual Interface IRQ Mask (NT Virtual/Link Ports only)	–	–	–	–	–	–	996h	A8Eh
09Ch	Clear Virtual Interface IRQ Mask (NT Virtual/Link Ports only)	–	–	–	–	–	–	997h	A8Fh

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
0A0h	Set Link Interface IRQ (NT Virtual/Link Ports only)	–	–	–	–	–	–	998h	A90h
0A4h	Clear Link Interface IRQ (NT Virtual/Link Ports only)	–	–	–	–	–	–	999h	A91h
0A8h	Set Link Interface IRQ Mask (NT Virtual/Link Ports only)	–	–	–	–	–	–	99Ah	A92h
0ACh	Clear Link Interface IRQ Mask (NT Virtual/Link Ports only)	–	–	–	–	–	–	99Bh	A93h
0B0h	NT Port Scratchpad_0 (NT Virtual/Link Ports only)	–	–	–	–	–	–	99Ch	A94h
0B4h	NT Port Scratchpad_1 (NT Virtual/Link Ports only)	–	–	–	–	–	–	99Dh	A95h
0B8h	NT Port Scratchpad_2 (NT Virtual/Link Ports only)	–	–	–	–	–	–	99Eh	A96h
0BCh	NT Port Scratchpad_3 (NT Virtual/Link Ports only)	–	–	–	–	–	–	99Fh	A97h
0C0h	NT Port Scratchpad_4 (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A0h	A98h
0C4h	NT Port Scratchpad_5 (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A1h	A99h
0C8h	NT Port Scratchpad_6 (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A2h	A9Ah
0CCh	NT Port Scratchpad_7 (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A3h	A9Bh
0D0h	NT Port Virtual Interface BAR1 Setup (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A4h	A9Ch
0D4h	NT Port Virtual Interface BAR2 Setup (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A5h	A9Dh
0D8h	NT Port Virtual Interface BAR3 Setup (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A6h	A9Eh
0DCh	NT Port Virtual Interface BAR4/5 Setup (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A7h	A9Fh
0E0h	NT Port Virtual Interface BAR5 Setup (NT Virtual/Link Ports only)	–	–	–	–	–	–	9A8h	AA0h
0E4h	***Reserved***	039h	353h	4F1h	80Bh	895h	91Fh	9A9h	AA1h
0E8h	***Reserved***	03Ah	354h	4F2h	80Ch	896h	920h	9AAh	AA2h
0ECh	***Reserved***	03Bh	355h	4F3h	80Dh	897h	921h	9ABh	AA3h
0F0h	***Reserved***	03Ch	356h	4F4h	80Eh	898h	922h	9ACh	AA4h
0F4h	***Reserved***	03Dh	357h	4F5h	80Fh	899h	923h	9ADh	AA5h
0F8h	Configuration Address Window (NT Virtual/Link Ports only)	–	–	–	–	–	–	9AEh	AA6h
0FCh	Configuration Data Window (NT Virtual/Link Ports only)	–	–	–	–	–	–	9AFh	AA7h
100h	Device Serial Number Extended Capability	040h	35Ah	4F8h	812h	89Ch	926h	9B0h	AA8h
104h	Serial Number (Lower DW)	041h	35Bh	4F9h	813h	89Dh	927h	9B1h	AA9h
108h	Serial Number (Higher DW)	042h	35Ch	4FAh	814h	89Eh	928h	9B2h	AAAh
138h	Power Budgeting Extended Capability	04Eh	368h	506h	820h	8AAh	934h	9BEh	AB6h
13Ch	Data Select	04Fh	369h	507h	821h	8ABh	935h	9BFh	AB7h

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
140h	Power Budgeting Data (next row overwrites this row)	050h	36Ah	508h	822h	8ACh	936h	9C0h	AB8h
	Power Budgeting Data, Data Select (offset 13Ch) = 00h	B81h	B8Eh	BB5h	BC2h	BCFh	BDCh	B67h	B74h
	Power Budgeting Data, Data Select (offset 13Ch) = 01h	B82h	B8Fh	BB6h	BC3h	BD0h	BDDh	B68h	B75h
	Power Budgeting Data, Data Select (offset 13Ch) = 02h	B83h	B90h	BB7h	BC4h	BD1h	BDEh	B69h	B76h
	Power Budgeting Data, Data Select (offset 13Ch) = 03h	B84h	B91h	BB8h	BC5h	BD2h	BDFh	B6Ah	B77h
	Power Budgeting Data, Data Select (offset 13Ch) = 04h	B85h	B92h	BB9h	BC6h	BD3h	BE0h	B6Bh	B78h
	Power Budgeting Data, Data Select (offset 13Ch) = 05h	B86h	B93h	BBAh	BC7h	BD4h	BE1h	B6Ch	B79h
	Power Budgeting Data, Data Select (offset 13Ch) = 06h	B87h	B94h	BBBh	BC8h	BD5h	BE2h	B6Dh	B7Ah
	Power Budgeting Data, Data Select (offset 13Ch) = 07h	B88h	B95h	BBCh	BC9h	BD6h	BE3h	B6Eh	B7Bh
144h	Power Budget Capability	051h	36Bh	509h	823h	8ADh	937h	9C1h	AB9h
148h	Virtual Channel Extended Capability	052h	36Ch	50Ah	824h	8AEh	938h	9C2h	ABAh
14Ch	Port VC Capability 1	053h	36Dh	50Bh	825h	8AFh	939h	9C3h	ABBh
150h	Port VC Capability 2	054h	36Eh	50Ch	826h	8B0h	93Ah	9C4h	ABCh
154h	Port VC Status and Control (next row overwrites this row)	055h	36Fh	50Dh	827h	8B1h	93Bh	9C5h	ABDh
	Port VC Status and Control (must load after VC Arbitration Table (offsets 1B8h to 1C4h)	B80h	B8Dh	BB4h	BC1h	BCEh	BDBh	B66h	B73h
158h	VC0 Resource Capability	056h	370h	50Eh	828h	8B2h	93Ch	9C6h	ABEh
15Ch	VC0 Resource Control	057h	371h	50Fh	829h	8B3h	93Dh	9C7h	ABFh
160h	VC0 Resource Status	058h	372h	510h	82Ah	8B4h	93Eh	9C8h	AC0h
164h	VC1 Resource Capability	059h	373h	511h	82Bh	8B5h	93Fh	9C9h	AC1h
168h	VC1 Resource Control	05Ah	374h	512h	82Ch	8B6h	940h	9CAh	AC2h
16Ch	VC1 Resource Status	05Bh	375h	513h	82Dh	8B7h	941h	9CBh	AC3h
1B8h	VC Arbitration Table Phase 7-0	06Eh	388h	526h	840h	8CAh	954h	9DEh	AD6h
1BCh	VC Arbitration Table Phase 15-8	06Fh	389h	527h	841h	8CBh	955h	9DFh	AD7h
1C0h	VC Arbitration Table Phase 23-16	070h	38Ah	528h	842h	8CCh	956h	9E0h	AD8h
1C4h	VC Arbitration Table Phase 31-24	071h	38Bh	529h	843h	8CDh	957h	9E1h	AD9h
1C8h	ECC Check Disable	072h	38Ch	52Ah	844h	8CEh	958h	9E2h	ADAh
1CCh	Error Handler 32-Bit Error Status ***(Factory Test Only)***	073h	38Dh	52Bh	845h	8CFh	959h	9E3h	ADBh
1D0h	Error Handler 32-Bit Error Mask ***(Factory Test Only)***	074h	38Eh	52Ch	846h	8D0h	95Ah	9E4h	ADCh
1D4h	***Reserved***	075h	–	52Dh	–	–	–	–	–
1D8h	***Reserved***	076h	–	52Eh	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
1DCh	Debug Control	077h	–	–	–	–	–	9E7h	ADFh
1E0h	Power Management Hot Plug User Configuration	078h	392h	530h	84Ah	8D4h	95Eh	9E8h	AE0h
1E4h	Egress Control and Status	079h	393h	531h	84Bh	8D5h	95Fh	9E9h	AE1h
1E8h	Bad TLP Count	07Ah	394h	532h	84Ch	8D6h	960h	9EAh	AE2h
1ECh	Bad DLLP Count	07Bh	395h	533h	84Dh	8D7h	961h	9EBh	AE3h
1F0h	PLX-Specific Relaxed Ordering Enable	07Ch	396h	534h	84Eh	8D8h	962h	9ECh	AE4h
1F4h	Software-Controlled Lane Status	07Dh	397h	535h	84Fh	8D9h	963h	9EDh	AE5h
1F8h	ACK Transmission Latency Limit	07Eh	398h	536h	850h	8DAh	964h	9EEh	AE6h
1FCh	***Reserved***	07Fh	–	537h	–	–	–	–	–
200h	***Reserved***	080h	–	538h	–	–	–	–	–
204h	***Reserved***	081h	–	539h	–	–	–	–	–
208h	***Reserved***	082h	–	53Ah	–	–	–	–	–
20Ch	***Reserved***	083h	–	53Bh	–	–	–	–	–
210h	Phy User Test Pattern 0	084h	–	53Ch	–	–	–	–	–
214h	Phy User Test Pattern 4	085h	–	53Dh	–	–	–	–	–
218h	Phy User Test Pattern 8	086h	–	53Eh	–	–	–	–	–
21Ch	Phy User Test Pattern 12	087h	–	53Fh	–	–	–	–	–
220h	Physical Layer Command and Status	088h	–	540h	–	–	–	–	–
224h	Port Configuration	089h	–	541h	–	–	–	–	–
228h	Physical Layer Test	08Ah	–	542h	–	–	–	–	–
22Ch	Physical Layer ***(Factory Test Only)***	08Bh	–	543h	–	–	–	–	–
230h	Physical Layer Port Command	08Ch	–	544h	–	–	–	–	–
234h	SKIP Ordered-Set Interval	08Dh	–	545h	–	–	–	–	–
238h	Quad 0 SerDes Diagnostic Data	08Eh	–	546h	–	–	–	–	–
23Ch	Quad 1 SerDes Diagnostic Data	08Fh	–	547h	–	–	–	–	–
240h	Quad 2 SerDes Diagnostic Data	090h	–	548h	–	–	–	–	–
244h	Quad 3 SerDes Diagnostic Data	091h	–	549h	–	–	–	–	–
248h	SerDes Nominal Drive Current Select	092h	–	54Ah	–	–	–	–	–
24Ch	SerDes Drive Current Level Select 1	093h	–	54Bh	–	–	–	–	–
250h	SerDes Drive Current Level Select 2	094h	–	54Ch	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
254h	SerDes Drive Equalization Level Select 1	095h	–	54Dh	–	–	–	–	–
258h	SerDes Drive Equalization Level Select 2	096h	–	54Eh	–	–	–	–	–
25Ch	***Reserved***	097h	–	54Fh	–	–	–	–	–
260h	Serial EEPROM Status and Control	098h	–	–	–	–	–	–	–
264h	Serial EEPROM Buffer	099h	–	–	–	–	–	–	–
28Ch	***Reserved***	0A3h	–	55Bh	–	–	–	–	–
290h	***Reserved***	0A4h	–	55Ch	–	–	–	–	–
2C8h	Bus Number CAM 0	0B2h	–	56Ah	–	–	–	–	–
2CCh	Bus Number CAM 1	0B3h	–	56Bh	–	–	–	–	–
2D0h	***Reserved***	0B4h	–	56Ch	–	–	–	–	–
2D4h	***Reserved***	0B5h	–	56Dh	–	–	–	–	–
2E8h	Bus Number CAM 8	0BAh	–	572h	–	–	–	–	–
2ECh	Bus Number CAM 9	0BBh	–	573h	–	–	–	–	–
2F0h	Bus Number CAM 10	0BCh	–	574h	–	–	–	–	–
2F4h	Bus Number CAM 11	0BDh	–	575h	–	–	–	–	–
308h	I/O CAM_0 and I/O CAM_1	0C2h	–	57Ah	–	–	–	–	–
30Ch	***Reserved***	0C3h	–	57Bh	–	–	–	–	–
318h	I/O CAM_8 and I/O CAM_9	0C6h	–	57Eh	–	–	–	–	–
31Ch	I/O CAM_10 and I/O CAM_11	0C7h	–	57Fh	–	–	–	–	–
348h	AMCAM_0 Memory Limit and Base	0D2h	–	58Ah	–	–	–	–	–
34Ch	AMCAM_0 Prefetchable Memory Limit and Base[31:0]	0D3h	–	58Bh	–	–	–	–	–
350h	AMCAM_0 Prefetchable Memory Base[63:32]	0D4h	–	58Ch	–	–	–	–	–
354h	AMCAM_0 Prefetchable Memory Limit[63:32]	0D5h	–	58Dh	–	–	–	–	–
358h	AMCAM_1 Memory Limit and Base	0D6h	–	58Eh	–	–	–	–	–
35Ch	AMCAM_1 Prefetchable Memory Limit and Base[31:0]	0D7h	–	58Fh	–	–	–	–	–
360h	AMCAM_1 Prefetchable Memory Base[63:32]	0D8h	–	590h	–	–	–	–	–
364h	AMCAM_1 Prefetchable Memory Limit[63:32]	0D9h	–	591h	–	–	–	–	–
368h	***Reserved***	0DAh	–	592h	–	–	–	–	–
36Ch	***Reserved***	0DBh	–	593h	–	–	–	–	–
370h	***Reserved***	0DCh	–	594h	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
374h	***Reserved***	0DDh	–	595h	–	–	–	–	–
378h	***Reserved***	0DEh	–	596h	–	–	–	–	–
37Ch	***Reserved***	0DFh	–	597h	–	–	–	–	–
380h	***Reserved***	0E0h	–	598h	–	–	–	–	–
384h	***Reserved***	0E1h	–	599h	–	–	–	–	–
3C8h	AMCAM_8 Memory Limit and Base	0F2h	–	5AAh	–	–	–	–	–
3CCh	AMCAM_8 Prefetchable Memory Limit and Base[31:0]	0F3h	–	5ABh	–	–	–	–	–
3D0h	AMCAM_8 Prefetchable Memory Base[63:32]	0F4h	–	5ACh	–	–	–	–	–
3D4h	AMCAM_8 Prefetchable Memory Limit[63:32]	0F5h	–	5ADh	–	–	–	–	–
3D8h	AMCAM_9 Memory Limit and Base	0F6h	–	5AEh	–	–	–	–	–
3DCh	AMCAM_9 Prefetchable Memory Limit and Base[31:0]	0F7h	–	5AFh	–	–	–	–	–
3E0h	AMCAM_9 Prefetchable Memory Base[63:32]	0F8h	–	5B0h	–	–	–	–	–
3E4h	AMCAM_9 Prefetchable Memory Limit[63:32]	0F9h	–	5B1h	–	–	–	–	–
3E8h	AMCAM_10 Memory Limit and Base	0FAh	–	5B2h	–	–	–	–	–
3ECh	AMCAM_10 Prefetchable Limit and Memory Base[31:0]	0FBh	–	5B3h	–	–	–	–	–
3F0h	AMCAM_10 Prefetchable Memory Base[63:32]	0FCh	–	5B4h	–	–	–	–	–
3F4h	AMCAM_10 Prefetchable Memory Limit[63:32]	0FDh	–	5B5h	–	–	–	–	–
3F8h	AMCAM_11 Memory Limit and Base	0FEh	–	5B6h	–	–	–	–	–
3FCh	AMCAM_11 Prefetchable Limit and Memory Base[31:0]	0FFh	–	5B7h	–	–	–	–	–
400h	AMCAM_11 Prefetchable Memory Base[63:32]	100h	–	5B8h	–	–	–	–	–
404h	AMCAM_11 Prefetchable Memory Limit[63:32]	101h	–	5B9h	–	–	–	–	–
660h	Ingress Control	198h	–	650h	–	–	–	–	–
664h	***Reserved***	199h	–	651h	–	–	–	–	–
668h	Ingress Port Enable	19Ah	–	652h	–	–	–	–	–
680h	I/OCAM_0 Upper Port 0	1A0h	–	658h	–	–	–	–	–
684h	I/OCAM_1 Upper Port 1	1A1h	–	659h	–	–	–	–	–
688h	***Reserved***	1A2h	–	65Ah	–	–	–	–	–
68Ch	***Reserved***	1A3h	–	65Bh	–	–	–	–	–
690h	***Reserved***	1A4h	–	65Ch	–	–	–	–	–
694h	***Reserved***	1A5h	–	65Dh	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
698h	***Reserved***	1A6h	–	65Eh	–	–	–	–	–
69Ch	***Reserved***	1A7h	–	65Fh	–	–	–	–	–
6A0h	I/OCAM_8 Upper Port 8	1A8h	–	660h	–	–	–	–	–
6A4h	I/OCAM_9 Upper Port 9	1A9h	–	661h	–	–	–	–	–
6A8h	I/OCAM_10 Upper Port 10	1AAh	–	662h	–	–	–	–	–
6ACh	I/OCAM_11 Upper Port 11	1ABh	–	663h	–	–	–	–	–
6B0h	***Reserved***	1ACh	–	664h	–	–	–	–	–
6B4h	***Reserved***	1ADh	–	665h	–	–	–	–	–
6B8h	***Reserved***	1AEh	–	666h	–	–	–	–	–
6BCh	***Reserved***	1AFh	–	667h	–	–	–	–	–
6C0h	BAR0 for Port 0	1B0h	–	668h	–	–	–	–	–
6C4h	BAR1 for Port 0	1B1h	–	669h	–	–	–	–	–
6C8h	BAR0 for Port 1	1B2h	–	66Ah	–	–	–	–	–
6CCh	BAR1 for Port 1	1B3h	–	66Bh	–	–	–	–	–
6D0h	***Reserved***	1B4h	–	66Ch	–	–	–	–	–
6D4h	***Reserved***	1B5h	–	66Dh	–	–	–	–	–
6D8h	***Reserved***	1B6h	–	66Eh	–	–	–	–	–
6DCh	***Reserved***	1B7h	–	66Fh	–	–	–	–	–
6E0h	***Reserved***	1B8h	–	670h	–	–	–	–	–
6E4h	***Reserved***	1B9h	–	671h	–	–	–	–	–
6E8h	***Reserved***	1BAh	–	672h	–	–	–	–	–
6ECh	***Reserved***	1BBh	–	673h	–	–	–	–	–
6F0h	***Reserved***	1BCh	–	674h	–	–	–	–	–
6F4h	***Reserved***	1BDh	–	675h	–	–	–	–	–
6F8h	***Reserved***	1BEh	–	676h	–	–	–	–	–
6FCh	***Reserved***	1BFh	–	677h	–	–	–	–	–
700h	BAR0 for Port 8	1C0h	–	678h	–	–	–	–	–
704h	BAR1 for Port 8	1C1h	–	679h	–	–	–	–	–
708h	BAR0 for Port 9	1C2h	–	67Ah	–	–	–	–	–
70Ch	BAR1 for Port 9	1C3h	–	67Bh	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
710h	BAR0 for Port 10	1C4h	–	67Ch	–	–	–	–	–
714h	BAR1 for Port 10	1C5h	–	67Dh	–	–	–	–	–
718h	BAR0 for Port 11	1C6h	–	67Eh	–	–	–	–	–
71Ch	BAR1 for Port 11	1C7h	–	67Fh	–	–	–	–	–
720h	***Reserved***	1C8h	–	680h	–	–	–	–	–
724h	***Reserved***	1C9h	–	681h	–	–	–	–	–
728h	***Reserved***	1CAh	–	682h	–	–	–	–	–
72Ch	***Reserved***	1CBh	–	683h	–	–	–	–	–
730h	***Reserved***	1CCh	–	684h	–	–	–	–	–
734h	***Reserved***	1CDh	–	685h	–	–	–	–	–
738h	***Reserved***	1CEh	–	686h	–	–	–	–	–
73Ch	***Reserved***	1CFh	–	687h	–	–	–	–	–
740h	VC0 Port 0 Capability	1D0h	–	688h	–	–	–	–	–
744h	VC1 Port 0 Capability	1D1h	–	689h	–	–	–	–	–
748h	VC0 Port 1 Capability	1D2h	–	68Ah	–	–	–	–	–
74Ch	VC1 Port 1 Capability	1D3h	–	68Bh	–	–	–	–	–
750h	***Reserved***	1D4h	–	68Ch	–	–	–	–	–
754h	***Reserved***	1D5h	–	68Dh	–	–	–	–	–
758h	***Reserved***	1D6h	–	68Eh	–	–	–	–	–
75Ch	***Reserved***	1D7h	–	68Fh	–	–	–	–	–
760h	***Reserved***	1D8h	–	690h	–	–	–	–	–
764h	***Reserved***	1D9h	–	691h	–	–	–	–	–
768h	***Reserved***	1DAh	–	692h	–	–	–	–	–
76Ch	***Reserved***	1DBh	–	693h	–	–	–	–	–
770h	***Reserved***	1DCh	–	694h	–	–	–	–	–
774h	***Reserved***	1DDh	–	695h	–	–	–	–	–
778h	***Reserved***	1DEh	–	696h	–	–	–	–	–
77Ch	***Reserved***	1DFh	–	697h	–	–	–	–	–
780h	VC0 Port 8 Capability	1E0h	–	698h	–	–	–	–	–
784h	VC1 Port 8 Capability	1E1h	–	699h	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
788h	VC0 Port 9 Capability	1E2h	–	69Ah	–	–	–	–	–
78Ch	VC1 Port 9 Capability	1E3h	–	69Bh	–	–	–	–	–
790h	VC0 Port 10 Capability	1E4h	–	69Ch	–	–	–	–	–
794h	VC1 Port 10 Capability	1E5h	–	69Dh	–	–	–	–	–
798h	VC0 Port 11 Capability	1E6h	–	69Eh	–	–	–	–	–
79Ch	VC1 Port 11 Capability	1E7h	–	69Fh	–	–	–	–	–
7A0h	***Reserved***	1E8h	–	6A0h	–	–	–	–	–
7A4h	***Reserved***	1E9h	–	6A1h	–	–	–	–	–
7A8h	***Reserved***	1EAh	–	6A2h	–	–	–	–	–
7ACh	***Reserved***	1EBh	–	6A3h	–	–	–	–	–
7B0h	***Reserved***	1ECh	–	6A4h	–	–	–	–	–
7B4h	***Reserved***	1EDh	–	6A5h	–	–	–	–	–
7B8h	***Reserved***	1EEh	–	6A6h	–	–	–	–	–
7BCh	***Reserved***	1EFh	–	6A7h	–	–	–	–	–
7C0h	***Reserved***	1F0h	–	6A8h	–	–	–	–	–
7C4h	***Reserved***	1F1h	–	6A9h	–	–	–	–	–
7C8h	***Reserved***	1F2h	–	6AAh	–	–	–	–	–
7CCh	***Reserved***	1F3h	–	6ABh	–	–	–	–	–
7D0h	***Reserved***	1F4h	–	6ACh	–	–	–	–	–
7D4h	***Reserved***	1F5h	–	6ADh	–	–	–	–	–
7D8h	***Reserved***	1F6h	–	6AEh	–	–	–	–	–
7DCh	***Reserved***	1F7h	–	6AFh	–	–	–	–	–
7E0h	***Reserved***	1F8h	–	6B0h	–	–	–	–	–
7E4h	***Reserved***	1F9h	–	6B1h	–	–	–	–	–
7E8h	***Reserved***	1FAh	–	6B2h	–	–	–	–	–
7ECh	***Reserved***	1FBh	–	6B3h	–	–	–	–	–
7F0h	***Reserved***	1FCh	–	6B4h	–	–	–	–	–
7F4h	***Reserved***	1FDh	–	6B5h	–	–	–	–	–
7F8h	***Reserved***	1FEh	–	6B6h	–	–	–	–	–
7FCh	***Reserved***	1FFh	–	6B7h	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
800h	***Reserved***	200h	–	6B8h	–	–	–	–	–
804h	***Reserved***	201h	–	6B9h	–	–	–	–	–
808h	***Reserved***	202h	–	6BAh	–	–	–	–	–
80Ch	***Reserved***	203h	–	6BBh	–	–	–	–	–
810h	***Reserved***	204h	–	6BCh	–	–	–	–	–
814h	***Reserved***	205h	–	6BDh	–	–	–	–	–
818h	***Reserved***	206h	–	6BEh	–	–	–	–	–
81Ch	***Reserved***	207h	–	6BFh	–	–	–	–	–
820h	***Reserved***	208h	–	6C0h	–	–	–	–	–
824h	***Reserved***	209h	–	6C1h	–	–	–	–	–
828h	***Reserved***	20Ah	–	6C2h	–	–	–	–	–
82Ch	***Reserved***	20Bh	–	6C3h	–	–	–	–	–
830h	***Reserved***	20Ch	–	6C4h	–	–	–	–	–
834h	***Reserved***	20Dh	–	6C5h	–	–	–	–	–
838h	***Reserved***	20Eh	–	6C6h	–	–	–	–	–
83Ch	***Reserved***	20Fh	–	6C7h	–	–	–	–	–
840h	Port 0 VC Capability_1	210h	–	6C8h	–	–	–	–	–
844h	Port 1 VC Capability_1	211h	–	6C9h	–	–	–	–	–
848h	***Reserved***	212h	–	6CAh	–	–	–	–	–
84Ch	***Reserved***	213h	–	6CBh	–	–	–	–	–
860h	Port 8 VC Capability_1	218h	–	6D0h	–	–	–	–	–
864h	Port 9 VC Capability_1	219h	–	6D1h	–	–	–	–	–
868h	Port 10 VC Capability_1	21Ah	–	6D2h	–	–	–	–	–
86Ch	Port 11 VC Capability_1	21Bh	–	6D3h	–	–	–	–	–
9F4h	INCH FC Update Pending Timer	27Dh	–	735h	–	–	–	–	–
9FCh	INCH Mode	27Fh	–	737h	–	–	–	–	–
A00h	INCH Threshold Port 0 or 8 VC0 Posted	280h	–	738h	–	–	–	–	–
A04h	INCH Threshold Port 0 or 8 VC0 Non-Posted	281h	–	739h	–	–	–	–	–
A08h	INCH Threshold Port 0 or 8 VC0 Completion	282h	–	73Ah	–	–	–	–	–
A0Ch	INCH Threshold Port 0 or 8 VC1 Posted	283h	–	73Bh	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
A10h	INCH Threshold Port 0 or 8 VC1 Non-Posted	284h	–	73Ch	–	–	–	–	–
A14h	INCH Threshold Port 0 or 8 VC1 Completion	285h	–	73Dh	–	–	–	–	–
A18h	INCH Threshold Port 1 or 9 VC0 Posted	286h	–	73Eh	–	–	–	–	–
A1Ch	INCH Threshold Port 1 or 9 VC0 Non-Posted	287h	–	73Fh	–	–	–	–	–
A20h	INCH Threshold Port 1 or 9 VC0 Completion	288h	–	740h	–	–	–	–	–
A24h	INCH Threshold Port 1 or 9 VC1 Posted	289h	–	741h	–	–	–	–	–
A28h	INCH Threshold Port 1 or 9 VC1 Non-Posted	28Ah	–	742h	–	–	–	–	–
A2Ch	INCH Threshold Port 1 or 9 VC1 Completion	28Bh	–	743h	–	–	–	–	–
A30h	INCH Threshold Port 10 VC0 Posted	28Ch	–	744h	–	–	–	–	–
A34h	INCH Threshold Port 10 VC0 Non-Posted	28Dh	–	745h	–	–	–	–	–
A38h	INCH Threshold Port 10 VC0 Completion	28Eh	–	746h	–	–	–	–	–
A3Ch	INCH Threshold Port 10 VC1 Posted	28Fh	–	747h	–	–	–	–	–
A40h	INCH Threshold Port 10 VC1 Non-Posted	290h	–	748h	–	–	–	–	–
A44h	INCH Threshold Port 10 VC1 Completion	291h	–	749h	–	–	–	–	–
A48h	INCH Threshold Port 11 VC0 Posted	292h	–	74Ah	–	–	–	–	–
A4Ch	INCH Threshold Port 11 VC0 Non-Posted	293h	–	74Bh	–	–	–	–	–
A50h	INCH Threshold Port 11 VC0 Completion	294h	–	74Ch	–	–	–	–	–
A54h	INCH Threshold Port 11 VC1 Posted	295h	–	74Dh	–	–	–	–	–
A58h	INCH Threshold Port 11 VC1 Non-Posted	296h	–	74Eh	–	–	–	–	–
A5Ch	INCH Threshold Port 11 VC1 Completion	297h	–	74Fh	–	–	–	–	–
B80h	***Reserved***	2E0h	–	798h	–	–	–	–	–
B84h	***Reserved***	2E1h	–	799h	–	–	–	–	–
B88h	***Reserved***	2E2h	–	79Ah	–	–	–	–	–
B98h	***Reserved***	2E6h	–	79Eh	–	–	–	–	–
B9Ch	***Reserved***	2E7h	–	79Fh	–	–	–	–	–
BE8h	Ingress One-Bit ECC Error Count	2FAh	–	7B2h	–	–	–	–	–
BECh	PLX-Specific Relaxed Completion Ordering (Ingress) ***(Silicon Revisions BB/BC Only)***	2FBh	–	7B3h	–	–	–	–	–
BFCh	PLX-Specific Relaxed Ordering Mode (Ingress)	2FFh	–	7B7h	–	–	–	–	–

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
C00h	ITCH VC&T Threshold_1	300h	–	7B8h	–	–	–	–	–
C04h	ITCH VC&T Threshold_2	301h	–	7B9h	–	–	–	–	–
C08h	ITCH VC&T Threshold_3	302h	–	7BAh	–	–	–	–	–
C0Ch	***Reserved***	303h	–	7BBh	–	–	–	–	–
C10h	***Reserved***	304h	–	7BCh	–	–	–	–	–
C14h	***Reserved***	305h	–	7BDh	–	–	–	–	–
C18h	***Reserved***	306h	–	7BEh	–	–	–	–	–
C1Ch	***Reserved***	307h	–	7BFh	–	–	–	–	–
C20h	***Reserved***	308h	–	7C0h	–	–	–	–	–
C24h	***Reserved***	309h	–	7C1h	–	–	–	–	–
C28h	***Reserved***	30Ah	–	7C2h	–	–	–	–	–
C2Ch	***Reserved***	30Bh	–	7C3h	–	–	–	–	–
C30h	***Reserved***	30Ch	–	7C4h	–	–	–	–	–
C34h	***Reserved***	30Dh	–	7C5h	–	–	–	–	–
C38h	***Reserved***	30Eh	–	7C6h	–	–	–	–	–
C3Ch	Memory BAR2/3 Address Translation[31:0]	–	–	–	–	–	–	9EFh	AE7h
C40h	Memory BAR2/3 Address Translation[63:32]	–	–	–	–	–	–	9F0h	AE8h
C44h	Memory BAR4/5 Address Translation[31:0]	–	–	–	–	–	–	9F1h	AE9h
C48h	Memory BAR4/5 Address Translation[63:32]	–	–	–	–	–	–	9F2h	AEAh
C4Ch	Memory BAR2/3 Limit[31:0]	–	–	–	–	–	–	9F3h	AEBh
C50h	Memory BAR2/3 Limit[63:32]	–	–	–	–	–	–	9F4h	AECh
C54h	Memory BAR4/5 Limit[31:0]	–	–	–	–	–	–	9F5h	AEDh
C58h	Memory BAR4/5 Limit[63:32]	–	–	–	–	–	–	9F6h	AEEh
C5Ch	Lookup Table Entry 0	–	–	–	–	–	–	9F7h	AEFh
C60h	Lookup Table Entry 1	–	–	–	–	–	–	9F8h	AF0h
C64h	Lookup Table Entry 2	–	–	–	–	–	–	9F9h	AF1h
C68h	Lookup Table Entry 3	–	–	–	–	–	–	9FAh	AF2h
C6Ch	Lookup Table Entry 4	–	–	–	–	–	–	9FBh	AF3h
C70h	Lookup Table Entry 5	–	–	–	–	–	–	9FCh	AF4h
C74h	Lookup Table Entry 6	–	–	–	–	–	–	9FDh	AF5h

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
C78h	Lookup Table Entry 7	–	–	–	–	–	–	9FEh	AF6h
C7Ch	Lookup Table Entry 8	–	–	–	–	–	–	9FFh	AF7h
C80h	Lookup Table Entry 9	–	–	–	–	–	–	A00h	AF8h
C84h	Lookup Table Entry 10	–	–	–	–	–	–	A01h	AF9h
C88h	Lookup Table Entry 11	–	–	–	–	–	–	A02h	AFAh
C8Ch	Lookup Table Entry 12	–	–	–	–	–	–	A03h	AFBh
C90h	Lookup Table Entry 13	–	–	–	–	–	–	A04h	AFCh
C94h	Lookup Table Entry 14	–	–	–	–	–	–	A05h	AFDh
C98h	Lookup Table Entry 15	–	–	–	–	–	–	A06h	AFEh
C9Ch	Lookup Table Entry 16	–	–	–	–	–	–	A07h	AFFh
CA0h	Lookup Table Entry 17	–	–	–	–	–	–	A08h	B00h
CA4h	Lookup Table Entry 18	–	–	–	–	–	–	A09h	B01h
CA8h	Lookup Table Entry 19	–	–	–	–	–	–	A0Ah	B02h
CACh	Lookup Table Entry 20	–	–	–	–	–	–	A0Bh	B03h
CB0h	Lookup Table Entry 21	–	–	–	–	–	–	A0Ch	B04h
CB4h	Lookup Table Entry 22	–	–	–	–	–	–	A0Dh	B05h
CB8h	Lookup Table Entry 23	–	–	–	–	–	–	A0Eh	B06h
CBCh	Lookup Table Entry 24	–	–	–	–	–	–	A0Fh	B07h
CC0h	Lookup Table Entry 25	–	–	–	–	–	–	A10h	B08h
CC4h	Lookup Table Entry 26	–	–	–	–	–	–	A11h	B09h
CC8h	Lookup Table Entry 27	–	–	–	–	–	–	A12h	B0Ah
CCCh	Lookup Table Entry 28	–	–	–	–	–	–	A13h	B0Bh
CD0h	Lookup Table Entry 29	–	–	–	–	–	–	A14h	B0Ch
CD4h	Lookup Table Entry 30	–	–	–	–	–	–	A15h	B0Dh
CD8h	Lookup Table Entry 31	–	–	–	–	–	–	A16h	B0Eh
CDCh	Lookup Table Entry 32	–	–	–	–	–	–	A17h	B0Fh
CE0h	Lookup Table Entry 33	–	–	–	–	–	–	A18h	B10h
CE4h	Lookup Table Entry 34	–	–	–	–	–	–	A19h	B11h
CE8h	Lookup Table Entry 35	–	–	–	–	–	–	A1Ah	B12h
CECh	Lookup Table Entry 36	–	–	–	–	–	–	A1Bh	B13h

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
CF0h	Lookup Table Entry 37	–	–	–	–	–	–	A1Ch	B14h
CF4h	Lookup Table Entry 38	–	–	–	–	–	–	A1Dh	B15h
CF8h	Lookup Table Entry 39	–	–	–	–	–	–	A1Eh	B16h
CFCh	Lookup Table Entry 40	–	–	–	–	–	–	A1Fh	B17h
D00h	Lookup Table Entry 41	–	–	–	–	–	–	A20h	B18h
D04h	Lookup Table Entry 42	–	–	–	–	–	–	A21h	B19h
D08h	Lookup Table Entry 43	–	–	–	–	–	–	A22h	B1Ah
D0Ch	Lookup Table Entry 44	–	–	–	–	–	–	A23h	B1Bh
D10h	Lookup Table Entry 45	–	–	–	–	–	–	A24h	B1Ch
D14h	Lookup Table Entry 46	–	–	–	–	–	–	A25h	B1Dh
D18h	Lookup Table Entry 47	–	–	–	–	–	–	A26h	B1Eh
D1Ch	Lookup Table Entry 48	–	–	–	–	–	–	A27h	B1Fh
D20h	Lookup Table Entry 49	–	–	–	–	–	–	A28h	B20h
D24h	Lookup Table Entry 50	–	–	–	–	–	–	A29h	B21h
D28h	Lookup Table Entry 51	–	–	–	–	–	–	A2Ah	B22h
D2Ch	Lookup Table Entry 52	–	–	–	–	–	–	A2Bh	B23h
D30h	Lookup Table Entry 53	–	–	–	–	–	–	A2Ch	B24h
D34h	Lookup Table Entry 54	–	–	–	–	–	–	A2Dh	B25h
D38h	Lookup Table Entry 55	–	–	–	–	–	–	A2Eh	B26h
D3Ch	Lookup Table Entry 56	–	–	–	–	–	–	A2Fh	B27h
D40h	Lookup Table Entry 57	–	–	–	–	–	–	A30h	B28h
D44h	Lookup Table Entry 58	–	–	–	–	–	–	A31h	B29h
D48h	Lookup Table Entry 59	–	–	–	–	–	–	A32h	B2Ah
D4Ch	Lookup Table Entry 60	–	–	–	–	–	–	A33h	B2Bh
D50h	Lookup Table Entry 61	–	–	–	–	–	–	A34h	B2Ch
D54h	Lookup Table Entry 62	–	–	–	–	–	–	A35h	B2Dh
D58h	Lookup Table Entry 63	–	–	–	–	–	–	A36h	B2Eh
D5Ch	NT Link Interface VC0 Resource Control	–	–	–	–	–	–	A37h	B2Fh
D60h	NT Link Interface VC1 Resource Control	–	–	–	–	–	–	A38h	B30h
D64h	NT Link Interface VC Capability 1	–	–	–	–	–	–	A39h	B31h

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
D68h	BAR0 = ***Reserved*** (Virtual)	–	–	–	–	–	–	A3Ah	B32h
D6Ch	BAR1 (Virtual)	–	–	–	–	–	–	A3Bh	B33h
D70h	BAR2 (Virtual)	–	–	–	–	–	–	A3Ch	B34h
D74h	BAR3 (Virtual)	–	–	–	–	–	–	A3Dh	B35h
D78h	BAR4 (Virtual)	–	–	–	–	–	–	A3Eh	B36h
D7Ch	BAR5 (Virtual)	–	–	–	–	–	–	A3Fh	B37h
D80h	BAR1 Setup	–	–	–	–	–	–	A40h	B38h
D84h	BAR2 Setup	–	–	–	–	–	–	A41h	B39h
D88h	BAR3 Setup	–	–	–	–	–	–	A42h	B3Ah
D8Ch	BAR4 Setup	–	–	–	–	–	–	A43h	B3Bh
D90h	BAR5 Setup	–	–	–	–	–	–	A44h	B3Ch
D94h	Requester ID Translation LUT Entry 0	–	–	–	–	–	–	A45h	B3Dh
D98h	Requester ID Translation LUT Entry 1	–	–	–	–	–	–	A46h	B3Eh
D9Ch	Requester ID Translation LUT Entry 2	–	–	–	–	–	–	A47h	B3Fh
DA0h	Requester ID Translation LUT Entry 3	–	–	–	–	–	–	A48h	B40h
DA4h	Requester ID Translation LUT Entry 4	–	–	–	–	–	–	A49h	B41h
DA8h	Requester ID Translation LUT Entry 5	–	–	–	–	–	–	A4Ah	B42h
DACh	Requester ID Translation LUT Entry 6	–	–	–	–	–	–	A4Bh	B43h
DB0h	Requester ID Translation LUT Entry 7	–	–	–	–	–	–	A4Ch	B44h
DB4h	Requester ID Translation LUT Entry 0_1	–	–	–	–	–	–	A4Dh	B45h
DB8h	Requester ID Translation LUT Entry 2_3	–	–	–	–	–	–	A4Eh	B46h
DBCh	Requester ID Translation LUT Entry 4_5	–	–	–	–	–	–	A4Fh	B47h
DC0h	Requester ID Translation LUT Entry 6_7	–	–	–	–	–	–	A50h	B48h
DC4h	Requester ID Translation LUT Entry 8_9	–	–	–	–	–	–	A51h	B49h
DC8h	Requester ID Translation LUT Entry 10_11	–	–	–	–	–	–	A52h	B4Ah
DCCh	Requester ID Translation LUT Entry 12_13	–	–	–	–	–	–	A53h	B4Bh
DD0h	Requester ID Translation LUT Entry 14_15	–	–	–	–	–	–	A54h	B4Ch
DD4h	Requester ID Translation LUT Entry 16_17	–	–	–	–	–	–	A55h	B4Dh
DD8h	Requester ID Translation LUT Entry 18_19	–	–	–	–	–	–	A56h	B4Eh
DDCh	Requester ID Translation LUT Entry 20_21	–	–	–	–	–	–	A57h	B4Fh

Table A-1. PEX 8524V and PEX 8524 Serial EEPROM Memory Map *(Cont.)*

Register Offset	Register Name	Port Register Loaded from Listed Serial EEPROM Address						Non-Transparent Ports	
		Station 0		Station 1					
		Port 0	Port 1	Port 8	Port 9	Port 10	Port 11	Link	Virtual
DE0h	Requester ID Translation LUT Entry 22_23	–	–	–	–	–	–	A58h	B50h
DE4h	Requester ID Translation LUT Entry 24_25	–	–	–	–	–	–	A59h	B51h
DE8h	Requester ID Translation LUT Entry 26_27	–	–	–	–	–	–	A5Ah	B52h
DECh	Requester ID Translation LUT Entry 28_29	–	–	–	–	–	–	A5Bh	B53h
DF0h	Requester ID Translation LUT Entry 30_31	–	–	–	–	–	–	A5Ch	B54h
DF4h	NT Port Link Interface Capture Bus and Device Number	–	–	–	–	–	–	–	B55h
DF8h	NT Port Virtual Interface Control	–	–	–	–	–	–	–	B56h
FB4h	PCI Express Enhanced Capability Header	30Fh	399h	7C7h	851h	8DBh	965h	A5Dh	B57h
FB8h	Uncorrectable Error Status	310h	39Ah	7C8h	852h	8DCh	966h	A5Eh	B58h
FBCh	Uncorrectable Error Mask	311h	39Bh	7C9h	853h	8DDh	967h	A5Fh	B59h
FC0h	Uncorrectable Error Severity	312h	39Ch	7CAh	854h	8DEh	968h	A60h	B5Ah
FC4h	Correctable Error Status	313h	39Dh	7CBh	855h	8DFh	969h	A61h	B5Bh
FC8h	Correctable Error Mask	314h	39Eh	7CCh	856h	8E0h	96Ah	A62h	B5Ch
FCCh	Advanced Error Capabilities and Control	315h	39Fh	7CDh	857h	8E1h	96Bh	A63h	B5Dh
FD0h	Header Log_0	316h	3A0h	7CEh	858h	8E2h	96Ch	A64h	B5Eh
FD4h	Header Log_1	317h	3A1h	7CFh	859h	8E3h	96Dh	A65h	B5Fh
FD8h	Header Log_2	318h	3A2h	7D0h	85Ah	8E4h	96Eh	A66h	B60h
FDCh	Header Log_3	319h	3A3h	7D1h	85Bh	8E5h	96Fh	A67h	B61h
N/A	CRC Value								BE4h

Appendix B General Information

B.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table B-1. PEX 8524VBB/BC 680-Ball PBGA Product Ordering Information

Part Numbers	Description
PEX8524-BB25VBI	PEX 8524VBB 6-Port, 24-Lane PCI Express Switch Plastic BGA package (680-ball, 35 x 35 mm)
PEX8524-BB25VBI G	PEX 8524VBB 6-Port, 24-Lane PCI Express Switch Plastic BGA package (680-ball, 35 x 35 mm), Lead-Free RoHS Green package
PEX8524-BC25VBI	PEX 8524VBC 6-Port, 24-Lane PCI Express Switch Plastic BGA package (680-ball, 35 x 35 mm)
PEX8524-BC25VBI G	PEX 8524VBC 6-Port, 24-Lane PCI Express Switch Plastic BGA package (680-ball, 35 x 35 mm), Lead-Free RoHS Green package
PEX8524-BC25V B I G G – Lead-free, RoHS Compliant, Fully Green I – Industrial Temperature B – Plastic Ball Grid Array package V – 35 x 35 mm package BB or BC – Silicon Revision 25 – Signaling Rate (2.5 Gbps) 8524 – Part Number PEX – PCI Express product family	
PEX 8524VRDK-1	PEX 8524VBC (35 x 35 mm) Rapid Development Kit with x16 edge connector and x1 adapter
PEX 8524VRDK-4	PEX 8524VBC (35 x 35 mm) Rapid Development Kit with x16 edge connector and x4 adapter
PEX 8524VRDK-8	PEX 8524VBC (35 x 35 mm) Rapid Development Kit with x16 edge connector and x8 adapter

Table B-2. PEX 8524BB/BC 644-Ball PBGA Product Ordering Information

Part Numbers	Description
PEX8524-BB25BI	PEX 8524BB 6-Port, 24-Lane PCI Express Switch Plastic BGA package (644-ball, 31 x 31 mm)
PEX8524-BB25BI G	PEX 8524BB 6-Port, 24-Lane PCI Express Switch Plastic BGA package (644-ball, 31 x 31 mm), Lead-Free RoHS Green package
PEX8524-BC25BI	PEX 8524BC 6-Port, 24-Lane PCI Express Switch Plastic BGA package (644-ball, 31 x 31 mm)
PEX8524-BC25BI G	PEX 8524BC 6-Port, 24-Lane PCI Express Switch Plastic BGA package (644-ball, 31 x 31 mm), Lead-Free RoHS Green package
PEX8524-BC25BI G G – Lead-free, RoHS Compliant, Fully Green I – Industrial Temperature B – Plastic Ball Grid Array package BB or BC – Silicon Revision 25 – Signaling Rate (2.5 Gbps) 8524 – Part Number PEX – PCI Express product family	
PEX 8524-BB RDK	PEX 8524BB (31 x 31mm) Rapid Development Kit with x8 edge connector
PEX 8524-BC RDK	PEX 8524BC (31 x 31mm) Rapid Development Kit with x8 edge connector
x1 Adapter	PCI Express x16 to x1 Adapter
x4 Adapter	PCI Express x16 to x4 Adapter

B.2 United States and International Representatives, and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

B.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support/, or call 800 759-3735 (domestic only) or 408 774-9060.